GREENSPRING COMPUTERS, INC.
ASSEMBLY NAME: VIPC610
REVISION LEVEL: C 93050B
REVISION DATE: 11-Apr-94
ELEC ASSY#: 4001610263
COMPL ASSY#: 6001610263
SHIP ASSY#: 9001610263

Part Number	DESCRIPTION	PER	LOCATION
1001281026	SMT Fuse, 1206, 1.0 amp	6	F1-F6
1002022020	SKT, DIP, MS, 20 pin	5	U4,U5,U11,U12,U17
1002022024	SKT, DIP, MS, 24 pin	2	U13,U15
1003127226	CHIP CAP,TANT,22µF,6.0V,CASE SIZE C	8	C2-5,C8,C11,C14,21
1003127685	CHIP CAP,TANT,6.8µF,20V,CASE SIZE C	8	C6,7,9,10,12,13,15,16
1003133100	CHIP CAP,CER,10pF,100V,CASE 1206	1	C1
1003133104	CHIP CAP,CER,.1µF,50V,CASE 1206	18	C16-C20,BYPASS
1003661102	EMI FILTER, 25VDC, 1000pF	12	L1-L12
1004100101	RES, 100 Ω, 1206 CHIP, 5%	2	R4,R20
1004100102	RES, 1K Ω, 1206 CHIP, 5%	3	R1,R2,R9
1004100103	RES, 10K Ω, 1206 CHIP, 5%	4	R3,R6-8
1004100201	RES, 200 Ω, 1206 CHIP, 5%	4	R10-R13
1004100202	RES, 2K Ω, 1206 CHIP, 5%	1	R5
1004100330	RES, 33 Ω, 1206 CHIP, 5%	4	R21-R24
1004210105	RES NET, 6 PIN, 5 RES, 1MΩ	1	RP7
1004252103	RES NET,16 PIN SOIC,15 RES,10K	6	RP1-RP6
1005023692	TRANS, MMBT2369, SOT-23	1	Q1
1005039042	TRANS, 2N3904, SOT-23	2	Q2,Q4
1005039062	TRANS, 2N3906, SOT-23	1	Q3
1005110746	DIODE, ZENER, 1N746A	1	D1
1005257311	LED, GREEN, REC	4	LED1-LED4
1006011040	HDR, STR, 1 X 40	3	E1,E4-E12,E14,E15
1006011050	HDR, STR, 2 x 25	2	E2,E13
1006022096	CONN,DIN,MALE,RA,96 PIN	2	P1,P2
1006031050	CONN,SCH HDR,STR,2 X 25,MALE	2	J2,J4
1006032050	CONN, SCH HDR, RA, 2x25, MALE	2	J1,J3
1006973280	CONN, HD, HEADER, 50 PIN	8	J5-J12
1007030520	IC, 74ALS520, TI ONLY	2	U3,U4
1007040000	IC, 74F00	1	U10
1007040074	IC, 74F74	1	U14
1007040245	IC, 74F245 TI ONLY	2	U1,U2
1007050138	IC, 74HC138	2	U20,U21
1007050760	IC, 74AS760, TI ONLY	1	U16
1007070020	IC, 74HCT20	1	U18
1007070123	IC, 74HCT123	2	U22,U23
1007070373	IC, 74HCT373, TI ONLY	5	U6-U9,U19
1007421881	PAL, 18V8Z25N, G42205B	1	U5
1007622210	CMOS PAL, 22V10A, G42203E	1	U15
1007721681	GAL, 16V8-25, 1/4 POWER, G42208A	1	U11

GREENSPRING COMPUTERS, INC.
ASSEMBLY NAME: VIPC610
REVISION LEVEL: C 93050B
REVISION DATE: 11-Apr-94
ELEC ASSY#: 4001610263
COMPL ASSY#: 6001610263
SHIP ASSY#: 9001610263

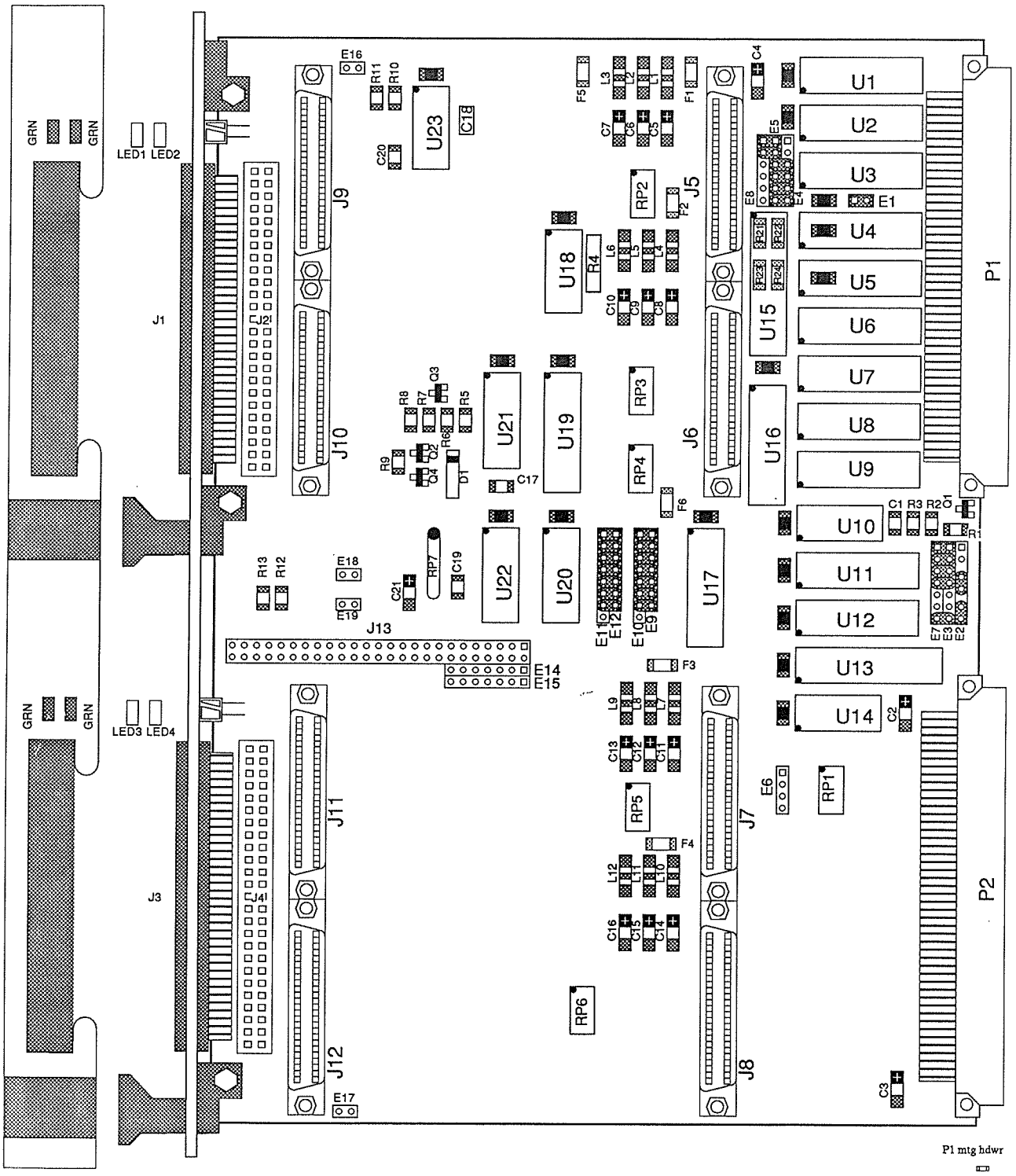
Part Number	DESCRIPTION	PER	LOCATION
1007721681	GAL, 16V8-25, 1/4 POWER, G42209A	1	U17
1007722101	GAL, 20V8-25, 1/4 POWER, G42206B	1	U13
1009000001	Shunt	29	
2005011000	MS,SLOT,PAN,M2.5X10MM	4	
2005120001	NUT,HEX,ZP,M2.5	4	
3001610263	PCB, VIPC610 C	1	
3003461100	EJ FNT PNL, VIPC610, 4HP, 6U	1	

Header Table

1 X 2	E1
1 X 4	E6
1 X 6	E4,E5,E8
1 X 7	E3,E7,E9,E11,E14,E15
1 X 8	E10,E12
2 x 25	E13
2 X 3	E2

REVISIONS

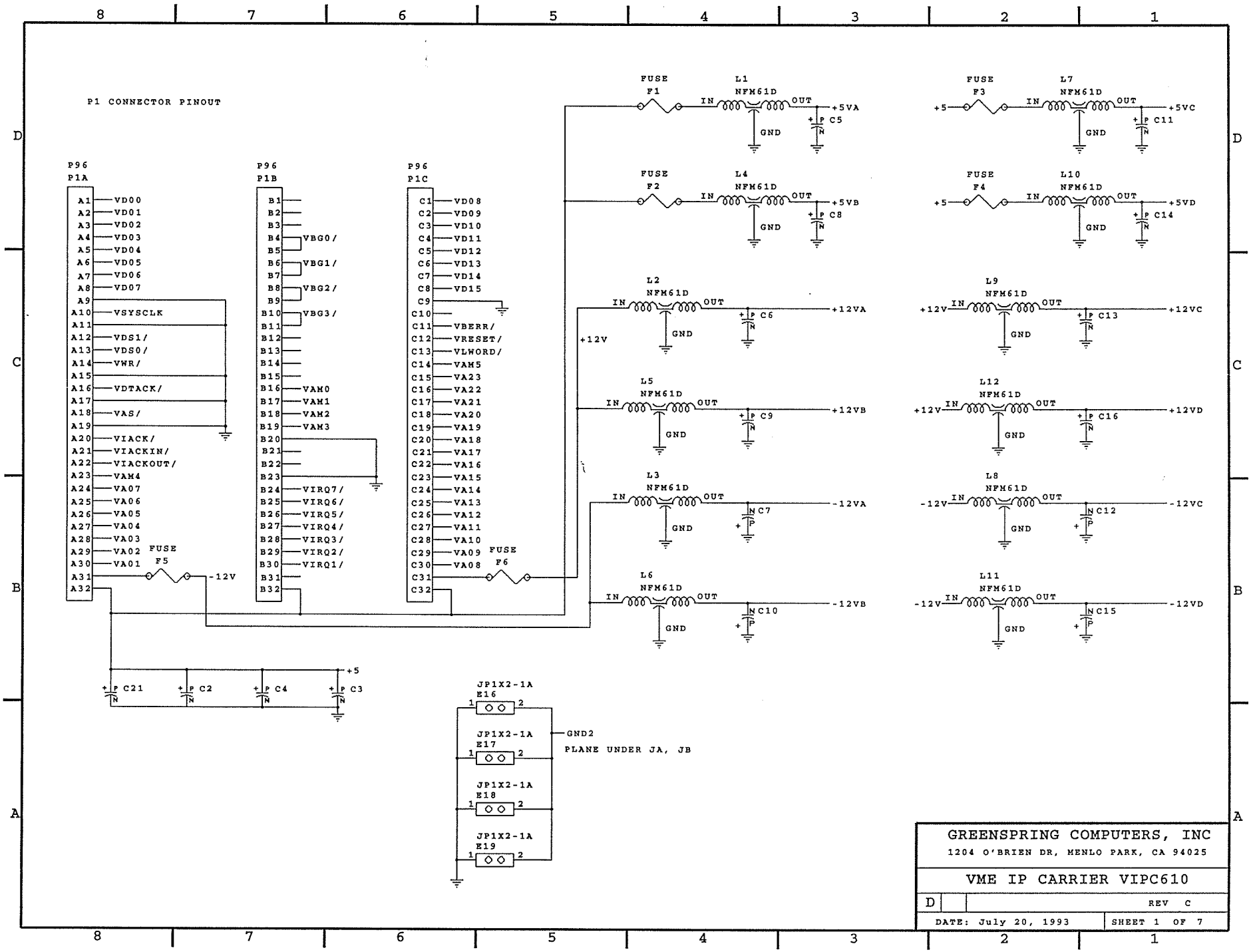
ECO #	DESCRIPTION	DATE
93050	Release To Production	29 Sep 1993
93050B	Correct Fuse Value	24 Jan 1994
	Add Header Table	23 Mar 1994
	Add P1 Mtg Hdwr	24 Mar 1994
	Add Bypass Capacitor under U4	Apr 11, 1994

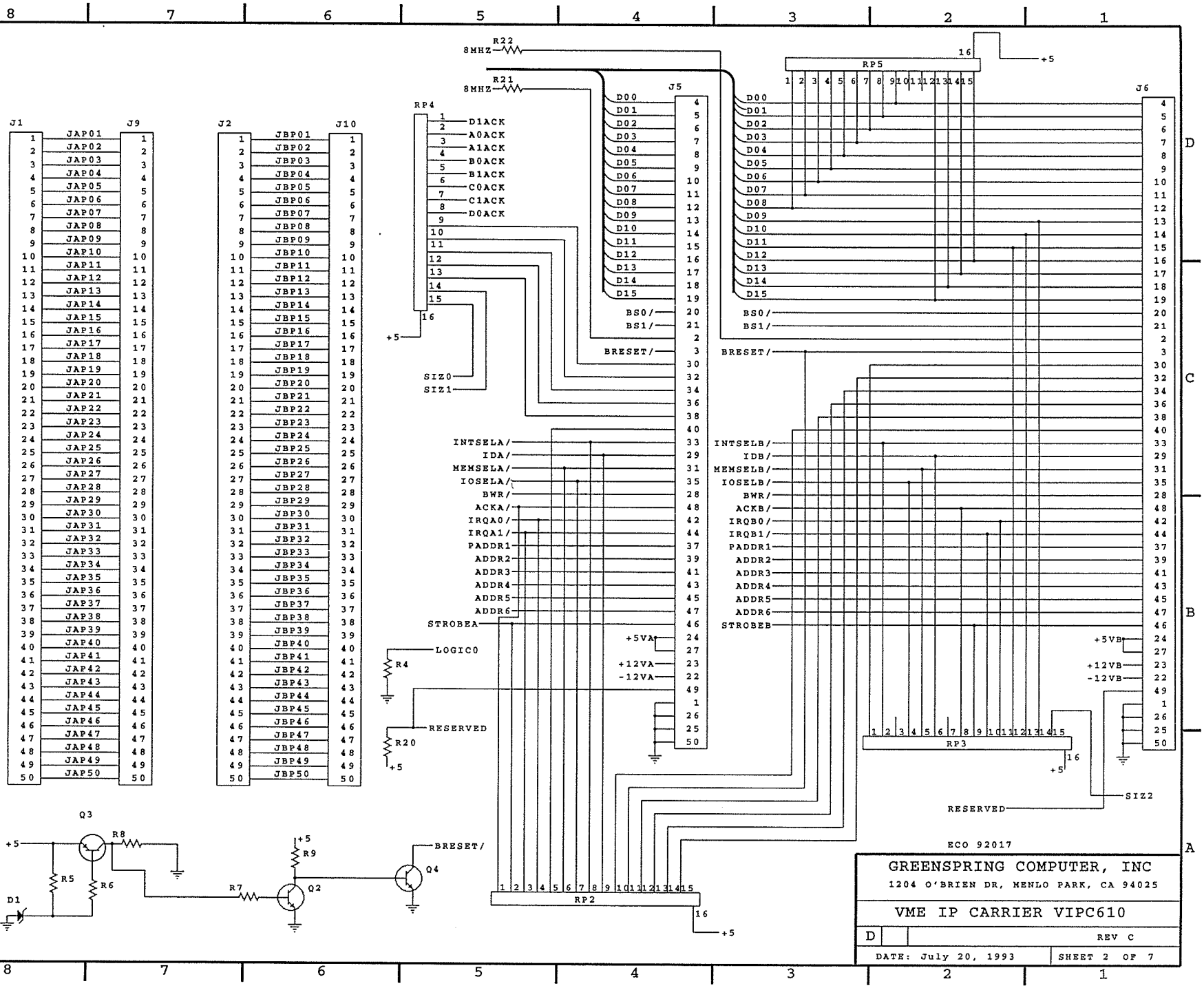


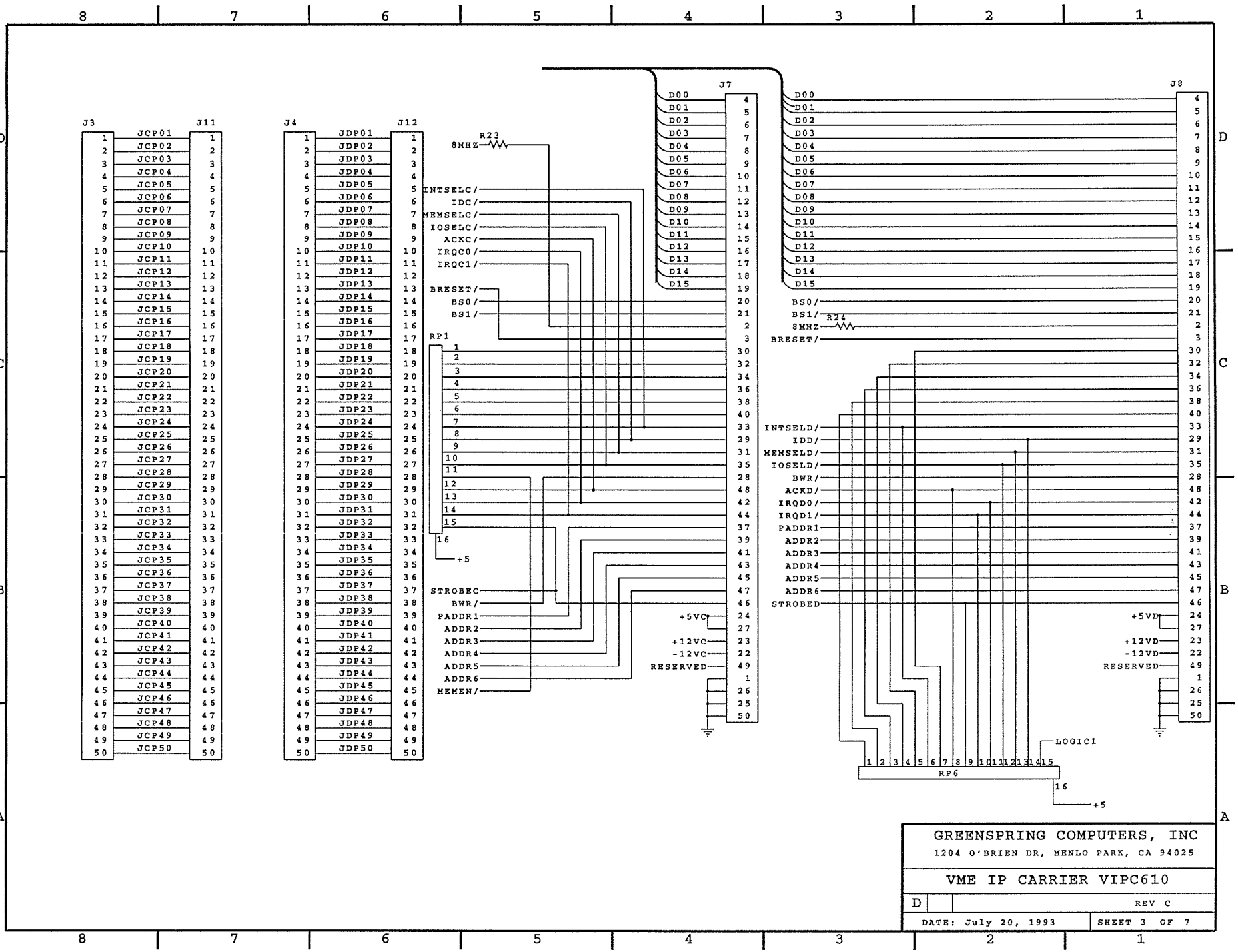
Assembly Notes:

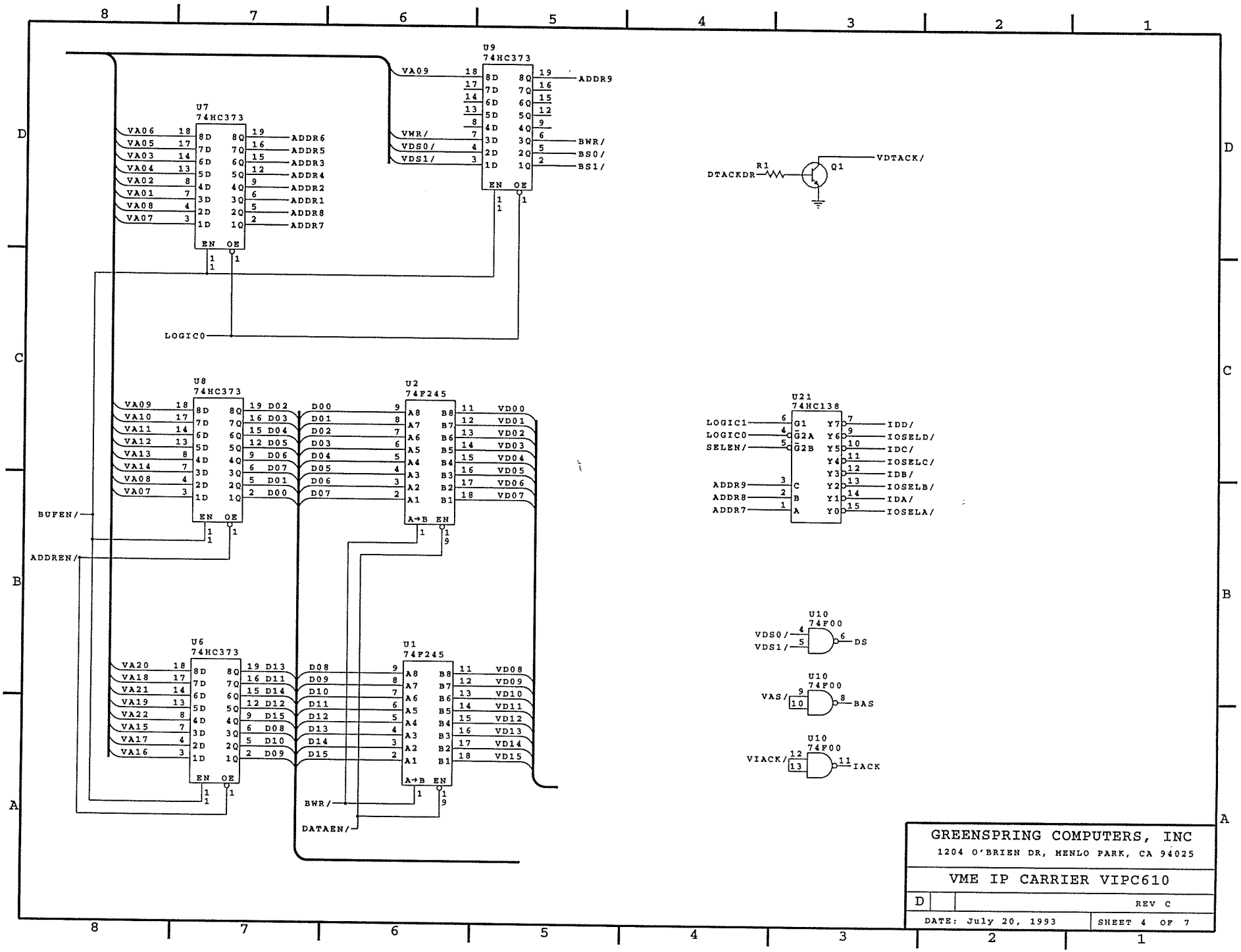
1: Component Lead Length On Solder Side Is Not To Exceed .040".
2: Assemble Per Quality Standards IPC Class II.
3: Exposed Copper On Solder Side Is Not Acceptable.
4: Warp / Twist Not To Exceed .010".
5: Connectors P1, P2, J1-J12 Must Be Parallel With Board.
6: All Locations Are Filled Except E16-19 (mask off these locations).
7: Load Headers and Shunts Per This Drawing.

GREENSPRING COMPUTERS, INC.		
	ASSEMBLY:4001610263	DRAWN BY: Fred Trevor
VIPC610 ELECTRONIC ASSEMBLY		
REV: C	Apr 11, 1994	SHEET: 1 of 1

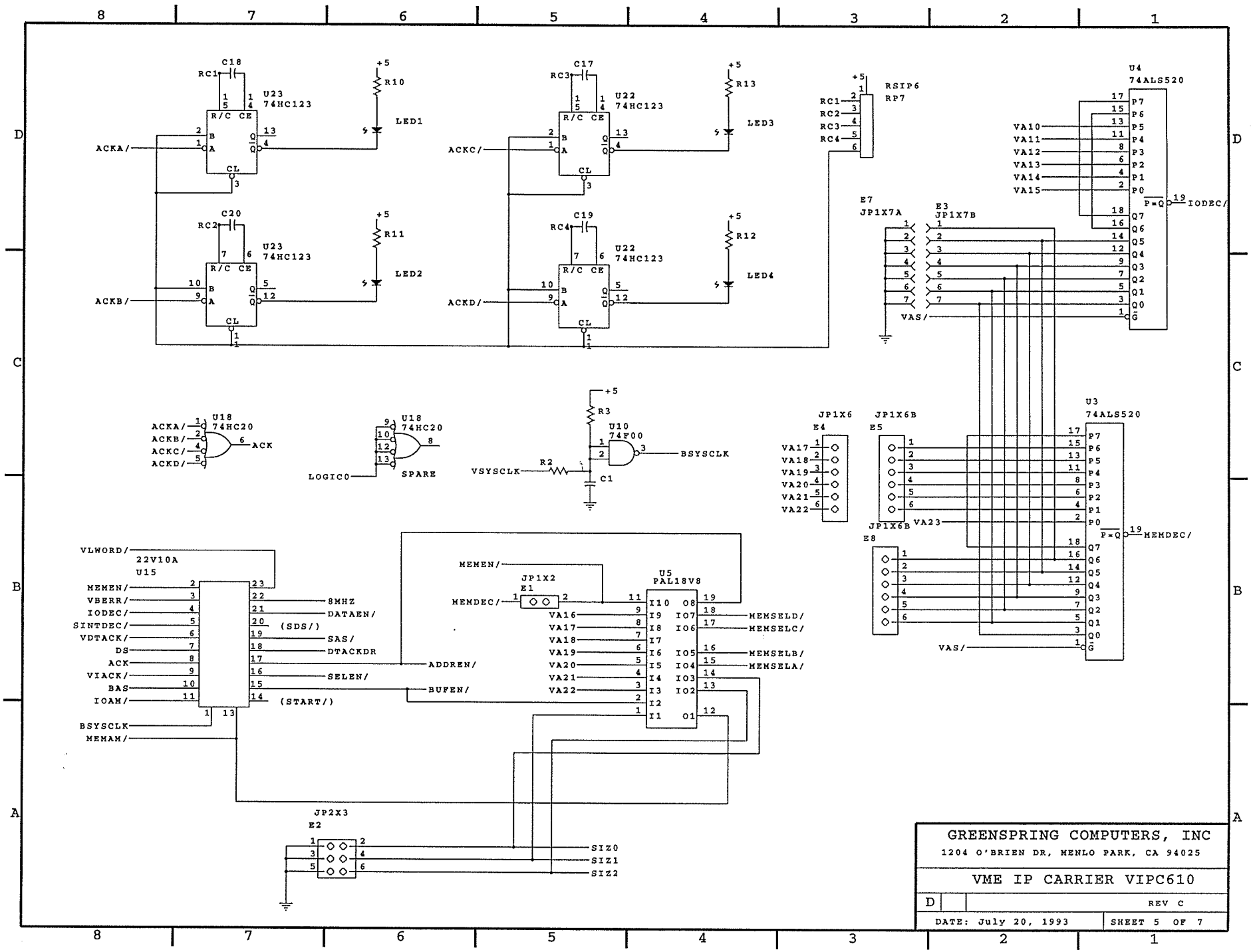

P1 CONNECTOR PINOUT
P96 P1A
A1 VD00
A2 VD01
A3 VD02
A4 VD03
A5 VD04
A6 VD05
A7 VD06
A8 VD07
A9
A10 VSYSCLK
A11
A12 VDS1/
A13 VDS0/
A14 VWR/
A15
A16 VDTACK/
A17
A18 VAS/
A19
A20 VIACK/
A21 VIACKIN/
A22 VIACKOUT/
A23 VAM4
A24 VA07
A25 VA06
A26 VA05
A27 VA04
A28 VA03
A29 VA02
A30 VA01
A31
A32
P96 P1B
B1
B2
B3
B4 VBG0/
B5
B6 VBG1/
B7
B8 VBG2/
B9
B10 VBG3/
B11
B12
B13
B14
B15
B16 VAM0
B17 VAM1
B18 VAM2
B19 VAM3
B20
B21
B22
B23
B24 VIRQ7/
B25 VIRQ6/
B26 VIRQ5/
B27 VIRQ4/
B28 VIRQ3/
B29 VIRQ2/
B30 VIRQ1/
B31
B32
P96 P1C
C1 VD08
C2 VD09
C3 VD10
C4 VD11
C5 VD12
C6 VD13
C7 VD14
C8 VD15
C9
C10
C11 VBERR/
C12 VRESET/
C13 VLWORD/
C14 VAM5
C15 VA23
C16 VA22
C17 VA21
C18 VA20
C19 VA19
C20 VA18
C21 VA17
C22 VA16
C23 VA15
C24 VA14
C25 VA13
C26 VA12
C27 VA11
C28 VA10
C29 VA09
C30 VA08
C31
C32
FUSE F5
-12V
FUSE F6
+5
C21
C2
C4
C3
JP1X2-1A E16
JP1X2-1A E17
JP1X2-1A E18
JP1X2-1A E19
GND2
PLANE UNDER JA, JB
FUSE F1
L1 NFM61D
IN
OUT
GND
+5VA
C5
FUSE F2
L4 NFM61D
+5VB
C8
L2 NFM61D
+12V
+12VA
C6
L5 NFM61D
+12VB
C9
L3 NFM61D
-12VA
C7
L6 NFM61D
-12VB
C10
FUSE F3
+5
L7 NFM61D
+5VC
C11
FUSE F4
L10 NFM61D
+5VD
C14
L9 NFM61D
+12VC
C13
L12 NFM61D
+12VD
C16
L8 NFM61D
-12V
-12VC
C12
L11 NFM61D
-12VD
C15
GREENSPRING COMPUTERS, INC
1204 O'BRIEN DR, MENLO PARK, CA 94025
VME IP CARRIER VIPC610
D
REV C
DATE: July 20, 1993
SHEET 1 OF 7


J1
J9
JAP01
JAP02
JAP03
JAP04
JAP05
JAP06
JAP07
JAP08
JAP09
JAP10
JAP11
JAP12
JAP13
JAP14
JAP15
JAP16
JAP17
JAP18
JAP19
JAP20
JAP21
JAP22
JAP23
JAP24
JAP25
JAP26
JAP27
JAP28
JAP29
JAP30
JAP31
JAP32
JAP33
JAP34
JAP35
JAP36
JAP37
JAP38
JAP39
JAP40
JAP41
JAP42
JAP43
JAP44
JAP45
JAP46
JAP47
JAP48
JAP49
JAP50
J2
J10
JBP01
JBP02
JBP03
JBP04
JBP05
JBP06
JBP07
JBP08
JBP09
JBP10
JBP11
JBP12
JBP13
JBP14
JBP15
JBP16
JBP17
JBP18
JBP19
JBP20
JBP21
JBP22
JBP23
JBP24
JBP25
JBP26
JBP27
JBP28
JBP29
JBP30
JBP31
JBP32
JBP33
JBP34
JBP35
JBP36
JBP37
JBP38
JBP39
JBP40
JBP41
JBP42
JBP43
JBP44
JBP45
JBP46
JBP47
JBP48
JBP49
JBP50
R22
8MHZ
R21
8MHZ
RP4
D1ACK
A0ACK
A1ACK
B0ACK
B1ACK
C0ACK
C1ACK
D0ACK
+5
SIZ0
SIZ1
J5
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
BS0/
BS1/
BRESET/
INTSELA/
IDA/
MEMSELA/
IOSELA/
BWR/
ACKA/
IRQA0/
IRQA1/
PADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
STROBEA
+5VA
+12VA
-12VA
LOGIC0
R4
RESERVED
R20
+5
RP5
16
+5
J6
D00
D01
D02
D03
D04
D05
D06
D07
D08
D09
D10
D11
D12
D13
D14
D15
BS0/
BS1/
BRESET/
INTSELB/
IDB/
MEMSELB/
IOSELB/
BWR/
ACKB/
IRQB0/
IRQB1/
PADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
STROBEB
+5VB
+12VB
-12VB
RP3
16
+5
SIZ2
RESERVED
RP2
16
+5
Q3
R8
+5
R5
R6
D1
R7
Q2
+5
R9
BRESET/
Q4
ECO 92017
GREENSPRING COMPUTER, INC
1204 O'BRIEN DR, MENLO PARK, CA 94025
VME IP CARRIER VIPC610
D
REV C
DATE: July 20, 1993
SHEET 2 OF 7

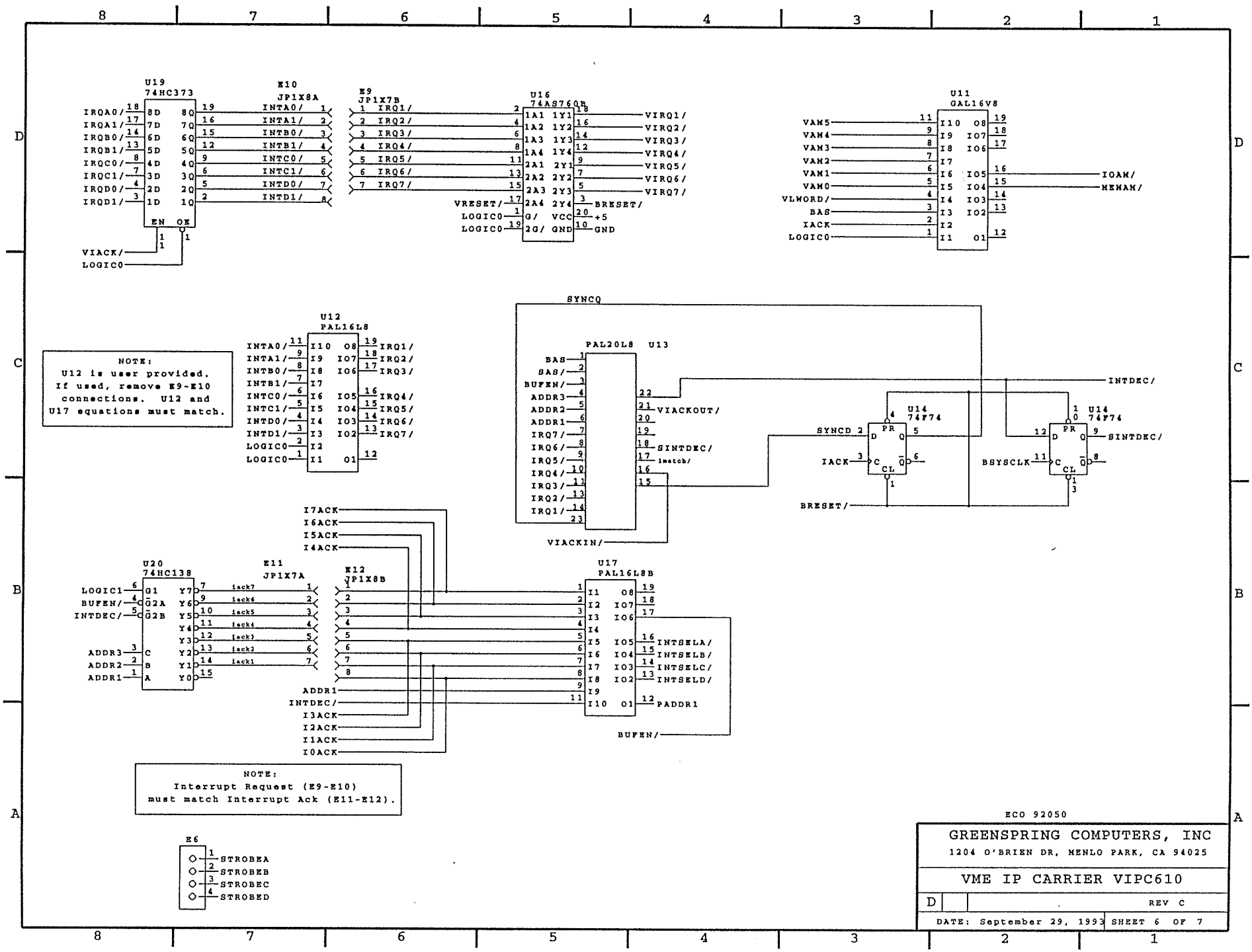

J3
J11
JCP01 JCP02 JCP03 JCP04 JCP05 JCP06 JCP07 JCP08 JCP09 JCP10 JCP11 JCP12 JCP13 JCP14 JCP15 JCP16 JCP17 JCP18 JCP19 JCP20 JCP21 JCP22 JCP23 JCP24 JCP25 JCP26 JCP27 JCP28 JCP29 JCP30 JCP31 JCP32 JCP33 JCP34 JCP35 JCP36 JCP37 JCP38 JCP39 JCP40 JCP41 JCP42 JCP43 JCP44 JCP45 JCP46 JCP47 JCP48 JCP49 JCP50
J4
J12
JDP01 JDP02 JDP03 JDP04 JDP05 JDP06 JDP07 JDP08 JDP09 JDP10 JDP11 JDP12 JDP13 JDP14 JDP15 JDP16 JDP17 JDP18 JDP19 JDP20 JDP21 JDP22 JDP23 JDP24 JDP25 JDP26 JDP27 JDP28 JDP29 JDP30 JDP31 JDP32 JDP33 JDP34 JDP35 JDP36 JDP37 JDP38 JDP39 JDP40 JDP41 JDP42 JDP43 JDP44 JDP45 JDP46 JDP47 JDP48 JDP49 JDP50
R23
8MHZ
INTSELC/
IDC/
MEMSELC/
IOSELC/
ACKC/
IRQC0/
IRQC1/
BRESET/
BS0/
BS1/
RP1
+5
STROBEC
BWR/
PADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
MEMEN/
J7
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15
+5VC
+12VC
-12VC
RESERVED
J8
D00 D01 D02 D03 D04 D05 D06 D07 D08 D09 D10 D11 D12 D13 D14 D15
BS0/
BS1/
R24
8MHZ
BRESET/
INTSELD/
IDD/
MEMSELD/
IOSELD/
BWR/
ACKD/
IRQD0/
IRQD1/
PADDR1
ADDR2
ADDR3
ADDR4
ADDR5
ADDR6
STROBED
+5VD
+12VD
-12VD
RESERVED
LOGIC1
RP6
+5
GREENSPRING COMPUTERS, INC
1204 O'BRIEN DR, MENLO PARK, CA 94025
VME IP CARRIER VIPC610
D
REV C
DATE: July 20, 1993
SHEET 3 OF 7

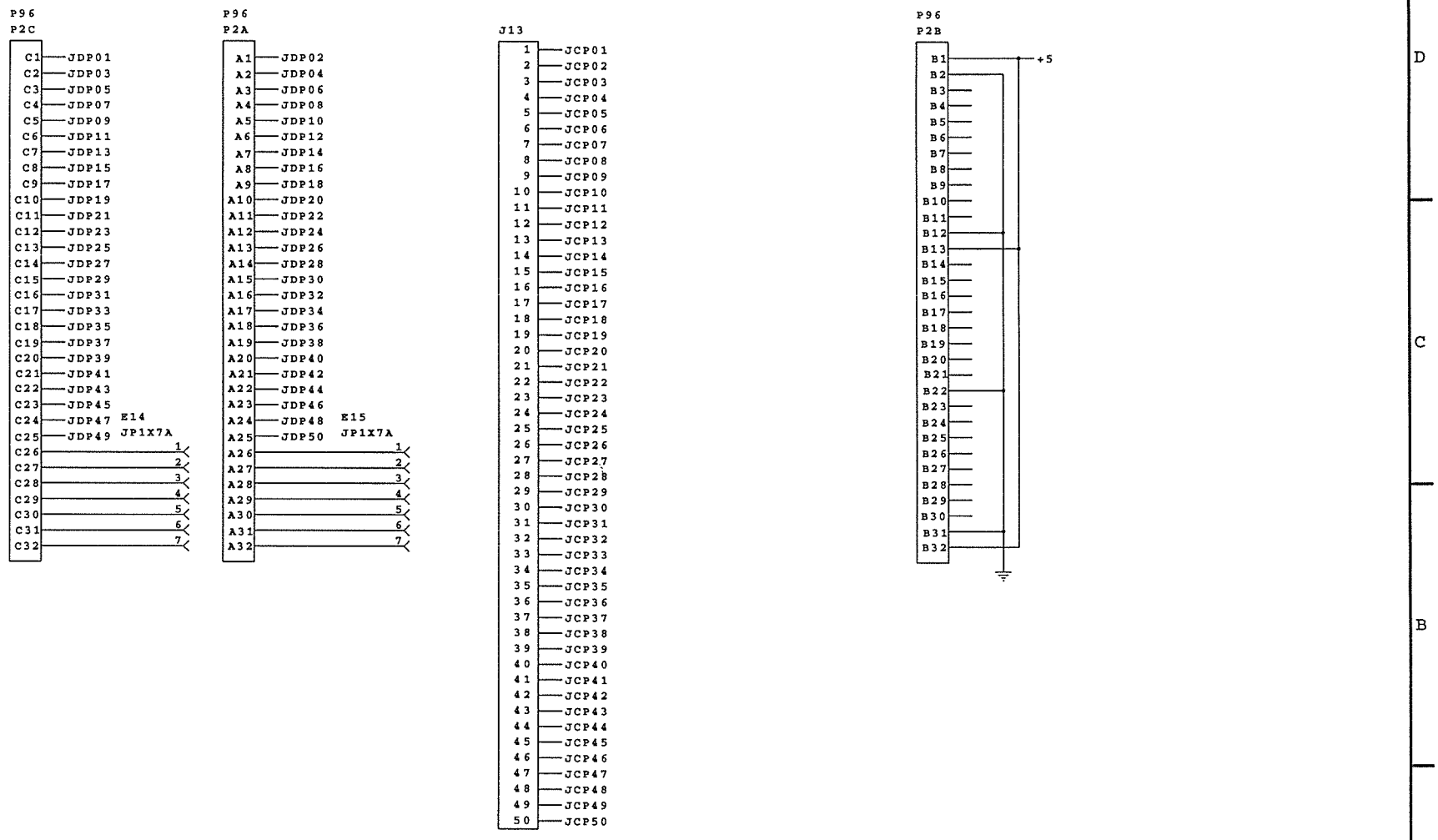


GREENSPRING COMPUTERS, INC	
1204 O'BRIEN DR, MENLO PARK, CA 94025	
VME IP CARRIER VIPC610	
D	REV C
DATE: July 20, 1993	SHEET 4 OF 7



GREENSPRING COMPUTERS, INC	
1204 O'BRIEN DR, MENLO PARK, CA 94025	
VME IP CARRIER VIPC610	
D	REV C
DATE: July 20, 1993	SHEET 5 OF 7


U19
74HC373
E10
JP1X8A
E9
JP1X7B
U16
74AS760B
U11
GAL16V8
U12
PAL16L8
NOTE:
U12 is user provided.
If used, remove E9-E10
connections. U12 and
U17 equations must match.
SYNCQ
PAL20L8 U13
U14
74F74
U14
74F74
INTDEC/
VIACKOUT/
SINTDEC/
imatch/
VIACKIN/
SYNCD 2
IACK
BSYSCLK
BRESET/
SINTDEC/
I7ACK
I6ACK
I5ACK
I4ACK
U20
74HC138
E11
JP1X7A
E12
JP1X8B
U17
PAL16L8B
INTSELA/
INTSELB/
INTSELC/
INTSELD/
PADDR1
BUFEN/
I3ACK
I2ACK
I1ACK
I0ACK
NOTE:
Interrupt Request (E9-E10)
must match Interrupt Ack (E11-E12).
E6
STROBEA
STROBEB
STROBEC
STROBED
ECO 92050
GREENSPRING COMPUTERS, INC
1204 O'BRIEN DR, MENLO PARK, CA 94025
VME IP CARRIER VIPC610
D
REV C
DATE: September 29, 1993
SHEET 6 OF 7



GREENSPRING COMPUTERS, INC	
1204 O'BRIEN DR, MENLO PARK, CA 94025	
VME IP CARRIER VIPC610	
D	REV C
DATE: July 20, 1993	SHEET 7 OF 7

```
PARTNO          G42203E;
NAME            G42203E;
REVISION        E;
DATE            25 SEPTEMBER  91;
DESIGNER        DAVE BLISS;
COMPANY         GREENSPRING COMPUTERS, INC.;
ASSEMBLY        VIPC610B;
LOCATION        U15;
DEVICE          p22V10;
FORMAT          J;

/*  COPYRIGHT 1989, GREENSPRING COMPUTERS, INC. */

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*      This PAL is the primary controller for the 6U VME                */
/*      IP Carrier VIPC610                                               */
/*                                                                       */
/*      Allowable target device is CMOS 22V10 only.                      */
/*      Compile with CUPL -jlxm1 .                                       */
/*                                                                       */
/*************************************************************************/

/**     INPUTS  **/

PIN     1       =       BSYSCLK;/* Buffered VME bus SYSCLK*              */
PIN     2       =       !MEMEN; /* Memory Address Decode for IPs         */
PIN     3       =       !VBERR; /* VME bus BERR*                         */
PIN     4       =       !IODEC; /* I/O Decode from comparitor            */
PIN     5       =       !SINTDEC;/* Interrupt Cycle from synchronizer    */
PIN     6       =       !VDTACK;/* VME bus DTACK*                        */
PIN     7       =       DS;     /* VME bus DS1* OR DS0*                  */
PIN     8       =       ACK;    /* Acknowledge input from IPs            */
PIN     9       =       !VIACK; /* VME bus IACK*                         */
PIN     10      =       BAS;    /* VME bus AS*, buffered                 */
PIN     11      =       !IOAM;  /* VME bus AM<5:0>= SHORT I/O SPACE      */
PIN     13      =       !MEMAM; /* VME bus AM<5:0>= Std. Mem. Access     */
PIN     23      =       !VLWORD;/* VME bus LWORD                         */


/**  OUTPUTS  **/

PIN     22      =       8MHZ;           /* Clock for IPs                 */
PIN     21      =       !DATAEN;        /* Enables VME to IP Data Buffers*/
PIN     20      =       !SDS;           /* Synchronized Data Strobe      */
PIN     19      =       !SAS;           /* Synchronized Address Strobe   */
PIN     18      =       DTACKDR;        /* to VME bus DTACK*             */
PIN     17      =       !ADDREN;        /* Enables VME address to IPs    */
PIN     16      =       !SELEN;         /* IO and ID selector enable     */
PIN     15      =       !BUFEN;         /* Control line buffer enable    */
PIN     14      =       !START;         /* Beginning of cycle            */


/**  LOGIC EQUATIONS  **/

/*      START activates one cycle following the select cycle for each of */
/*      cycle types, i.e. memory, I/O, or Interrupt. It's purpose is to  */
/*      provide an interlock to prevent assertion of DTACK too early     */
/*      relative to availability of data from IP.                        */
START.D         =       !8MHZ & ADDREN & !DTACKDR
                #       !8MHZ & DATAEN & !DTACKDR
                #       !8MHZ & SELEN & !DTACKDR
                #       START & 8MHZ;

/*      This is the clock to the Industry Packs (IPs).
```

```
Most of the signals to the IPs must by synchronized to this signal,
thus it appears in most terms below.  It is the VME bus SYSCLK
divided by two.
*/
8MHZ.D          =       !8MHZ;

/*      SDS is the synchronized VME bus data strobe. The input is
the OR of DS1 and DS0.  The selectors on this board do not recogize
a VME bus cycle until this signal is true.  This is also the
handshake signal with DTACK*.
*/
SDS.D           =       DS;

/*      SAS is the synchronized VME bus address strobe. The selectors
on this board do not recogize a VME bus cycle until this signal is true.
DTACK and BERR are included in this term because address lines are
not guaranteed to be valid when DTACK or BERR are asserted.
*/
SAS.D           =       BAS & !VDTACK & !VBERR & !ACK;

/*      ADDREN is used on memory reads and writes to the IPs.
This signal is high for exacly one clock.  The conditions are that
the decoder output is true, AS* and DSx* have been recognized
(synchronized) and the modifier codes are true.  "!ADDREN" and
"!DATAEN" are used to shut down after the one clock. The "!BUFEN"
term guarantees that on closely spaced VME cycles (or where DTACK
overlaps the next cycle) we recognize two distinct cycles.
*/
ADDREN.D        =       !8MHZ & SAS & SDS & MEMEN & MEMAM & !VIACK
                                & !DATAEN & !ADDREN & !BUFEN
                #       ADDREN & 8MHZ;

/*      DATAEN turns on upon one of three conditions:
(i) an interrupt cycle,
(ii) an I/O cycle, or
(iii) a memory cycle after ADDREN.
It stays on as long as the VME bus data strobe is still true,
then turns off synchronous to the 8MHZ clock.  */
DATAEN.D        =       !8MHZ & SAS & SDS & VIACK & SINTDEC & !BUFEN
                #       !8MHZ & SAS & SDS & !VIACK & IODEC & IOAM & !BUFEN
                #       !8MHZ & ADDREN
                #       DATAEN & 8MHZ
                #       DATAEN & SDS;

/*      SELEN enables the I/O and ID (in the I/O space) selector
that generates the signals to the IPs.
*/
SELEN.D         =       !8MHZ & SAS & SDS & !VIACK & IODEC & IOAM & !BUFEN
                #       SELEN & 8MHZ
                #       SELEN & SDS;

/*      BUFEN enables the interrupt selector that generates the
signals to the IPs. It is similar to SELEN.  It also has a second,
unrelated purpose: it causes the memory decode signals to latch,
and also latches the primary address latches. Finally, it is also
used to gate the MEMSEL and BS signals to the IPs. On IO and ID
signals it stays on one clock longer than SELEN to hold addresses
valid during IOSEL turnoff.
*/
BUFEN.D         =       !8MHZ & SAS & SDS & MEMEN & MEMAM & !VIACK
                                & !DATAEN & !ADDREN & !BUFEN
                #       !8MHZ & SAS & SDS & !VIACK & IODEC & IOAM & !BUFEN
                #       !8MHZ & SAS & SDS & VIACK & SINTDEC & !BUFEN
                #       BUFEN & SELEN
                #       BUFEN & 8MHZ
                #       BUFEN & SDS;
```

```
/*      DTACKDR turns on DTACK* on the VME bus as soon as
a valid (gated by !8MHZ) Acknowledge is received from either Pack.
It stays on until handshaked with SDS.  Note that on memory cycles
the Pack may generate an "early" ACK, which is ignored, because
DATAEN is not valid yet.  The first SDS term is needed to keep DTACK
from turning on a second time, after DS* has gone away, but before ACK
from the IP has gone away. (DATAEN stays on either one or two clocks
after SDS, but SDS must be off two clock minimum.)
*/
DTACKDR.D       =       DATAEN & ACK & SDS & !8MHZ & START
                #       DTACKDR & SELEN
                #       DTACKDR & 8MHZ
                #       DTACKDR & SDS;


/**  HOUSEKEEPING EQUATIONS  **/

8MHZ.ar         =       'b'0;
8MHZ.sp         =       'b'0;
DATAEN.ar       =       'b'0;
DATAEN.sp       =       'b'0;
SDS.ar          =       'b'0;
SDS.sp          =       'b'0;
SAS.ar          =       'b'0;
SAS.sp          =       'b'0;
DTACKDR.ar      =       'b'0;
DTACKDR.sp      =       'b'0;
ADDREN.ar       =       'b'0;
ADDREN.sp       =       'b'0;
SELEN.ar        =       'b'0;
SELEN.sp        =       'b'0;
BUFEN.ar        =       'b'0;
BUFEN.sp        =       'b'0;
START.sp        =       'b'0;
START.ar        =       'b'0;
```

```
PARTNO          G42205B;
NAME            G42205B;
REVISION        B;
DATE            17 Aug 92;
DESIGNER        DAVE BLISS;
COMPANY         GREENSPRING COMPUTERS, INC.;
ASSEMBLY        VIPC610B;
LOCATION        U5;
DEVICE          f18v8zs;
FORMAT          j;

/*  COPYRIGHT 1992, GREENSPRING COMPUTERS, INC.  */

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*      This PAL is part of the memory decoder for the VIPC610.          */
/*      It also performs some gating and latching functions.             */
/*                                                                       */
/*                                                                       */
/*                                                                       */
/*                                                                       */
/*      G42205A is a "makefrom" based on G42204B. Changes part from a    */
/*      16v8 to an 18v8 in order to add MEMAM to select decode logic     */
/*                                                                       */
/*      Rev. B, 17 Aug 92, adds ADDREN as an input and set term          */
/*      timing qualifier in order to prevent false selects occurring     */
/*      as a result of address/address modifiers changing prior to de-   */
/*      assertion of address strobe.                                     */
/*************************************************************************/

/**     INPUTS  **/

PIN     1       =       SIZ1;           /* Memory size from jumper group*/
PIN     2       =       !BUFEN;         /* Buffer enable input          */
PIN     3       =       VA22;           /* VME bus Address 22           */
PIN     4       =       VA21;           /* VME bus Address 21           */
PIN     5       =       VA20;           /* VME bus Address 20           */
PIN     6       =       VA19;           /* VME bus Address 19           */
PIN     7       =       VA18;           /* VME bus Address 18           */
PIN     8       =       VA17;           /* VME bus Address 17           */
PIN     9       =       VA16;           /* VME bus Address 16           */
PIN     11      =       !MEMEN;         /* Memory enable from decoder   */
PIN     12      =       !MEMAM;         /* Memory addr. modifier decode */
PIN     13      =       SIZ2;           /* Memory size from jumper group*/
PIN     14      =       SIZ0;           /* Memory size from jumper group*/
PIN     19      =       !ADDREN;        /* Ack drive signal to VDTACK   */

/**  OUTPUTS  **/

PIN     18      =       !MEMSELD;       /* Memory Select for Pack D     */
PIN     17      =       !MEMSELC;       /* Memory Select for Pack C     */
PIN     16      =       !MEMSELB;       /* Memory Select for Pack B     */
PIN     15      =       !MEMSELA;       /* Memory Select for Pack A     */


/**  INTERMEDIATE EQUATIONS  **/

/*      Shunt (jumper) in is logic zero, shown below as "!SIZ,"
Shunt out is logic one, as "SIZ."
*/
siz_64K         =       !SIZ0 & !SIZ1 & !SIZ2;
                                /*  64 KB per IP, 256 KB on carrier     */
siz_128K        =        SIZ0 & !SIZ1 & !SIZ2;
                                /*  128 KB per IP,  512 KB on carrier   */
siz_256K        =       !SIZ0 &  SIZ1 & !SIZ2;
                                /*  256 KB per IP,  1 MB on carrier     */
```

```
siz_512K        =       SIZ0 &  SIZ1 & !SIZ2;
                                /*  512 KB per IP,  2 MB on carrier     */
siz_1M          =      !SIZ0 & !SIZ1 &  SIZ2;
                                /*  1 MBper IP,  4 MB on carrier        */
siz_2M          =       SIZ0 & !SIZ1 &  SIZ2;
                                /*  2 MBper IP,  8 MB on carrier        */
siz_4M          =      !SIZ0 &  SIZ1 &  SIZ2;
                                /*  2 MBper IP,  16 MB on carrier       */
siz_8M          =       SIZ0 &  SIZ1 &  SIZ2;
                                /*  8 MBper IP,  16 MB on carrier       */
                                /*  This is not supported               */

MEMSEL          =      MEMEN & MEMAM & ADDREN;
                                /*  Address lines and modifiers decode. */


/**  LOGIC EQUATIONS  **/

/*      MEMSELA turns when when the primary memory comparitor
output (MEMSEL) is true, and the appropriate address lines for
the memory size are low.  It stays on during BUFEN to permit address
pipelining.  It is gated by BUFEN to become synchronous with the
8 MHz clock.
*/
MEMSELA         =       MEMSEL & !SIZ2 & !SIZ1 & !SIZ0 & !VA16 & !VA17 & BUFEN
                #       MEMSEL & !SIZ2 & !SIZ1 &  SIZ0 & !VA17 & !VA18 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 & !SIZ0 & !VA18 & !VA19 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 &  SIZ0 & !VA19 & !VA20 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 & !SIZ0 & !VA20 & !VA21 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 &  SIZ0 & !VA21 & !VA22 & BUFEN
                #       MEMSELA & BUFEN;

/*      MEMSELB turns when when the primary memory comparitor
output (MEMSEL) is true, and the appropriate address lines for
the memory size are valid.  It stays on during BUFEN to permit address
pipelining.  It is gated by BUFEN to become synchronous with the
8 MHz clock.
*/
MEMSELB         =       MEMSEL & !SIZ2 & !SIZ1 & !SIZ0 & VA16 & !VA17 & BUFEN
                #       MEMSEL & !SIZ2 & !SIZ1 &  SIZ0 & VA17 & !VA18 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 & !SIZ0 & VA18 & !VA19 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 &  SIZ0 & VA19 & !VA20 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 & !SIZ0 & VA20 & !VA21 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 &  SIZ0 & VA21 & !VA22 & BUFEN
                #       MEMSELB & BUFEN;

/*      MEMSELC turns when when the primary memory comparitor
output (MEMSEL) is true, and the appropriate address lines for
the memory size are valid.  It stays on during BUFEN to permit address
pipelining.  It is gated by BUFEN to become synchronous with the
8 MHz clock.
*/
MEMSELC         =       MEMSEL & !SIZ2 & !SIZ1 & !SIZ0 & !VA16 & VA17 & BUFEN
                #       MEMSEL & !SIZ2 & !SIZ1 &  SIZ0 & !VA17 & VA18 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 & !SIZ0 & !VA18 & VA19 & BUFEN
                #       MEMSEL & !SIZ2 &  SIZ1 &  SIZ0 & !VA19 & VA20 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 & !SIZ0 & !VA20 & VA21 & BUFEN
                #       MEMSEL &  SIZ2 & !SIZ1 &  SIZ0 & !VA21 & VA22 & BUFEN
                #       MEMSELC & BUFEN;

/*      MEMSELD turns when when the primary memory comparitor
output (MEMSEL) is true, and the appropriate address lines for
the memory size are high.  It stays on during BUFEN to permit address
pipelining.  It is gated by BUFEN to become synchronous with the
8 MHz clock.
*/
```

```
MEMSELD     =    MEMSEL & !SIZ2 & !SIZ1 & !SIZ0 & VA16 & VA17 & BUFEN
                 MEMSEL & !SIZ2 & !SIZ1 &  SIZ0 & VA17 & VA18 & BUFEN
                 MEMSEL & !SIZ2 &  SIZ1 & !SIZ0 & VA18 & VA19 & BUFEN
                 MEMSEL & !SIZ2 &  SIZ1 &  SIZ0 & VA19 & VA20 & BUFEN
                 MEMSEL &  SIZ2 & !SIZ1 & !SIZ0 & VA20 & VA21 & BUFEN
                 MEMSEL &  SIZ2 & !SIZ1 &  SIZ0 & VA21 & VA22 & BUFEN
                 MEMSELD & BUFEN;
```

```
PARTNO          G42206B;
NAME            G42206B;
REVISION        B;
DATE            12/18/91;
DESIGNER        DAVE BLISS (KIM RUBIN);
COMPANY         GREENSPRING COMPUTERS, INC.;
ASSEMBLY        VIPC610B;
LOCATION        U13;
DEVICE          g20v8;
FORMAT          j;

/*  COPYRIGHT 1990, GREENSPRING COMPUTERS,INC.
/*********************************************************************/
/*                                                                   */
/*      This PAL is the interrupt controller for the                 */
/*      6U VMEbus IP carrier.  The basic output of this PAL          */
/*      is whether a VMEbus interrupt input is ours, or should       */
/*      be passed on.                                                */
/*                                                                   */
/*      Allowable target device is GAL as 20L8 only.                 */
/*                                                                   */
/*      Rev A   3/1/89  XKR                                          */
/*      GAL     3/5/90  XKR                                          */
/*      G42206B 12/18/91 DB                                          */
/*      G42206B is a "makefrom" based on G40406A for VIPC610 Rev. B. */
/*      The P/N has changed in order to adopt the new numbering scheme. */
/*********************************************************************/


/**     INPUTS  **/


PIN     14      =       !IRQ1;  /* Latched Int Req from jumper group    */
PIN     13      =       !IRQ2;  /* Latched Int Req from jumper group    */
PIN     11      =       !IRQ3;  /* Latched Int Req from jumper group    */
PIN     10      =       !IRQ4;  /* Latched Int Req from jumper group    */
PIN     9       =       !IRQ5;  /* Latched Int Req from jumper group    */
PIN     8       =       !IRQ6;  /* Latched Int Req from jumper group    */
PIN     7       =       !IRQ7;  /* Latched Int Req from jumper group    */
PIN     6       =       ADDR1;  /* Latched VME bus address 1            */
PIN     5       =       ADDR2;  /* Latched VME bus address 2            */
PIN     4       =       ADDR3;  /* Latched VME bus address 3            */
PIN     2       =       !SAS;   /* Synchronized VME bus AS*             */
PIN     1       =       BAS;    /* Buffered AS from VMEbus              */
PIN     3       =       !BUFEN; /* Buffer enable from control PAL       */
PIN     16      =       !VIACKIN;/* VME bus IACKIN*                     */
PIN     18      =       !SINTDEC;/* From sychronizer                    */
PIN     23      =       SYNCQ;  /* Q output from Int Synch  FF          */


/**  OUTPUTS  **/


PIN     15      =       SYNCD;  /* D input to Int Synch FF              */
PIN     17      =       !IMATCH;/*  intemediate output                  */
PIN     22      =       !INTDEC;/* Interrupt Decode output             */
PIN     21      =       !VIACKOUT;/* VME bus IACKOUT*                   */


/**  INTERMEDIATE EQUATIONS  **/


intmatch        =       ((IRQ1 & !ADDR3 & !ADDR2 &  ADDR1)/*  level 1   */
                #        (IRQ2 & !ADDR3 &  ADDR2 & !ADDR1)/*  level 2   */
                #        (IRQ3 & !ADDR3 &  ADDR2 &  ADDR1)/*  level 3   */
                #        (IRQ4 &  ADDR3 & !ADDR2 & !ADDR1)/*  level 4   */
                #        (IRQ5 &  ADDR3 & !ADDR2 &  ADDR1)/*  level 5   */
```

```
                #         (IRQ6 &  ADDR3 &  ADDR2 & !ADDR1)/*  level 6   */
                #         (IRQ7 &  ADDR3 &  ADDR2 &  ADDR1));/*  level 7 */


/**  LOGIC EQUATIONS  **/


IMATCH          =         intmatch;

/*      SYNCD is the data to the interrupt synchronizing FF.
It is simply the OR of the possible interrupt requests.
*/
SYNCD           =         IRQ1
                #         IRQ2
                #         IRQ3
                #         IRQ4
                #         IRQ5
                #         IRQ6
                #         IRQ7;

/*      INTDEC means that it is our interrupt. For this to be true,
the interrupt synchronzing FF output Q must be true, and also the
VMEbus address lines must match one of our requests.  INTDEC, once true,
is held by BUFEN so that the INTSEL signals to the IPs will not
deselect asynchronously.  This output is asynchronous because VIACKIN
can come at any time...either before or after VAS, VIACK, etc.  It is
synchronized in a 74F74.
*/
INTDEC          =         SYNCQ & VIACKIN & SAS & IMATCH
                #         SINTDEC & BUFEN;

/*      VIACKOUT is VMEbus IACKOUT*.  This is true if and only if
INTDEC is not true, but a VMEbus cycle is in progress and we
have IACKIN*. There are two reasons that we would pass IACK.
(1) We have no interrupt pending, in which case SYNCQ is low.
(2) We have an interrupt pending but this cycle is not for that,
in which case the address lines do not match and the term "intmatch"
is low.  VIACKOUT goes away with the VMEbus AS*.
*/
VIACKOUT        =         !SYNCQ & VIACKIN & SAS & BAS
                #         SYNCQ & VIACKIN & SAS & BAS & !IMATCH;
```

```
PARTNO          G42208A;
NAME            G42208A;
REVISION        A;
DATE            19 DEC 91;
DESIGNER        DAVE BLISS;
COMPANY         GREENSPRING COMPUTERS, INC.;
ASSEMBLY        VIPC610B;
LOCATION        U11;
DEVICE          g16v8;  /* as 16L8  */
FORMAT          j;

/*  COPYRIGHT 1989, GREENSPRING COMPUTERS, INC.  */

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*      This PAL is address modifier decoder for the VIPC610B.           */
/*                                                                       */
/*      Rev A:                                                           */
/*      GAL                                                              */
/*************************************************************************/

/**     INPUTS  **/

PIN     1       =       LOGIC0;         /* Input permanently tied to 0  */
PIN     2       =       IACK;           /* Interrupt Acknowledge        */
PIN     3       =       BAS;            /* Board Address Strobe         */
PIN     4       =       !VLWORD;        /* VME Long Word                */
PIN     5       =       VAM0;           /* VME Address Modifier 0       */
PIN     6       =       VAM1;           /* VME Address Modifier 1       */
PIN     7       =       VAM2;           /* VME Address Modifier 2       */
PIN     8       =       VAM3;           /* VME Address Modifier 3       */
PIN     9       =       VAM4;           /* VME Address Modifier 4       */
PIN     11      =       VAM5;           /* VME Address Modifier 5       */


/**  OUTPUTS  **/

PIN     16      =       !IOAM;          /* VAM<5:0>=29h or 2Dh.         */
PIN     15      =       !MEMAM;         /* VAM<5:0>=39h, 3Ah, 3Dh, or   */
                                        /*          3Eh.                */
PIN     14      =       !SPARE;         /*                              */

/*   INTERMEDIATE VARIABLES                                             */

ipenable        =       (BAS & !VLWORD & !IACK);
field am        =       [VAM5..0];
/**  LOGIC EQUATIONS  **/

/*
!IOAM activates when address modifiers <5:0> decode a 29h or 2Dh.


*/

IOAM            =       ipenable & am:[29]
                #       ipenable & am:[2D];

/*
!MEMAM activates when address modifiers <5:0> decode a 39h, 3Ah, 3Dh, or 3Eh.
*/

MEMAM           =       ipenable & am:[39]
                #       ipenable & am:[3A]
                #       ipenable & am:[3D]
                #       ipenable & am:[3E];
```

```
PARTNO          G42209A;
NAME            G42209A;
REVISION        A;
DATE            31 Oct 91;
DESIGNER        DAVE BLISS;
COMPANY         GREENSPRING COMPUTERS,INC.;
ASSEMBLY        VIPC610 Rev. B;
LOCATION        U17;
DEVICE          g16v8;
FORMAT          j;

/* COPYRIGHT 1989, GREESPRING COMPUTERS, INC.  */

/*************************************************************************/
/*                                                                       */
/*                                                                       */
/*      This PAL is the interrupt decoder for the                        */
/*      6U VMEbus IP carrier.                                            */
/*                                                                       */
/*      This PAL may be used to implement special interrupt maps         */
/*      The default equations simply match straight jumpering            */
/*      and straight encode/decoding                                     */
/*                                                                       */
/*      Allowable target device is CMOS 16V8 only.                       */
/*      Compile with CUPL -jlxm1.                                        */
/*                                                                       */
/*      Rev B same as A.  10 Mar 89                                      */
/*      GAL     18 June 90                                               */
/*      G42209A is a "make-from" based on G42207C. It is identical       */
/*      except for the input pin assignment order which has been         */
/*      reversed.       31 Oct 91                                        */
/*************************************************************************/


/**     INPUTS  **/

PIN     1       =       !IRQ7;  /* From VMEbus via decoder              */
PIN     2       =       !IRQ6;  /* From VMEbus via decoder              */
PIN     3       =       !IRQ5;  /* From VMEbus via decoder              */
PIN     4       =       !IRQ4;  /* From VMEbus via decoder              */
PIN     5       =       !IRQ3;  /* From VMEbus via decoder              */
PIN     6       =       !IRQ2;  /* From VMEbus via decoder              */
PIN     7       =       !IRQ1;  /* From VMEbus via decoder              */
PIN     8       =       !IRQ0;  /* Bonus position input                 */
PIN     9       =       ADDR1;  /* From VMEbus interface                */
PIN     11      =       !INTDEC;/* From ICON610 PAL                     */
PIN     17      =       !BUFEN; /* From BCON610 PAL                     */


/**  OUTPUTS  **/

PIN     16      =       !INTSELA;       /* To Pack A                    */
PIN     15      =       !INTSELB;       /* To Pack B                    */
PIN     14      =       !INTSELC;       /* To Pack C                    */
PIN     13      =       !INTSELD;       /* To Pack C                    */
PIN     12      =       PADDR1;         /* IP address line 1            */


/**  INTERMEDIATE EQUATIONS  **/

INTSELA         =       IRQ1
                #       IRQ2
                #       INTSELA & BUFEN ;
```

```
INTSELB         =       IRQ3
                #       IRQ4
                #       INTSELB & BUFEN ;

INTSELC         =       IRQ5
                #       IRQ6
                #       INTSELC & BUFEN ;

INTSELD         =       IRQ7
                #       IRQ0
                #       INTSELD & BUFEN ;

PADDR1          =       INTDEC & IRQ2
                #       INTDEC & IRQ4
                #       INTDEC & IRQ6
                #       INTDEC & IRQ0
                #       !INTDEC & ADDR1 ;
```

```
PARTNO          G52211B;
NAME            G52211B;
REVISION        B;
DATE            Jan 20, 1992;
DESIGNER        DAVE BLISS (KIM RUBIN);
COMPANY         GREENSPRING COMPUTERS,INC.;
ASSEMBLY        VIPC610;
LOCATION        U17;
DEVICE          g16v8;
FORMAT          j;

/* COPYRIGHT 1989, GREESPRING COMPUTERS, INC.  */

/*************************************************************************/
/*      VIPC610 Rev B Option -01                                         */
/*                                                                       */
/*      This PAL is the interrupt decoder for the                        */
/*      6U VMEbus IP carrier.                                            */
/*                                                                       */
/*      This PAL is the mate to G52212B, which makes the VIPC610B        */
/*      look like two VIPC310s.                                          */
/*              Revisions                                                */
/*      XKR     A       14 Sept 1989                                     */
/*      CJS     B       21 June 1990    Corrects Padr1 polarity on       */
/*                                      Iack cycle                       */
/*      DJB     B       20 Jan 1992     G52211B is a "makefrom" based    */
/*                                      on G42201B "special". It is      */
/*                                      identical except for the input   */
/*                                      pin assignment order, which has  */
/*                                      been reversed.                   */
/*                                                                       */
/*      Remove any shunts and wires on E9, E10, E11, and E12             */
/*                                                                       */
/*      Add wire wrap wires:    E10-1 to E12-8                           */
/*                              E10-2 to E12-5                           */
/*                              E10-3 to E12-2                           */
/*                              E10-4 to E12-1                           */
/*                                                                       */
/*      Add shunts:             E11-3 to E12-3                           */
/*                              E11-4 to E12-4                           */
/*                              E11-6 to E12-6                           */
/*                              E11-7 to E12-7                           */
/*************************************************************************/


/**     INPUTS  **/

/*      IRQs are interrupt acknowledges from the VMEbus.
        INTs are interrupt requests from the IPs.
*/
PIN     1       =       !INTB1; /* From IP IRQ latch via wire           */
PIN     2       =       !INTB0; /* From IP IRQ latch via wire           */
PIN     3       =       !IRQ5;  /* From VMEbus via decoder              */
PIN     4       =       !IRQ4;  /* From VMEbus via decoder              */
PIN     5       =       !INTA1; /* From IP IRQ latch via wire           */
PIN     6       =       !IRQ2;  /* From VMEbus via decoder              */
PIN     7       =       !IRQ1;  /* From VMEbus via decoder              */
PIN     8       =       !INTA0; /* From IP IRQ latch via wire           */
PIN     9       =       ADDR1;  /* From VMEbus interface                */
PIN     11      =       !INTDEC;/* From ICON610 PAL                     */
PIN     17      =       !BUFEN; /* From BCON610 PAL                     */


/**  OUTPUTS  **/
```

```
PIN     16      =       !INTSELA;       /* To Pack A                    */
PIN     15      =       !INTSELB;       /* To Pack B                    */
PIN     14      =       !INTSELC;       /* To Pack C                    */
PIN     13      =       !INTSELD;       /* To Pack D                    */
PIN     12      =       PADDR1;         /* IP address line 1            */

/** LOGIC EQUATIONS **/


INTSELA         =       INTA0 & IRQ4
                #       INTA1 & IRQ5
                #       INTSELA & BUFEN ;

INTSELB         =       INTB0 & IRQ2
                #       INTB1 & IRQ1
                #       INTSELB & BUFEN ;

INTSELC         =       !INTA0 & IRQ4
                #       !INTA1 & IRQ5
                #       INTSELC & BUFEN ;

INTSELD         =       !INTB0 & IRQ2
                #       !INTB1 & IRQ1
                #       INTSELD & BUFEN ;

PADDR1          =       INTDEC & IRQ5
                #       INTDEC & IRQ1
                #       !INTDEC & ADDR1 ;
```

```
PARTNO          G52212B;
NAME            G52212B;
REVISION        B;
DATE            20 Jan 92;
DESIGNER        DAVE BLISS (KIM RUBIN);
COMPANY         GREENSPRING COMPUTERS, INC.;
ASSEMBLY        VIPC610;
LOCATION        U12;
DEVICE          g16v8;  /* as 16L8  */
FORMAT          j;

/*  COPYRIGHT 1989, GREENSPRING COMPUTERS, INC.   */
/*********************************************************************/
/*                                                                   */
/*      This PAL is the interrupt encoder for the                    */
/*      VIPC610 IP carrier.  The basic output of this PAL            */
/*      goes through a driver, then to the VMEbus IRQ* lines.        */
/*                                                                   */
/*      This part makes the VIPC610 look like two VIPC310 boards.    */
/*                                                                   */
/*      Rev A:  14 Sept 89                                           */
/*      GAL:    18 June 90                                           */
/*      REV B:  27 JULY 90   REVED WITH NO CHANGES TO MATCH G42201 PAL */
/*      G52212B is same for Rev. B boards as G42202B is for Rev. A   */
/*      boards; matches g52211b PAL.                                 */
/*********************************************************************/


/**     INPUTS  **/

PIN     11      =       !INTA0;         /* From IP A                */
PIN     9       =       !INTA1;         /* From IP A                */
PIN     8       =       !INTB0;         /* From IP B                */
PIN     7       =       !INTB1;         /* From IP B                */
PIN     6       =       !INTC0;         /* From IP C                */
PIN     5       =       !INTC1;         /* From IP C                */
PIN     4       =       !INTD0;         /* From IP D                */
PIN     3       =       !INTD1;         /* From IP D                */


/**  OUTPUTS  **/

PIN     19      =       !IRQ1;          /* To VMEbus IRQ1*          */
PIN     18      =       !IRQ2;          /* To VMEbus IRQ2*          */
PIN     17      =       !IRQ3;          /* To VMEbus IRQ3*          */
PIN     16      =       !IRQ4;          /* To VMEbus IRQ4*          */
PIN     15      =       !IRQ5;          /* To VMEbus IRQ5*          */
PIN     14      =       !IRQ6;          /* To VMEbus IRQ6*          */
PIN     13      =       !IRQ7;          /* To VMEbus IRQ7*          */


/**  INTERMEDIATE EQUATIONS  **/


/**  LOGIC EQUATIONS  **/

IRQ1    =       INTB1
        #       INTD1 ;

IRQ2    =       INTB0
        #       INTD0 ;

IRQ4    =       INTA0
        #       INTC0 ;

IRQ5    =       INTA1
        #       INTC1 ;
```