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**Description and Instructions
For An
ECL 16 Channel Fanout Module
With Camac Programmable Pulse Width**

**Jefferson Lab
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10 October 2000

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1.0 Introduction

The detector subsystems at Jefferson Lab use commercial discriminator modules to create logic level signals from analog pulses. The discriminator or comparator modules allow the user to set a predetermined threshold that prevents undesired analog signals from creating logic level signals. The desired analog signals that cross the threshold limit produce typical logic signals such as NIM or ECL levels that drive the inputs of front end instrumentation modules.

On many occasions the discriminated logic level pulses drive two types of instrumentation modules. For instance, a Time to Digital Converter [TDC] and Scaler module may be connected to the same discriminator unit. If the user desires another logic level output from the discriminator module the need for a logic fanout unit is created.

2.0 Purpose of Module

The sixteen-(16) channel ECL fanout module described in this manual is designed to distribute two differential ECL outputs for each differential ECL input channel. Each input channel can accept a wide range of input pulse widths and the user can program the pulse width output via CAMAC command. All pulse width outputs are controlled from one command. Inputs of various widths will be converted to the programmed pulse width. The default output pulse width is user configurable and is normally set for 200nS. The module will power-up with the default pulse width output setting.

3.0 Brief Functional Description

The ECL Fanout with programmable output width module is comprised of the following four (4) sections:

- I. CAMAC Interface and Power Supply Distribution
- II. ECL Input
- III. Pulse Width Control
- IV. ECL Output

• CAMAC Interface Registers and Power Distribution

The ECL programmable pulse width fanout module follows the IEEE-583-1975 standard for modular instrumentation, signal levels and interface definitions of the CAMAC standard backplane.

The CAMAC write lines, and bus control lines are connected to a Xilinx® Complex Programmable Logic Device[CPLD]. The CPLD decodes the CAMAC command listed in the following tables as a valid command and initiates the proper read or write function. The proper CAMAC backplane acknowledge signal is returned to the CAMAC controller to verify that a CAMAC cycle was executed properly.

The ECL programmable pulse width fanout module uses three CAMAC backplane supplied voltages. Each voltage passes through a properly rated fuse. The CAMAC backplane power requirement defines a well-regulated very low voltage ripple [noise] and the voltages are not regulated on board the module. Table 2 lists the required voltages and measured current requirements.

Backplane Voltage	Required Current	Total Power: 14.08 Watts	Fuse
+ 6 VDC	0.100 Amps	0.6 W	1 Amp [F1]
+12 VDC	0.081 Amps	0.972 W	1 Amp [F2]
-12 VDC	0.043 Amps	0.516 W	1 Amp [F3]
-6 VDC	2.0 Amps	12 W	3 Amp [F4]

• ECL Input Section

The ECL inputs are received differentially from the front panel connector P1. Each input pair is terminated to 100Ω. ECL polarity is labeled on the front panel and the input signals should follow this convention for proper operation.

• Pulse Width Control Section

Pulse width is controlled by use of a MC10198 ECL monostable device. The pulse width is set by a combination of external resistor and capacitor. One feature of the MC10198 is the ability to control the output pulse width by

changing the voltage on pin seven of the device. The ECL programmable pulse width is precisely adjusted by changing the voltage applied to the control pin. A twelve bit Digital to Analog Converter is used to set the voltage via CAMAC command.

- **Pulse Width Control Section (Continued)**

The default maximum pulse width at power on is set by the combination of resistor and capacitor values. In this case the default [maximum] setting at power on is 200nS. The user can program the pulse width by CAMAC command, which essentially drives the DAC to a precise voltage setting. The different voltage settings from the DAC change the output pulse width from the MC10198.

Each MC10198 can be configured using a jumper to operate in either a non-updating or updating mode. In non-updating mode the programmed pulse will not produce another pulse, or accept another trigger, until the initial pulse is complete. The monostable device has a finite recovery time before accepting another input [trigger]. The updating mode will produce an output pulse for every input pulse received. If the input pulses arrive at a high rate the output will be at a constant level or “on” until the input [trigger] is removed. The updating or non updating feature can be changed on a channel by channel basis by installing or removing a jumper.

- **ECL Output Section**

Dual outputs for each input channel are driven by use of a MC10H101 ECL line driver. Each output is driven differentially to the front panel output connectors P2 and P3. The polarity of the ECL signals is identical to the input connector scheme and the connectors are polarized. The seventeenth (17th) connector pair is unused.

Each output pin is pulled down to –5.2V through a 470Ω resistor. This enables the user to view the output pulse width using an oscilloscope probe that is terminated to 1MegΩ.

4.0 Specifications

Single Wide CAMAC IEEE-STD 583-1975 module

INPUT Specifications

Front Panel

P1: Two (2) rows by seventeen (17) pin polarized connector.

17th pair not connected

Nominal ECL voltage levels required from source device.

Maximum input frequency:	This is a function of output pulse width setting assuming non-updating mode. For 15ns output pulse width setting, the maximum input frequency is 30Mhz.
Minimum input pulse width:	>3nS.

Output Specifications

Front Panel

P2 and P3: Two (2) rows by seventeen (17) pin polarized connector.

17th pair not connected

Minimum output pulse width:	15nS
Maximum output pulse width:	User adjustable. Default setting is 200nS. Maximum pulse width can be adjusted and will require calibration in the Electronics lab.
Maximum output current	50mA per channel
Input to Output Delay:	<10nS per channel <1nS deviation for all channels
Pulse Width Jitter:	<1nS per channel <3ns deviation for all channels

Digital to Analog Converter: [Pulse Width Control]

12 Bit resolution. User selectable full scale range of +2.5Vdc; +5.0Vdc; or +10.0 volt full scale.

Jumper selectable range. Default setting is +2.5Vdc

12 bit data is straight binary format. 0V = 0000h; +Full Scale = 0FFFh

Data is latched into Xilinx CPLD during Camac Write cycle.

5.0 Instructions

5.0.1 Setting the user selectable jumpers.

a) Updating and Non-Updating Mode [J1 – J16]

The user can select the output mode for each monostable circuit. The user should record the jumper settings for each channel. The jumpers will be installed as default and which places each monostable in the NON-updating mode. Removing the jumper places the monostable in updating mode.

b) Full Scale DAC output [J17 – J19]

The programmable pulse width is achieved by varying the voltage to each monostable circuit's control pin. The full scale DAC output can be changed by a jumper. Normally users should not modify the default jumper position as the board has been calibrated in the lab with the selected DAC setting.

5.0.2 CAMAC Commands

The module produces a valid response, [X=1] for the following CAMAC functions:

F16	A0	Write Data to DAC
F0	A0	Read Data
F9	A0	Clear Command

The F16 command is the only command that is implemented on the Xilinx CAMAC decoder chip. The Read [F0] and Clear [F9] functions will produce a valid command response and illuminate the 'N' indicator light on the front panel of the module, but are not used for the present design.

The F16 – A0 command is used to write data to the twelve bit DAC. The data is in "straight" binary format where 0x0000 sets the DAC to zero and 0x0FFF sets the DAC to full scale. Setting the DAC to zero programs the widest [default] output pulse.

Graph 1 on the following page shows the typical curve for DAC counts vs. pulse width output. The curve is typical of all channels on the board.

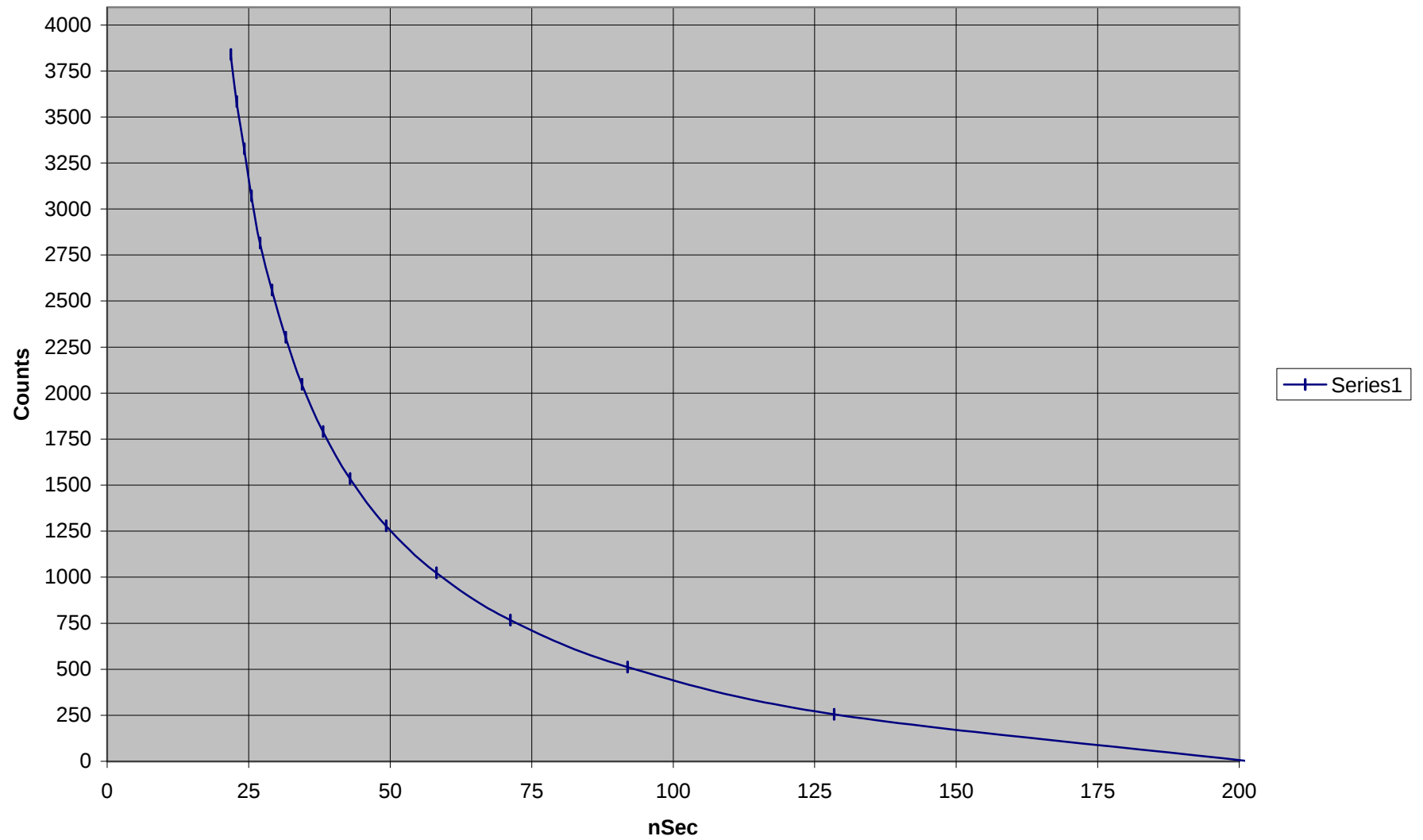
6.0 Appendices [

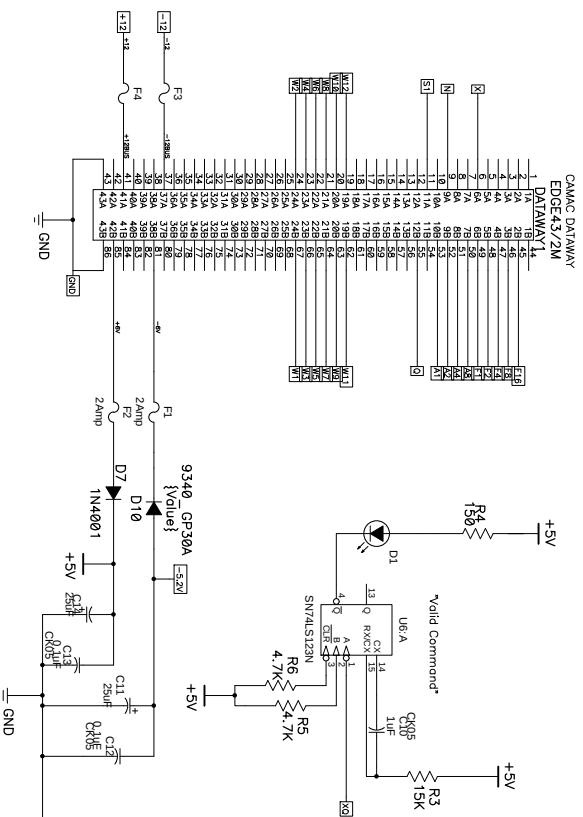
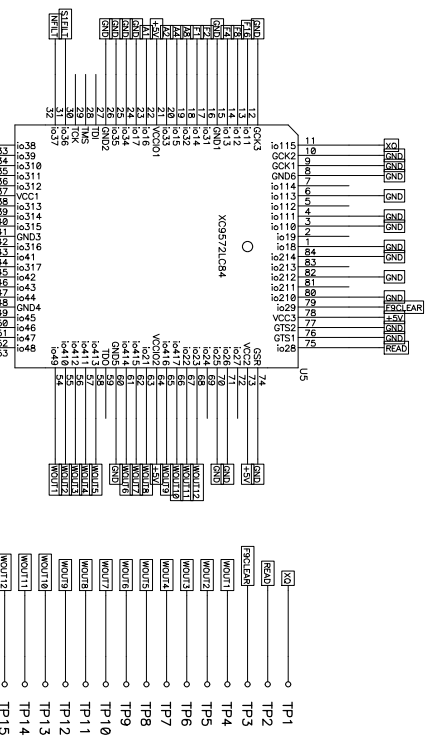
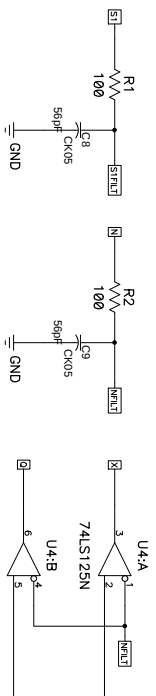
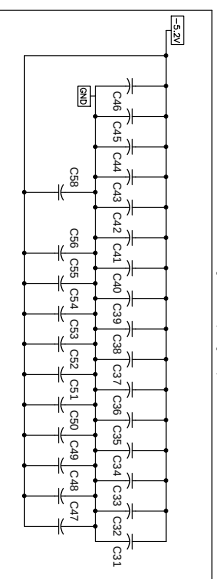
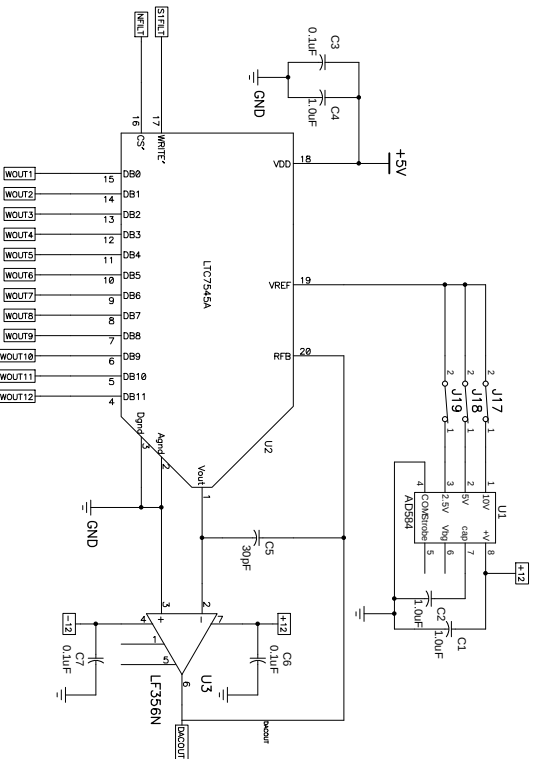
6.0.1 Schematics

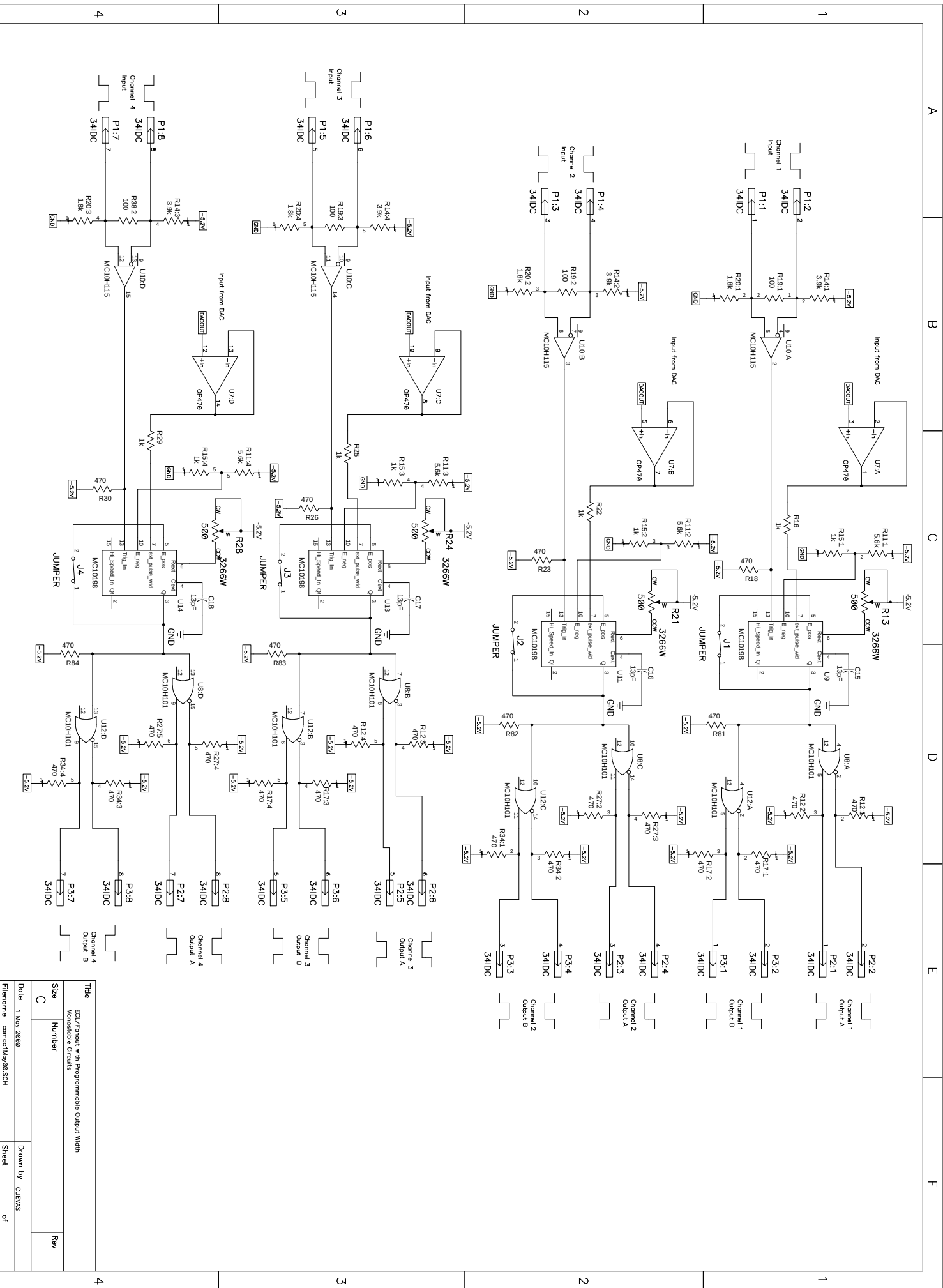
6.0.2 Component Designator Diagram

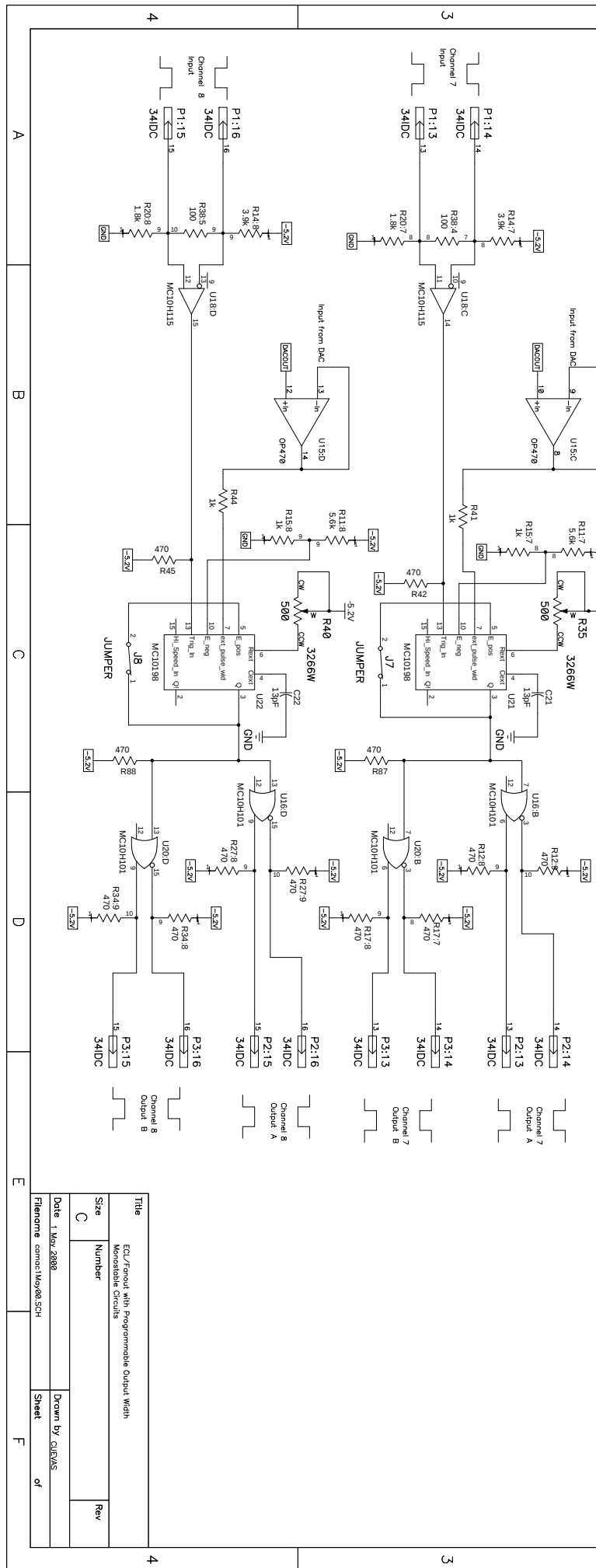
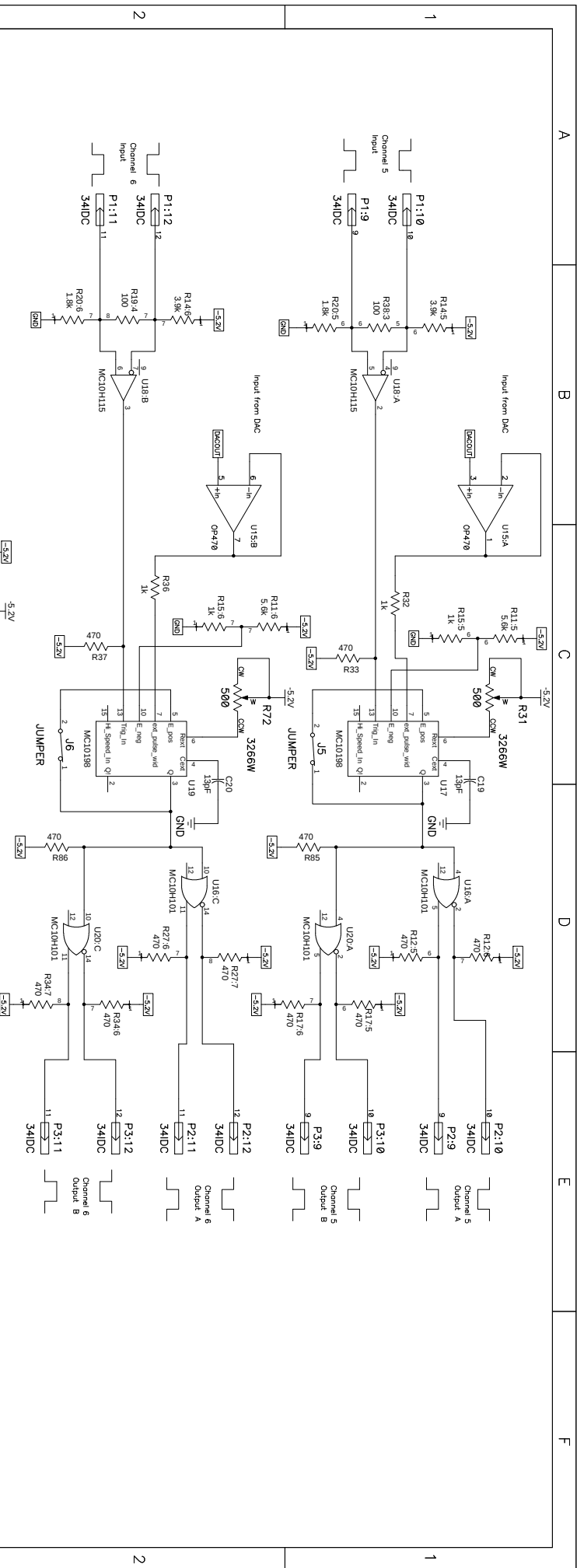
6.0.3 Parts List

DAC Counts Vs Pulse Width

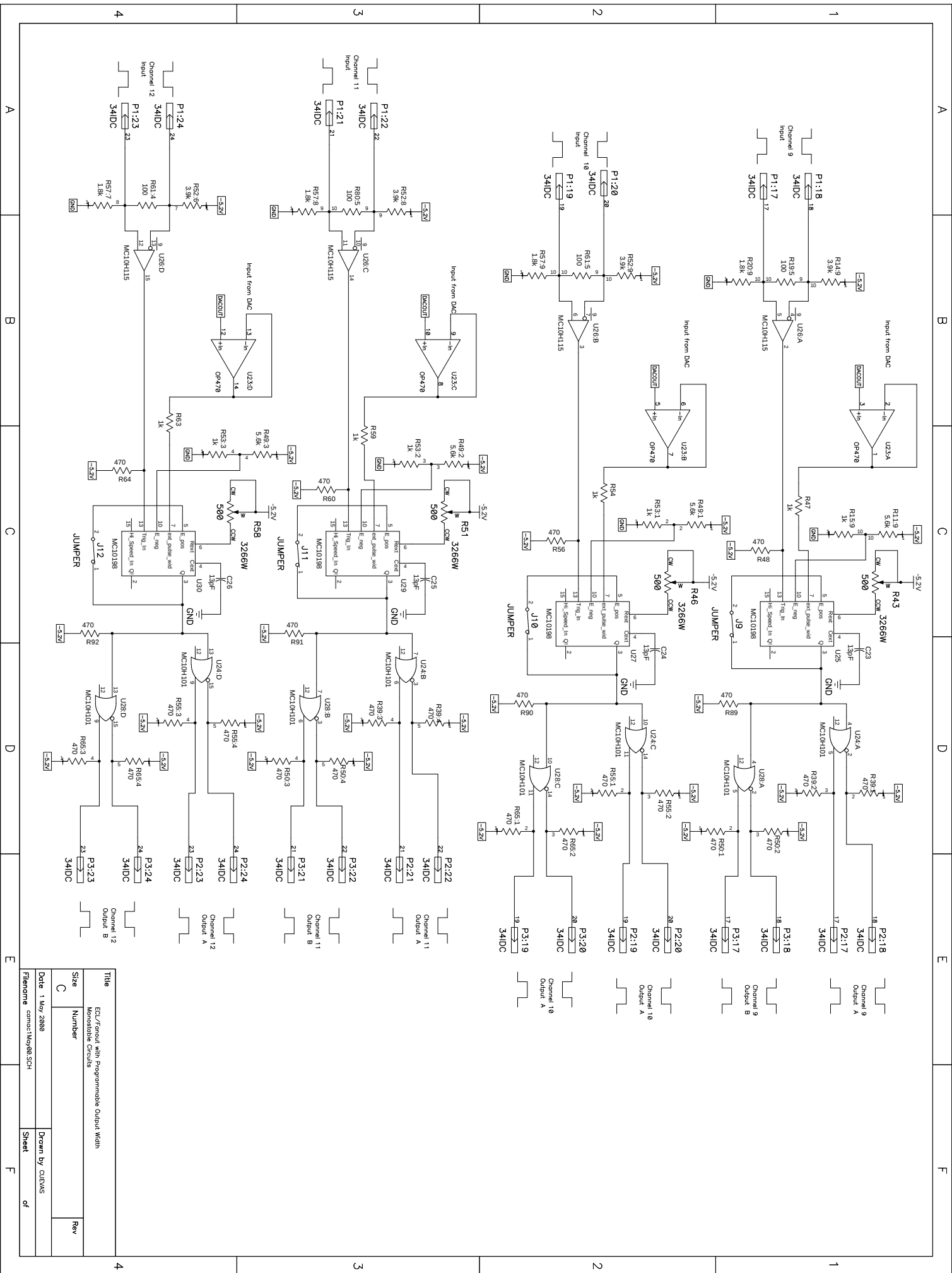




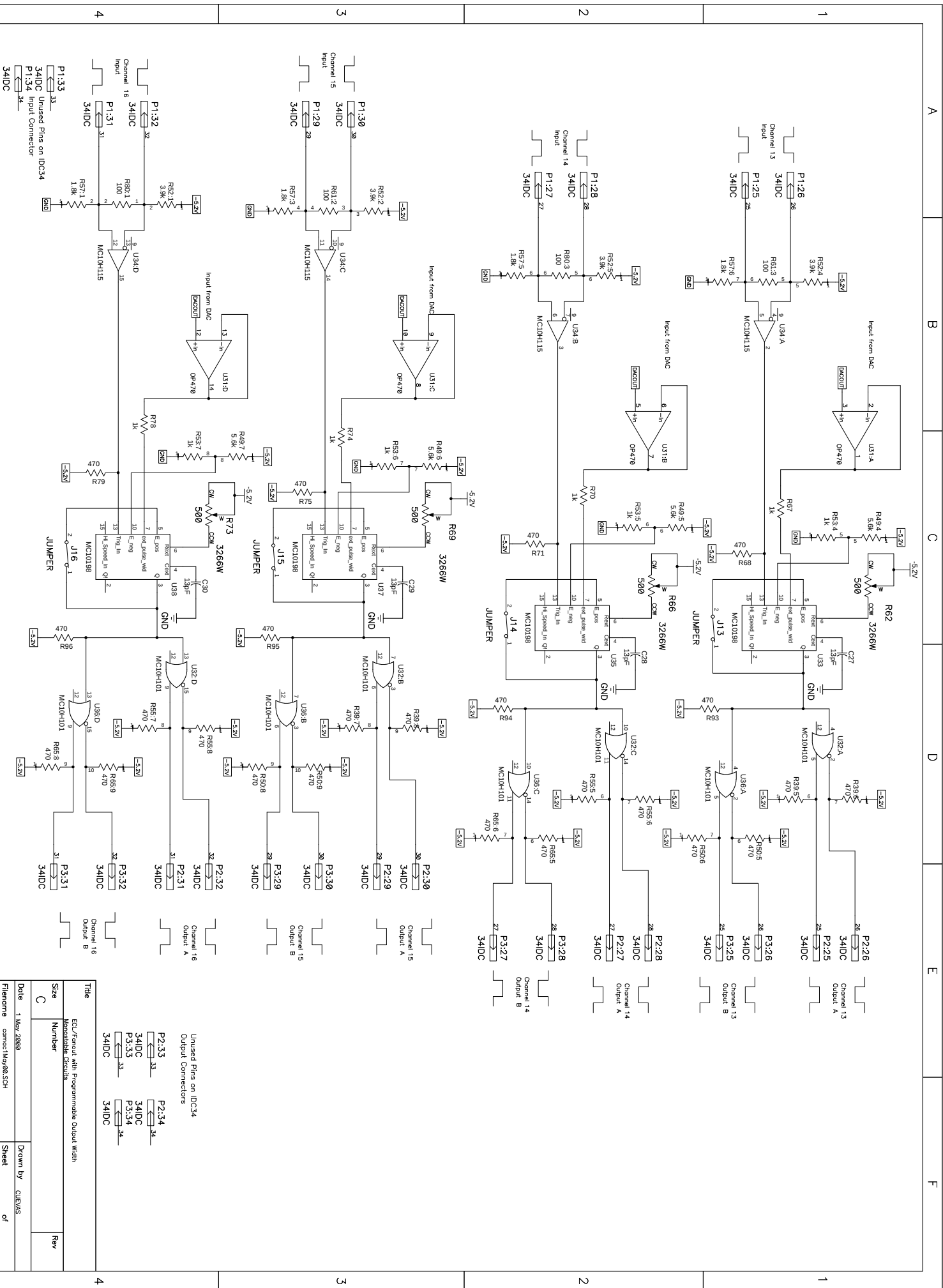




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Date		1 May 2000	
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Sheet		of	
Drawn by		CUEVMS	



Title		ECU/Front with Programmable Output Width	
Size		Monostable Circuits	
Number		Rev	
C		C	
Date 1 May 2008		Drawn by CLW/S	
Filename cmos1Map08.SCH		Sheet of	



Title	
EQ/Fenout with Programmable Output Width	
Modifiable Circuits	
Size	Number
C	

Date	
1 May 2088	
Filename	
connectWay0805CH	
Sheet	
1 of 4	

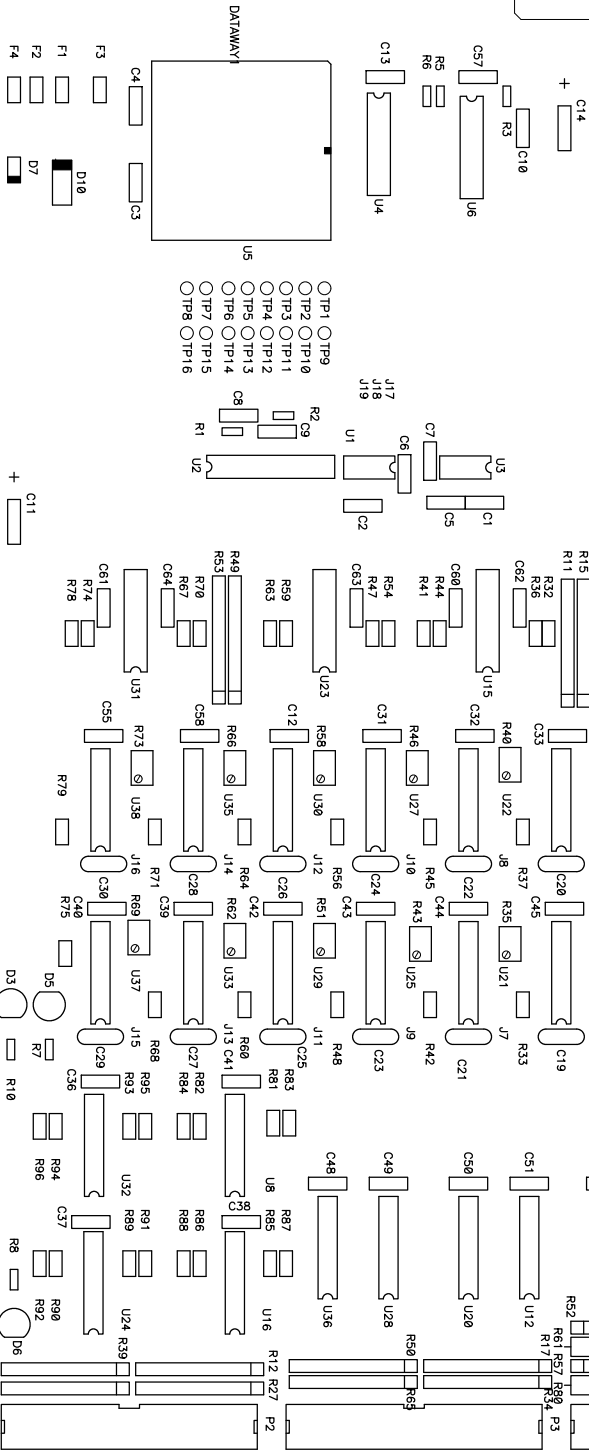
P2:33	
34IDC	
P2:34	
34IDC	
P3:33	
34IDC	
P3:34	
34IDC	

Unused Pins on IDC34
Output Connectors

P2:33	P2:34
34IDC	34IDC
P3:33	P3:34
34IDC	34IDC

JLAB ECL_FANOUT PCB

JEFFERSON LAB
FAST ELECTRONICS GROUP
ECL FANOUT
10/11/00
MADE IN THE U.S.A.



Drill Symbol Table		
Hole Dia (inch)	Symbol	Quantity
0.018	+	17
0.022	×	20
0.030	⊗	488
0.031	⊗	32
0.032	⊗	52
0.035	⊗	134
0.038	⊗	598
0.055	⊗	2
0.144	⊗	22

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