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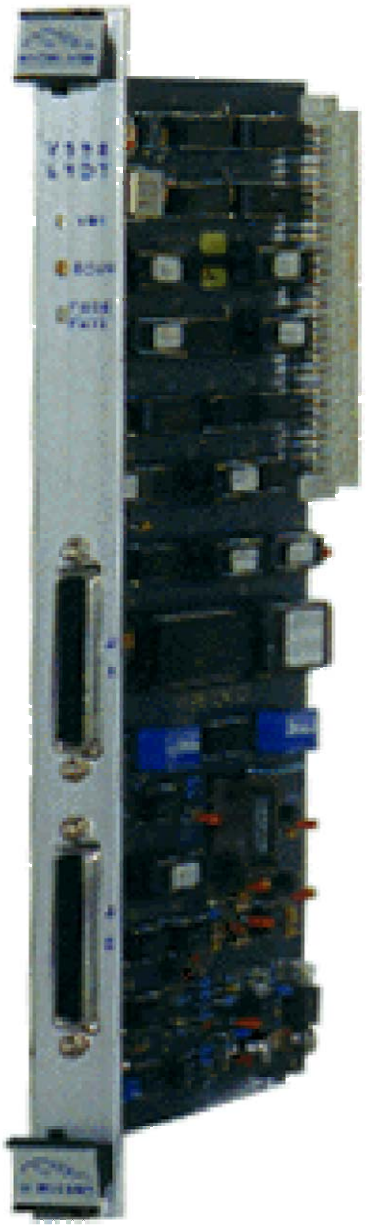

V550

8-CHANNEL

LVDT

SCANNER

VME MODULE

Technical Manual

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18 Otis Street, San Francisco, CA 94103
Phone 415-551-1700 • Fax 415-551-5129
www.highlandtechnology.com

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1. SPECIFICATIONS

Feature	Description
CONFORMANCE	Complies with ANSI/IEEE 1014-1987 VMEbus specification. VXIC specification, Revision 1.4.
DEVICE TYPE	Register based slave: A16:D16:D08(EO).
PACKAGING	Single-width, 6U VME or B-size VXI module.
POWER REQUIRED	+12 : 500mA; +5 : 3A; -12 : 500 mA.
LVDT DRIVE	Standard 3 Vrms, 2.4 KHz; other levels and frequencies available. Drive is differential to minimize capacitive error effects. Wiring shorts on any channel will not damage the module or disturb measurements of other channels.
RESOLUTION	16 bits.
ACCURACY	Better than ±50 PPM.
STABILITY	Temperature influence < 1 PPM per degree C; long-term drift< 4 PPM per year.
SCAN TIME	Time to scan all eight channels varies from 84 ms to 1.8 s depending on user-selected filtering factors.
DATA FORMAT	Signed two's complement 16-bit data.
CONNECTORS	Two front-panel mounted female DB-25s, five leads per LVDT.

2. OVERVIEW

The model V550 is a 6U, one-slot VME module which will acquire position data from up to eight LVDT (linear variable differential transformer) position sensors. The LVDT sensors are excited by an ultra-stable synthesized sinewave generator, and conditioned by a precision 16-bit A/D converter followed by digital signal processing. The resident microprocessor supervises scanning and signal conditioning, and places updated position data in VME-accessible dual-ported data registers for instant access from the VME bus.

The V550 provides 16-bit resolution, allowing sub-micron measurement with commercially available LVDTs. Users may select a range of DSP filtering factors to trade off position noise against acquisition rate.

The V550 provides unprecedented signal acquisition accuracy. Total RMS error (including absolute error, noise, and all drifts) is typically under 1.5 LSBs, equivalent to less than 25 PPM of full-scale span.

Features of the V550 include:

- Conditions eight LVDT-type position transducers.
- Self-scanning with onboard microprocessor.
- Presents scaled, normalized position data to the VME bus.
- 16-bit resolution with programmable noise filtering.
- 6U single-width VME module.

2.1 PART NUMBERS AND ORDERING INFORMATION

Standard V550 versions are:

MODEL	ASSEMBLY NO.	EXCITATION FREQUENCY
V550-1	22A550-1	2.4KHz
V550-2	22A550-2	4.8KHz

Units are generally factory-set for 2.50-volts RMS excitation level, with 32-cycle sampling and unity scaling. Please call Highland to discuss availability of other excitation levels and scaling, or if special processing algorithms or linearization are required.

2.2 LVDT BASICS

An LVDT is a physical displacement sensor. It consists of a cylindrical insulating form on which three solenoidal coils are wound. The center coil (the primary) is generally driven by a high-frequency sine wave source and, by magnetic coupling, it induces sinusoidal voltages in the two adjacent secondary coils. A movable magnetic core piece is arranged to slide down the axis of the core varying the magnetic coupling between the primary and the two secondaries. When the core is in the "center" location, the two induced secondary voltages will be equal. When the core is moved off center, one secondary voltage will increase and the other decrease. LVDTs are designed to produce as linear as possible a relationship between core position and secondary outputs.

LVDTs are very reliable sensors, and are usable in extreme environments, ranging from liquid helium temperatures to 1100 degrees F, and vacuums to extreme pressures. They are also available for use in high radiation ambients.

A typical LVDT will use 2.5-volt RMS primary drive at 2.4KHz, and have primary and secondary impedances of several hundred ohms. Rated full-scale motion ranges are available from ±0.005 inches to 10 inches. Usable resolution can extend into the microinch range. Rotary-input "RVDT" sensors are also available. With the core centered, secondary voltages are typically around 0.5 times the primary voltage.

An LVDT interface generally consists of a sine wave excitation oscillator, secondary voltage amplifiers, a detector circuit, and an output filter.

2.3 LVDT POSITION DETECTION TECHNIQUES

Several LVDT detector circuit techniques are currently in use:

PHASE-SENSITIVE DETECTOR

Most detector circuits operate by placing both secondaries in a series-opposing connection (such that zero net signal is produced when the core is centered) and processing this "off-null" net voltage through a phase-sensitive detector and filter. The phase-sensitive detector technique gives good linearity and resolution. Such systems, however, tend to have poor temperature coefficients because the computed position depends on excitation signal amplitude, LVDT coupling coefficients, and primary-to-secondary phase shifts.

The V550 is capable of measuring LVDT position in the phase-sensitive detector mode; see Section 2.6.

RATIOMETRIC DETECTOR

Integrated circuits are available to process LVDT signals by a ratiometric technique. Each separate LVDT secondary voltage is converted to DC by an active (or sometimes passive) rectifier circuit. These DC values are lowpass filtered and then applied to an analog computation circuit which computes position as a function of the ratio of the rectified secondary signals. Such circuits are relatively insensitive to excitation level and LVDT coupling ratios, but are inclined to introduce additional linearity errors and tend to have a poor response speed/output ripple tradeoff. External induced noise will also cause a ratiometric detector to indicate an erroneous position. Since even "shielded" LVDTs are excellent magnetic hum pickup coils, the nonsynchronous ratiometric detector can produce unpredictable position data in typical industrial and lab environments.

HIGHLAND DSP TECHNIQUE

The V550 uses an LVDT processing algorithm which is both synchronous and ratiometric. The separate LVDT secondary voltages are sampled and digitized by a precision 16-bit analog-to-digital converter, and groups of samples are processed to compute position. An onboard microprocessor supervises sample acquisition and processing, with user-alterable parameters used to specify sample density and speed/noise tradeoffs. The technique is insensitive to excitation voltage variations, provides inherent zero-ripple performance, and uses signal-processing software to "extract" true LVDT secondary signals from uncorrelated noise. Hum rejection is excellent, even at higher acquisition speeds. The V550 will typically demonstrate total RMS error (including absolute error, all drifts, and noise) of below 1.5 LSBs, corresponding to RMS errors below 25 PPM of full-scale span. This is about 100:1 better than the error levels demonstrated by the best analog signal processing circuits.

2.4 LVDT ACCURACY

Several factors influence LVDT accuracy. Any LVDT has inherent position nonlinearity, which becomes worse over larger core displacements. Typical units are linear to ±0.1% at half of rated displacement, 0.25% at rated span, and are usable to perhaps 150% of nominal displacement if increased nonlinearity is permissible. Zero offset ("null position") and gain factors vary slightly with temperature. Additional errors can be caused by excessive wiring resistance and capacitance, or by the presence of ferromagnetic

objects near the LVDT casing. The reader is referred to the *Handbook of Measurement and Control*, available on request from the Schaevitz Corporation (Pennsauken, NJ) for a detailed discussion of LVDT construction and applications.

While LVDTs demonstrate extreme resolution (sub-micron in many cases) and short-term repeatability, users should be aware that LVDTs must be individually calibrated and can demonstrate significant temperature sensitivity and non-linearity relative to their potential resolution.

Note that the reported position of an LVDT will "fold back" (appear to reverse) if the core is positioned too far off center. The V550 is programmed to sense extreme core over-travel (including a missing core) and report a corresponding error position, but the user should be aware that position ambiguities may still result from core overtravel with certain LVDTs. If possible, LVDTs should be installed as far away as possible from possible sources of AC magnetic fields, such as power transformers, AC power conductors, solenoids, motors, or electromagnets. LVDTs are not especially sensitive to moderate DC magnetic fields.

LVDTs should also be isolated from sources of mechanical vibration. Should any external influences cause the indicated position to jitter, one may program the V550 to process more waveform cycles and thus integrate out the disturbing influence. Most large-mass LVDT-instrumented systems make excellent seismometers, commonly sensing vibrations from building machinery and nearby freeways. At higher acquisition speeds, such mechanical noise will often limit position resolution to tens or hundreds of times the expected limits.

2.5 COMMENTS ON NON-RATIOMETRIC POSITION DETECTION

The V550 functions best when used in the ratiometric detection mode, reporting position proportional to (A-B)/(A+B), where A and B are the LVDT secondary voltages. Some LVDTs (especially some layer-wound long-stroke devices) may have inconstant A+B voltages and thus produce a nonlinear response when using this ratiometric technique. The V550 module incorporates an optional non-ratiometric measurement algorithm which simulates a phase-sensitive detector/lowpass filter arrangement. This mode may be invoked via the on-board OPTIONS DIPswitch or by manipulation of individual LVDT parameter registers.

Although the non-ratiometric mode may improve linearity for certain LVDT types, there are several disadvantages to using this mode:

1. In the non-ratiometric mode, reported LVDT position depends directly on the amplitude of the LVDT primary excitation. This excitation can be expected to vary with module ambient temperature, leadwire length and temperature, and LVDT temperature.

2. Reported position will depend on the setting of the LVDT drive adjustment trimpot, so this level must be set very carefully to insure module interchangeability.

3. In this mode, resistive and capacitive cable effects may be expected to be greater than in ratiometric mode.

3. THEORY OF OPERATION

3.1 MICROPROCESSOR AND VME INTERFACE

The V550 module includes a microprocessor/VME interface section which includes the following elements:

1. The microprocessor, a Motorola MC68B03.

2. Program read-only memory; a 27128 (16k bytes) is standard.

3. Program RAM (CPU-resident 128 bytes).

4. A dual-port memory, accessible by both the microprocessor and the VME bus. The DPM is physically a 2k by 16-bit array but, for this application, is mapped such that it appears to be a contiguous block of 32 16-bit registers.

5. Associated clock, decode logic, DPM arbitration logic, and watchdog timer/reset circuits.

3.2 LVDT ACQUISITION SECTION

The V550 module also contains the LVDT excitation and data acquisition front-end, containing the following subsections:

SINE WAVE SOURCE. The microprocessor's crystal-controlled clock is used to control a direct-digital sine wave synthesizer, whose output is then smoothed by a multipole switched-capacitor lowpass filter to produce a high-purity, amplitude and frequency-stable sine wave.

EXCITATION AMPLIFIER AND MULTIPLEXER. The excitation sine wave is amplified by a pair of inverting and non-inverting power amplifiers to produce a push-pull, low-impedance differential drive. Pairs of power MOSfets are enabled under microprocessor control to allow the power drive to be connected to one LVDT at a time. Trimpot R33 allows adjustment of LVDT drive level from zero to about 8-volts RMS, with typical drive being 2.5 VRMS at 2.4KHZ.

INPUT MULTIPLEXER AND A/D. A 16-channel analog multiplexer is used to select one LVDT secondary signal at a time. Once a single LVDT is selected and excitation drive applied, its two secondary outputs are selected and digitized a number of times to define the secondary waveforms for analysis. Multiplexed secondary signals are applied to a non-inverting preamplifier and then to a 16-bit sampling A/D converter.

Digitized LVDT secondary waveforms are processed by the microprocessor to produce position data. Section 5.3 discusses scaling of LVDT secondary voltages to reported positions.

4. SETUP AND INSTALLATION

4.1 SWITCH SETUPS

Two DIPswitches are provided on the V550 module. The ADDRESS switch selects the base address at which the VME bus master can address the V550s 32 16-bit registers. The V550 is always addressed in the VXI-register range, namely in the hex address range C000 - FF80 of the VME 16-bit address space, responding to hex address modifiers 29 and 2D.

The ADDRESS switch is SW2, located near R11 and U27. Sections 1 through 8 of this switch correspond to VME address bits 13 through 6 respectively. Setting all switch sections OFF selects the lowest address, C000 hex. Specific switch weightings are...

SECTION	VME ADD BIT	HEX VALUE
8	13	2000
7	12	1000
6	11	800
5	10	400
4	9	200
3	8	100
2	7	80
1	6	40

Note that the module responds only to those addresses which have bits 14 and 15 high; thus the actual bus address is C000 plus the "hex value" contributed by all ON DIPswitch positions. Although the V550 will operate normally at hex address FFC0 (e.g., all switches ON), this address is reserved by the VXI specification for use by dynamically configurable modules and should not be used for V550s.

A second "OPTIONS" DIPswitch SW1 is provided on the V550. This switch is read at powerup time and loads the initial operating parameters for all eight LVDT acquisition channels; these powerup setups may, of course, be altered by subsequent writes to the eight individual LVDT PARAMETER registers.

In normal operation, SW1 section 8 is left OFF, and sections 1 through 5 select default LVDT parameters. If section 8 is ON at reset time, the module will execute self-test diagnostics as described in Section 4.6.

SW1 switch positions 1 and 2 select the number of waveforms processed to compute LVDT position. The typical value is 32 waves; others may be selected for improved resolution and immunity to electrical noise and vibration, or fewer waveforms may be processed to allow higher-rate sampling. The fastest scan rate (sampling only 2 waveform cycles per measurement) is somewhat noisier than the slower rates (in the 3 LSB RMS range). Switch positions are...

S2	S1	CYCLES PROCESSED	ACQ TIME PER LVDT	TOTAL SCAN TIME
-	-	2	8.75 msec	70 msec
-	ON	8	13.1 msec	105 msec
ON	-	32	34 msec	270 msec

ON	ON	128	112	msec	900 msec

SW1 switch position 3 allows for LVDT span expansion. The V550 normally reports position as (VA-VB)/(VA+VB), which scales any possible set of LVDT secondary voltages into the 16-bit signed position value reported by the module. Should a particular LVDT produce secondary voltages which change little as the core is moved, or should only a small portion of the LVDTs full span be of interest, it is possible to "gain up" the reported LVDT position to increase measurement resolution and better fit usable core motion to the available 16-bit data range. Switch 3 operates as follows:

S3	SPAN MAGNIFICATION FACTOR
-	1.00 (no magnification)
ON	2.00

Switch position 4, when ON, invokes the non-ratiometric measurement mode. Refer to Section 2.6 for a discussion of this option.

SW1 position 5 selects the format in which the module reports position data. If this switch section is OFF, data is reported in two's complement format; if this switch is ON, data will be in offset binary. Sections 5.3 and 5.4 discuss position scaling and data formats in further detail.

4.2 LVDT DRIVE LEVEL

A trimpot is provided to allow adjustment of the LVDT excitation level. The excitation is measured "line-to-line" across the ends of an LVDT primary, and is normally set to 2.50 volts RMS. If SW1 DIPswitch sections 1, 3, and 8 are set ON (and the module reset to effect reading the switch), the V550 will park on LVDT 0, allowing steady-state measurement of LVDT drive between J1 connector pins 12 and 25 (or between internal test points TP1 and TP2). If the factory setting of 2.50 VRMS is not ideal for the particular LVDTs used, adjust drive level before beginning operation. Note that a selected LVDT primary will normally show a DC offset of about -5.5 volts relative to ground, and excitation should be measured from end to end of the LVDT primary.

Remember to return the DIPswitch to its normal position and RESET the module before resuming normal operation. For optimum position measurement resolution, LVDT drive level should be such that the LVDT secondary voltages are as great as possible without ever exceeding the linear input range of the preamp and A/D converter of the V550. The preamp is normally set up with a gain of 1.0, and the A/D range is ±5.0 volts, so the LVDT input voltages should not ever exceed ±4.5 volts peak at any LVDT operating position. Most LVDTs will generate secondary voltages somewhat below ±5 volts peak when positioned at their rated maximum positions and when excited by 2.5 volts RMS. If the LVDT output exceeds the ±5 volt limit, the module will report the POSITION ERROR value.

As an aid in setting proper LVDT drive voltages, a VME readable "A+B AMPLITUDE" register is available for each LVDT. This value is proportional to the LVDT "VA+VB" voltage output. When the LVDT drive level is correctly set, this value, interpreted as an unsigned 16-bit integer, should be in the range of 25000 to 35000, with an ideal value of +30000.

If the user prefers, the LVDT secondary voltages may be monitored with an oscilloscope and the LVDT drive level adjusted for ±4.0 to ±4.5 volts peak at the higher-voltage secondary when the LVDT is positioned at its maximum-travel positions.

4.3 PHYSICAL INSTALLATION

The V550 may be installed in any VME crate conforming with the IEEE 1014 specification. Only mandatory (+5, ±12) power supplies are required. The module does not use interrupts, but does provide internal bus grant jumpers such as to not break system interrupt paths.

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ALWAYS SWITCH OFF CRATE POWER BEFORE
INSERTING OR REMOVING ANY MODULES

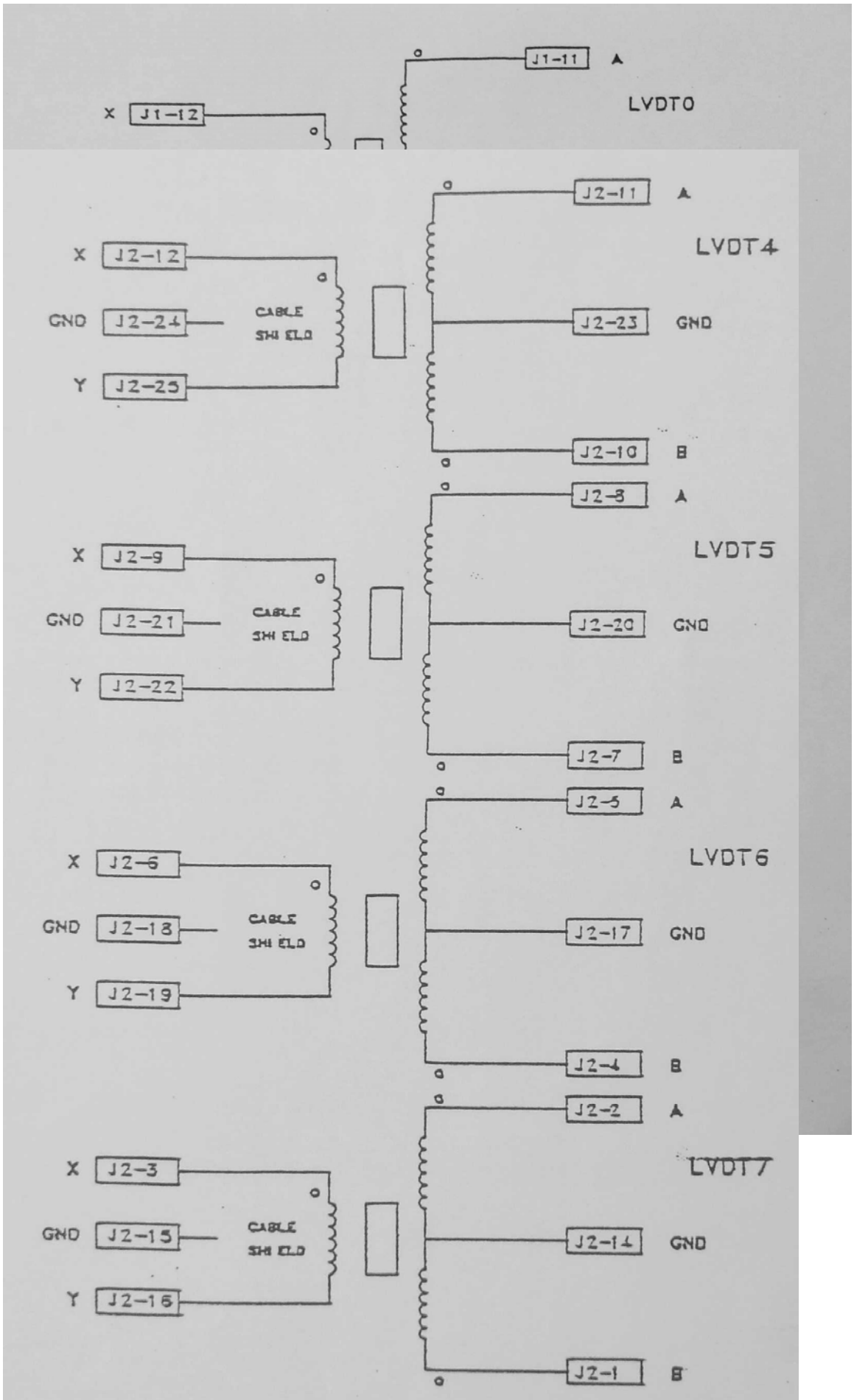
****

4.4 CONNECTOR TYPES AND PINOUTS

The V550 has two front-panel mounted female D25 connectors. LVDT connections are as noted on the two following pages. It is recommended that LVDT wiring be shielded overall. For short cable runs with low impedance LVDTs, all LVDT leads may be run without wire-to-wire shielding. An LVDT with 1K secondaries can generally tolerate about 5 feet of such cabling, with lower impedance units tolerating proportionally more cable length. Longer cable runs should use cable with individually shielded pairs, one for each LVDT winding.

Various LVDT manufacturers use different wiring conventions and lead color codes. The following examples illustrate connection of typical LVDTs to the V550 channel "0" input:

SYM	SIGNAL	V550 PIN	SCHAEVITZ	DAYTRONIC	SANGAMO
X	PRI HI	J1-12	YEL/BLK	YELLOW	YEL/BLK
Y	PRI LO	J1-25	YEL/RED	BROWN	YEL/RED
A+	SEC HI	J1-11	BLACK	BLACK	BLACK
A-	SEC GND	J1-23	GREEN	GREEN	GREEN
B+	SEC HI	J1-10	RED	RED	RED
B-	SEC GND	J1-23	BLUE	BLUE	BLUE
-	SHIELD	J1-24			


J1-11
A
LVDT0
X
J1-12
J2-11
A
LVDT4
X
J2-12
GND
J2-24
CABLE SHIELD
Y
J2-25
J2-23
GND
J2-10
B
J2-8
A
LVDT5
X
J2-9
GND
J2-21
CABLE SHIELD
Y
J2-22
J2-20
GND
J2-7
B
J2-5
A
LVDT6
X
J2-6
GND
J2-18
CABLE SHIELD
Y
J2-19
J2-17
GND
J2-4
B
J2-2
A
LVDT7
X
J2-3
GND
J2-15
CABLE SHIELD
Y
J2-16
J2-14
GND
J2-1
B

4.5 INITIAL POWERUP

If the OPTIONS DIPswitch SW2 is in the "normal" mode (e.g., self-test is disabled by setting section 8 OFF) the module will powerup in the following sequence:

1. At powerup time, or in response to a bus SYSRESET operation, the internal microprocessor will be reset. The SYSFAIL bus line will be asserted by the V550, and the front panel PASS/FAIL LED will illuminate red.

2. The V550 will execute four internal self-tests: POWERUP OK, CPU RAM TEST, PROGRAM ROM CHECKSUM, and DUAL-PORT MEMORY TEST. During the DPM test, the VME-accessible register file will be briefly written with test data patterns and verified, so the VME system must not write to the module during this interval.

   At the successful completion of each test, the amber SCAN LED will flash twice.

3. When all four tests have passed, all 32 DPM registers will be cleared, the SYSFAIL line will be dropped, and the PASS/FAIL LED will go green. Immediately after the group register clears, the first eight VME registers will be loaded with VXI and module-specific parameter values.

4. The processor will next read the OPTIONS DIPswitch. If switch position 8 is ON, a selected self-test will be run; see Section 4.6. If section 8 is OFF, the switch sections 1-5 will be read and used to set all eight LVDT PARAMETER registers.

5. Once default LVDT parameters are loaded, normal LVDT scanning begins. At the end of each scan, the SCAN LED state is inverted; this LED will thus blink at half the LVDT scan rate.

The entire startup sequence will take about 3 seconds. For the 22550A preliminary firmware release, any startup errors will cause the firmware program to "hang", and the internal watch-dog timer will reset the processor and repeat the startup sequence. Code Rev 22550B will include more proper VXI-style startup logic.

4.6 SELF-TEST FACILITIES

If the V550 is reset with section 8 of the OPTIONS switch ON, the module will enter self-test mode. The low 3 positions of the OPTIONS switch will be read to determine one of eight possible tests to be run.

The detailed self-test mode powerup sequence is as follows:

A. Steps 1-3 of the normal powerup sequence are followed, as noted in Section 4.5.

B. The OPTIONS DIPswitch section 8 is sensed ON; SYSFAIL is cleared and the PASS/FAIL LED goes green.

C. The low 3 DIPswitch positions are read and one of eight possible test routines is executed. If the routine passes, the SCAN LED will blink twice; if the test fails, the SCAN LED will display one long blink, the PASS/FAIL LED will go (and remain) red, and SYSFAIL will be asserted.

D. If switch position 8 is still ON, the program loops back to step C above. If not, a normal powerup/ operate sequence is initiated.

The eight self-tests are...

S3	S2	S1	TEST
--	--	--	IGNORE DPM ; allows DPM tests from VME bus
--	--	ON	TEST LOW DPM ; tests first 16 registers
--	ON	--	TEST HIGH DPM ; tests last 16 registers
--	ON	ON	TEST ALL DPM ; tests all 32 registers
ON	--	--	WRITE PATTERN TO DPM ; pattern = FF00h + reg index
ON	--	ON	PARK ON LVDT 0 ; assists in setting LVDT drive
ON	ON	--	GATE LVDT DRIVE ON/OFF ; keys on/off sinewave gen
ON	ON	ON	WIGGLE SYSFAIL ; exercises SYSFAIL driver

5. PROGRAMMING

5.1 DUAL-PORT MEMORY CONSIDERATIONS

The primary data interchange and control mechanism between the V550 and the VME bus is the 32-word by 16-bit dual-port memory located on the module. Because both the VME bus and the microprocessor have full read/write access to all DPM locations, an "anti-collision" mechanism is needed to prevent data usage conflicts and interlock problems. In the V550, this interlocking is accomplished by the simple means of assigning, by convention, certain locations in DPM as being written into only by VME, and other locations as being written into only by the microprocessor. Although normal operation of the V550 assumes that the VME port will adhere to the documented conventions of register read/write use, system design is such that no unusual events will occur should the VME port write to a module "read only" DPM location. If the VME-side computer were to alter a "module output data" location (say, by writing into an LVDT position register), the V550 will restore that data in the next scan.

5.2 VME REGISTER ADDRESSES

The V550 interfaces to the VME bus through a group of 16-bit data registers. The registers are a contiguous block of 16-bit registers with beginning address selected by the SW2 DIPswitch as noted in Section 4.1. Register functions are listed below, assuming that the first register ("VXID") is located at the module base address:

REG NAME	BYTE OFFSET	WORD INDEX	REGISTER FUNCTION
VXID	00h	0	VXI ID/LOGICAL ADDRESS REGISTER
VTYPE	02	1	VXI DEVICE TYPE
VCSR	04	2	VXI STATUS/CONTROL REGISTER
PGID	06	3	FIRMWARE PROGRAM ID
PREV	08	4	PROGRAM REVISION
PHAS	0A	5	PHASE ANGLE
OPTS	0C	6	DIPSWITCH AND OTHER OPTIONS
SCAN	0E	7	SCAN COUNTER
LVDT0	10h	8	LVDT POSITION 0
LVDT1	12	9	LVDT POSITION 1
LVDT2	14	A	LVDT POSITION 2
LVDT3	16	B	LVDT POSITION 3
LVDT4	18	C	LVDT POSITION 4
LVDT5	1A	D	LVDT POSITION 5
LVDT6	1C	E	LVDT POSITION 6
LVDT7	1E	F	LVDT POSITION 7
AMP0	20h	10	A+B AMPLITUDE, LVDT 0
AMP1	22	11	A+B AMPLITUDE, LVDT 1
AMP2	24	12	A+B AMPLITUDE, LVDT 2
AMP3	26	13	A+B AMPLITUDE, LVDT 3
AMP4	28	14	A+B AMPLITUDE, LVDT 4
AMP5	2A	15	A+B AMPLITUDE, LVDT 5
AMP6	2C	16	A+B AMPLITUDE, LVDT 6
AMP7	2E	17	A+B AMPLITUDE, LVDT 7

PAR0	30h	18	PARAMETERS, LVDT 0
PAR1	32	19	PARAMETERS, LVDT 1
PAR2	34	1A	PARAMETERS, LVDT 2
PAR3	36	1B	PARAMETERS, LVDT 3
PAR4	38	1C	PARAMETERS, LVDT 4
PAR5	3A	1D	PARAMETERS, LVDT 5
PAR6	3C	1E	PARAMETERS, LVDT 6
PAR7	3E	1F	PARAMETERS, LVDT 7

The VXID register is the VXI-compatible ID/LOGICAL ADDRESS register. It contains the value FEEE hex, the "F" digit denoting a register based, 16-bit VME/VXI device, and the "EEE" hex digits being the registered identification of Highland Technology as the manufacturer.

The VTYPE register contains the hex value 5816, equivalent to the number 22550 decimal, the VXI-standard module type.

The VCSR register is the VXI-compatible control/status register. After initial powerup tests, this register will display the hex value C (decimal 12), corresponding to the "PASSED" and "READY" VXI flags.

The PGID register identifies the microprocessor program version; it generally contains the hex value 5816, equivalent to 22550 decimal; special versions may contain other values.

The PREV register contains, in its low byte, an ASCII code identifying the revision of the microprocessor program. The typical value is 41 hex, corresponding to the character "A."

The PHAS register contains a value which indicates the phase angle at which LVDT waveforms are sampled. The standard value is zero.

The OPTS register contains, in its low byte, the value expressed in the OPTIONS DIPswitch SW1. The presented value is a snapshot of the switch value taken at powerup reset time. The high byte of the OPTS register is reserved to flag future options.

The 16-bit SCAN COUNTER register increments once each time that all 8 LVDTs are scanned and their positions updated. It is a good indicator that the module is "alive" and scanning normally.

The LVDT POSITION registers each contain a signed, 16-bit value which represents the position of the associated LVDT. This data may be in two's complement or offset binary. Refer to Sections 5.3 and 5.4 for notes on position scaling.

The LVDT PARAMETER registers may be read and written from the VME bus. At powerup time or following a module reset, the low 5 bits of the module DIPswitch are read and loaded into all eight PARAMETER registers to establish the default operating mode for all LVDTs. The user may alter these parameters by executing VME write operations onto the eight individual PARAMETER locations.

Only the low 6 bits of the PARAMETER registers are used; the two LSBs (VME data bits 0 and 1) control the number of carrier cycles acquired to compute position data; bit 2 controls position range

magnification; bit 3 selects non-ratiometric conversion; bit 4 selects offset binary data format. The 6th PARAMETER bit (VME logical bit 5) is the SKIP LVDT bit. If this bit is set, data for this LVDT will not be acquired and the overall scan rate for other LVDTs will correspondingly increase; the POSITION and A+B AMPLITUDE values of skipped LVDTs will be zero.

In summary, the low 6 PARAMETER bits are...

LOGICAL BIT	5	4	3	2	1	0
FUNCTION	SKIP	OFFBIN	NONRAT	MAG	CY1	CY0

Detailed bit functions are as described in Section 4.1. Note that, at powerup time, sections 1-5 of the OPTIONS DIPswitch are read and loaded into bits 0-4 of all PARAMETER registers.

5.3 RATIOMETRIC LVDT POSITION SCALING

LVDT positions are reported to the VME bus as 16-bit integers, in either two's complement or offset binary format (see Section 4.1 and 5.2 for format selection).

- In two's complement, the position integer, PI, is computed by the V550 as:

  PI = K * 32768 * (VA - VB) / (VA + VB)

- In offset binary, the position integer, PI, is computed by the V550 as:

  PI = K * 32768 (1 + (VA - VB) / VA + VB)

Where: PI is the reported position (signed two's complement or unsigned 16-bit integer, depending on setting).

K is selected LVDT gain factor (1 or 2).

VA is LVDT secondary A voltage.

VB is LVDT secondary B voltage.

The exact engineering unit scaling of a particular LVDT depends on the LVDT construction and is best done experimentally. Proceed as follows:

1. Set the V550 LVDT scanner for ratiometric mode (two's complement or offset binary).

2. Install LVDT in a fixture that provides independent position reading with better resolution and accuracy than expected from the LVDT (such as a linear glass scale with digital readout).

3. Find the LVDT null point (V550 will report 0, PI position integer for two's complement format or 32768 for offset binary data) and declare 0 position there for the independent position reading fixture.

4. Move the LVDT core to maximum positive position (e.g., if LVDT is ±125mm, and total span 250mm, this would be +125mm) and record the PI, the position integer coming out of the V550 for maximum positive position.

   If you get an error indication from the V550 when taking the LVDT core to its maximum positive position (PI = 32768 for two's complement format, 65535 for offset binary), you have two options:

   - Reduce drive level until error indication disappears (see Section 4.2).

     Or, if you will not be using the whole positive span of the LVDT in your system, back off LVDT core from maximum positive position to the highest position where you intend to move it. If the error indication disappears then take this point as your new maximum positive position, leave the drive level alone, and proceed to next step.

   If the PI, position integer returned for the maximum positive position is under 16384 for two's complement or 49152 for offset binary, you may double your resolution by setting your LVDT gain K to two (2), see Section 5.2.

5. Compute the slope constant 'S' as

$$S = \frac{\text{MAXIMUM POSITIVE POSITION - LVDT NULL POSITION}}{\text{PI FOR MAX POSITION - PI FOR NULL POSITION}}$$

   Where S dimensions will be engineering units/PI LSB

6. In possession of the slope constant, now we can compute the position in engineering units, PEU, for two's complement data format as (e.g., in Basic):

```
IF POSITION INTEGER >32767 THEN

PEU = S * (PI-65536)

ELSE

PEU = S * PI

END IF
```

   And for offset binary as:

```
PEU = S * (PI - 32768)
```

   Where PI is the position integer.

5.4 NON-RATIOMETRIC POSITION SCALING

When an LVDT is operated in the optional non-ratiometric mode, the position integer, PI reported by the V550 is proportional to VA-VB,

the difference between the LVDT "A" and "B" secondaries. This value depends on the LVDT position, LVDT transfer function (sensitivity), and primary excitation amplitude.

In two's complement, the position integer PI, is computed by the V550 as:

PI = K * 32768 * (VA-VB)

In offset binary the position integer P is computed by the V550 as:

PI = K * 32768 * [1 + (VA-VB)]

Where: PI is the reported position (signed two's complement or unsigned 16-bit integer, depending on setting), in volts. LSB = 10/65536 volts.

K is selected LVDT gain factor (1 or 2),
VA is LVDT secondary A voltage, and
VB is LVDT secondary B voltage.

The exact engineering unit scaling of a particular LVDT depends on the LVDT construction and is best done experimentally.

The LVDT calibration/scaling procedure for non-ratiometric mode is identical to the one for ratiometric mode, but is repeated below for convenience:

1. Set the V550 LVDT scanner for non-ratiometric mode (two's complement or offset binary).

2. Install LVDT in a fixture that provides independent position reading with better resolution and accuracy than expected from the LVDT (such as a linear glass-scale with digital read out).

3. Find the LVDT null point (V550 will report 0, PI integer for two's complement format or 32768 for offset binary data) and declare 0 position there for the independent position reading fixture.

4. Move the LVDT core to maximum positive position (e.g., if LVDT is ±125mm, total span 250mm, this would be +125mm) and record the position integer PI coming out of the LVDT for maximum positive position.

   If you get an error indication from the V550 when taking the LVDT core to its maximum positive position (32768 for two's complement format, 65535 for offset binary), you have two options:

   - Reduce drive level until error indication disappears (see Section 4.2).

     Or, if you will not be using in your system the whole positive span of the LVDT anyway, then back off LVDT core from maximum positive position to the highest position where you intend to move it. If the error indication disappears then take this point as your

new maximum positive position, leave the drive level alone, and proceed to next step.

If the PI, position integer returned for the maximum positive position is under 16384 for two's complement or 49152 for offset binary, you may double your resolution by setting your LVDT gain K to two (2), see Section 5.2.

5. Compute the slope constant 'S' as

$$S = \frac{\text{MAXIMUM POSITIVE POSITION - LVDT NULL POSITION}}{\text{PI FOR MAX POSITION - PI FOR NULL POSITION}}$$

Where S dimensions will be engineering units/integer. (To be truly accurate S units are engineering units/volts.)

6. In possession of the slope constant, now we can compute the position in engineering units, PEU, for two's complement data format as (e.g., in Basic):

```
IF POSITION INTEGER >32767 THEN

PEU = S * (PI-65536)

ELSE

PEU = S * PI

END IF
```

And for offset binary as:

```
PEU = S * (PI - 32768)
```

Where PI is the position integer.

5.5 ERROR DETECTION AND REPORTING

If the V550 senses LVDT signals which are considered unusable for reliable position measurement, the POSITION value will revert to its "error" value as noted above. Conditions which produce the error indication are:

1. Either the "A" or "B" LVDT secondary signal is out of phase with the "X" phase excitation, indicating a wiring error.

2. Any sampled LVDT secondary voltage approaches the ±5.00volt A/D full-scale limits, indicating excess LVDT drive levels or a wiring problem.

3. The "A+B" sum voltage is too low to allow accurate position calculation. This may be caused by low excitation voltage, a missing LVDT core, or wiring problems. The error is declared if the sum of the secondary voltages is less than about 0.1 volts RMS, corresponding to an integer value of +1000 as reported in the appropriate "A+B AMPLITUDE register.