OPERATOR'S MANUAL

MODEL 1110

VME ADC/TDC TESTER

CE

LeCroy

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

ELECTROSTATIC DISCHARGE PROTECTION

The Model 1110 is shipped in ESD protective packaging. Do not remove the module from the anti-static packaging unless you are in a static-free environment.

COOLING

It is imperative that the Model 1110 VME ADC/TDC Tester be well cooled. Be sure the cooling fans move sufficient air to maintain an exhaust air temperature of below 50 degrees C.

INSTALLATION

Crate Power should be turned OFF during insertion or removal of modules in accordance with the VME bus specification.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

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Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

PRODUCT DESCRIPTION

2.1 INTRODUCTION

The Model 1110 ADC/TDC Tester is a programmable Pulse Generator in a VME 6U x 160mm single width package, primarily designed as a test instrument for servicing VME ADCs and TDCs.

START and STOP outputs are included for testing TDCs. The time difference between these outputs is programmable with a 16-bit DAC. For ADC testing, multiple charge outputs and a 0-10 V DAC output are available. A FAST CLEAR output is also included. All logic signals have both NIM and dECL outputs on LEMO and Header connectors.

Two other registers are implemented, one for triggering the module and the other to define the Full Scale Range of the charge output and masking the front panel Fast Clear.

2.2 SPECIFICATION

- VME 6U x 160 mm single width
- A24/D16 VME Module
- Responds to the following address modifier (AM) codes: 39, 3B, 3D and 3F
- Uses 0x0006 locations of A24 VME address space
- Power Requirements: ±12 and ±5 V

2.3 CONTROLS

2.3.1 Registers

All programmability of Model 1110 outputs are through the VME interface. Registers are mapped directly to the VME address space. See the Operating Instructions for implementation.

Register Name	Description
Trigger	Generates cycle when written to
Width DAC	Controls START-STOP time difference, GATE width, and DAC LEMO voltage
Charge DAC	Controls charge delivered to all charge outputs
Fast Clear / Charge Range	Enables/disables Fast clear output, sets charge output range

2.3.2 Base Address DIP

The module base address is determined by an 8-position DIP switch located near the top of the board (SW1 = A16, SW8 = A24). See installation page for instructions on setting the Base Address.

2.4 FRONT PANEL OUTPUTS, SWITCHES AND INDICATORS

2.4.1 LEMO Outputs

CHARGE (Q OUT): Programmable in 4 ranges: 0 to 300 pC, 0 to 600 pC, 0 to 900 pC, 0 to 1200 pC; 16 bit resolution.

DAC (DAC OUT): 0 to 10 V DC level; 16 bit resolution.

FAST CLEAR (FC OUT): 0 to -800 mV pulse, nominal width 30 nsec.

GATE (GTE OUT): 0 to -800 mV pulse, width programmable 30 to 2400 nsec.

START (STR OUT): 0 to -800 mV pulse, nominal width 10 nsec.

STOP (STP OUT): 0 to -800 mV pulse, nominal width 10 nsec.

2.4.2 Charge Fanout Header

The 1110 has a 16 channel fan-out. The signal pin is on left side of the connector; the right side is tied to ground. It is programmable in 4 ranges: 0 to 300 pC, 0 to 600 pC, 0 to 900 pC, and 0 to 1200 pC.

2.4.3 ECL Outputs

Pins on the left side of the connector are -1.8 V quiescent, rising to -0.8 mV when becoming “true”. Pins on the left side of the connector are complimentary.

START (STR): Equivalent of LEMO STR OUT.

STOP (STP): Equivalent of LEMO STP OUT.

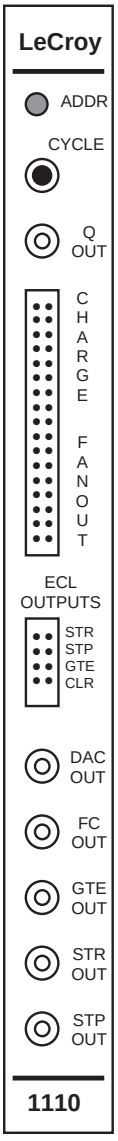
GATE (GTE): Equivalent of LEMO GTE OUT.

FAST CLEAR (CLR): Equivalent of LEMO FC OUT.

2.4.4 Other Front Panel Objects

Cycle Button: Depressing cycle button initiates trigger cycle.

ADDR LED: Flashes to indicates VME access.



INSTALLATION

GENERAL

Before inserting the Model 1110 VME ADC/TDC Tester into any VME crate, the base address must first be set. The 8-position DIP switch defines the module VME address, decoded from address lines A16 to A24; e.g., for Address 0x00, set SW1 to SW8 to be CLOSED (UP at the OPEN end of switch).

To set Address 0x80 set SW8 to be OPEN (Down at the OPEN end of switch). To set Address 0x01 set SW1 to be OPEN.

4.1 VME ADDRESS MAP

The Model 1110 occupies the following VME A24 address space (hexadecimal):

Base address + 0x0000 to 0x0006

The internal memory map in hexadecimal is as follows:

Base Address	+	0x0000:	Trigger Register
Base Address	+	0x0002:	Width DAC Register
Base Address	+	0x0004:	Charge DAC Register
Base Address	+	0x0006:	Fast Clear Mask and Charge Range Select

4.2 TRIGGER REGISTER OPERATION

The Trigger register is “WRITE ONLY” and can only be accessed via A24/D16 VME transfers. Writing anything to the Trigger register causes a cycle to occur generating START, STOP, GATE, FAST CLEAR and CHARGE outputs.

4.3 FAST CLEAR MASK AND CHARGE RANGE REGISTER OPERATION

The Fast Clear Mask and Charge Range register is “WRITE ONLY”, and can only be accessed via A24/D16 VME transfers. Four bits of data (IDATA0 - IDATA3) are used in this register, determining the FAST CLEAR and the Charge range.

4.3.1 FAST CLEAR Mask

VME IDATA0 enables or disables generation of the front panel FAST CLEAR pulse.

IDATA0 = 0; Fast clear enabled
IDATA0 = 1; FAST CLEAR disabled.

4.3.2 Charge Range Selection

VME IDATA1- IDATA3 are used to provide the CHARGE output range selection (duplicating range values are by design):

IDATA3	IDATA2	IDATA1	CHARGE RANGE
0	0	0	No Charge Output
0	0	1	300 pC
0	1	0	300 pC
0	1	1	600 pC
1	0	0	600 pC
1	0	1	900 pC
1	1	0	900 pC
1	1	1	1200 pC

4.4 WIDTH REGISTER AND DAC OPERATION

The Width register is “WRITE ONLY” and can only be accessed via A24/D16 data transfers. The 16 bit DAC that is programmed by this register controls:

1. The width of the GATE output.
2. Time interval between the START and STOP outputs.
3. The voltage output to DAC OUT.

For the timing output (numbers 1 and 2 above), the full scale width is 2400 ns, with an LSB of ~36.6 ps. The formula for calculating the appropriate DAC codes and output widths are:

DAC Code = 65535 * (Desired Value in ns) / 2400

For the DAC output (number 3 above), the range is 0 to 10 V, with an LSB of ~0.15 mV. The conversion formula is:

DAC Code = 65535 * [1.0- (Desired Value in Volts) / 10]

4.5 CHARGE DAC REGISTER OPERATION

The Charge DAC registers is “WRITE ONLY” and can only be accessed via A24, D16 data transfers. The 16 bit DAC that is programmed by this register controls the charge output to the LEMO and HEADER Q outputs.

Charge DAC Code = 65535 * [1.0 - (Desired Value in pC) / (Full Scale Range in pC)]

This section is provided to outline the theory behind the hardware. The information is provided to aid the user in understanding the function of this device and is not intended as a guide for repair.

5.1 1110 ADC/TDC TESTER

The VME connector P1, located on sheet 1 of the schematic, contains all the signal and power supply lines used by the module, together with the derived power supplies.

Sheet 2 of the schematic shows the primary interaction with the VME bus. All the VME bus control signals are buffered with U21, U23, U24 and U25 before being decoded by PAL U26. During all VME bus cycles, address bits A16 to A24 are compared with the 8 position DIP switch (Base Address) settings; if valid U23 pin 19 generates a valid address signal which, in turn, generates the latched address strobe (LAS) and delayed address strobe (DLAS) to the PAL, the PAL then generates the VME bus DTACK signal in response.

On addressing the Width DAC register (Base address + 0x0002) the PAL generates WCLK0 and WCLK1 clock signals latching VME data via U13 and U16 into the width DAC (U3). Similarly the Charge DAC register (Base address + 0x0004) clocks QCLK0 and QCLK1 are generated, latching VME data via U14 and U15 into Charge DAC (U2). Monostable U1 is used to drive the front panel led for each accepted VME command and to provide an 100 nsec pulse to drive the Trigger circuit at (Base address + 0x0000). IDATA0 is latched with (Base address + 0x0006) at U18 to provide the Fast Clear enable or disable.

Sheet 3 contains all the timing and the START, STOP, GATE and FAST CLEAR outputs. The width DAC is applied to U11 which provides an attenuated level to the STOP comparator U10 pin 7. A Ramp generator initiated by each trigger command is applied to the START comparator U10 pin 9 and these outputs generate the START, STOP and GATE outputs at both ECL and NIM levels. U4 enables or disables monostable U5 from issuing the FAST CLEAR on the back edge of the GATE pulse, U6 providing the pulse width of the FAST CLEAR signal.

Sheet 4 contains the Charge output circuitry. The QDAC output is applied to the two FETs Q1 and Q5 which are switched by the QSTART pulse to Q3 base. Q5 outputs charge through the Charge Fan-out from panel header, Q1 outputs charge to the front panel Q OUT LEMO connector. This output range is selected by IDATA1, IDATA2 and IDATA3 via U17 and relays K1, K2 and K3.

Calibration Procedure

Model 1110 VME ADC/ADC Tester

1. Before inserting the 1110 in the VME Crate, determine the Base Address from the 8-Position DIP switch.

2. For this exercise it is assumed the base address is 0x80.

3. Switch on and allow 10 minutes to reach stable operating conditions.

4. Run any VME Program such as VIC (National Instruments).

5. Loop Trigger command 0x800000 a thousand times and check that the Front Panel LED is lit.

6. Program the Width DAC to Min. Address 0x800002 set to 0xffff.

   Note: A value of 0xffff is equivalent to 0 V at the 'DAC OUT' and to Max. START - STOP interval of 2400 nsec.

7. Connect DVM to 'DAC OUT' and adjust pot R54 for a reading of 0 V ±10 mV.

8. Change data to Max. (0x0000) and adjust pot R52 for 10 V ±10 mV.

9. Check for 5.00 V ±10 mV with data set to 0x7fff (Mid Scale).

10. Program Width DAC back to Min. (0xffff). Check the voltage at U11 pin 6, should be 2 V ±0.25 V.

11. Record the voltage at U10 pin 9. (-3.000 V ±0.5 V) ..... Vref _____

12. Change data Max. (0x0000) and adjust pot R102 for a reading at U11 pin 6 of Vref + 800 mV.

13. Adjust pot R104 for a reading at U10 pin 10 for a value in Step 12 -20 mV.

    Note: Vref = -3.125 V then U11 pin 6 would be -2.325 V and U10 pin 10 -2.345 V.

14. Change the data to 0x7fff (Mid Scale).

15. Connect Oscilloscope to 'GATE OUT'. Write any data to Base Address (0x800000) and cycle by looping a number of times (10000). Check for 1.2 μsec wide NIM Pulse at 'GATE OUT'.

16. Loop checking for 'START OUT' to 'STOP OUT' timing of 1.2 μsec.

17. Connect 'START OUT' and 'STOP OUT' of the 1110 to the 'START' and 'STOP' of a HP5370B or similar Counter. Set the HP5370B as follows:

FUNCTION:	T1
STATISTICS:	Mean
TRIG LVL:	0.3 V (Channels A & B)
SAMPLE SIZE:	100
ARMING:	+T1 Only
INPUTS:	Slope Neg, 50 Ω, ÷1, DC, STEP (Channels A & B)

18. Program Width DAC back to Min. (0xffff). Write any data to Base Address (0x800000) and cycle by looping a number of times (10000). Adjust pot R101 for a reading of 2400 nsec ±1 nsec.

19. Program Width DAC to (0x0334). Write any data to Base Address (0x800000) and cycle by looping a number of times (10000). Adjust pot R104 for a reading of 30 nsec ±1 nsec.

20. Program the Q DAC to Min. Address 0x800004 set to 0xffff.

21. Connect DVM to U2 pin 17 and adjust pot R51 for a reading of 0 V ±10 mV.

22. Change data to Max. (0x0000) and adjust pot R48 for 10.00 V ±10 mV.