OPERATOR'S MANUAL

MODEL 1151E & 1151N

16 CHANNEL VME SCALERS

Revised
January , 1994

(ECO 1002 , 1003)

5 THEORY OF OPERATION

CAUTION

Before inserting the module, the user must set its base address on four rotary hex switches, making sure that the selected page is located in an unused portion of the microprocessor's memory space. The base address must be different for every module in the same systems. The first 256 bytes following the base address are allocated to the 1151 module.

Inserting the module while the VME crate is powered up can damage the scaler. Voltages of +5 and -12 must be present on the backplane with sufficient current drive to power all the inserted modules. The ventilation of the modules should be in proportion to the power consumption. Care should be taken to prevent any obstruction to the air inlets and outlets.

Due to power consumption requirements, the 1151 module must only be plugged into backplanes containing both P1 and P2 connectors.

1.0 General Information

1.1 Purpose

This manual is intended to provide instruction regarding the setup and operation of the Model 1151 VME scaler. In addition, it describes the theory of operation and presents other information regarding its application.

1.2 Unpacking and Inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please contact the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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Research Systems Division
700 Chestnut Ridge Road
Chestnut Ridge, NY 10977-6499
Tel. (914) 578-6030

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Software products are licensed for single machine use. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

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Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

LeCroy

1151E SCALER WITH ECL INPUTS
1151N SCALER WITH NIM INPUTS

- **16 Channels/Single-Width, 6 U VME Module**
- **High-Speed Counting, 80 MHz**
- **NIM or ECL Inputs**
- **32-Bit Dynamic Range**
- **Common Gate to Control Counting**
- **Bidirectional Counting with Preset**
- **Fast Readout via VME Backplane**

FOR COUNTING AND PRE-SET SCALING IN CONTROL SYSTEMS AND EXPERIMENTS

The VME Models 1151E and 1151N count 16 sources of detector pulses and logic signals from physics research experiments or monitor/control applications. High counting rates and wide dynamic range are coupled to flexible control for count up or count down requirements.

Two versions are available depending on the input signal standard and connector selected. Model 1151N accepts standard NIM signals via LEMO style 00 connectors. Model 1151E accepts ECL signals and connectors, and is compatible with LeCroy high density ECLine instrumentation.

The readout of this instrument is in accordance with the VME Standard (ANSI/IEEE-1014). Therefore, this scaler may be controlled and read out with standard VME hardware systems (e.g. VME Master) and software packages.

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FUNCTIONAL DESCRIPTION

A scaler is a pulse counter used to register pulses from discriminator and fast logic modules. Modern scalers usually do not have a visual readout display (i.e., they are "blind"), but rather communicate through a bus system (in this case VME) to a host computer.

Each input of the Model 1151 is capable of running at speeds up to 80 MHz. Each channel counts up to 2^{32} (> 4 billion), high enough that it will not overflow under most applications.

In addition, any scaler may be used as a preset counter. A preset channel will count down from its initial value and then generates an OR'd NIM output pulse when it reaches zero.

The 1151 module is made up of two intermeshed systems. One section of circuits operates in real time to count the number of incoming pulses present at the front-panel coincident with a common gate signal. The gate signal is a required input signal. The gate is used to define a time window during which pulses on the 16 individual inputs will be counted.

The second section of the Model 1151 operates under control of the VME bus to setup the counters, and then read and/or reset their contents. The external logic must coordinate the interaction of these two systems to provide meaningful test data.

SPECIFICATIONS

Inputs: 16 scaler inputs. Model 1151N, NIM levels, Lemo 00 connector, 50 Ω termination. Model 1151E, ECL levels, 34-pin IDC header, 100 Ω termination.

Input Pulse Width: Minimum pulse width: 5 nsec. Maximum rate: 80 MHz.

Gate Input: NIM levels, Lemo 00 connector, 50 Ω termination.

CLEAR: Negative NIM level, Lemo 00 connector, 50 Ω termination. Minimum pulse width: 70 nsec.

TRIG OUT: NIM levels, Lemo 00 connector, output is generated when any counter reaches zero in count-down mode.

Configuration: 32-bit, bidirectional binary scalers; 16 independent channels with common gate input. Any one channel may be used as a preset counter. Preset output generates an OR'd NIM pulse output.

VME Control: A24 D16/D32 VME protocol. Module Address may be set with digital switches. VME functions include: Read scalers content, Write preset, General reset, 16-bit identification register.

Indicators: A channel LED lights up for 1 msec when a channel is counting. DTACK LED lights for 1 msec when the module is addressed. BERR lights for 1 msec when a module response error occurs.

Size: 6U Eurocard format.

Power: +5 V at 9.0 A, -12 V at 0.2 A.

Allocation of Address Space

Base Address	Function Implementation
0xFE	Rev Number, Serial Number
0xFC	Manufacturer Number, Module Type
0xFA	Fixed Module ID
:	:
0xBC	Read Scaler 16
:	:
0x84	Read Scaler 2
0x80	Read Scaler 1
:	
0x7C	Read, Reset, Write, Preset 16
:	:
0x44	Read, Reset, Write, Preset 2
0x40	Read, Reset, Write, Preset 1
:	
:	:
0x00	Generate Module Reset

This instrument was designed by CEN SACLAY, France.

2.0 PRODUCT DESCRIPTION

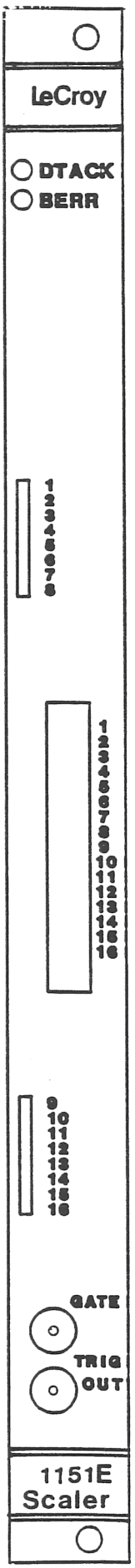
2.1 OVERVIEW

The LeCroy 1151N and 1151E VME Scaler modules were designed to count up to 16 separate channels of NIM/ECL level input pulses, respectively, from detector or logic signals, in physics research experiments and/or monitoring/controlling applications. The modules consist of 16 counting registers of 32 bit each, and have a maximum frequency of 80 MHz. Each counter can be reset to zero and placed in either an up count or a down count (preset count) mode. A preset count can be written into each register which automatically institutes a down count mode, and the receipt of each input pulse would then decrement the count by 1. When any of the down count registers reaches its terminal count (all 1's), a NIM level TRIGOUT pulse is generated on a front-panel connector.

The TRIGOUT signal, indicates that one of the 16 channels has received a "preset count plus one" number of input pulses. The TRIGOUT signal is delayed 20 nS relative to the input pulse that causes its generation. The same condition can be used to trigger a Bus Interrupter Module which can then generate a VME Bus Interrupt under program control.

The modules conform to the VME standard for double-height boards (6U 160mm), with both P1 and P2 rear connectors. The front panel contains 16 counting inputs, the GATE input, the TRIGOUT output, and 18 LED's located near each connector to indicate the presence of the corresponding signals. Two other LED's indicate the DTACK and BERR signals which are generated by the module on the VME Bus. See Figure 1 for details of the front-panel layout.

A VME Bus master can read the contents of the counting registers, with or without resetting them to zero, or can write in the value of the preset count and automatically force a down count mode. A VME Bus write to a particular location or a VME Bus SYSRESET signal will reset all the registers to zero.


LeCroy
DTACK
BERR
1
2
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4
5
6
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8
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3
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7
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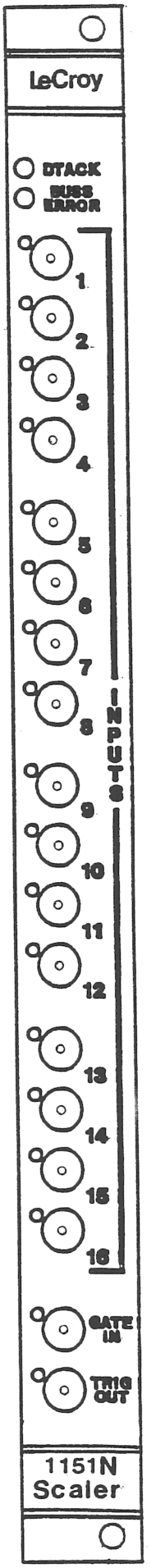
15
16
GATE
TRIG
OUT
1151E
Scaler


LeCroy
DTACK
BUSS
ERROR
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15
16
INPUTS
GATE
IN
TRIG
OUT
1151N
Scaler

Figure 1

2.2 SPECIFICATIONS

INPUTS:

16 PULSE INPUTS	to be counted during presence of GATE signal, minimum pulse width 5 nS.
	Model 1151N - NIM levels, terminated into 50 Ω.
	Model 1151E - ECL level input.
RESET	F/P fast clear; NIM level input.
GATE IN	Count enable signal; NIM level input.

OUTPUTS:

TRIGOUT	pulse output whenever any of the 16 registers is set to a down count mode and is decremented to all ones, indicating that the number of input pulses during the GATE signal has reached pre-set count + 1; NIM level output.

CAPABILITY Sixteen 32-bit binary up/down counting registers, Maximum count per register - 4,294,967,295, Maximum counting frequency - 80 MHz

LED Displays:

16 inputs(red)	denotes status of input levels.
GATE (red)	denotes presence of GATE signal.
TRIGOUT (red)	denotes that one of the 16 channels received preset number of input pulses during GATE signal.
DTACK (green)	denotes module access on VME Bus.
BERR (red)	denotes module bus error.

VME Interface: VME A24 with D16, D32 Protocol. Base address on module set by four hexadecimal switches.
VME read of each count register with reset to zero.
VME read of each count register without reset to zero.
VME write of preset count into each count register with automatic setting of register into down-count mode.
VME reset of all registers to zero.
VMEbus SYSRESET to reset all registers to zero.

VME read of module manufacturing information.
VME read of module identifier.
VME BERR is generated whenever an invalid access is detected by the modul

Connectors: Model 1151E (ECL) front-panel - 34 pin flat ribbon connector 2 pins/channel.

Model 1151N (NIM) - 16 front-panel LEMO coaxial connectors terminated in 50 Ω.

RST, GATE, TRIGOUT - 3 front-panel LEMO coaxial connectors.

Power Supply + 5 V @ 9.0 Amps, -12V @ 0.2 Amps.

2.3 Controls and Connectors

2.3.1 Inputs

The 16 counting inputs are located in the center of the front-panel and are numbered 1 to 16 top to bottom. They are comprised of either 16 LEMO coaxial connectors terminated in an impedance of 50 ohms for NIM signal level inputs, or a flat ribbon connector for ECL inputs. The GATE signal input connector is a LEMO coaxial connector terminated with 50 Ω. The RST input provides the user with a NIM level fast clear which resets all channels to zero.

2.3.2 Outputs

At the bottom of the panel is the TRIGOUT output on a LEMO coaxial connector terminated in 50 Ω.

2.3.3 Displays

At the top of the panel is a green LED marked DTACK which lights for about one millisecond each time the module is successfully accessed and responds with the DTACK signal on the VME bus. Below it is a red LED marked BERR which lights for about 1 mS whenever the module is accessed erroneously and responds with a BERR (Bus Error) signal on the VME Bus. Due to the 1 mS persistence, a single DTACK on BERR will be seen.

An LED is present at each input connection, to indicate the presence of the corresponding signal. It must be noted that a single input pulse will not be discernible on the LED. A series of input pulses must occur before its presence can be viewed. Essentially, the brightness of the LED will be proportional to the frequency of the pulses.

2.4 VME Interface

The module operates in an A24 D32/D16 mode. The address of the module must be specified in a 24-bit field and the data to and from the module can appear in either 32 or 16 bit word formats. The 6 address modifier bits (AM0 - AM5) must be either hex 3D or 39, to specify a 24 bit address field in either a supervisory or non-privileged data access mode respectively.

The base address on the module is selected by means of four hexadecimal rotary switch located on a sub-assembly that plugs into the board. Each base address (16 MSB's), reserves a page of 256 locations (8 LSB's) for each module. Address bits A23 - A20 are set with the top most switch, bits A11 - A8 are the bottom most switch.

A VME Bus D16 word write to address (BASE + 0x00) causes a Master Reset, which resets the contents of all 16 counting registers to zero and also sets all bits of the Preset Count Register to the preset count mode. For this write only, the data on the bus is disregarded.

Reading of the 16 counting registers can occur at two address fields relative to the base. In the first field, between (BASE + 0x40) thru (BASE + 0x7C), the registers can be read and then automatically reset to zero. In the second field, located between (BASE + 0x80) thru (BASE + 0xBC), the registers can be read without any effect on the register contents. One LWORD access containing 32 bits or two 16 bit word accesses, can be used.

A read cycle of one LWORD at address (BASE+0x40) will read the contents of Register No. 1 as a 32-bit word, with the contents reset to zero after the read. This read will also set the corresponding bit in the Preset Count Register to the count state. A D16 word read access at address (BASE + 0x40) will read out the 16 most significant bits (MSB) of the counter, while a D16 word read access at address (BASE + 0x42) will read out the 16 least significant bits (LSB) After the LSB read, the entire 32-bit counter will be reset to zero and the corresponding bit in the Preset Count Register set to the count state. The latter will not occur after the MSB read.

Base Address +	Function Description
0xFE	Read Revision # / Serial #
0xFC	Read Manufacturer # / Module Type
0xFA	Read Fixed Module ID #
...	...
0xF0	Unused address space
...	...
0xBC	Read Scaler Channel # 16
0xB8	Read Scaler Channel # 15
0xB4	Read Scaler Channel # 14
0xB0	Read Scaler Channel # 13
0xAC	Read Scaler Channel # 12
0xA8	Read Scaler Channel # 11
0xA4	Read Scaler Channel # 10
0xA0	Read Scaler Channel # 9
0x9C	Read Scaler Channel # 8
0x98	Read Scaler Channel # 7
0x94	Read Scaler Channel # 6
0x90	Read Scaler Channel # 5
0x8C	Read Scaler Channel # 4
0x88	Read Scaler Channel # 3
0x84	Read Scaler Channel # 2
0x80	Read Scaler Channel # 1
...	...
0x7C	Read, Reset, Write, Preset, Ch # 16
0x78	Read, Reset, Write, Preset, Ch # 15
0x74	Read, Reset, Write, Preset, Ch # 14
0x70	Read, Reset, Write, Preset, Ch # 13
0x6C	Read, Reset, Write, Preset, Ch # 12
0x68	Read, Reset, Write, Preset, Ch # 11
0x64	Read, Reset, Write, Preset, Ch # 10
0x60	Read, Reset, Write, Preset, Ch # 9
0x5C	Read, Reset, Write, Preset, Ch # 8
0x58	Read, Reset, Write, Preset, Ch # 7
0x54	Read, Reset, Write, Preset, Ch # 6
0x50	Read, Reset, Write, Preset, Ch # 5
0x4C	Read, Reset, Write, Preset, Ch # 4
0x48	Read, Reset, Write, Preset, Ch # 3
0x44	Read, Reset, Write, Preset, Ch # 2
0x40	Read, Reset, Write, Preset, Ch # 1
...	...
0x1F	Unused address space
...	...
0x00	Master Reset

Figure 2 Allocation of Address Space

Registers 2, 3, ... 16 can be similarly accessed at addresses (BASE + 0x44), (BASE + 0x48),.(BASE + 0x7C), to read out a 32 bit LWORD of the entire contents or as a 16 bit word of the MSB's. Accesses to the intermediate even addresses (BASE + 0x46), (BASE + 0x50),...(BASE + 0x7D) will read out the 16 LSB's. Reset of the counter contents to zero and setting of the Preset Count Register bit to the count mode will take place either after a LWORD read or after a D16 word read of the LSB's, and not after a D16 word read of the MSB's. For this reason the MSB should be read out first.

A LWORD read access at address (BASE + 0x80) will read out the entire 32 bit contents of Register 1 without any reset to zero, or any change to the Preset Count Register. A D16 word read access at addresses (BASE + 0x80) and (BASE + 0x82) will read out the 16 MSB's and 16 LSB's of the Register 1 respectively, without any reset to zero or change to the Preset Count Register. Registers 2 - 16 can be similarly accessed at addresses (BASE + 0x84), (BASE + 0x88), (BASE + 0xBC) without any reset of the register contents. LWORD read accesses at the addresses shown in the table will yield the contents of the entire 32 bit register.

To write a preset count into a register, VME Bus write accesses must be made to addresses (BASE + 0x40) - (BASE + 0x7C). A write cycle of an LWORD to address (BASE + 0x40) will write a 32-bit value into Register No. 1 and set the appropriate bit in the preset count register to the preset count state. D16 word write accesses to address (BASE + 0x40) and (BASE + 0x42) will modify the 16 MSB's then LSB's and sets the preset count register bit. Any D16 or D32 write to a counting register will set the corresponding bit in the Preset Count Register to a preset count mode.

The three highest addresses locations are used for module identification as follows:

	15 10	9 0	
BASE + 0xFC	No. of Mfg.	Module Type	LeCroy Mfg. # = 4 1151E/N Module Type = 7

	15 12	11 0	
BASE + 0xFE	Revision	Serial No. of Module	Revision # = 1 Serial # = 2

	15 8	7 0
BASE + 0xFA	0xFA	0xF5

Fixed Module Identifier

The BERR (bus error) signal will be generated when an access to an unused location or an invalid access to a used location is detected. For each VME Bus access to an address within the page, the module will respond either with a DTACK or a BERR.

3.0 INSTALLATION

3.1 General

The user must take into consideration the fact that operations on the front-panel are being executed in real time, and are performed asynchronously with those occurring on the VME Buses. In particular, one should avoid writing a preset value to a counting register, while the latter is in the process of counting. Reading a counting register without a reset to zero will not disturb the functioning of the counter, although the value read may be incorrect if the counter is in the process of updating.

External logic must be used to ensure the proper coordination of front end operations and those linked to the VME bus (See Section 4.5 Sequence of Operation).

The 1151 Scaler is a standard 6U 160mm VME module and can be used in any slot in a VME crate. Voltages of +5 and -12 must be present on the backplane with sufficient current drive to power all the inserted modules. The ventilation of the modules should be in proportion to the power consumption. Care should be taken to prevent any obstruction to the air inlets and outlets.

Due to power consumption requirements, the 1151 module MUST only be plugged into backplanes containing both P1 and P2 connectors. Inserting the module with the crate powered up must be avoided.

3.2 Setting in Base Address

Before inserting the module, the user must set its base address on four rotary hex switches, making sure that the selected page is located in an unused portion of the microprocessor's memory space. The base address must be different for every module in the same systems. The first 256 bytes following the base address are allocated to the module.

3.3 Cabling the 1151

The logic pulses which the 1151 will count are generated by a separate discriminator and sent via cables to the scaler. The 1151N accepts NIM levels and uses LEMO connectors in the front-panel inputs. The 1151E accepts ECL levels via ribbon cable to a front-panel 34-pin connector. If the distance between scaler and discriminator is short then a flat ribbon cable can be used(LeCroy part # STP-DL/34-L). If the distance is over 1 meter, it is recommended to use twist and flat cable (LeCroy part # DC2/34-L) where L is length in feet.

3.4 Setting the Input Signals

For either the 1151N or 1151E versions, the minimum input pulse duration is 5 nS. Adjust the output of the discriminator to ensure this minimum width.

A negative going NIM signal must be applied to the GATE input to enable the counting. During the presence of the GATE signal, the 16 registers will count the negative going transitions on the leading edge of the input pulses.

3.5 Connecting the Trigger Output

A NIM signal will appear on the TRIGOUT coaxial connector whenever any one of the 16 counters is in the preset count mode and reaches its terminal count. It will be substantially equal in duration to the width of the corresponding input pulse but will be delayed by about 20 nS relative to that input pulse. This output can be used by other units in determining the counting status of the scaler.

4.1 Role of the Bus

Upon the startup of an acquisition program, reading the identification registers makes it possible to check the presence on the modules at the provided address space. It also facilitates the setting up of a data base in which to record the history of the module.

In the acquisition program itself, VME bus accesses permit reading the contents of any register with or without reset to zero, writing a preset count into any register, and simultaneously resetting the contents of all registers to zero.

Access to the on board bus interrupt module (BIM) is effected via the VME Bus. The BIM can be initialized and enabled to generate an interrupt when any counter in a preset mode reaches (preset count + 1).

4.2 Preset Count Register

A 16 bit register is used to store the mode of the 16 counting registers, each one of which can be either in a count (up count) or preset count (down count) mode. One bit is allocated per channel to establish the mode of its corresponding counting register. A bit will be set to the preset count state whenever a valid VME Bus write is performed on its counting register, either as a long word or a D16 write to either the LSB or MSB of the register. A bit will be set to the count state whenever a valid VME Bus read is performed on it's counting register, either as a long word or as a D16 read of the LSB portion. A VME Bus D16 read of the MSB portion of the counting register will not change the bit. A master reset will place all 16 counting registers in the preset count mode. This register is comprised of two 8 bit addressable latch chips (74H259).

4.3 Format of the data

32 bit Transfers

The 32 bits of each counter can be accessed at addresses BASE + 0x40, BASE +0 x44, BASE + 0x7C (read with reset to zero / write) or at addresses BASE + 0x80, BASE + 0x84, BASE + 0xBC (read only with no reset) on date bits 0 - 31.

16 bit Transfers

The 32 bits of each counter are also available as two 16 bit words. The 16 most significant bits can be accessed at addresses BASE+0x40, BASE + 0x44, BASE + 0x7C (read / write with no reset) or at addresses BASE + 0x80, BASE + 0x84, BASE + 0xBC (read only with no reset) with counter bits 16 - 31 appearing on VME Bus data bits 0 - 16, respectively. The 16 least significant bits can be accessed at addresses BASE +0x42" BASE + $46, BASE + 0x82, BASE + 0x86, BASE + 0x8A (read only with no reset) with counter bits 0 - 15 appearing on VME Bus data bits 0 - 15, respectively.

4.4 Concurrent Actions

When performing 16 bit reads of the counters within address range BASE + 0x40, BASE + 0x7C, the MSB's must be read first as this does not disturb the contents. After reading the LSB's, all 32 bits of the counter are reset to zero. Reading with reset to zero also resets the corresponding bit in the preset count register, which places the counter in the count mode. The bit in the preset count register is set to a one placing the counter in the preset count mode whenever a write access of an kin is made to the corresponding counter.

A counter may be loaded with a 16 bit word write, if it is desired that the other 16 bits be zero and a read/reset has been performed.

4.5 Sequence of Operations

The general sequence of operations to be performed for each acquisition is as follows:

Initialization (via the VME bus)

- Total module reset (write to BASE + 0x00).
- Write-in of one or more preset counts.

Real-time operation

- Open the GATE input by setting it to a low state
- While the GATE is open, the pulse signals present at the 16 inputs will be counted
- Before reading the contents of the counters, stop the counting by closing the GATE input (setting it to a high state).

- The TRIGOUT signal can be used to close the GATE.
- Since counters in preset count mode continue down counting after reaching (preset count - 1) if the GATE is open, the count of the total number of input pulses will be accurate.
- The read program can re-initialize the module and restart the counting.

4.6 Software

After choosing the base address of the module by means of the on-board rotary switches, the absolute addresses corresponding to the labels (symbolic names) used in the program must be determined.

4.7 Programming

For systems using one of Motorola's 68000 family of microprocessors access to the counter registers will generally be by means of a MOVE.L (move 32 bit long word) instruction. With certain precautions, two MOVE.W (move 16 bit word) instructions may be used.

To effect a Master Reset, a write word cycle (.W) to address (BASE + 0x00) of the module should be executed. The CLEAR instruction is to be avoided due to the fact that, on some 680xx's, this instruction causes a read followed by a write cycle. The read cycle to (BASE + 0x00) would trigger a BERR signal.

For reading of the identifiers, the source addresses should be (BASE + 0xFA), (BASE + 0xFC), and (BASE + 0xFE). For other microprocessors, the appropriate memory access instructions must be used to execute the proper VME Bus read and write cycle that will not cause a BERR signal to be generated.

4.8 Registers

Figure 4 describes the functions executed by the hardware when addresses within the module page are accessed by the software.

ADDRESS	MODE	RESPONSE	FUNCTION EXECUTED
BASE+0x00	Write L	BERR	No action
	Read L	BERR	No action
	Write W	DTACK	Even or odd word, total Module Reset
	Read W	BERR	No action
	Write B	BERR	Even or odd byte, no action
	Read B	BERR	Even or odd byte, no action
BASE+0x40 to BASE+0x7C	Read L	DTACK	Read 32 bits of counter w/reset to zero and place counter in count mode.
	Write L	DTACK	Write 32 bit preset count & place counter in preset count mode.
	Read W	DTACK	Even word, read 16 MSB's w/no reset.
	W	DTACK	Odd word, read 16 LSB's w/reset to zero & set counter to count mode.
	Write W	DTACK	Even word, write 16 MSB's & place counter into preset count mode.
	Read B	BERR	Odd or even byte, no action.
	Write B	BERR	Odd or even byte, no action.
BASE+0x80 to BASE+0xBC	Read L	DTACK	Read 32 bits of counter w/no reset
	Write L	BERR	No action
	Read W	DTACK	Even word, read 16 MSB's w/no reset.
	W	DTACK	Odd work, read 16 LSB's w/no reset.
	Write W	BERR	Even or odd word, no action.
	Read B	BERR	Odd or even byte, no action.
	Write B	BERR	Odd or even byte, no action.
BASE+0xFA	Read L,B	BERR	No action
	Write L,B	BERR	No action
	Read L,B	DTACK	Validation 0xFAF5
	Write W	BERR	No action

Figure 4: Memory Map

4.9 Initialization

Issuing the SYSRESET command on the VME Bus resets all the modules residing on the bus. If an individual module reset is desired, the total module reset command must be used.

5.1 Introduction

The 1151 module is made up of two intermeshed systems. One section of circuits operates in real time to count the number of incoming pulses present at the front-panel coincident with a common gate signal. Another section of circuits operates under control of the VME Bus to setup the counters, and then read and/or reset their contents. The external logic must coordinate the interaction of these two systems to provide meaningful test data.

This module is chiefly implemented in "FAST" TTL logic. A block diagram appears in Figure 5 below. Double lines are used to denote connections to the VME Bus.

5.2 Real Time System

This circuitry operates on the 16 counting inputs, the GATE input, and the TRIGOUT output. It contains the 16 counting registers with their associated controls, the 16 input signal level/TTL level converters, and the TRIGOUT generator.

5.2.1 Level Converters

Model 1151N - The NIM level input signals enter via 17 front- panel LEMO coaxial connectors terminated in 50 _ resistors. The conversion from NIM level to TTL level is accomplished in two stages. Each NIM signal is applied to the base of an NPN 2N918 transistor (Count inputs to T1 - T16, GATE input to T17), whose emitter output provides a level shift of -700 mV. The NIM input voltage range of 0/-800 mV is thus shifted to -700 mV/-1500 mV, compatible with standard ECL levels. These ECL level signals are then fed into 10H125 ECL/TTL converters (IC3, IC6, IC9, IC12, IC36) whose TTL outputs are applied to the coincidence circuits.

Model 1151E - The 16 ECL level input signals enter via a 34 pin flat signals are fed directly into the 10H125 ECL/TTL converters (IC3, IC6, IC9 IC12). The NIM level GATE input enters via a front panel LEMO connector and is applied to transistor T17 and ECL/TTL converter IC36.

5.2.2 Coincidence Circuits

The "ANDing" of each count input with the common GATE signal is achieved in four 74F00 chips (IC17, IC22, IC27, IC32). The minimum required overlap time between GATE and input is 5 nS, and the maximum dispersion between channels is about 0.5 nS. The output coincidence signals are applied to the clock inputs of the corresponding counters and also to two stage integrator circuits that feed the 16 front -panel LED's.

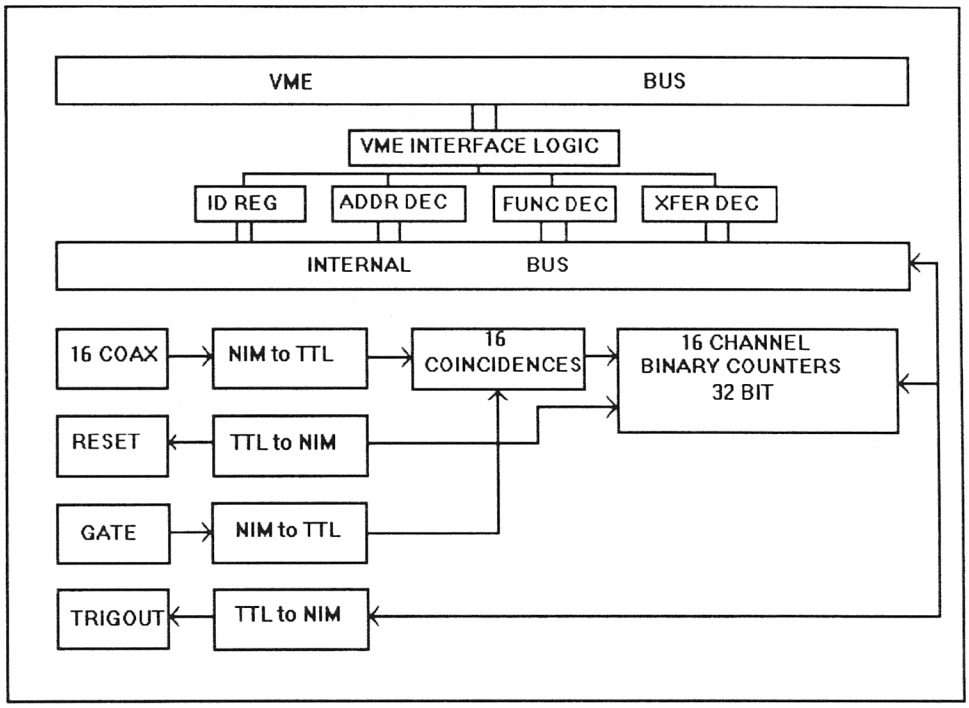


Figure 5: Block Diagram of the 1151 Scaler

5.2.3 TRIGOUT Output

When a count register in preset count mode reaches its terminal count (TC) of all ones, the corresponding count input is fed into the TRIGOUT output. This is accomplished by "ANDing" the TC signal from each counter with its corresponding count input and then "ORing" all 16 signals. Each of four identical 16L8 PALS labeled (IC129, IC134, IC138, IC142) combines the signals for four of the channels, and a 74F20 (IC137) "OR's" the four PAL outputs. The output of the 74F20, which is the TTL TRIGOUT signal, feeds three separate circuits. First, it is fed back into IC138 to generate the GIT signal, which sets a 74F74 flip flop (IC148) to provide an interrupt trigger at pin 19 of the BIM chip (IC153). Secondly, it is applied to a 10H124 (IC37) TTL/ECL converter and then to a ECL/NIM conversion circuit. The latter is comprised of a pair of two 2N918 transistors (T18 and T19), whose bases are driven by the two complementary outputs of the 10H124. The collector of one of the transistors provides the NIM level output at the front-panel TRIGOUT LEMO connector, which is capable of supplying a nominal 16 mA to a 50 _ load.

5.2.4 Counting Registers

Each counting register is made up of four synchronous, 8-bit 74F779 counters. (IC60, IC77, IC93, IC110 for channel 1 - 4). The pulse output of each coincidence circuit is "OR'd" in two 74F00 gates with write pulses derived from the (IC39 for channel 1) to provide separate clock pulses to the 16 MSB's and ±6 LSB's of the counters. This permits writes or resets to zero in either 16 or 32 bit widths. The clock pulses to each of the last three counters for each input channel are delayed by one 74F08 gate each to compensate for propagation delays in the preceding counters (IC40 for channel 1).

5.3 Counting Register Commands and Controls

The registers are arranged in groups of four, covering four channels, and have four common 16L8 Pal's in common. Two addressable 74F259 8 bit registers (IC133, IC154) store the mode (up count on preset count) of each counter, allocating one bit per channel. The information from these registers are used in IC130, IC135, IC139 and IC143 to generate the S0 and S1 select inputs to the counters establishing its working mode. Based on VME Bus signal decodes, IC131, IC136, IC140 and IC144 generate the OE (output enable) signals to the counters, enabling either 16 or 32 bits reads. IC39, IC44, IC49 and IC54 generate the write pulses to the counters. During writes, the data will contain either the preset count or all zeroes. IC129, IC134, IC138 and IC142 operates on the Terminal Count signals of its associated counters to generate one four channel contribution to the TRIGOUT signal.

5.4 VME BUS FUNCTIONS

5.4.1 Address Decoding

A subassembly on the board contains four hex rotary switches, two 74F520 8 bit comparators and two 74ALS138 1 of 8 decoders. The 16 most significant bits of the VME Bus address (A8 to A23) are compared on a bit by bit basis with the settings of the four hex rotary switches and an output generated when all 16 bits compare. In addition, VME Bus address bits A4 to A7 are decoded during the above compare and generate 16 additional outputs, which are not used in the current design.

VME Bus address bits A8 to A23 are used to select the base address of the module and reserve a page of 256 bytes. Figure 3 shows the address assignments within the page. The least significant address bits (A1 - A7) are buffered by a 74F244 chip (IC159) and applied to PAL (IC156) which decodes the functions used. The latter generates the VALEC (valid read) and VALWR (valid write) signals which set up VME Bus data transfers.

The VME Bus address modifiers, AM0 to AM5, are decoded by (IC128) and combined with the base address decode and VME Bus signal as to produce the VALADR (Valid Address) signal for the decoding PAL.

5.4.2 Function Decoding

VME Bus function decoding takes place in IC156. Two 74F244 bus receivers (IC147 and IC159) provide buffering between the VME Bus and the internal bus. IC156 utilizes internal bus signals INA1 - INA7, INWR, INLWRD, INRESET, INDS0 and INDS1, in conjunction with the VALADR signal of the PAL (IC128).

When the PAL decodes a VME Bus access that is not executable, due to an unused address, an unacceptable format, or an invalid write, it will generate the INBERR signal. When the PAL decodes an executable operation, it will generate both the appropriate decode signal and also the INDTACK signal.

The PAL output signals can be grouped into two categories: signals that indicate the decode state and signals that generate timing. Some signals must be maintained until after the end of the VME Bus cycle to perform secondary operations, such as resetting the register contents after a read.

The signal RAZTOT is generated upon decode of a word write access to BASE + 0x00 or the receipt of SYSRESET on the VME Bus. RAZTOT will cause a module reset.

The following PAL output signals indicate decode states:

1. MINA1, MINA2, MINA3 - Address bits A1, A2, and A3, respectively, maintained for 30 nS. after the end of the VME Bus cycle.

2. ECHGRA, ECHGRB, ECHGRC, ECHGRD - selects a group of 4 registers. Selection within the group is accomplished by decoding INA2 and INA3. Signal INA1 selects either the LSB or MSB for 16 bit data transfers.

3. MEMPREC1, MEMPREC2 - selects one of the two 8 bit preset count state registers.

4. LECIDEN - selects the identification register

5. VALWR, VALLEC, BYPASWR, BYPASLEC, ECRZERO - used to execute data transfers between the internal bus and the VME Bus.

The following are PAL output timing signals:

1. RAZCLK - to reset register contents to zero.

2. WRINT - to generate write accesses.

5.4.3 Data Transfers

The counters communicate with the internal data bus via tri-state bi-directional output circuits.

Reading Data - Pal's (IC131, IC136, IC140, IC144) send the contents of either 2 or 4 stages of the selected register as a function of INLWRD on the interior bus. The signals VALEC and BYPASLEC control the transfer of this data unto the VME Bus.

Resetting the Counter to Zero - For those VME Bus reads that mandate reset of the register to zero after the read, the reset is accomplished by writing in 32 zeroes. The 16 zeroes for the LSB's are derived from 74F244 bus drivers IC38 and IC59. These 16 zeroes are transferred to the MSB's by means of 74F245 transceivers IC76 and IC109. The reset signals are delayed 35 nS relative to the read by means of "ANDing" the INSD0 and INDS1 signals in a 74LS20 (IC137) and then delaying the output in a 74LS31 (IC155). Pal's IC130, IC135, IC139 and IC143 set up the register for a write.

During a 16 bit word read, the zero reset of the entire register occurs only after the LSB read. Therefore, the MSB should read first.

The RAZTOT signal, generated upon decode of a word write to BASE + 0x0 or upon receipt of the SYSRESET signal, resets all registers to zero by the same procedure described above. Pal's IC39, IC44, IC49 and IC54 generate the clock signals necessary for the write.

Write of Preset Count

Pal's IC130, IC135, IC139 and IC143 set up the addressed register for a write cycle. The signals VALWR and BYPASWR control VME writes to either 2 or 4 stages of the register. A write to a register automatically sets the corresponding bit in the 16 bit preset count register (IC133 and IC154) to the preset count (down count) mode.

Read of the Three Identifier Words

PAL IC156 generates the LECIDEN (Read Identifier) signal. This signal enables two 16L8 Pal's labeled IC126 and IC127, to feed out one of three stored 16 bit words onto the data bus, each PAL supplying 8 bits. The Pal's decode address bits INA1, INA2, and INA3 and respond with one of three unique words only if 0xA, 0xC, or 0xE, corresponding to 32 bit addresses BASE + 0xFA, BASE + 0xFC, or BASE + 0xFE, is detected.

5.4.4 Generating VME Bus Protocol

The signals VALEC and VALWR, generated by IC156 control read and write paths, respectively, between the internal data bus and the VME data bus.

The signal BYPASLEC, generated by PAL IC156, controls feeding the 16 MSB's of the internal data bus onto the 16 LSB's of the VME Bus during even address 16 bit reads. The signal BYPASWR, also generated by IC156 controls feeding the 16 LSB's on the VME Bus onto the 16 MSB's of the internal data bus during even address writes.

PAL IC156 determines whether valid or invalid VME Bus accesses have been made and then generates either a INDTACK or INBERR signal, respectively, except for valid BIM accesses. The NIM issues its own DTACK. Therefore, the INDTACK signal from the PAL is "OR'd" with the DTACK signal from the BIM in a 74F00 (IC150) and then fed to the VME Bus DTACK signal via a 74F38 open collector gate (IC132). The INBERR signal feeds the VME Bus BERR signal via another 74F38 open collector gate (IC150). These two signals are delayed relative to the bus decodes by "ANDing" the two data strobes, DS0 and DS1, in a 74F20 gate (IC137) and then passing it through a 74LS31 delay element (IC155) before having it feed the PAL.

5.5 LED Indications

The two signals INDTACK and INBERR drive two 74123 1 mS monostable circuits (IC1) whose outputs feed LED's. R63 and CH2 control the one-shot timing for DTACK, while R38 and CH1 do likewise for BERR. Thus, the green LED for DTACK and the red LED for BERR will light for 1 mS each time their respective signals are sent. 16 Led's, situated close to the 16 count inputs, indicate the presence of the input signals. There are also 2 LED's to indicate the presence of the GATE input signal and TRIGOUT output signal, each situated close to its respective connector.

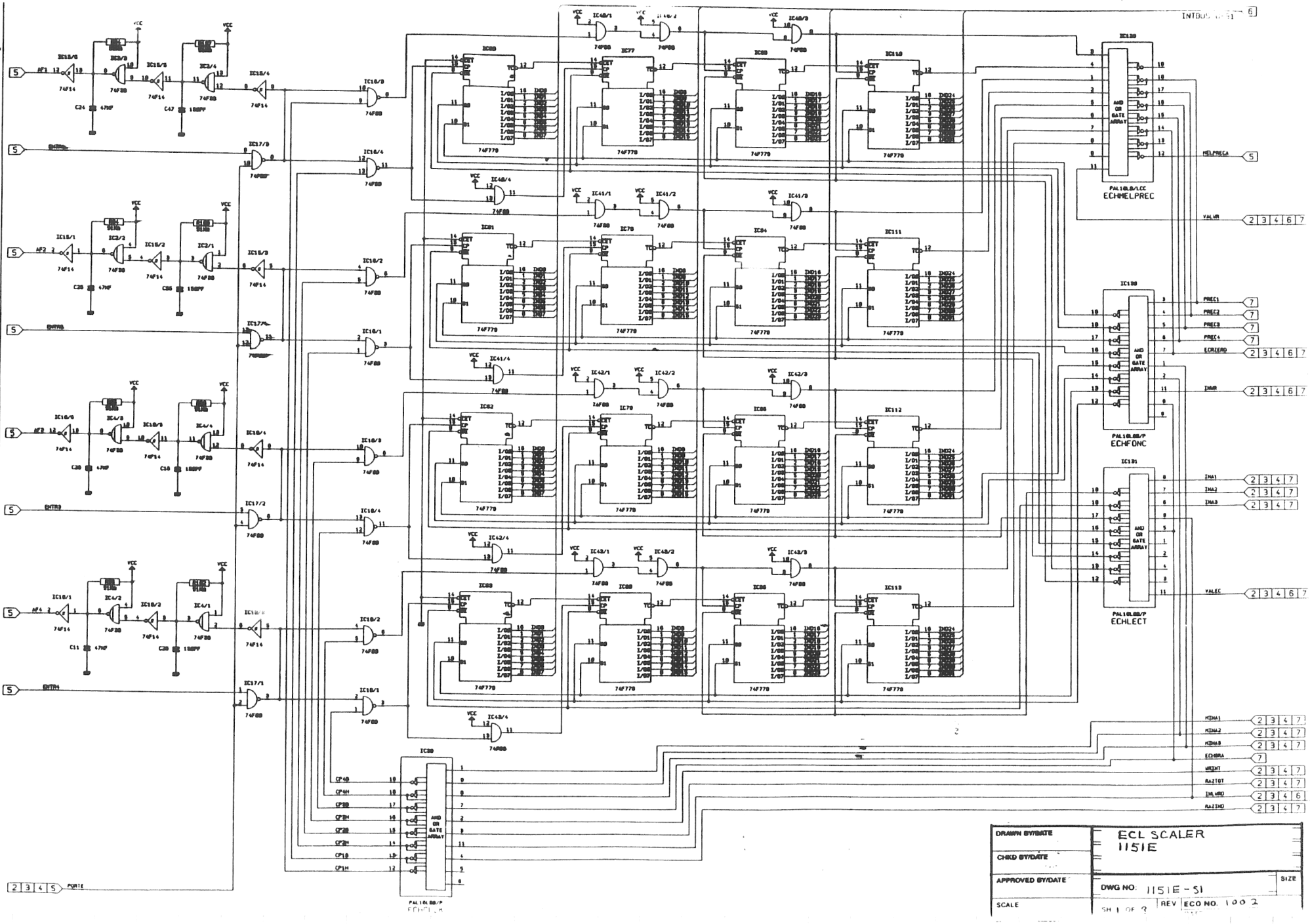
5.6 Power Supplies

The 1151 requires +5 V and -12 V from the VME bus. The -5v used by the ECL circuits is derived from the -12v using a MC7905.2 regulator (RG1).

PART NUMBER	DESCRIPTION REMARK	QTY PER
102412151	CAP CERA DISC 100V 150 PF C15,C16,C18,C20,C22, C29,C34,C39,C44, C47-C50,C55,C57,C59 C61,C63.	18
103326473	CAP CERA MONO 50V .047UF C11-C14,C17,C19,C21, C23-C25,C30,C33,C35, C38,C40,C43,C45. C28.	18
103327103	CAP CERA MONO 50V .01 UF C1-C5,C7-C10,C26, C27,C31,C32,C36,C37, C41,C42,C46,C51-C54, C60,C62,C65-C90. C56,C58,C64.	53
140493105	CAP TANT METAL CASE 1 UF CH1,CH2	2
146424106	CAP MINI ALUM 20% 10 UF CH3-CH5.	3
161225101	RES CARBON FILM 100 OHMS R134-R137.	4
161225150	RES CARBON FILM 15 OHMS R55 R139	2
161225224	RES CARBON FILM 220 K R38,R63.	2
161225331	RES CARBON FILM 330 OHMS R1,R2.	2
161225390	RES CARBON FILM 39 OHMS R62,R92.	2
161225470	RES CARBON FILM 47 OHMS R91.	1
161225471	RES CARBON FILM 470 OHMS R90.	1
161225510	RES CARBON FILM 51 OHMS R19 R20 R37 R138	4
161225513	RES CARBON FILM 51 K R56-R60,R64,R68,R70, R74,R76,R80,R82,R86, R89,R94-R115.	36
161225561	RES CARBON FILM 560 OHMS R61,R93.	2
161225681	RES CARBON FILM 680 OHMS R88 R140	2
190042102	RESISTOR NETWORK 1 K RS1	1
190892510	RESISTOR NETWORK 51 OHMS	6
205790910	IC 24 MACRO EPLD EP910 DO NOT KIT, SEND TO PROGRAMMING CENTER FOR PROGRAMMING. IC156.	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
207244124	IC QUAD TTL-MECL 10H124 IC37.	1
207244125	IC QUAD MECL-TTL 10H125 IC3,IC6,IC9,IC12, IC36.	5
208127001	IC VOLT REG -5.2V 7905.2 RG1.	1
230110005	DIODE SWITCHING 1N4448 DS1,DS2.	2
256233209	DIODE LED RED TIL209A DL2.	1
256532232	DIODE LED (GRN) TIL232-1 DL1.	1
270171918	TRANSISTOR NPN 2N918 T17-T20	4
400381040	SOCKET IC SOLD TAIL DIP-40 ICI158,TB1,ICI153.	3
402130001	CONN RT ANGL PC MTG LEMO JX17-JX19	3
403119234	HDR DBL ROW RT ANGL 34 JM1.	1
405812002	SOCKET STRIP SOLDR 20 POS	2
454311032	HDR SOLD TAIL/MALE 32 JM1 FOR 1151E-1 BOARD	2
454610096	HDR SOLD TAIL/MALE 96 JE1,JE2.	2
500860302	INSULATOR FOR TO-220	1
540407000	VME PANEL EJECTOR KIT	1
550125110	SCREW PAN HD M2.5X10	5
552425100	NUT HEX M2.5	5
574409005	WASHER SHOULDER NYLON #4	1
597110001	SHIPPING CARTON FOR VME MODULES	1
597110002	SHIPPING FOAM FOR VME MODULES	1
711151001	PC BD PREASS'Y 1151E	1
711151011	PC BD PREASS'Y 1151E-1	1
721151002	FRONT PNL TAB BOT 1151E	1
721151003	FRONT PNL PREASS'Y 1151E	1
721151022	VME FRONT PANEL TOP TAB, LECROY	1
SM200172000	IC 2-INPUT NAND 74F00 IC16-IC18,IC21-IC23, IC26-IC28,IC31-IC33, IC150,IC152.	14
SM200172008	IC AND GATE 74F08 IC40-IC43,IC45-IC48, IC55-IC58. IC50-IC53 IC160	17
SM200172014	IC HEX INV 74F14 IC15,IC19,IC20,IC24, IC25,IC29,IC30,IC34, IC35.	9
SM200172038	IC 2-IN NAND 74F38	12

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM200172038	IC 2-IN NAND 74F38 IC2,IC4,IC5,IC7,IC8, IC10,IC11,IC13,IC14, IC132,IC149,IC151.	12
SM200172074	IC D-TYP FLOP 74F74 IC148.	1
SM200172259	IC 8-BIT DMUX/LATCH 74F259 IC133,IC154.	2
SM200173138	IC DECODER 74ALS138 IC2,IC3. FOR 1151E-1 BOARD.	2
SM200174020	IC 4-IN NAND 74LS20 IC137	1
SM200174031	IC DELAY ELEMENT 74LS31 IC155.	1
SM200272779	IC 8-BIT UP/DN BIN COUNTER 74F779 IC60-IC75,IC77-IC108 IC110-IC125.	64
SM200274123	IC MONOST MULTIVIBR LS123 IC1.	1
SM200372520	IC 8-BIT COMP 74F520 IC1,IC4. FOR 1151E-1 BOARD.	2
SM200472373	IC LATCH 74F373 IC159	1
SM205720116	IC PAL 16L8-7A DO NOT KIT, SEND TO PROGRAMMING CENTER FOR PROGRAMMING. IC129,IC134,IC138, IC142.	4
SM205720168	IC PAL-C 16L8-25 DO NOT KIT, SEND TO PROGRAMMING CENTER FOR PROGRAMMING. IC39,IC44,IC49,IC54, IC126-IC128,IC130, IC131,IC135,IC136, IC139-IC141,IC143, IC144.	16
SM206874245	IC OCTAL TRANS 74F245 IC76,IC109,IC145, IC146,IC157,IC158.	6
SM207178244	IC LINE DRIVER F244 IC38 IC59 IC147	3
SM209520016	ROTARY DIP SWITCH CD1-CD4	4
SM256002001	DIODE LED RED DL19,DL20.	2
SM256002208	DIODE LED RED 8X ARRAY DL3-DL18.	2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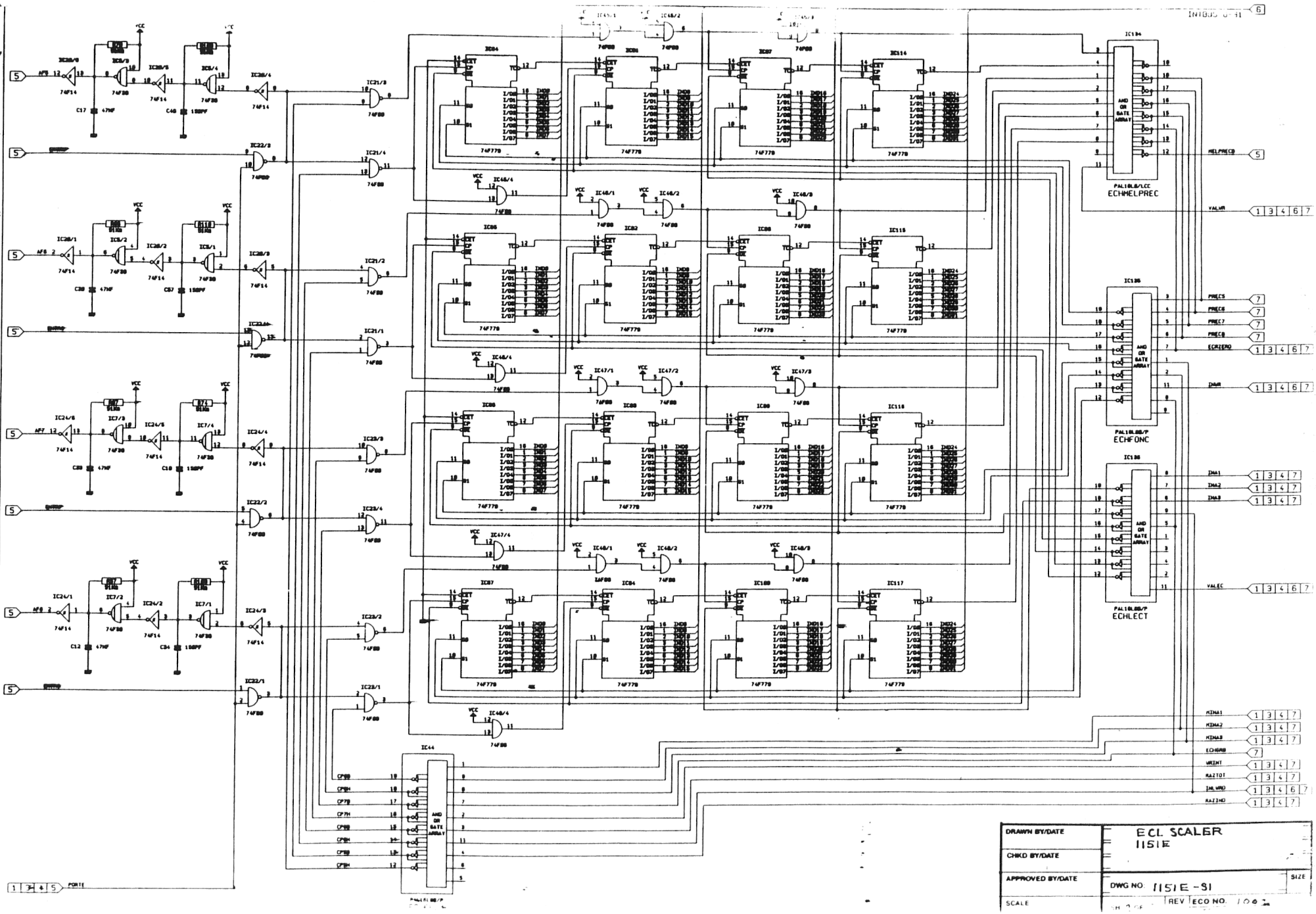
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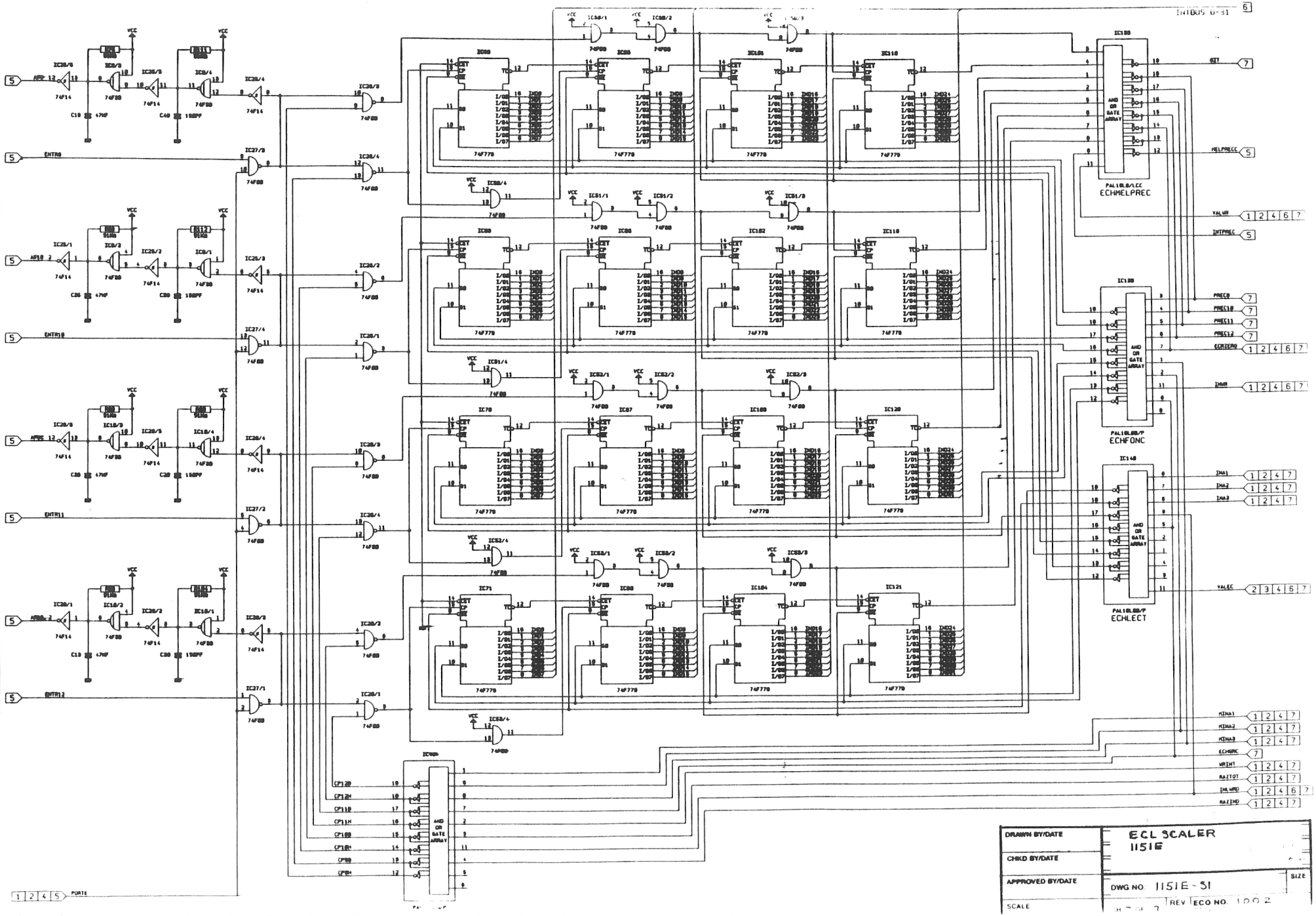
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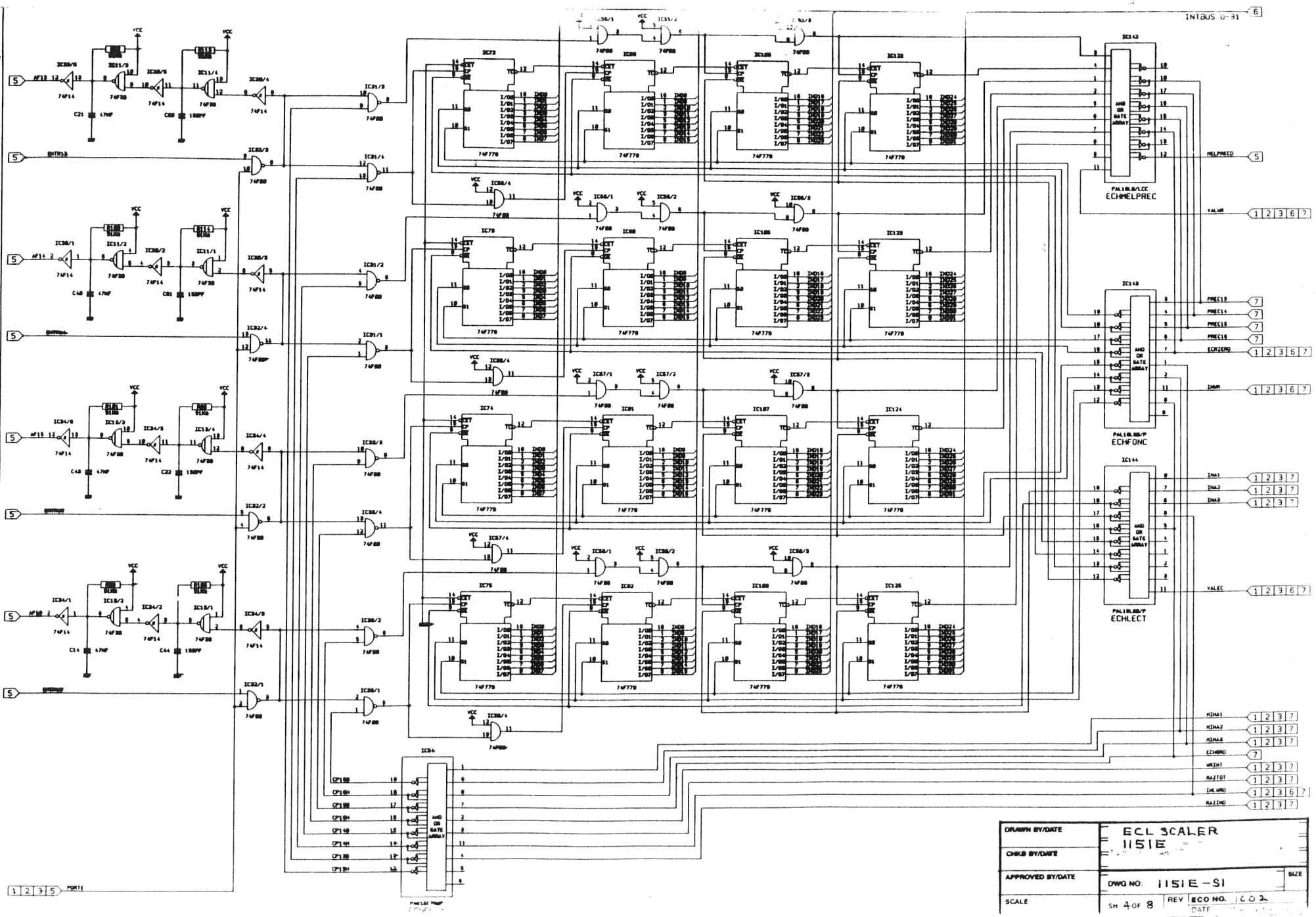
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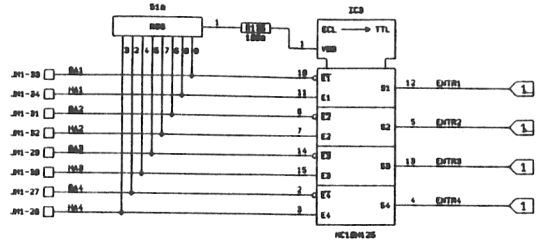

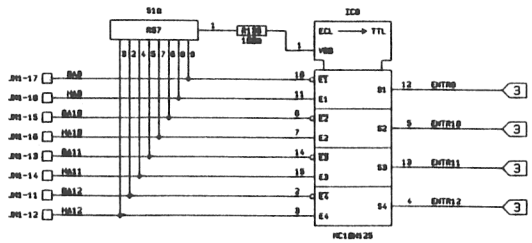

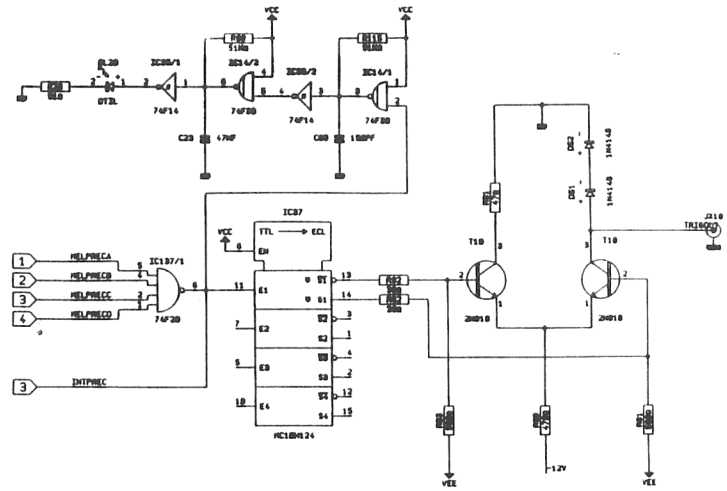

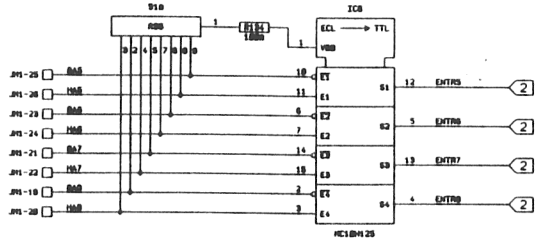

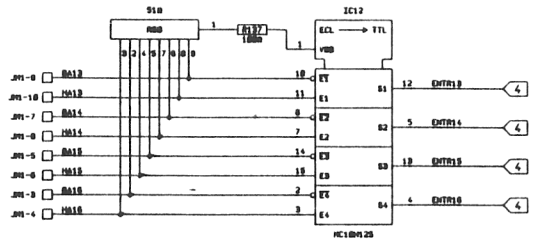

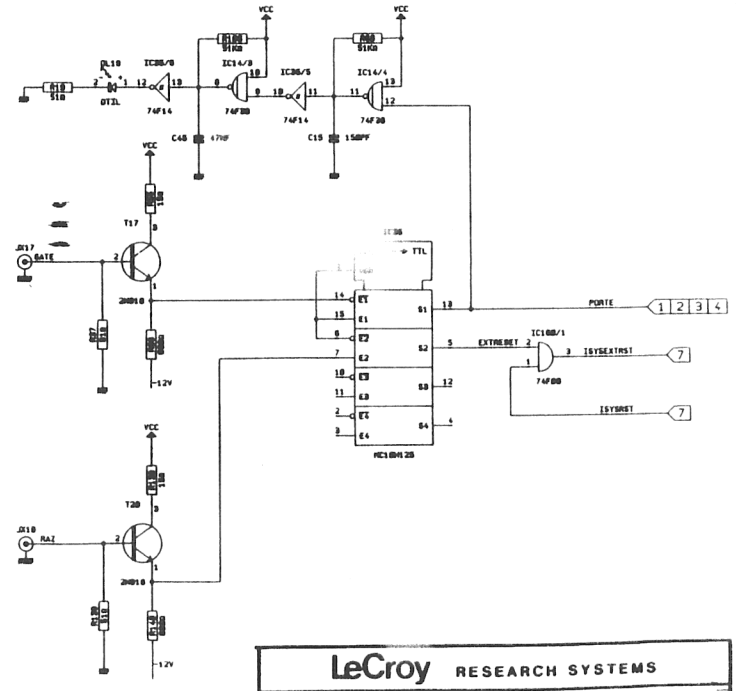

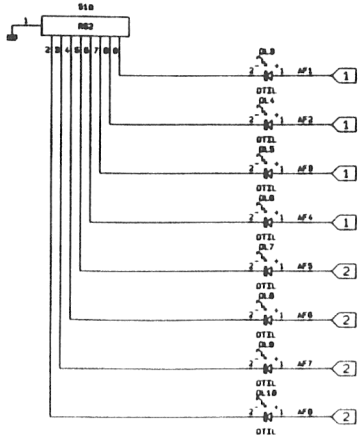

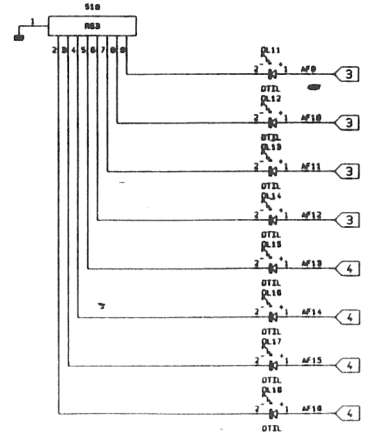

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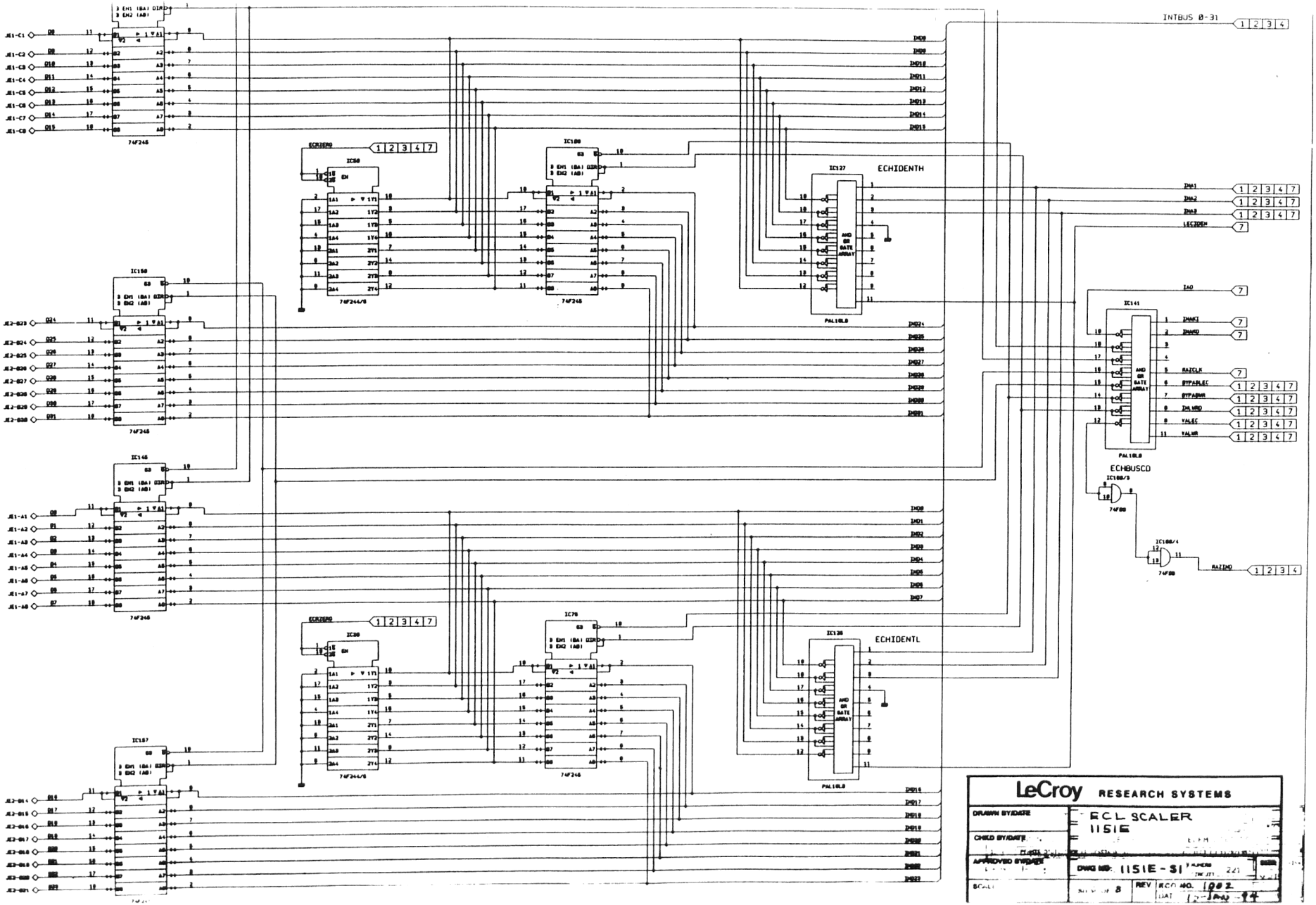
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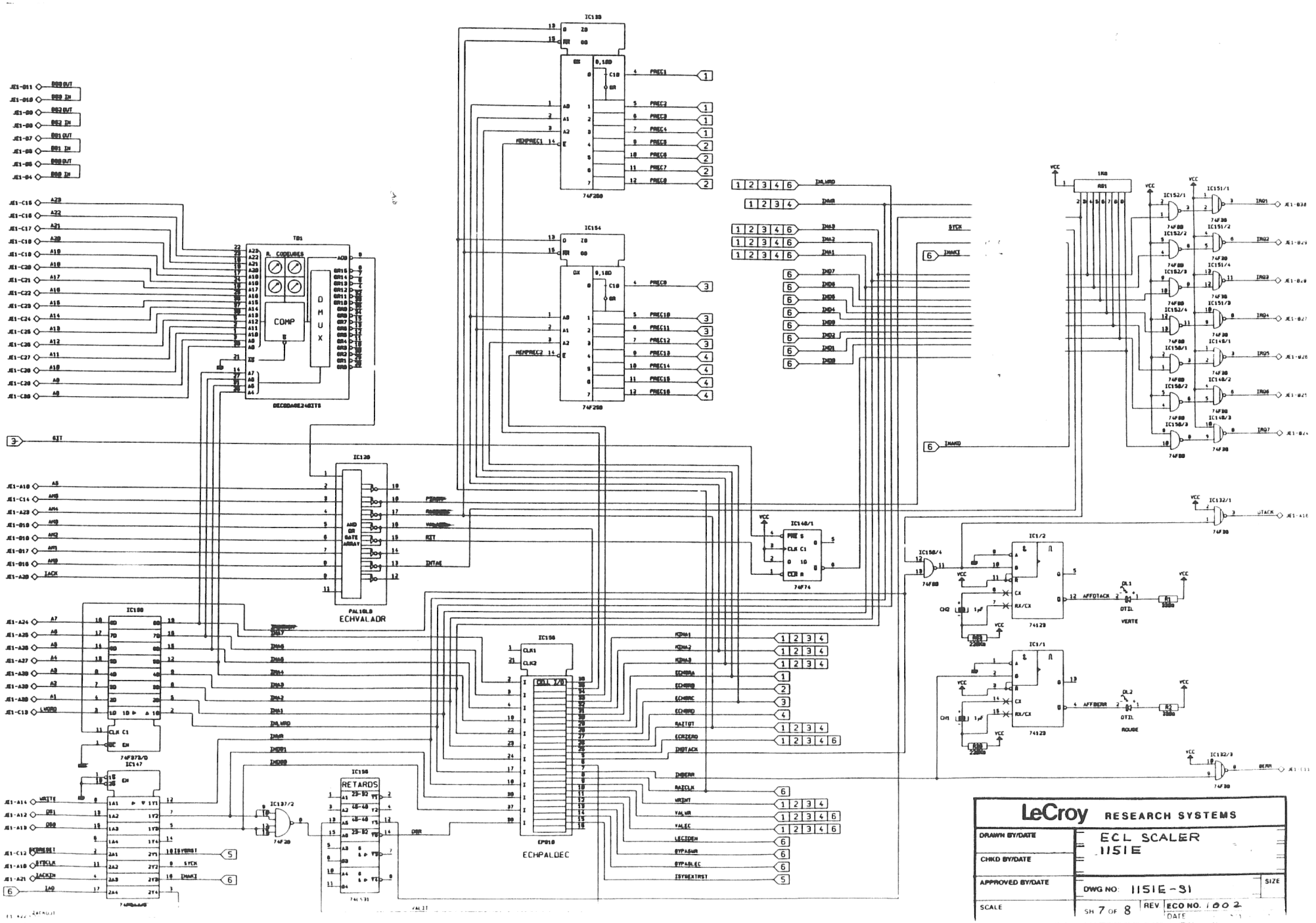
DWG NO. 1151E-S1
REV
ECO NO. 1002
DATE 12-JAN-94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TB1
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D M U X
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IC147
74F245
IC137/2
74F20
IC156
EP910
ECHPALDEC
RETARDS
IC158/1
74F74
IC158/4
74F08
IC1/2
74123
IC1/1
74123
IC151/1
IC152/1
IC151/2
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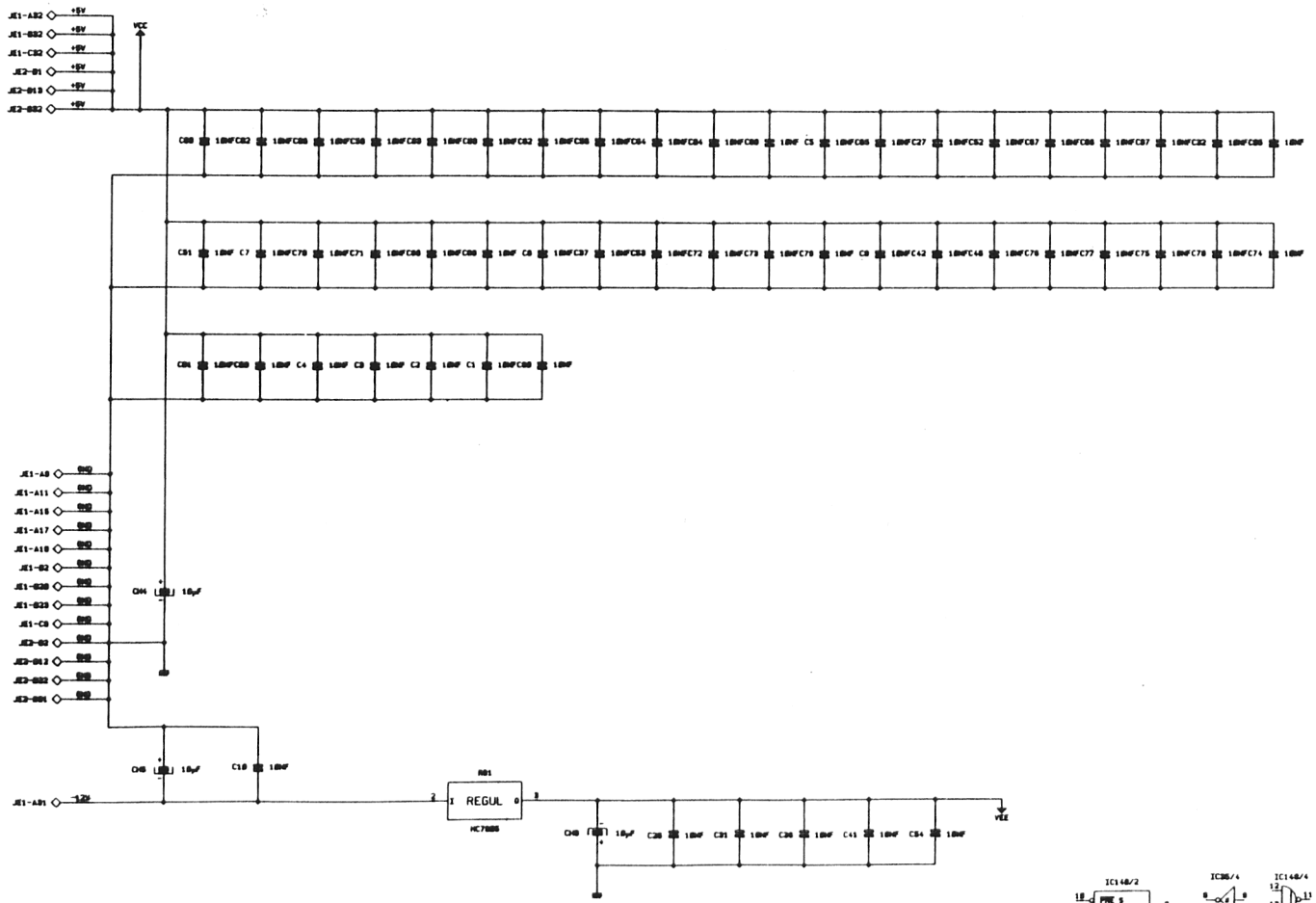
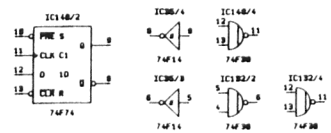
IC151/4
IC152/3
IC151/3
IC152/4
IC148/1
IC158/1
IC148/2
IC158/2
IC148/3
IC158/3
IC132/1
IC132/3
LeCroy RESEARCH SYSTEMS
DRAWN BY/DATE
CHKD BY/DATE
APPROVED BY/DATE
SCALE
ECL SCALER
1151E
DWG NO: 1151E-31
SIZE
SH 7 OF 8
REV
ECO NO. 1002
DATE



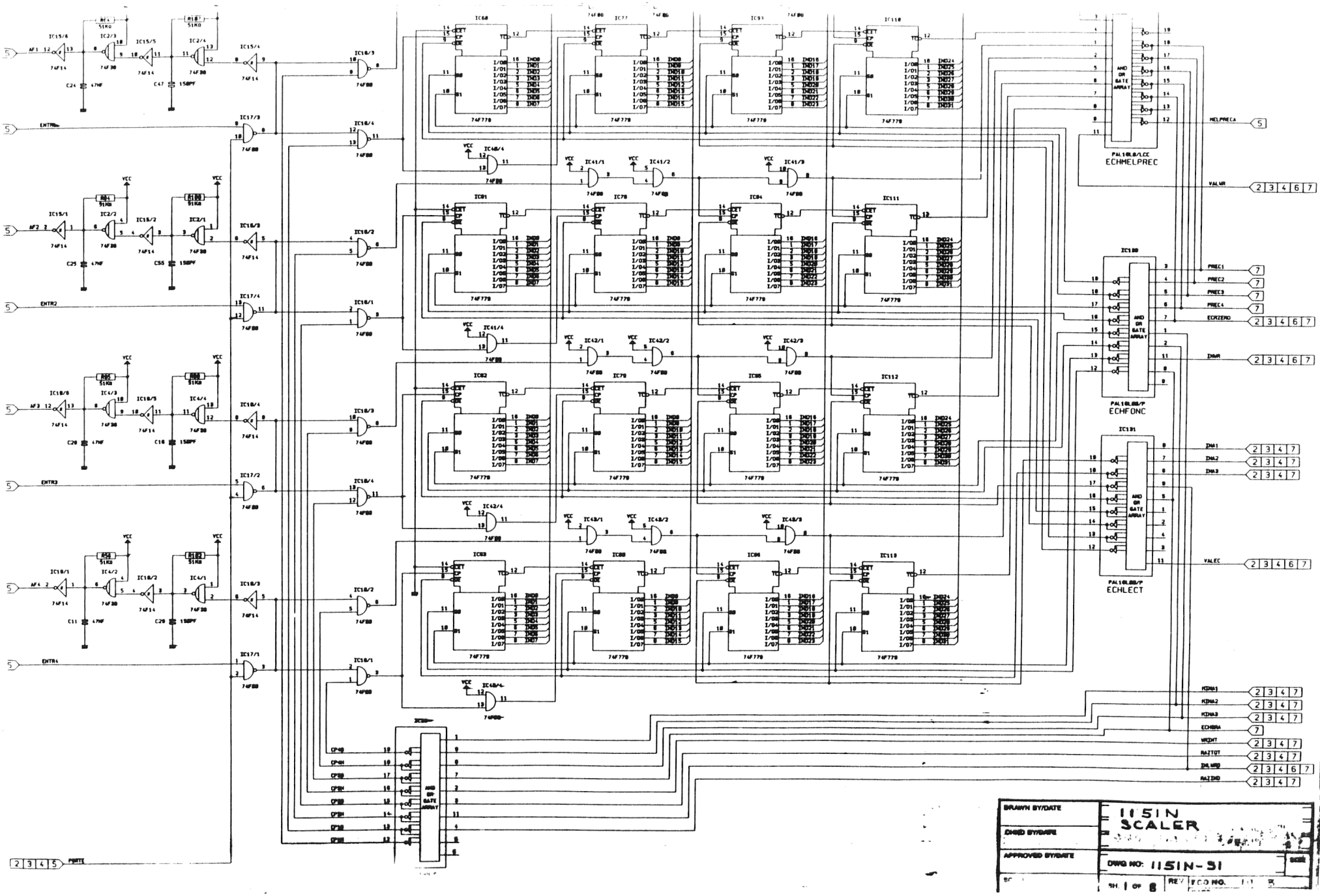


LeCroy RESEARCH SYSTEMS			
DRAWN BY/DATE	ECL SCALER 1151E		
CHKD BY/DATE			
APPROVED BY/DATE	DWG NO: 1151E-51		SIZE
SCALE	SH 8 OF 8	REV. ECO NO. 1002	DATE 15-JAN-91

PART NUMBER	DESCRIPTION REMARK	QTY PER
102412151	CAP CERA DISC 100V 150 PF C15, C16, C18, C20, C22, C29, C34, C39, C44, C47, C48, C49, C50, C55, C57, C59, C61, C63.	18
103326473	CAP CERA MONO 50V .047UF C11-C14, C17, C19, C21, C23-C25, C28, C30, C33, C35, C38, C40, C43, C45.	18
103327103	CAP CERA MONO 50V .01 UF C1-C10, C26, C27, C31, C32, C36, C37, C41, C42, C46, C51-C54, C56, C58, C60, C62, C64-C90.	54
140493105	CAP TANT METAL CASE 1 UF CH1, CH2.	2
146424106	CAP MINI ALUM 20% 10 UF CH3-CH5.	3
161225150	RES CARBON FILM 15 OHMS R39-R55, R116.	18
161225224	RES CARBON FILM 220 K R63, R96.	2
161225331	RES CARBON FILM 330 OHMS R1, R2.	2
161225390	RES CARBON FILM 39 OHMS R61, R92.	2
161225470	RES CARBON FILM 47 OHMS R91.	1
161225471	RES CARBON FILM 470 OHMS R90.	1
161225510	RES CARBON FILM 51 OHMS R3-R37, R117.	36
161225513	RES CARBON FILM 51 K R56-R60, R64, R68, R70, R74, R76, R80, R82, R86, R89, R94-R115.	36
161225561	RES CARBON FILM 560 OHMS R62, R93.	2
161225681	RES CARBON FILM 680 OHMS R65-R67, R69, R71-R73, R75, R77-R79, R81, R83-R85, R87, R88. R118.	18
190042102	RESISTOR NETWORK 1 K RS1	1
205790910	IC 24 MACRO EPLD EP910 IC156. DO NOT	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
205790910	IC 24 MACRO EPLD EP910 INCLUDE ON KIT. SEND TO THE PROGRAMMING CENTER FOR PROGRAMMING.	1
207244124	IC QUAD TTL-MECL 10H124 IC37.	1
207244125	IC QUAD MECL-TTL 10H125 IC3, IC6, IC9, IC12, IC36.	5
208127001	IC VOLT REG -5.2V 7905.2 RG1.	1
230110005	DIODE SWITCHING 1N4448 DS1, DS2	2
256233209	DIODE LED RED TIL209A DL2.	1
256532232	DIODE LED (GRN) TIL232-1 DL1.	1
270171918	TRANSISTOR NPN 2N918 T1-T20.	20
400381040	SOCKET IC SOLD TAIL DIP-40	3
402130001	CONN RT ANGL PC MTG LEMO JX1-JX19.	19
454311032	HDR SOLD TAIL/MALE 32 JM1. FOR 1151E-1 BOARD.	2
454610096	HDR SOLD TAIL/MALE 96 JE1, JE2.	2
500860302	INSULATOR FOR TO-220	1
540407000	VME PANEL EJECTOR KIT	1
550125110	SCREW PAN HD M2.5X10	5
552425100	NUT HEX M2.5	5
574409005	WASHER SHOULDER NYLON #4	1
597110001	SHIPPING CARTON FOR VME MODULES	1
597110002	SHIPPING FOAM FOR VME MODULES	1
711151011	PC BD PREASS'Y 1151E-1	1
711151021	PC BD PREASS'Y 1151N	1
721151021	FRONT PNL PREASS'Y 1151N	1
721151022	VME FRONT PANEL TOP TAB, LECROY	1
721151023	FRONT PNL TAB BOT PREASS'Y 1151N	1
SM200172000	IC 2-INPUT NAND 74F00 IC16-IC18,IC21-IC23, IC26-IC28,IC31-IC33, IC150, IC152.	14
SM200172008	IC AND GATE 74F08 IC40-IC48,IC50-IC53, IC55-IC58, IC160.	17
SM200172014	IC HEX INV 74F14 IC15, IC19, IC20, IC24, IC25, IC29, IC30, IC34, IC35.	9
SM200172038	IC 2-IN NAND 74F38	12

PART NUMBER	DESCRIPTION REMARK	QTY PER
SM200172038	IC 2-IN NAND 74F38 IC2, IC4, IC5, IC7, IC8, IC10, IC11, IC13, IC14, IC132, IC149, IC151.	12
SM200172074	IC D-TYP FLOP 74F74 IC148.	1
SM200172259	IC 8-BIT DMUX/LATCH 74F259 IC133, IC154.	2
SM200173138	IC DECODER 74ALS138 IC2, IC3. FOR 1151E-1 BOARD.	2
SM200174020	IC 4-IN NAND 74LS20	1
SM200174031	IC DELAY ELEMENT 74LS31 IC155	1
SM200272779	IC 8-BIT UP/DN BIN COUNTER 74F779 IC60-IC75, IC77-IC108, IC110-IC125.	64
SM200274123	IC MONOST MULTIVIBR LS123 IC1.	1
SM200372520	IC 8-BIT COMP 74F520 EC1, IC4. FOR 1151E-1 BOARD.	2
SM200472373	IC LATCH 74F373 IC159.	1
SM205720116	IC PAL 16L8-7A IC129, IC134, IC138, IC142. DO NOT INCLUDE ON KIT. SEND TO PROGRAMMING CENTER FOR PROGRAMMING.	4
SM205720168	IC PAL-C 16L8-25 IC39, IC44, IC49, IC54,IC126-IC128, IC130, IC131, IC135, IC136, IC139, IC140, IC141, IC143, IC144. DO NOT INCLUDE ON KIT. SEND TO PROGRAMMING CENTER FOR PROGRAMMING.	16
SM206874245	IC OCTAL TRANS 74F245 IC76, IC109, IC145, IC146, IC157, IC158.	6
SM207178244	IC LINE DRIVER F244	3
SM209520016	ROTARY DIP SWITCH CD1-CD4	4
SM256002001	DIODE LED RED DL3-DL20.	18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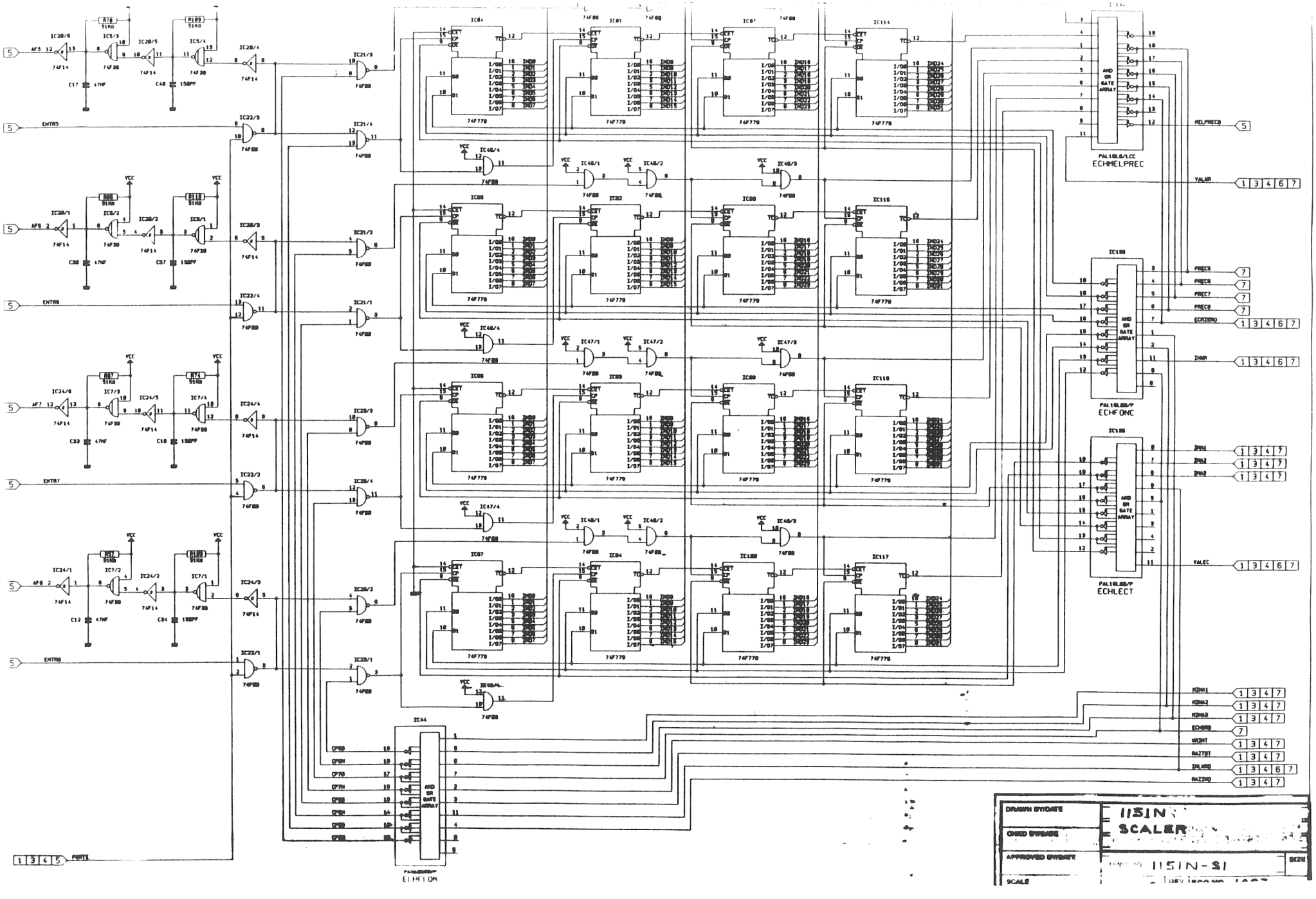
ECHFONC
ECHLECT
AND OR GATE ARRAY
74F778
74F00
74F14
74F30
MELPRECA
VALWR
PREC1
PREC2
PREC3
PREC4
ECHZERO
INWR
INA1
INA2
INA3
VALEC
ECHINA
WRONT
RAITOT
INLWD
RAIIND
ENTR1
ENTR2
ENTR3
ENTR4
PORTE
BRAWN BY/DATE
CHKD BY/DATE
APPROVED BY/DATE
1151N
SCALER
DWG NO: 1151N-51
SHT. 1 OF 8
REV
ECO NO.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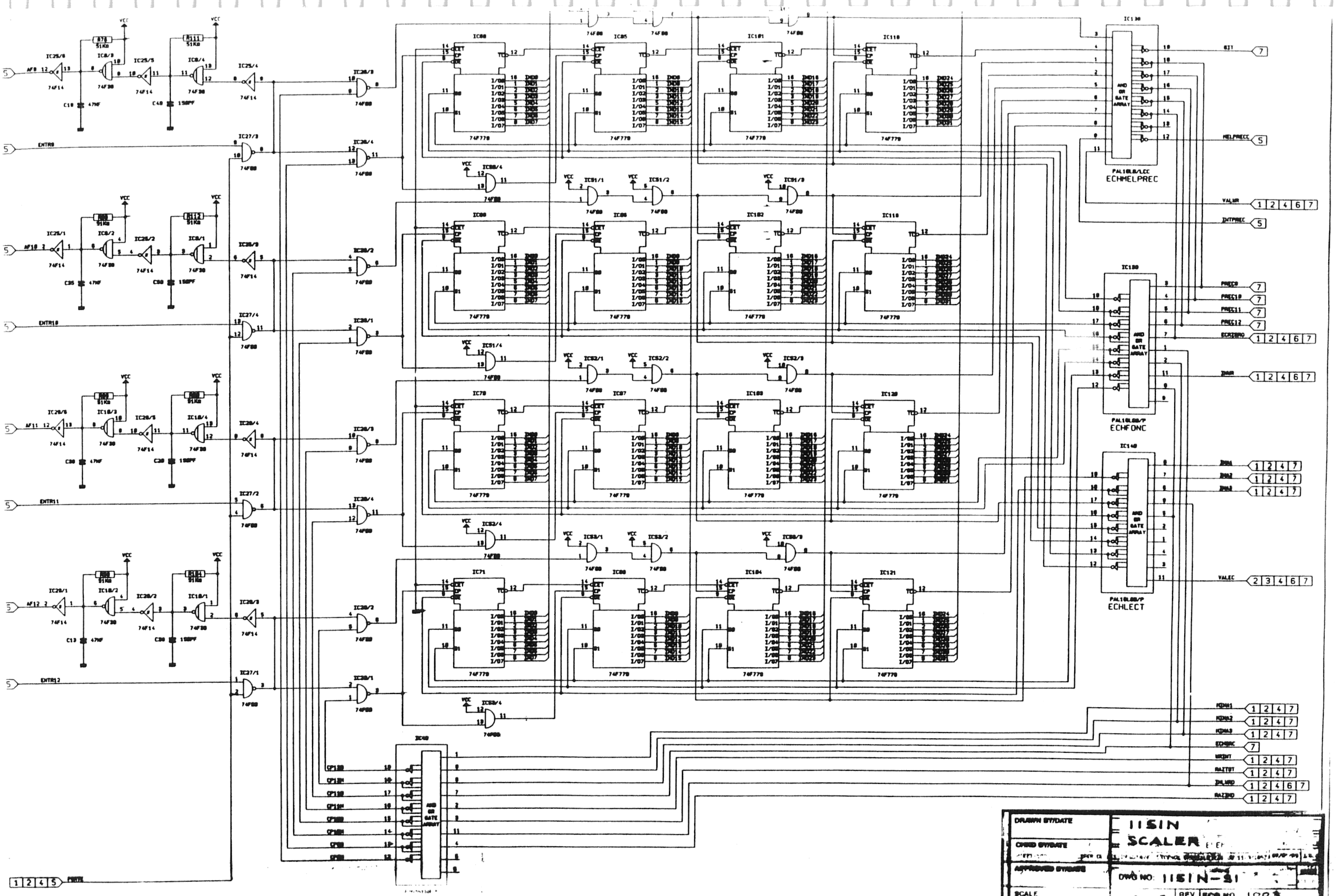
CHKD BY/DATE
APPROVED BY/DATE
SCALE
SIZE
115IN-SI



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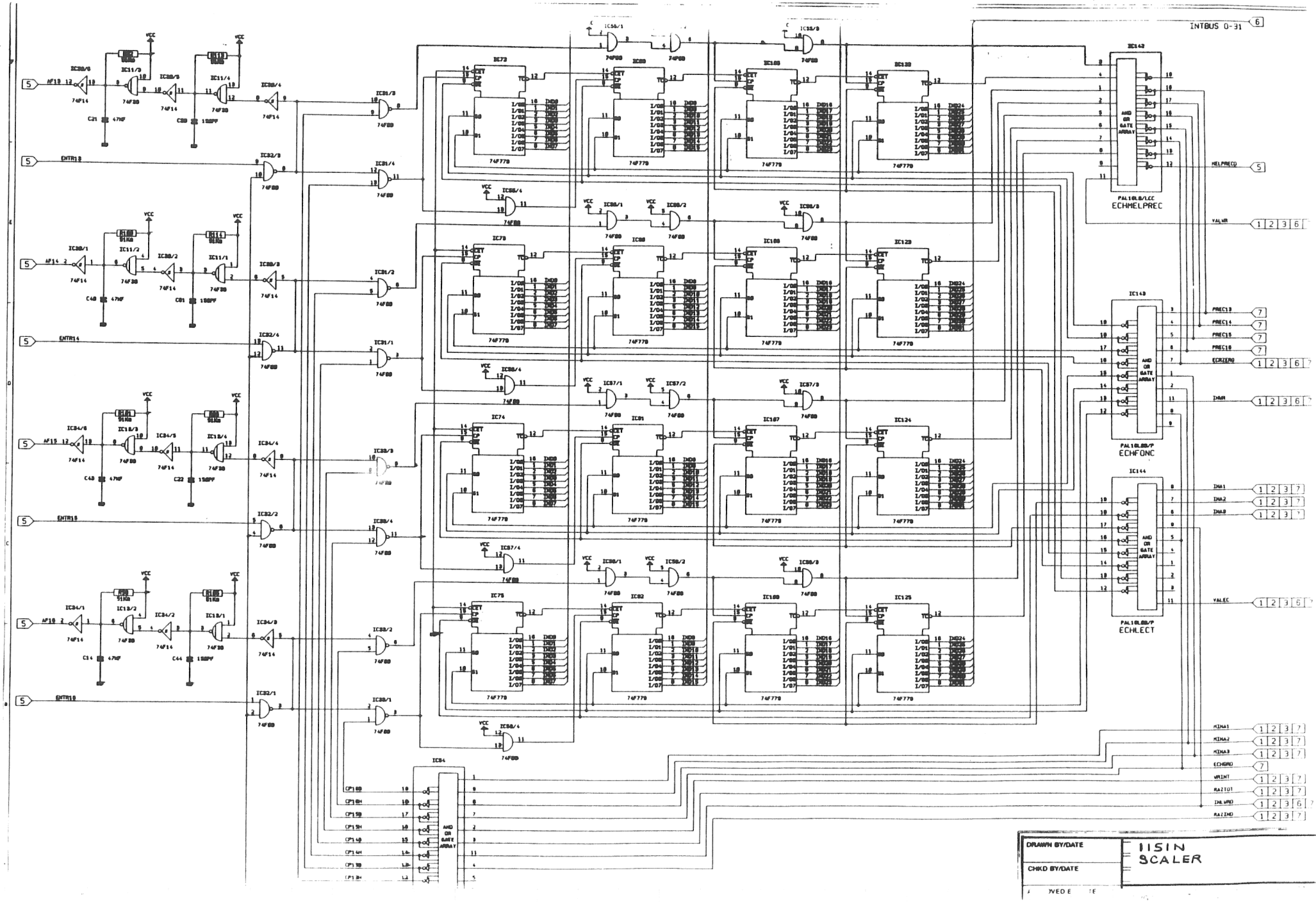
CHKD BY/DATE	
APPROVED BY/DATE	DWG NO: 11SIN-S1
SCALE	8	REV.	ECO NO. 1003	DATE 13-JAN-94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ECHFONC
ECHLECT
PAL16L8B/LCC
PAL16L8B/P
AND OR GATE ARRAY
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74F00
74F14
74F30
HELPRECO
VALWR
PREC13
PREC14
PREC15
PREC16
ECRIERO
INWR
INA1
INA2
INA3
VALEC
MINA1
MINA2
MINA3
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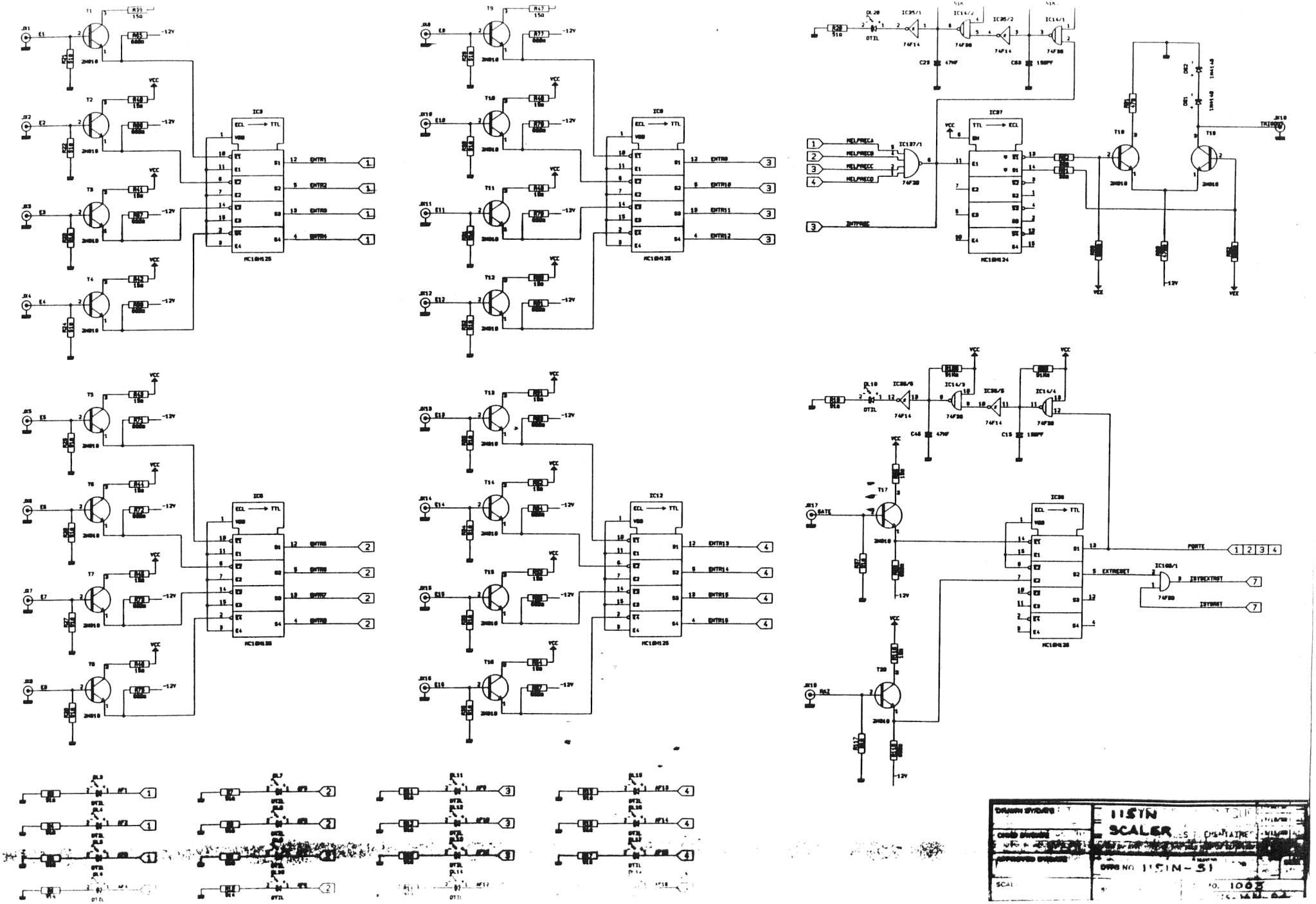
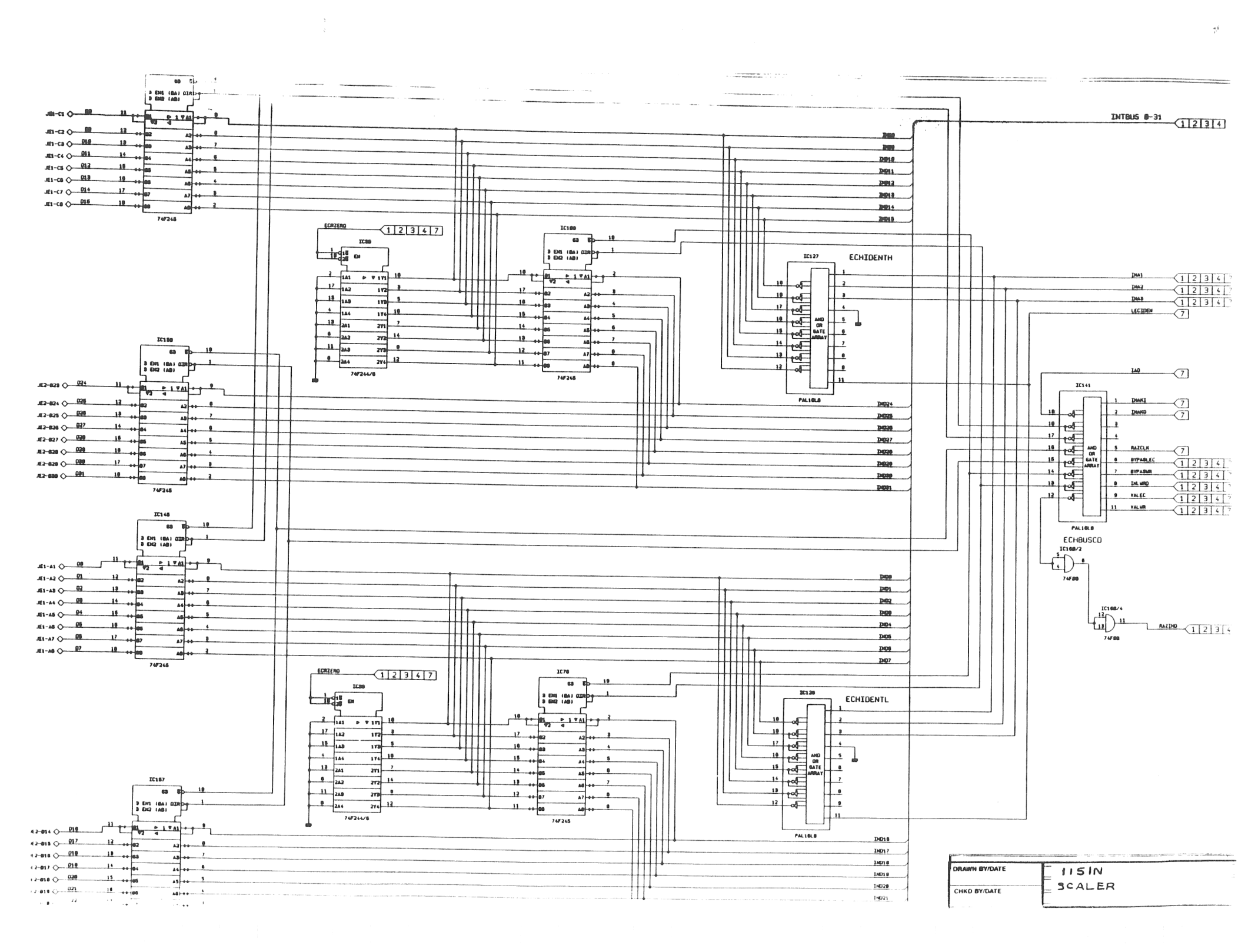
DRAWN BY/DATE
CHKD BY/DATE
11SIN
SCALER


115N
SCALER
115N-51


INTBUS B-31
ECHIDENTH
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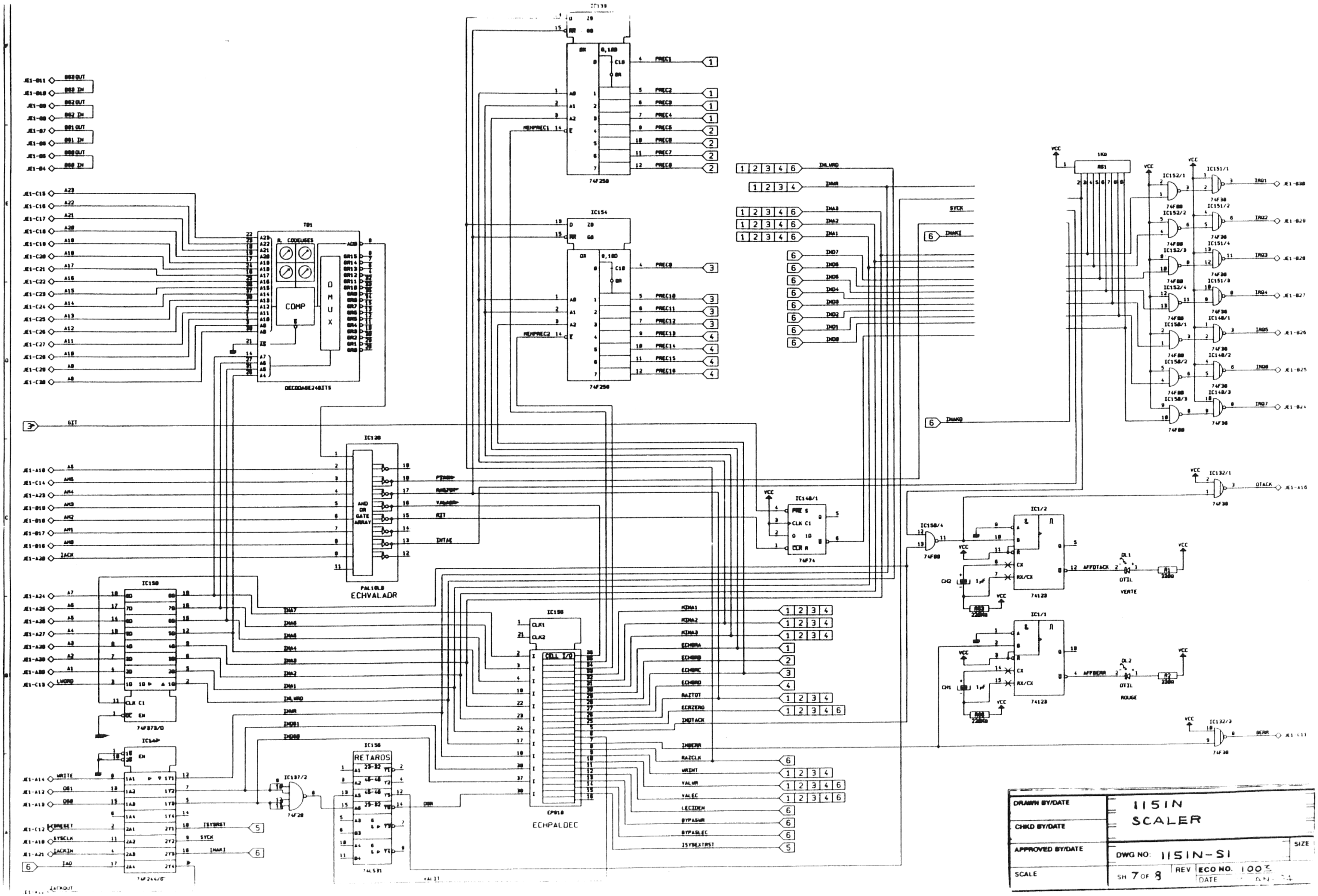
PAL16L8
AND OR GATE ARRAY
DRAWN BY/DATE
CHKD BY/DATE
115IN
SCALER



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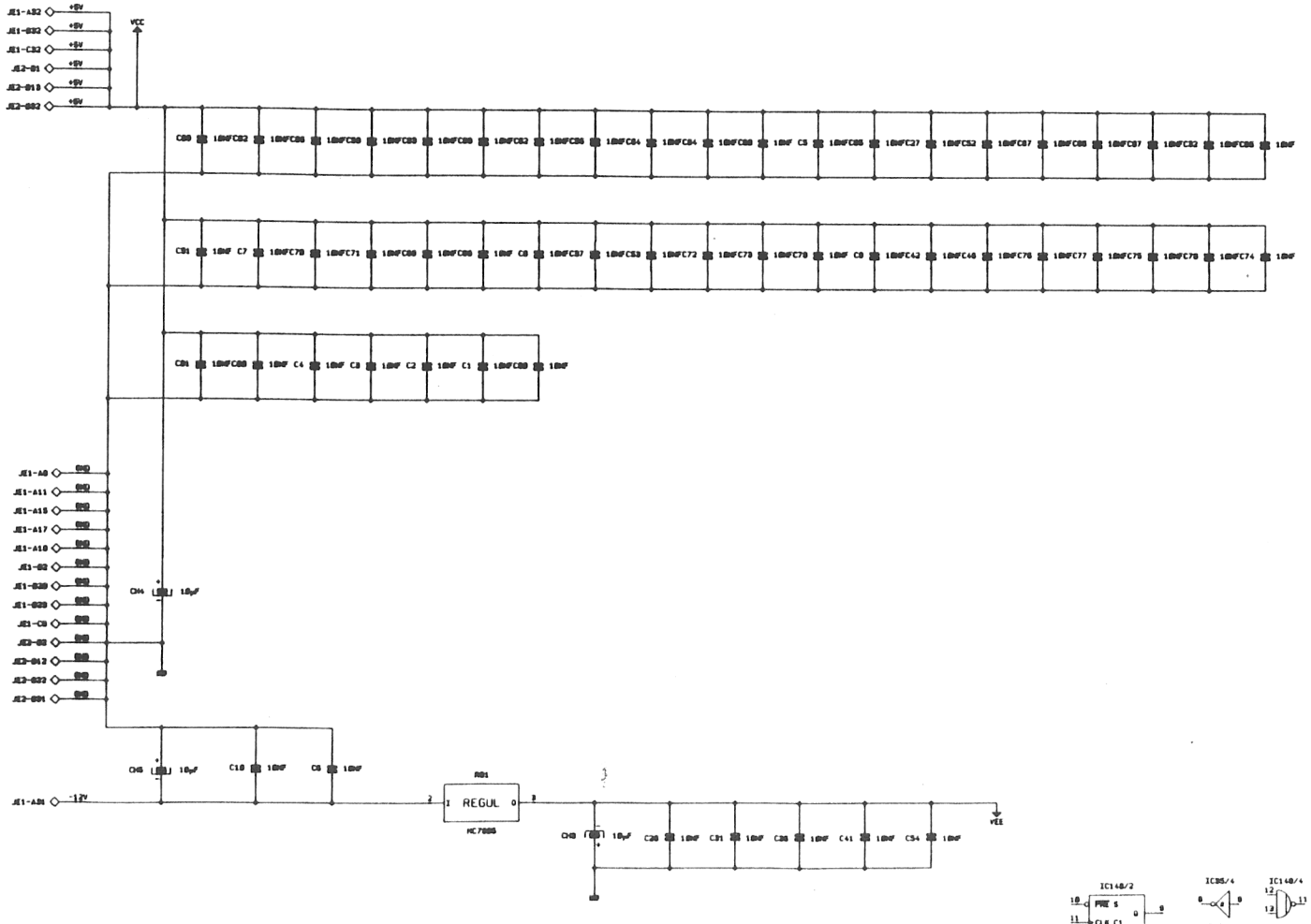
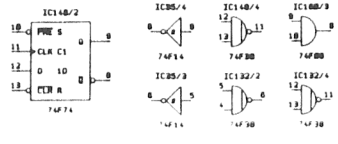
CHKD BY/DATE	
APPROVED BY/DATE	DWG NO: 115IN-S1
SCALE	SH 7 OF 8 · REV · ECO NO. 1003 · DATE





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CHKD BY/DATE	
APPROVED BY/DATE	DWG NO: 1151N-S1
SCALE	SH 8 OF 8 REV ECO NO. 1003 DATE 13-JAN-04