OPERATOR'S MANUAL

MODEL 1875A
(1872A)

FASTBUS TIME-TO-DIGITAL
CONVERTER

Revised
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(ECO 1202)

LeCroy

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TABLE OF CONTENTS

1. General Information

Purpose 1-1
Unpacking and Inspection 1-1
Warranty 1-1
Product Assistance 1-1
Maintenance Agreements 1-1
Documentation Discrepancies 1-2
Software Licensing Agreement 1-2
Service Procedure 1-2

2. Product Description

Overview 2-1
Features 2-1
Other Features 2-1

3. Installation

Equipment Needed 3-1
Resolution 3-1
Inputs 3-1
- Standard Input Scheme 3-1

Control Signal Inputs 3-2
- Com 3-2
- Measure Pause Interval (MPI) 3-3
- Clear 3-3

Trigger Outputs 3-3
Hits 3-3
Acquisition Timeout 3-3

4. Operating Instructions

N vs F Operating Modes 4-1
Chapter Organization 4-1
Initial Checkout 4-1
- Read the Module Identification and Mode 4-2
- Internal Test Pulsing and Readout 4-2
- Using the Test Pulser 4-3
- Checkout Using the Test Pulser and the LeCroy Model 1810 CAT 4-4

CSR0 Write 4-6
- Bit Type Definitions 4-6
- Control Bits 4-7
- Pulsed Bits 4-7

CSR0 Read 4-8
Output Data Word 4-9
N Mode Operation 4-10
- N Mode 4-10
- N Mode Readout Scheme 4-11

TABLE OF CONTENTS

F Mode Operation 4-15
The Internal Data Buffer 4-15
Conversion in Progress (CIP) and WAIT 4-16
Slave Status Responses 4-16
FASTBUS Broadcast Functions 4-17
CSR1 4-18
Writing to FASTBUS Register CSR1 4-19
Depth Field 4-19
F Mode Readout Schemes 4-20
F Mode - Readout with Next COM and CLEARs Blocked 4-20
F Mode - Readout with Next COM Allowed 4-24
F Mode - Readout During Next Conversion with CLEARs Blocked 4-28
F Mode - Readout During Next Conversion 4-32

5. Theory of Operation

MIQ401 - Input Monolithic 5-1
Time-to-Charge Conversion 5-2
Multiplexing and Conversion 5-2
Q_OUT Bus Interface 5-3
Integrators 5-3
Range Select 5-4
3X Amplifier and Level Shifter 5-4
Calibration 5-4

6. Additional Information

Auxiliary Connector 6-1
Fast Control Signals 6-1
User CSR Data Bus 6-1
AFC Voltages 6-1
AFC T-Pin Assert Broadcast 6-1
Trigger Outputs 6-1
Front Panel Dimensions 6-1

LeCroy

1875A 15-BIT, HIGH RESOLUTION TIME-TO-DIGITAL CONVERTER

- **High Density, 64 Channels Per FASTBUS Slot**
- **High Sensitivity, to 25 psec/Count**
- **Wide Dynamic Range, 12 or 15 Bits**
- **Short Conversion Time, 10 μsec + 2.5 μsec Per Hit Channel**
- **Fast Clear, ≤ 950 nsec**
- **On-Board Test Circuit**
- **Multiple Event Buffer, 8 Events**
- **Sparse Readout, 10 Megawords/sec**
- **Common Start Mode of Operation**

FOR TIME-OF-FLIGHT MEASUREMENTS AND MUON SPECTROSCOPY

The FASTBUS Model 1875A[1] features 64 channels of TDCs which operate in Common Start Mode. The 1875A offers a dynamic range of 15-bits in its 12-bit data by employing a bi-range transfer characteristic. This unit offers an extremely high sensitivity of up to 25 psec/count (200 psec on the associated high range) and is, therefore, ideal for measuring time intervals in nuclear, atomic, molecular and elementary particle physics time-of-flight experiments. For applications where less stringent requirements are needed, the resolution can be set by jumpers to 50 or 100 psec (400 psec and 800 psec, respectively on the associated high ranges). The unit is delivered configured for 50 psec resolution.

Model 1875A employs a time-to-charge converter principle followed by a common, multiplexed charge ADC. Only "hit" channels are converted. The conversion time is 10 μsec + 2.5 μsec per hit channel. The module contains a multiple event buffer which can store up to 8 events. This buffer can be read out at up to 10 megawords/sec, concurrently with the conversion of following events, thus reducing dead time and simultaneously increasing signal throughput rate.

The 1875A is compatible with the LeCroy 1800 Series data acquisition modules and the LIFT software package. A paddle card is offered to ease the routing and connection of the signal input cables.

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FUNCTIONAL DESCRIPTION

INPUT CIRCUIT

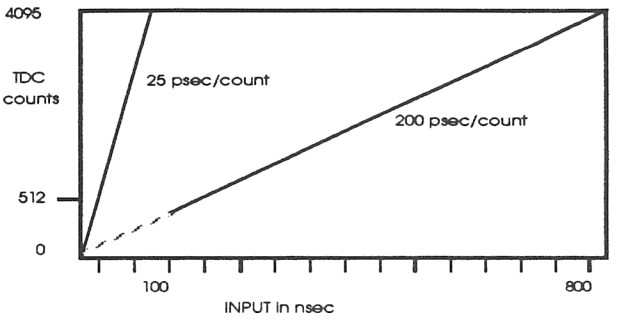
The 1875A input circuit uses time-to-charge converters to supply LeCroy Model MIQ401 4-Channel Charge Multiplexers with charge proportional to the time between Common Start and Stops. The MIQ401 is designed to do the integrate-and-store function as well as the output multiplexing to the common integrator & ADC.

In order to minimize turn-on effects of the charge storage circuitry, a minimum delay of 45 nsec between the Common Start and the first hit is required. The measurement window begins after this 45 nsec and ends one full scale later.

CONVERSION TECHNIQUE

In order to cover a wide dynamic range with a single 12-bit ADC, the 1875A uses a dual range technique (see graph). This scheme allows less than 1% quantization error from 2.5 nsec to 800 nsec for the most sensitive range setting and produces 15 bits of dynamic range.

When set to the highest of three possible sensitivity settings, inputs < 100 nsec digitize with a resolution of 25 psec per count and signals between 100 nsec and 800 nsec digitize with a resolution of 200 psec per count. The digitized output from each channel that was hit consists of a 12-bit amplitude word and a range bit (13th bit). The user can select "low range", "high range" or "auto range" under program control. These numbers scale with the two other jumper-selectable resolution settings.



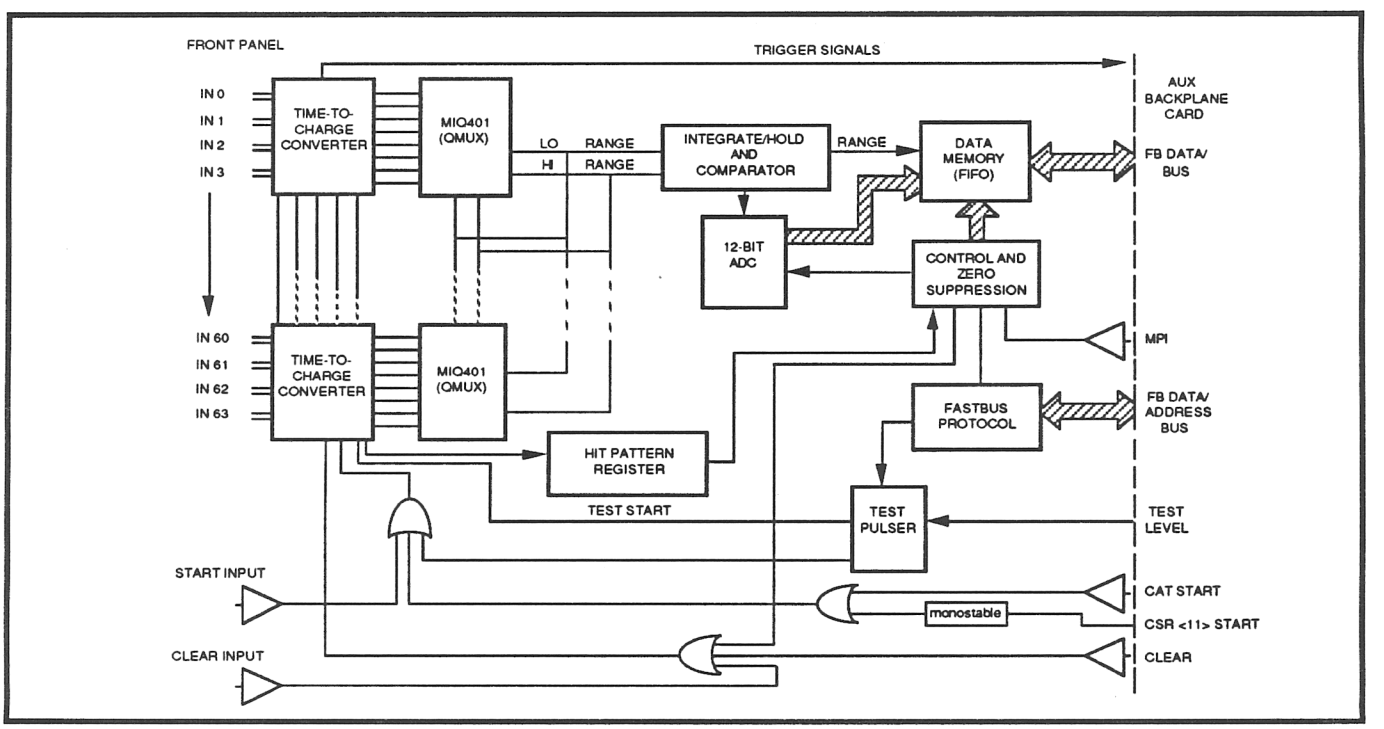
Dual Range Technique for Increased Dynamic Range

MULTIPLE EVENT BUFFERING

The module contains a multiple event buffer (digital memory) which can store up to eight events. Two pointers are used to allow the data acquisition program to follow the event flow.

CONTROL

The 1875A may be used with the optional Model 1810 CAT module which provides the calibration and trigger signals required by the TDC. Operation without a CAT is also possible using the software-selectable, front-panel Common Start and Fast Clear Inputs. Modules may be read out using any FASTBUS Master such as a LeCroy Model 1821 FASTBUS Segment Manager/ Interface (SM/I). In addition, the 1875A is compatible with the LIFT (LeCroy Interactive FASTBUS Toolkit) software package.



The Model 1875A Block Diagram

SELF TEST

The 1875A contains test circuits, allowing all TDC channels to be calibrated to approximately 3%. The calibration circuits are voltage-programmed pulse generators. A DC level (TEST REF) is bused from the LeCroy Model 1810 CAT module to all modules within the FASTBUS crate using the FASTBUS UR lines. When calibration is enabled via CSR 0, a write to CSR 0 <11> causes a Common Start-Stop pulse pair to deposit a well-defined charge (proportional to the TEST REF level) in each of the MIQ401 inputs.

[1] The 1875A is a successor to the 1875. The major differences are the sparsified readout and the conversion from Common Stop operation in the 1875 to Common Start operation in the 1875A.

SPECIFICATIONS

GENERAL

Type: Time-to-charge converter feeding into a Common, multiplexed charge ADC.
Channels: 64. The number of active channels is programmable between 1 and 64 in steps of 1 channel.
Hit Inputs: 64, differential ECL. Impedance 112 Ω. Unused inputs are allowed to float. Minimum width: 10 nsec.
Signal Input Connector: 4, 34-pin headers on front panel.
Common Start: Differential ECL input via a 2-pin front-panel connector or via TR5 (B51) line on the FASTBUS backplane, or via CSR 0 <11>. Must proceed hits by 45 nsec. May be driven by the LeCroy Model 1810 CAT Module. Width: 50 nsec to 2 µsec.
Conversion in Progress (CIP): Front-panel output to indicate an A-to-D conversion of signals is occurring. ECL signal on 2-pin header.
Fast Clear: Differential ECL input via a 2-pin front-panel connector or via backplane TR0 line (jumper enabled). Minimum width 20 nsec. Clears module and readies it for acceptance of a new event. Fast clear settling time is < 950 nsec to < 0.1% of reading or 1 count, whichever is greater.
Full Scale: Jumper selectable. Low Range: 100/200/400 nsec; High Range: 800 nsec/1.6 µsec/3.2 µsec. Full scale always corresponds to 4095 counts.
Sensitivity (Resolution): Jumper selectable. Low range: 25/50/100 psec/count ±3%; high range: 200/400/800 psec/count ±5%.
Pedestal: (calibrated at the minimum encodable stop time input for the slowest channel on the unit, i.e., the enable time) 300 ±200 counts. Pedestal correction may take place during data readout by LeCroy Model 1821 Segment Manager/Interface.
Enable Time: < 45 nsec when measured from front panel Common Start connector to the slowest of the 64 stop inputs. Channel-to-channel enable time variation: < ±3 counts.
Integral Non-Linearity: < ±3 counts low range, <±6 counts high range.
Differential Non-Linearity: No missing codes guaranteed; ±0.9 LSB, worst case from 10 - 100% full scale beyond pedestal.
R.M.S. Noise: 1.0 count typical, 2 counts maximum.
Interchannel Isolation: 1.0 count typical, 2.5 counts maximum.
Temperature Coefficient: Gain is ≤ 80 ppm/°C; Pedestal is ≤ 0.3 counts/°C.
Long Term Stability: ±(0.25% of reading +10 counts)/week.
ADC: 12 bits (4096 counts).
Conversion Time: 2.5 µsec for each channel that is stopped ("hit") + 10 µsec.
Multiple Event Buffer: The digital data memory is large enough to store the results of up to 8 events. A 3-bit event counter allows the user to keep track of how many events the readout is trailing the conversion.
Measure Pause Interval Input: Single-ended ECL signal via TR5 (B51) line on FASTBUS backplane. May be driven by the Model 1810 CAT Module. Trailing edge defines when conversion starts, if enabled by program. Can last up to 300 µsec after a Stop signal.
Calibration Test Feature: Allows the gain of any channel to be measured to approximately 3% when using the LeCroy Model 1810 CAT Module.
Packaging: Single-width FASTBUS module in conformance with FASTBUS Specification (ANSI/IEEE-960) 1986.
Power Requirements: 3.4 A at +5.0 V, 5.0 A at -5.2 V, 2.0 A at -2.0 V, 0.6 A at +15 V, 0.3 A at -15 V.

CONTROL FUNCTIONS IMPLEMENTED (CSR SPACE)

Module ID: $(1037)_h$.
Auto Range Select: Sets the readout conversion mode to Auto/Range.
Hi-Lo Range Select: Fixes the readout conversion mode to high or low range.

SPECIFICATIONS

Start Source: Selects between front panel or the FASTBUS TR5 line as the source of the Common Start. Writing CSR0 <11> to produce a Common Start is always enabled.
Test Enable: Enables test mode.
Trigger Personality Programming: Addressing supplied for sixteen 8-bit user-supplied registers.

FASTBUS CONTROL

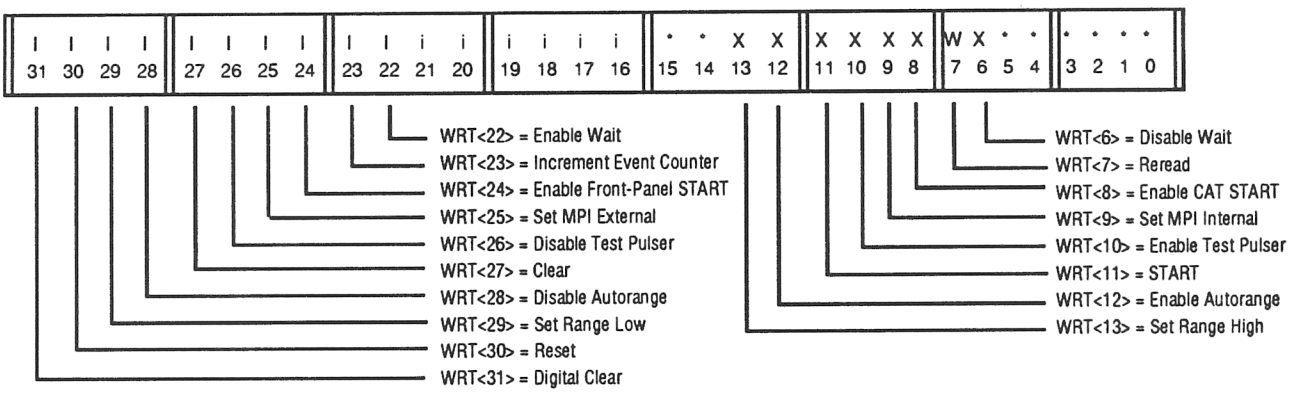
Implemented Addressing Modes: Geographical, Secondary, Broadcast.
Implemented Broadcast Functions:

Code	*Significance*	*Comments*
01_h	General Broadcast Select	Modules are selected and respond to subsequent data cycles.
09_h	Sparse Data Scan (SDS)	Modules containing data assert "T pin" on the following read data cycle.
09_h	Pattern Select	Modules seeing their T pin asserted on the following write data cycle become selected to respond to subsequent data cycle.
OD_h	All Device Scan	All modules assert their T pin on the following read data cycle.
DD_h	TDC SDS	Unique Sparse Data Scan for 1870 Series modules only. Follows standard SDS (see above).
ED_h	Personality Card	Sparse Data Scan: SDS Module asserts T pin if Personality Card requires service.

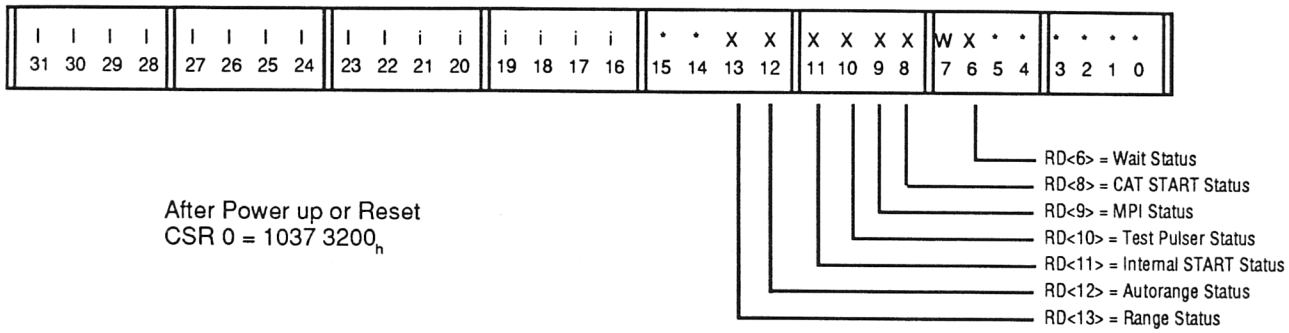
An h subscript indicates hexadecimal (base 16).

FASTBUS REGISTER CONFIGURATIONS

CSR 0 Write Bit Definitions

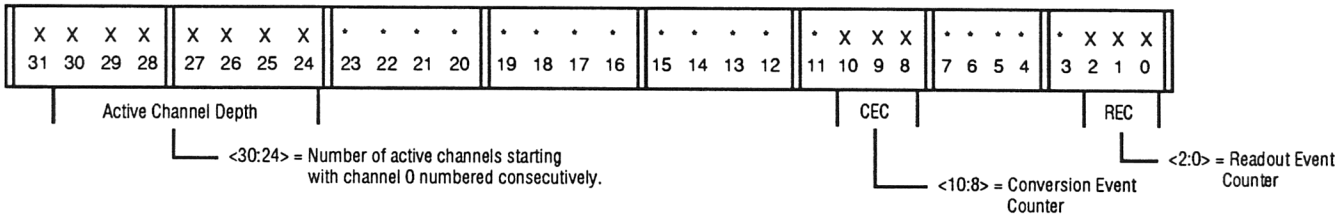


CSR 0 Read Bit Definitions

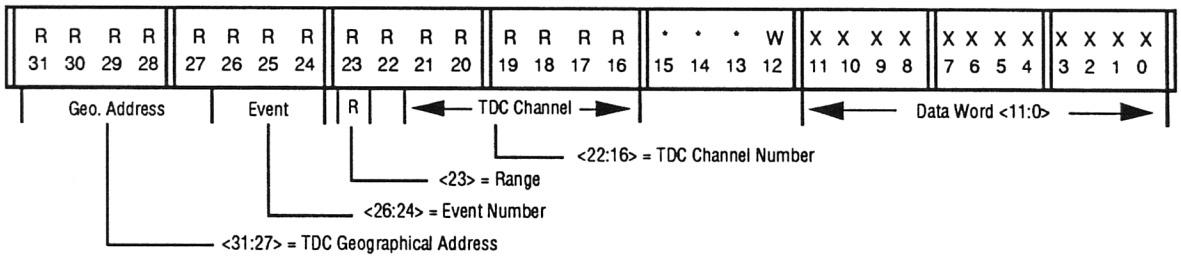


After Power up or Reset
CSR 0 = $1037\ 3200_h$

CSR 1 Bit Definitions



DSR 0 Output Data Word Bit Definitions



I – bits which give module ID upon read but are also implemented for write operations.
i – bits which give module ID upon read and are not used for write operations.
* – unused bits which read back zero.
R – bits implemented for read operations only.
W – bits implemented for write operations only.
X – bits implemented for read and write operations.

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CAUTION

COOLING

The high power dissipation of the 1872A/75A* requires that it be well cooled. It is suggested that a FASTBUS bin fan be used to maintain exhaust air temperature at less than 50° C.

POWER REQUIREMENT

The 1872A/75A uses significant power from the +5 V and -5.2 V power lines as well as -2 V and ±15 V power lines for most of its analog circuitry. Although power consumption to the ±15 V lines is relatively small; clean, ripple free, low noise supply voltages are needed to guarantee the performance of the 1872A/75A. Be sure that your crate can supply enough current to this and other modules, especially if multiple 1872A/75As are used.

Also, achieving optimum performance from the 1872A/75A requires the power supply to meet FASTBUS specifications, particularly regarding noise.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

* "1872A/75A" is used throughout this manual as an abbreviation referring to both the 1872A and the 1875A.

1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the Model 1872A/75A. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030, or your local field service office.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department or the local field service office for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc. and occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility.

For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping.

All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in New York.

Research Systems Division Customer Service (914) 578-6030

2 PRODUCT DESCRIPTION

OVERVIEW

The LeCroy Model 1872A and 1875A are fast converting, Common Start, sparsifying, 64-channel, time-to-digital converter modules designed for forefront elementary particle or nuclear physics experiments.

Each of the 64 inputs stop the measurement of a time which is started by the com input common to all channels. All inputs are DC-coupled, ECL. The 64 time signals are digitized and the results stored in the module's memory.

The module's physical dimensions, power requirements, control and readout protocol are in compliance with the FASTBUS ECL standard as outlined in the document, IEEE-960-1986. Up to 23 modules may be installed in an appropriately powered crate providing a total of 23x64 = 1472 TDC channels (in a standard 25 slot crate allowing two slots for a master). Larger systems can be built (within the FASTBUS specification) by connecting crate segments via Segment Interconnects (SI) or a LeCroy Model 1821 Segment Manager/Interface (SM/I) module.

FEATURES

The 1872A/75A employs a sparsification scheme to reduce conversion and readout time. Only channels which were hit are digitized and stored. Conversion time varies with the number of hits and is 10 μsec + 2.5 μsec per hit. A typical, 8 hit event will be converted in less than 30 μsec and a full 10 MHz data readout rate is supported in FASTBUS block transfer mode. Thus, a full crate with 184 hit channels (typical case) can be read out in less than 20 μsec (not including FASTBUS Master readout time).

The 1872A/75A digitizes time intervals with three jumper selectable resolutions: 25 psec/count, 50 psec/count, or 100 psec/count. Jumpers marked RESOLUTION, TESTER RESOLUTION AND RESOLUTION P4, P1 and P20 respectively, must be changed as indicated on the module, when changing resolutions. These settings result in full scale ranges of 100 nsec, 200 nsec, or 400 nsec for the 1872A. The 1875A has eight times greater full range as discussed below. See Chapter 5 for calibration details.

The 1872A/75A also contains an internal buffer for multiple events which may be used to eliminate data readout time as a contributor to experimental dead time. Data for the previous event can be read out while the current event is still being converted. Use of this internal buffering is exactly the same as in the LeCroy Model 1882/85F ADC modules and is referred to as F Mode Operation. Operation without internal buffering is referred to as N mode.

OTHER FEATURES

The 1872A digitizes time events into 12 bits. The 1875A provides a 15-bit dynamic range via 12-bit data word and a range bit (X8 or X1). The 1875A may be configured to automatically select the appropriate range for each channel on an event-by-event basis.

The module automatically clears the front end at the end of conversion although digitizing may be interrupted at any time and the modules reset for a new START by applying a CLEAR signal.

An on-board pulser permits time calibration of the TDC channels.

Sixty-four trigger outputs permit easy trigger logic interface.

3 INSTALLATION

EQUIPMENT NEEDED

One FASTBUS crate with the following voltage sources connected properly to backplane: +5.0 V (3.4 A), -5.2 V (5.0 A), -2.0 V (2.0 A), +15.0 V (0.6 A), -15.0 V (0.3 A). The crate should be an ECL backplane implementation.

FASTBUS Ancillary Logic such as the Struck Geographical Address Control Card (GAC) Model STR162 and the Arbitration Timing Control Card (ATC) Model STR163. The GAC card should be placed in the rear crate backplane in slot #23 (or 24 or 25) and the ATC card in slot #2 (or 3 or 4). If the crate also has two rear back-planes these cards should be plugged into the lower of the two backplanes. Also, inspect jumper settings on these cards and compare with manufacturer's recommendations.

A Crate Master, such as LeCroy Model 1821 Segment Manager Interface (SM/I), to execute standard FASTBUS cycles for control of module and transfer of data to the user's computer.

A Processor Interface (PI) such as a LeCroy Model 1821/DEC interface card with a DEC DR11-W Unibus of MDB DRV11-2 Qbus parallel I/O board used with the DEC computer line. A less expensive way of getting started with FASTBUS (for example, to check out a small number of crates of FASTBUS modules) is to use an IBM PC/AT™ with a LeCroy Model 1691A Interface Card which connects to the front panel of a LeCroy Model 1821 SM/I via a LeCroy DC4/34 data cable.

The software package LIFT (LeCroy Interactive FASTBUS software Toolkit) is available for the 1691A/IBM PC system providing the user with a substantial package of software to exercise and test FASTBUS modules with a LeCroy SM/I 1821. LIFT also includes an extensive software library which the user may employ in the development of his own data acquisition software.

RESOLUTION

Remove the side cover of the module and select the desired resolution with jumpers marked RESOLUTION, TESTER RESOLUTION and RESOLUTION (P4, P1 and P20 respectively) as indicated on the board. Although the time interval measurements have three coarse settings of full scale, each with an automatic low and high range change, the on-board test pulser relies entirely upon manual jumper adjustments. REMEMBER - ensure that all jumpers are set for the same resolution (see Section 4, "Using the Test Pulser"). Replace the side cover.

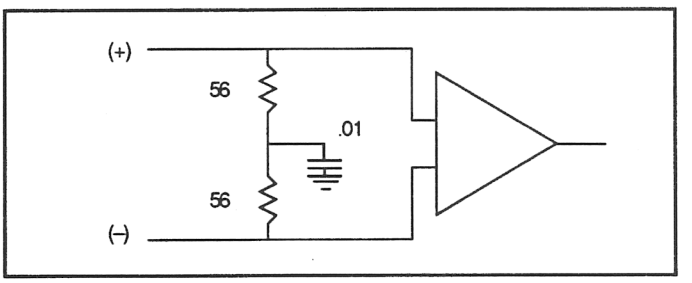
FULL SCALE

The acquisition timeout can be manually set to allow for 12-bit operation only. The P21 jumper normally is set to the 15-bit position. This allows for software selection of 12- or 15-bit range via CSR0. If only 12-bit (low range) operation is desired, the P21 jumper can be set to the 12-bit position. This will reduce the acquisition timeout by a factor of 8, but auto range and high range operation will be adversely affected. When P21 is set to 12-bit, the unit must be operated in Low Range only.

INPUTS

Standard Input Scheme

The use of coax cables as signal cables generally results in less pick-up of noise and EMI signals (especially when long cables are employed) and less crosstalk due to the concentric shielding of the center conductor.



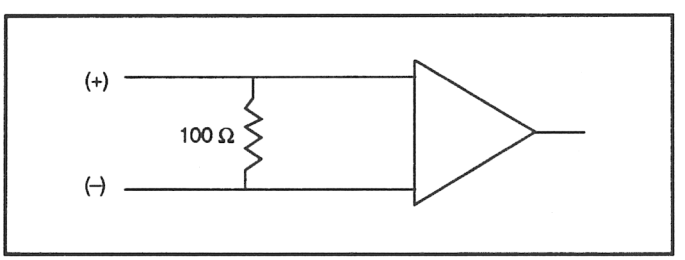
The use of twisted-pair cables generally results in lower cabling costs. Care should be taken by the user to install high quality, shielded cables with randomly twisted-pairs to minimize the effects of noise pickup and crosstalk.

All hit inputs are differential ECL and terminated by 112 Ω as shown. The terminations are SIP components and may be easily replaced to accommodate other transmission line, characteristic impedances.

CONTROL SIGNAL INPUTS

The following sections discuss module control signals sent to the module front panel or the FASTBUS backplane TR lines and include COM (Common), MPI (Measure Pulse Interval), and CLEAR. The COM and CLEAR signals can be triggered via writing appropriate bits in CSR0 (Control and Status Register 0), using standard FASTBUS protocol. The CSR0 bit definitions, use of the on-board pulser calibration, and the module signals used for FASTBUS data readout are discussed in later sections. COM and CLEAR may also be applied via front panel differential ECL input or via TR lines from a LeCroy Model 1810 CAT (calibration and timing) module, for example.

The differential ECL inputs are asserted when the pin labeled "+" is ECL high and the pin labeled "-" is ECL low. The COM and CLEAR front panel inputs are terminated into 100 Ω resistors, as shown.



COM

The beginning of the time interval which is digitized is defined by the COM signal and is common to all 64 channels. The COM signal is routed to all channels. The variation in COM edge receipt between the 64 channels is no more than 5 nsec.

Digital conversion will begin after the trailing edge of the MPI signal (see below).

A user COM can be applied to the module either through a differential ECL input, 2-pin front-panel connector or via the TR5 line on the FASTBUS backplane. The LeCroy Model 1810 CAT module may be used to apply both COM and CLEAR signals to the crate backplane. However, CAT COM must be enabled via CSR0, and this will disable the front panel STOP. The 1810 CAT module "ICA STOP" front panel input controls the leading edge of the FASTBUS TR5 line which the 1872A/75A can use as its Common Start.

In addition, the module may be started under program control by writing a "1" to CSR0<11>.

MEASURE PAUSE INTERVAL (MPI)

After a full scale timeout period measured from the COM arrival, the module disables acquisition and waits for an adjustable time period (referred to as the Measure Pause Interval, MPI) from the leading edge before it initiates a digitization or conversion cycle. Within limits, the MPI may be adjusted to provide additional time for experimental trigger logic to issue a CLEAR prior to conversion. Via appropriate bits in CSR0, the MPI may be determined by a labeled on-board potentiometer, MPI, or an external ECL signal applied to the FASTBUS line TR5. In the latter case, the end of the MPI is determined by the trailing edge of the applied ECL signal. This signal can be conveniently generated by the LeCroy Model 1810 CAT module. Use of the external MPI is strongly recommended for crates of multiple TDC modules to avoid possible module-to-module variations in the on-board potentiometer settings.

A time of 1 μsec is the minimum recommended MPI. Settings less than 1 μsec are possible with this module but channel zero may not attain the TDC resolution specification. Diminished resolution due to a short MPI setting should be expected to vary between modules. A time of 500 μsec is the maximum recommended MPI. Larger MPIs are permitted but performance becomes limited by the storage time of internal capacitors in the Qmux which should start to show significant droop after a millisecond. The on-board MPI potentiometer is typically set at the factory to 10 μsec.

CLEAR

A CLEAR signal may be sent to the module at any time and the module will be ready to receive another COM 950 nsec later. The CLEAR terminates all operations unconditionally and returns the module to the quiescent state. The FASTBUS registers are unaffected by a clear. A CLEAR signal may be applied to the module either through the 2-pin front-panel differential ECL input, or via a single ended ECL signal on the TR0 line on the FASTBUS backplane. A jumper must be in place, however, to permit CLEAR via the TR0 line. A module CLEAR can also be generated under program control by writing a "1" to the appropriate bit of CSR0.

TRIGGER OUTPUTS

During MPI, the hit data is available on the FASTBUS Aux connector of the trigger logic interface. Each of the 64 trigger ECL lines representing Channels 0 to 63 will go low if the corresponding channel was hit. This data is valid only during MPI.

HITS

In order to provide better performance of the TDC, a 45 nsec delay is required between the arrival of the COM and the earliest hit. Hits which arrive in less than 45 nsec after the COM will not be registered. Delaying the hits by a 45 nsec cable delay with respect to the COM will satisfy this requirement.

ACQUISITION TIMEOUT

The arrival of the COM starts acquisition of hits. When the acquisition timeout interval is over, acquisition is terminated and the MPI begins. The acquisition timeout delay is a function of both the resolution setting and the maximum number of bits to be digitized. The P20 jumper sets the LSB weighting; 25, 50 or 100 psec per LSB are selectable. Note that there is a corresponding jumper, P4, as well as P1 for the tester that should be set to the same setting.

Normally, the acquisition timeout is equal to approximately 1.2 times the resolution setting times 32,768. This is ideal for 15-bit operation. In the event that only 12-bit operation is desired, the P21 jumper can reduce the acquisition timeout by a factor of 8 by selecting the 12-bit position. Note that there is a corresponding jumper, P57, for the tester that should be set to the same setting.

CIP

The Conversion in Progress Signal (CIP) is available on the front panel of the 1875A. A pair of jumper holes labeled "CIP" and "TR7" near the FASTBUS connector allows bringing the CIP signal to the FASTBUS TR7 line. This signal could be used in a wire or'ed configuration to interface with trigger logic, for example. It is up to the user to ensure that there are no conflicts in the FASTBUS crate over the use of TR7. Note that the LeCroy 1810 CAT modules use TR7 to distribute a clock reference and would be incompatible with the use of CIP on TR7.

4 OPERATING INSTRUCTIONS

N VS. F OPERATING MODES

The 1872A/75A TDCs contain an internal buffer which can hold up to 8 events (each containing up to 64 words of data) in the module. Appropriately managed, this buffer can be used to virtually eliminate the contribution of data readout time to experimental dead time. However, for compatibility with other unbuffered FASTBUS slaves use of the N mode is recommended. Operating with the buffer disabled will be referred to as the N mode operation.

An 1872A/75A is placed in N mode via a hardware switch located on the bottom edge of the board and labeled "S1". The switch positions for N and F mode are labeled on the board.

CHAPTER ORGANIZATION

The rest of this chapter discusses the recommended initial checkout procedures which should be made with the 1872A/75A module in N mode unless otherwise specified. This is followed by a description of Control and Status Register, CSR0, and the output data word bit definitions. The N mode readout scheme is the simplest to implement and therefore is discussed next. Those features of the 1872A/75A which are peculiar to the F mode are then described including operation of the internal buffer, the SS (Slave Status) codes, and the CIP (Conversion in Progress) signal and WAIT assertion capability. Following this background information, some of the possible F mode readout schemes are then discussed. This chapter concludes with a number of sections on other useful features of the 1872A/75A.

INITIAL CHECKOUT

In this section, detailed recipes are given which should help the user begin to use the 1872A/75A in a FASTBUS system. These include reading the module identification (ID) and mode, internally starting and reading the module (no signal inputs), a discussion of the on-board test pulser mode and a checkout procedure with the LeCroy Model 1810 CAT module. Details on the various bit assignments of CSR0 and the output data word are covered in a later section.

Use of these recipes assumes a working knowledge of the FASTBUS standard. For those users not intimately familiar with FASTBUS, the LIFT software package provides keystroke macros to execute all primitive FASTBUS operations (see Section 3, *Installation*).

Read the Module ID and Mode

1. Assure the 1872A/75A is in N mode.
2. Install the TDC module according to instructions in the *Installation* section (Section 3).
3. Front-panel signal connections are not required.
4. Power up crate.
5. Address the module in CSR space (CSR0 now addressed).
6. Assure the module is completely Reset. Internally CLEAR module - write 0800 0000 (hex), wait 950 nsec, then Reset module - write 4000 0000 (hex).
7. Read the module (fetching the value of CSR0).
8. The 32-bit value read should be 1036 0200 (hex) if the module is an 1872A and 1037 3200 (hex) if the module is an 1875A.
9. To determine if indeed the module is in N mode by internally STARTing the module (once) - write 0000 0800 (hex).
10. Prepare to read CSR1 by doing a secondary address write with a value 1.
11. Read the module (CSR1). If the module is in N mode, the value read should be 4000 000 (hex). In F mode, the value would be 4000 0100 (hex). (The extra bit set in F mode corresponds to the value of the conversion event counter. See F mode operation page 4-15.)

If the above instructions are not understandable, then you should obtain additional information on the operation of FASTBUS systems. Failure to read out the indicated values upon power-up indicates a serious module or FASTBUS system problem. Since all FASTBUS operations discussed in the following sections are based on proper operation of FASTBUS and, in particular, the proper manipulation of CSR0 information, you should not proceed until the above procedure is completed successfully.

Internal Test Pulsing and Readout (no signal inputs)

1. Assure the 1872A/75A is in N mode.
2. Remove side cover; remove P55 jumper to disable sparsification.
3. Install the TDC module according to instructions in the *Installation* section (Section 3).
4. Front-Panel start signals should not be connected.
5. Power up crate.
6. Address module in CSR space. (CSR0 now addressed.)
7. Assure the module is completely Reset. Internally CLEAR module - write 0800 0000 (hex), wait 950 nsec, then Reset the module - write 4000 0000 (hex).
8. Cause a COM to occur by writing to the module (CSR0) 0000 0800 (hex). This causes a Start to be internally generated and the current front-panel inputs digitized. With the front-panel signals disconnected, this should provide a measure of the individual channel pedestals.
9. Assure that the Master waits 180 µsec (170 µsec plus the set MPI; see Section 3) for digitization to complete. The factory setting for the MPI is 10 µsec.
10. Address the module in data space.

11. Read the module 64 times fetching the output of digitization process. For example, for a 1872A/75A module located in slot (Geographical address) 17, the first five 32-bit data words in hexadecimal format should be of the form:

    8800 0000
    8801 0000
    8802 0000
    8803 0000
    8804 0000

    Bits <22:16> contain the TDC channel number. Bit <23> contains the digitization range. Bits <26:24> contain the event number (always zero in N mode). Bits <31:27> contain the geographic address of the module, which in this case for a value of 17 (decimal) results in value of 88 (hex) in the top byte of the output data word (bits 31 and 27 set). (See Output Data Word page 4-9.)

12. After 64 reads, the user can verify that a 65th read operation generates a Slave Status code, SS = 2 response, which indicates all valid data channels have been read out.

13. Remove module from the crate, replace P55 jumper to enable sparsification and replace side cover.

Using the Test Pulser

The 1872A/75A TDC modules have a voltage programmable test pulser. The test pulser is to be used to generate a common start pulse and a stop for each channel. The intended purpose of this pulser is to provide a quick self-check of the TDC channels and to enable a ±3% channel-to-channel and module-to-module calibration.

The test pulser is enabled for operation by setting CSR0<10>.

When the test pulser is enabled, a COM pulse from either the front panel, TR5, or CSR0<11> will generate an internal START and STOP for every channel according to a programming voltage. A jumper connector, P1, provides three programming sensitivities for the test pulser: 80, 160, or 320 nsec/V. A second jumper, P57, determines the test pulser's range: open = low, and shorted = high range. The tester setting is summarized in the following tables:

Sensitivity Adjustments

	Jumper P1 Settings		
TDC Resolution	25 ps	50 ps	100 ps
Low Range	10 ns/V	20 ns/V	40 ns/V
High Range	80 ns/V	160 ns/V	320 ns/V

Range Adjustments

Tester Range	**Jumper P57 Settings**
Low	Open (jumper removed)
High	Shorted (jumper applied)

Jumpers P57 and P1 are located at the top left corner of the TDC board.

The programming voltage should be applied to the module on the two unterminated restricted lines on the FASTBUS backplane UR0, and UR1. The test voltage inputs are high impedance, fully differential with large common mode rejection for at least a 2 V maximum common mode signal.

POSITIVE INPUT - UR1, PIN B56 usually positive.

NEGATIVE INPUT - UR0 PIN B55 usually ground reference.

Maximum voltage input is 10 V.

For bench testing this module, a 2-pin input header P2, is available under the side panel to which the user may apply the test voltage. The header is near the rear top of the module and the pin towards the back is the more positive.

Checkout Using the Test Pulser and the LeCroy Model 1810 CAT (Calibration & Timing Module)

In this section a detailed prescription is presented for using the LeCroy Model 1810 CAT to apply a test voltage to the backplane UR lines, and with the test pulser enabled apply an internal strobe to the TDC for test purposes. This procedure uses a number of the features of the TDC and CAT which make it a good tutorial on the operation of both. The 1810 has a 12-bit DAC and amplifier to allow the user to digitally program the voltage from any FASTBUS Master. With a 12-bit DAC, one should not expect the CAT to serve as a good calibration device for the 15-bit dynamic range of an 1875A TDC. Further, since the Test Pulser is intended only for testing, the Common START and STOPs which are generated have greater jitter than the measurement capabilities of the 1872A/75A.

1. Assure the jumpers are in the desired position.
2. Install the TDC module according to instructions in Section 3, *Installation.*
3. Install 1810 CAT module in a FASTBUS crate.
4. Front panel HIT signals should not be connected.
5. Power up crate.
6. Confirm that the CAT is addressable. Address the CAT module in CSR space. Read the module (CSR0 - ID) - should be 1039 0000 (hex).
7. Address the TDC module in CSR space.
8. Assure the TDC module is completely Reset. Internally Clear the module - write 0800 0000 (hex), wait 950 nsec, then Reset the module - write 4000 0000 (hex).

9. Enable the TDC module test pulser - write 0000 0400 (hex).
10. Address the CAT module in data space.
11. Set the CAT module data space NTA (Next Transfer Address) to 3, using a secondary address write: DS(u), MS=2, AD=3.
12. Write the desired Voltage to place on UR lines. 12-bits (4095) is 10 V full scale. When the TDC test pulser is enabled, 1 V will generate a common START and STOP separated as programmed on UR1 and UR0. To set the CAT to 1.0 V, write 0000 019A (hex) which is 410 (dec).
13. Address the 1872A/75A in CSR space.
14. Cause an Internal Test cycle to occur by writing to the module (CSR0) 0000 0800 (hex). This causes the internal common START and STOP test pulses.
15. Assure that the Master waits at least 180 µsec (10 µsec of MPI + 170 µsec of TDC conversion time).
16. Address the module in data space.
17. Read the module 64 times fetching the output digitization process. For example, for an 1872A/75A module located in slot (geographical address) 17, the first five 32-bit data words in hexadecimal format should be of the form:

    8800 0XXX
    8801 0XXX
    8802 0XXX
    8803 0XXX
    8804 0XXX

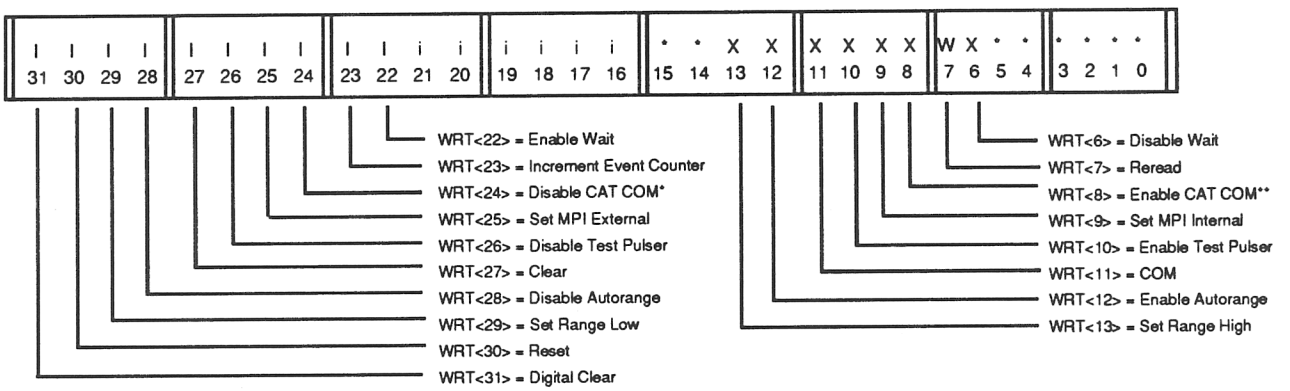
    This format is discussed later in the Output Data Word section, page 4-9. Here XXX is the TDC value which includes the time interval from the test pulser added to the channel pedestal.
18. After 64 reads, the user can verify that a 65th read operation generates a Slave Status, SS = 2 response, which indicates all valid data channels have been read out.
19. Repeat for different CAT voltages as desired beginning with step 10.

Note: The test pulser is the same in both the 1872A and the 1875A. The 1875A test circuitry has no knowledge of whether auto range is enabled or disabled. The tester does not automatically compensate according to the resolution selected for the board. The user must take care to ensure that the programmed voltage from the CAT (on UR1 & UR0), the jumpers controlling the on-board tester, and the board's resolution are all properly selected.

CSR0 WRITE

Bit Type Definitions

- **I** - bits which give module ID upon read, but are also implemented for write operations.
- **i** - bits which give module ID upon read and are not used for write operations.
- ***** - unused bits which read back zero.
- **R** - bits implemented for read operations only.
- **W** - bits implemented for write operations only.
- **X** - bits implemented for read and write operations.
- **T** - factory reserved; not for read or write operations; ignore value.



* (and Enable front panel COM)

** (and Disable front panel COM)

Control Bits

The 2-state control bits are set and reset by writing to different bits in CSR0. This strategy is described in the FASTBUS specification. Briefly, the state of the bit is set by writing a "1" to a specified bit in CSR0 and is reset by writing a "1" to a different bit CSR0. This is to allow the user to set or reset a control bit without having to remember the state of the other bits in the register. If a "0" is written to both bits associated with the control bit then no change will occur, if a "1" is written to both bits the results are undefined.

Wait (enable/disable): Allows/disallows the assertion of the WAIT signal. If enabled an 1872A/75A will assert WAIT when addressed in data space and the unit is NOT converting data. (See Conversion in Progress (CIP) and WAIT, page 4-16.)

MPI (set external/internal): Selects internal or backplane as source for Measure Pause Interval (See Section 3).

Test Pulser (enable/disable): Enables/disables internal test pulser for use with Internal COM as a calibration mode (See Using the Test Pulser, page 4-3.)

Autorange (enable/disable): Enables/disables autoranging, applies only to 1875As. Overrides the range selected via Range.

Range (high/low): Selects range only if autoranging is disabled (applies only to 1875As).

CAT COM (enable/disable): Enables/disables COM by LeCroy 1810 CAT module.

Pulsed Bits

Pulsed bits initiate an action in the unit whenever a "1" is written to the appropriate bit. All but the internal COM are "write only"; the action occurs entirely within the write cycle. The internal COM is long enough that a fast Master may be able to discern its duration. It has a position in CSR0 that will read a "1" for its duration.

Reread: Resets FIFO (FASTBUS side) to Channel 0. Does not affect event counters or TDC circuit.

Internal COM: Causes unit to generate its own COM.

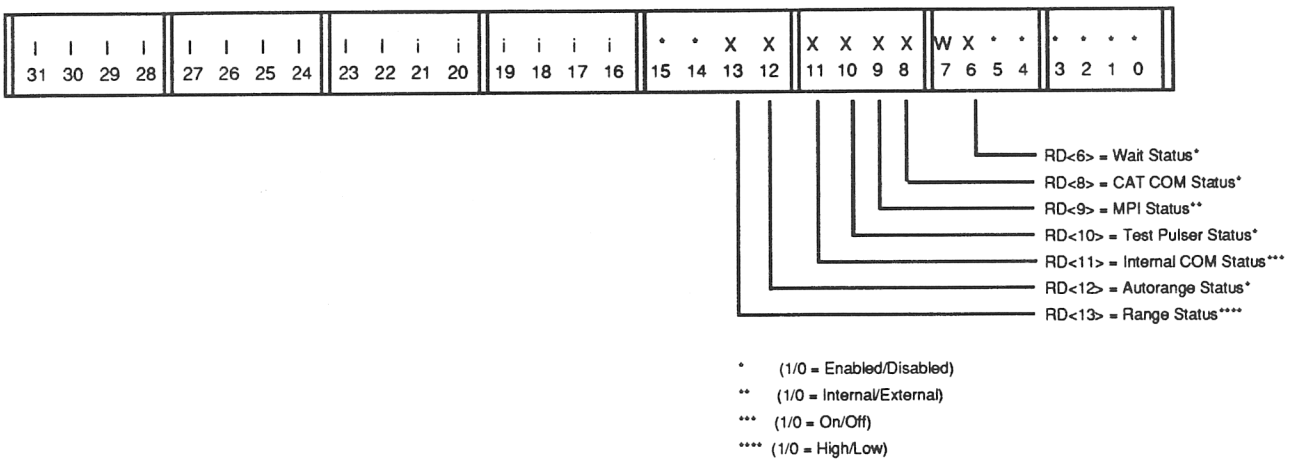
Increment Event Counter: Advance the Readout Event Counter to next event and reset the Data memory pointer (FIFO) to the beginning of that event (F-Mode only).

Clear: This bit has the same function as a hardware front-panel clear which clears the analog front end of the module.

Reset: Resets the 1872A/75A to a state identical with the power-up condition. Specifically, it resets CSR0 back to its default power-up condition, sets the number of active channels to 64, resets data memory (FIFO) pointer to beginning of event, and marks data as invalid.

Digital Clear: Resets data acquisition associated controls, but leaves the setup parameters alone. Specifically, it resets event counters, resets data memory (FIFO) pointer to beginning of event, marks data as invalid and issues CLEAR (see above).

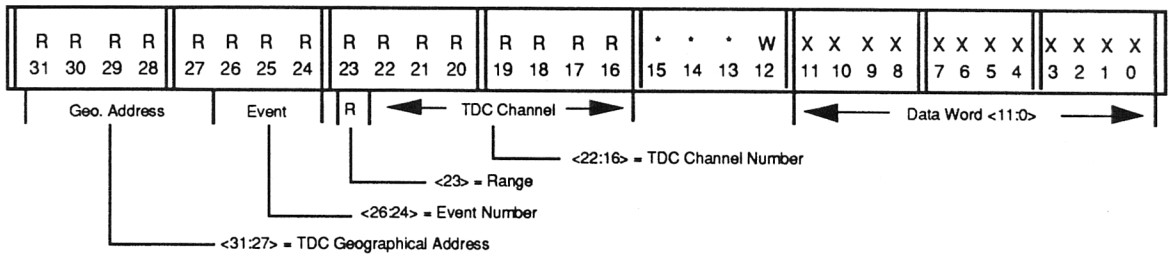
CONTROL AND STATUS REGISTER, CSR0 READ



CSR0 After Rest or Power-up
1872A 1036 0200
1875A 1037 3200

* front panel input status is the complement of the CAT status.

OUTPUT DATA WORD



Data Word: The digitized time interval which may range between 0 and 4095. The pedestal should be less than 15% of full scale for a particular range.

TDC Channel Number: Channels are numbered 0 to 63.

Range: A single bit which denotes the range used to digitize the current integral for that channel and event (1 = High Range).

Event Number: The value of a circular 3-bit counter indicating the location in the module's internal data buffer from which data was read. This value is useful only in readout schemes which use the internal buffering feature of the module.

TDC Geographical Address: The physical slot number of the FASTBUS crate in which the module is located.

N MODE OPERATION

N Mode

Both the N and F mode operation of the 1872A/75A are identical to the 1882/85F modes. The N mode is provided just as in the 1882/85F ADCs to aid compatibility with the older 1880N ADCs. This compatibility extends only so far as acquiring data and reading the 1872A/75A. Certain features of the 1880N, such as generating an invalid response when addressing CSR1 are not implemented.

Particular points to consider include:

1. If the user's software depends on the module ID number to locate units, it will have to be updated to allow for the new ID number.
2. To assure complete initialization after power-up, the 1872A/75A should be internally CLEARed, and RESET. This should be done once after the crate has been turned on.
3. The T-pin response for Sparse Data Scan (SDS - Broadcast cycles: 09_{16} OD_{16}, DD_{16}, and ED_{16}) is not generated until *after* the conversion is complete.
4. For a General Broadcast (01) the 1872A/75A requires the assertion of AK before becoming attached as a slave. This is only a problem if the FASTBUS crate does not have crate electronics.
5. Several bits have been added to CSR0. If the existing software has these bits equal to zero during CSR0 write cycles (expected condition) then no change is needed.
6. The format of reading secondary addresses in CSR space has changed slightly. The Invalid (bit 4), Not Available (bit 6), and Geographic Address (bits 27-31) bits are no longer available. Invalid is indicated by SS = 6. UCSR (bit 5) is now reflected in bits 30 and 31.
7. The reread function in 1872A/75A does not re-enable a T-pin response to a SDS type broadcast.
8. When an 1872A/75A asserts an SS = 2, it remains on the bus until it has been readdressed by a Secondary Address Cycle or by breaking the AS/AK lock and then carrying out a Primary Address Cycle (according to FASTBUS specification).

N Mode Readout Scheme

With the hardware switch S1, (located on the bottom edge of an 1872A/75A module), switched towards the "N" on the board, an 1872A/75A TDC is said to be in N mode. This mode makes the 1872A/75A operate in nearly the same fashion as an 1882N/85N ADC (see previous section); however, an 1872A/75A in N mode still has the features of the faster conversion time as well as support for FASTBUS block transfers at 10 MHz. As stated in earlier sections, N mode operation does not make use of the internal buffer in the 1872A/75A. In the F mode this buffer may be used to completely eliminate readout time as the contributor to experimental dead time; however, unless other slaves in the system have similar buffering, this advantage may not be realized. Thus, in many experimental setups the N mode operation should prove adequate.

Shown in Figure 1, is a typical timing diagram for the pertinent control signals used in acquiring and reading out data in the N mode. This readout scheme is referred to as "readout with next COM and CLEAR blocked" since in this scheme the user is required to disable all COM and CLEAR signals until data (from the previous "uncleared" COM) has been read out. This mode of readout is pretty much the standard way any FASTBUS slave is read out which does not buffer data internally.

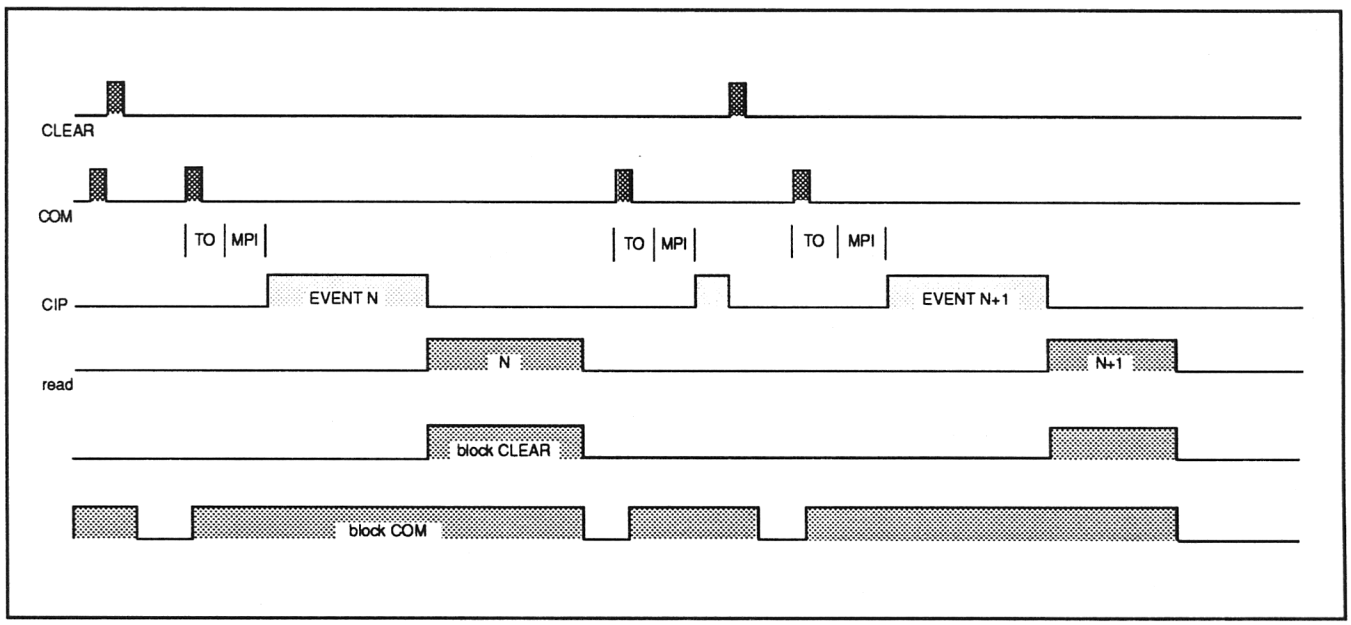


Figure 1
N Mode - Readout with next COM and CLEAR blocked
Timing Diagram

The functions of the COM and CLEAR signals have been described earlier (see Section 3). Notice that once a COM occurs, further COMs must be blocked by the user until either 950 nsec after a CLEAR or the data is read out. The interval labeled "MPI" (Measure Pulse Interval) is user adjustable (see Section 3) which allows additional time for the arrival of a CLEAR pulse. After the MPI has expired, the module begins the digital conversion process and during this time turns ON a front panel signal CIP (Conversion In Progress). Once conversion is complete (CIP goes OFF), readout of the module should begin via standard FASTBUS protocol in either random or block transfer modes. While reading out the data from the module (indicating by the "read" signal in Figure 1), the user must assure that no COM or CLEARs occur. Failure to prevent either COMs or CLEARs during this time will result in corrupted data.

Figures 2 and 3 show the hardware and software logic needed to implement this readout scheme. To ensure the TDC module is properly initialized, the user should CLEAR then RESET the module once after the crate power has been turned on. The Sparse Data Scan shown in the software logic diagram is optional. Note: In the N mode, the T-pin response is not enabled until *after* the digital conversion is complete.

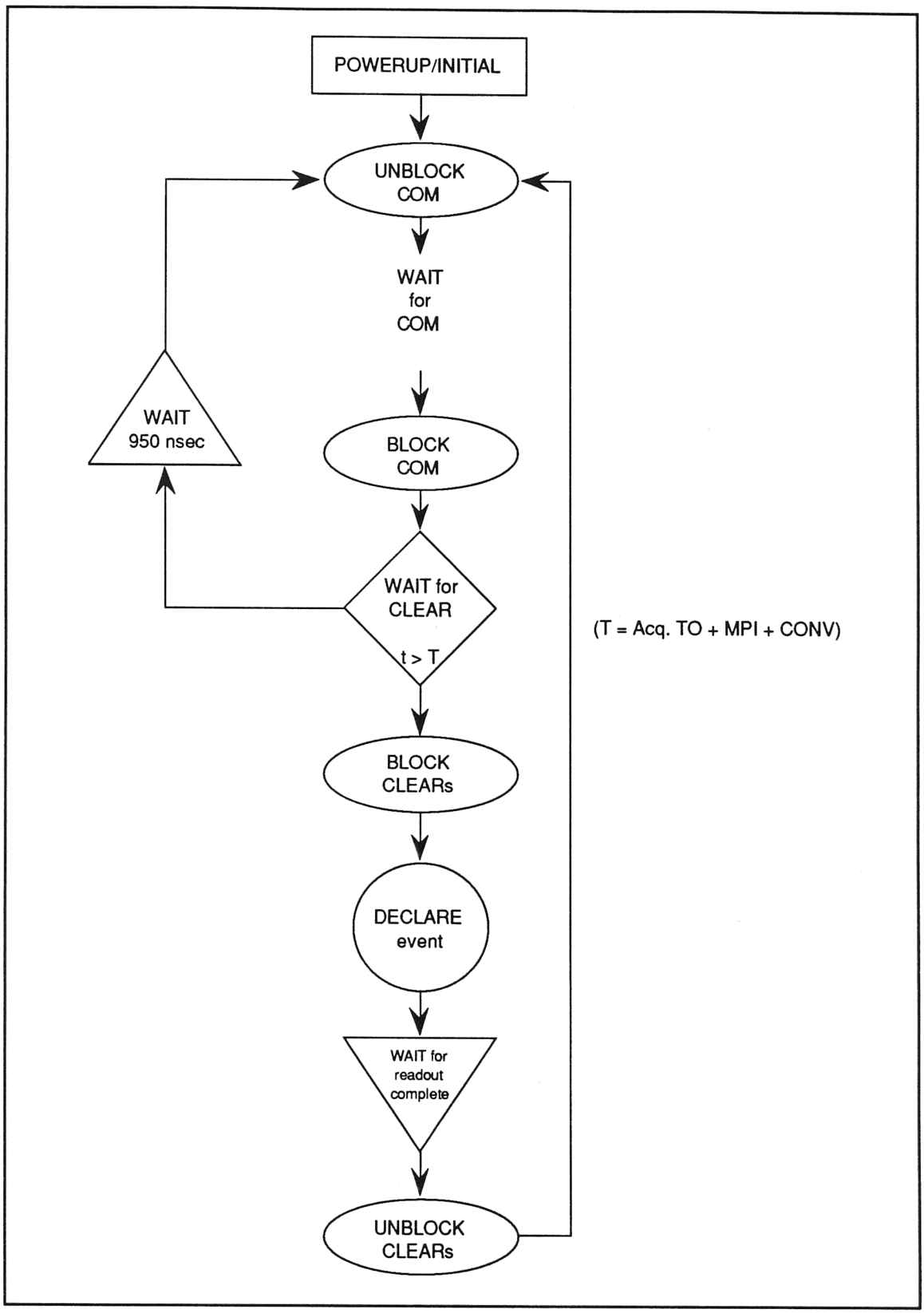


Figure 2
N Mode - Readout with next COM and CLEAR blocked
Hardware Logic

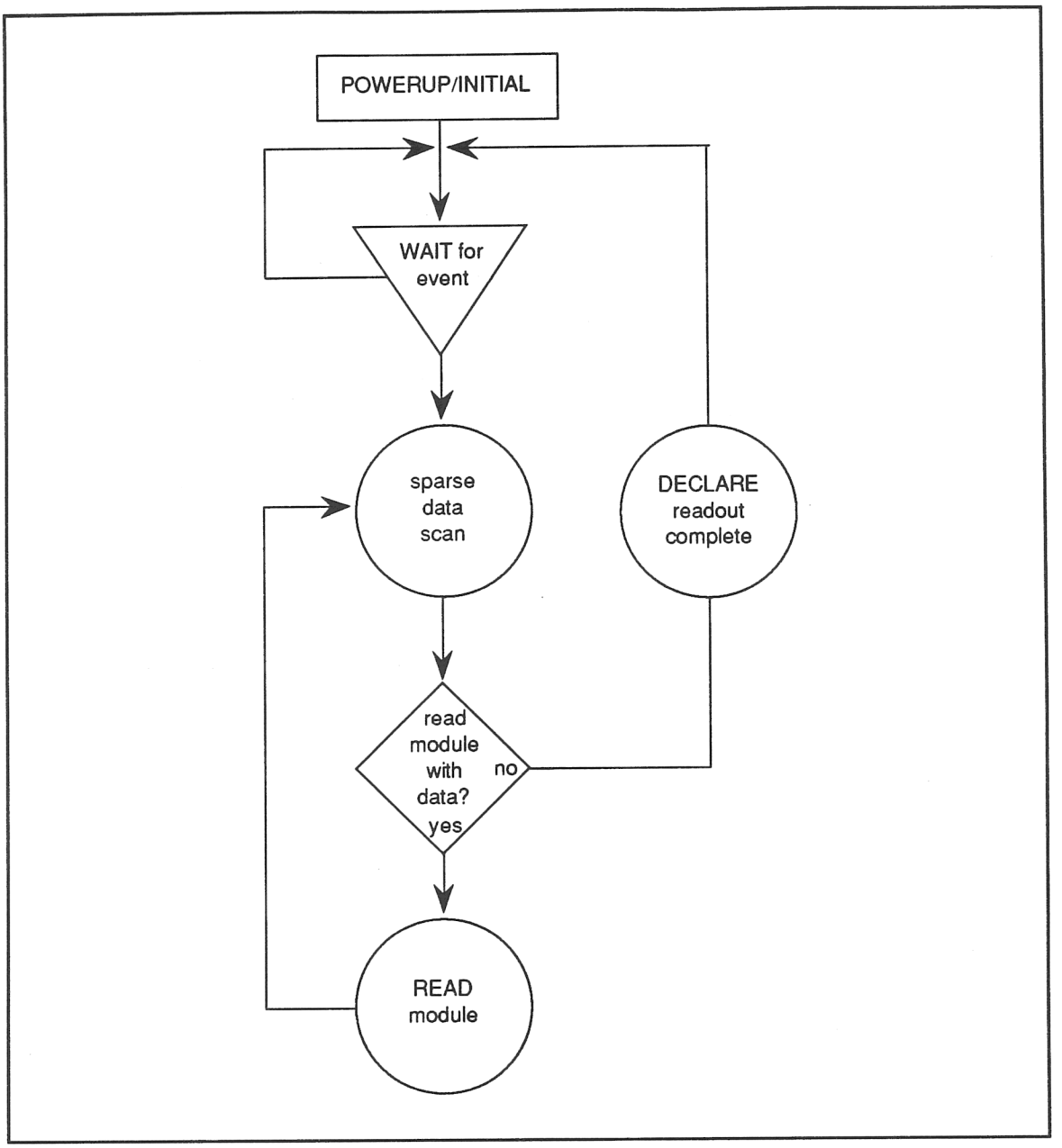
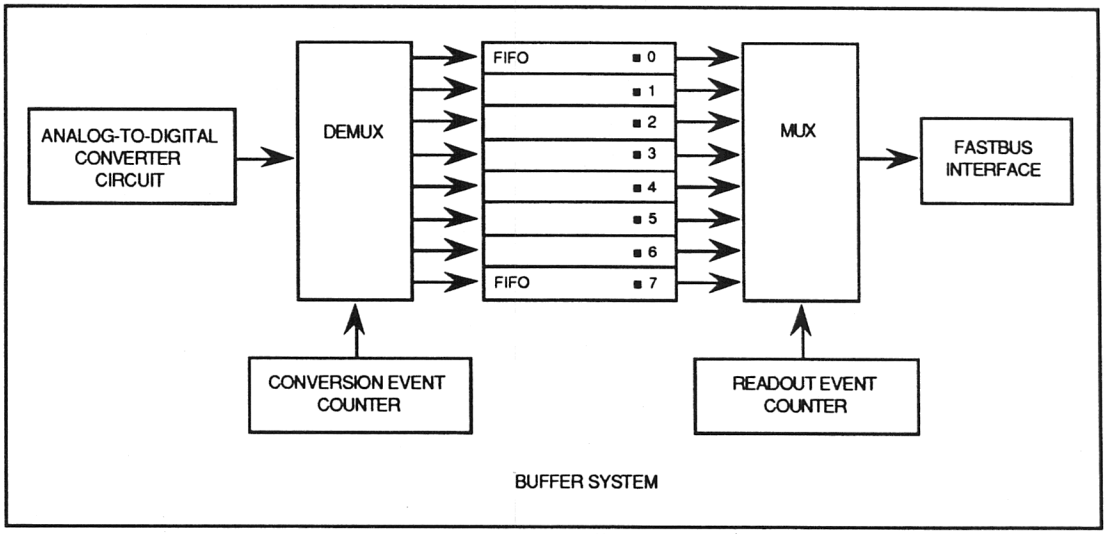


Figure 3
N Mode - Readout with next COM and CLEAR blocked
Software Logic

F MODE OPERATION

The Internal Data Buffer

Data resulting from a conversion is stored in eight 64-word event buffers. Each of these event buffers is a FIFO. The analog-to-digital converter may write to any FIFO. FASTBUS may read data from any FIFO, including the one currently connected to the A-to-D converter.



This structure allows the TDC conversion to occur concurrently with data readout. The conversion circuit writes data (from any hit Channel 0 to Channel 63) into the FIFO. FASTBUS reads data in the same order.

As schematically shown above, the 1872A/75A contains two event counters. The Conversion Event Counter (CEC) is incremented automatically by hardware after the A-to-D conversion of each event (up to 64 channels). The Readout Event Counter (REC) should be incremented by the user's software each time an event has been read out from FASTBUS.

Both the Full and Empty conditions are given by the event counters being equal. The difference is given by which counter was last incremented. If it was the Conversion Event Counter then the 1872A/75A is full. However, if it was the Readout Event Counter then the 1872A/75A is empty. Note that the definitions of Full and Empty are in units of entire events.

The intended use of the multiple event buffer is to implement a fixed delay of N events before readout (N typically being 1, and always less than 8). The user's software would allow N events to be converted and then read out one event during every succeeding A-to-D conversion. This type of programming precludes the possibility of overflow. As this is the intended use, only minimal support is given for the determination of overflow.

The buffer overflow condition is not indicated by any one single function on the 1872A/75A. Pending overflow is given by the combination of a SDS broadcast indicating the unit is not empty, and a read of CSR1 showing both event counters are equal. Thus, an overflow has not yet occurred, however, the unit is full. After the 1872A/75A is full, the user has until the next MPI to read the oldest event. During the MPI the TDC is prepared for writing Channel 0. Since FASTBUS reads events starting from Channel 0, this results in a Busy response, which

makes data from the old event unavailable. The beginning of the next Conversion Interval actually causes overflow and data in the Oldest buffer (the one indicated by the Read Event Counter) will be over-written. At this point, the Conversion Event Counter is disabled from incrementing.

To prevent overflow conditions from occurring, the Conversion In Progress (CIP) signal (which stays true while the full condition exists) should be used to prevent any more COM starts to be issued until some events are read out of the buffer.

Another feature of the 1872A/75A is that the incrementing of the Readout Event Counter is under user control. This means that if desired any event may be skipped by simply incrementing the Readout Event Counter. It is not necessary to actually spend the time reading all the data. This might be useful if higher level trigger logic is available.

Once an event is read out the readout event counter should be incremented. This can be done to all 1872A/75As in a crate by first broadcast addressing them. Sparse Data Scan operations generate correct responses only after the Readout Event Counter is incremented.

Conversion In Progress (CIP) and WAIT

Conversion in Progress (CIP) is a front-panel differential ECL logic signal which is true whenever an A-to-D conversion is in progress. For data readout modes in the 1872A/75A which make use of the data buffer internal to the module, the CIP is used as a signal to the FASTBUS Master that it may begin readout of a previously stored event (not the event being currently digitized). When the buffer full condition occurs, CIP stays true.

The WAIT signal provides a similar function for the readout mode discussed above, but via the FASTBUS backplane. By default the module powers up with the WAIT signal disabled. When the signal is enabled via CSR0, the 1872A/75A will assert the FASTBUS WAIT line when the module is actively being readout (addressed in data space and FASTBUS RD asserted) but the module is *not* performing an A-to-D conversion (CIP is false). In practice, a FASTBUS Master using the above-mentioned readout scheme would monitor the FASTBUS WAIT line and cease all FASTBUS operations when WAIT is asserted.

WARNING: Under FASTBUS specifications the Master may start a time out counter of up to 1 µsec when WAIT is asserted, after which time DS is removed and the Master must decide whether to try again or skip the operation. Some masters use a hardware monostable thus enabling WAIT can significantly impair its effective use as described above.

Both the CIP and WAIT features allow the user to direct the readout of the 1872A/75A modules *not* to occur during the time the module might possibly be stopped thus preventing FASTBUS control signals from contributing noise to the sensitive analog front end. The necessity for such readout schemes is very dependent on the noise environment in which the TDC modules are operated. The complications caused by the internal buffering necessary to appropriately use these signals should be carefully considered (see F Mode Readout Schemes, page 4-20).

SLAVE STATUS RESPONSES

The 1872A/75A generates one of three possible slave status responses on each data cycle.

SS Code	Meaning
0	Data read out successfully
1	Busy (see below)
2	End of block, all hit channels have been read out
6	Invalid, bad MS codes (Master's error)

Whenever the event counters have unequal values, no busy response is possible. The busy response is enabled only whenever the event counters are equal. At this point, if the channel to be read is greater than the last channel converted a busy response is issued. The data on this transfer is invalid (the FIFO is empty).

The full meaning of this response depends on whether the 1872A/75A contains at least one full event. If it does, then a busy response indicates that a buffer overflow has occurred. If not, the TDC has not yet converted the channel that FASTBUS is attempting to read. If the channel to be read out is Channel 0, the unit may be busy and waiting for a stop. For all other channels the unit is waiting for the next TDC conversion and should respond to another data cycle within several microseconds, unless a CLEAR has occurred.

For the case of writing to CSR1, the busy response means that digital conversion is in progress (CIP-High).

FASTBUS BROADCAST FUNCTIONS

The following discussion references nomenclature further detailed by Table 4.3.2 of the December 1983 *FASTBUS Specification, (DOE/ER-0189).*

The 1872A/75A modules respond to five cases of Broadcast Addressing even during conversion time. The first three are general FASTBUS specified modes that many FASTBUS modules will employ while the last two are unique to the LeCroy modules. Note that the case numbers correspond with the FASTBUS table.

General Broadcast 01 Case 1: The TDC module becomes selected and responds to subsequent data cycles.

Sparse Data Scan 09 Case 3: TDC modules respond by asserting TP during the following Read Data Cycle if data are present, independent of whether broadcast was done to CSR or DATA space. TPIN=false indicates that the 1872A/75A is empty. TPIN=true indicates that the 1872A/75A is not empty. The transition from false to true occurs at the end of an A-to-D conversion, indicating one full event is available.

Pattern Select 09 Case 3: TDC modules seeing TP during the next Write Data Cycle are selected and respond to subsequent Read or Write Data Cycles.

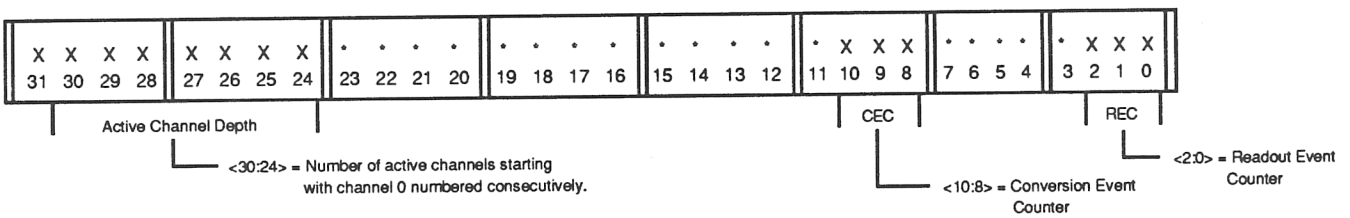
All Devices Assert $0D_{16}$ Case 4: The TDC module asserts the TP on the following Read Cycle.

TDC Sparse Data Scan DD_{16} Case 7a: Same as broadcast 09 above, but specifically for TDC modules.

AFC T-Pin Assert ED_{16} Case 7b: TDC modules respond by asserting TP during the following Read Data Cycle if an installed AFC card is asserting TRIG (J2-B53) on the Auxiliary FASTBUS connector.

Note that Broadcast addressing, although a very powerful tool, must be used with great care, since handshaking and SS responses are not produced by the Slave modules, preventing error checking.

CSR1



Power-up 4000 0000

Writing to FASTBUS Register CSR1

The Event Counters are not intended to be written. They are correctly altered by internal circuits and CSR0 operations. Technically seen, they are read/write registers and may be written to if desired, (e.g., for testing). *Note that the internal control circuits which keep track of events and indicate valid memory in response to Sparse Data Scans are not capable of following arbitrary changes in event numbers.*

The response sequence for Sparse Data Scan is:
Data is marked invalid on Power-up, CSR0 Reset or CSR0 Clear.

When an A-to-D conversion is complete, the Conversion Event Counter is incremented and data is marked valid.

When a CSR0 Increment Event Counter is executed, the Conversion Event Counter is compared to the Readout Event Counter. If the counters are equal the data is marked invalid, otherwise the data remains valid.

Depth Field

The depth field allows the user to program the number of active channels within a module. This can be an important parameter when ways are needed to reduce conversion time or when all the channels of a module are not needed in a specific application.

The depth field is intended as a setup parameter to be initialized on power up and then left alone. In this manner bits 24 through 30 would be written as the desired depth with bits 0 through 2 and 8 through 10 zeroed (this is consistent with the power-up condition).

Reasonable values for the depth field are limited to decimal numbers between 1 and 64. Values above 64 will be truncated to 64 without negative side effects. A value of 0 is possible and allowed although not meaningful.

Note: The active channels are always counted starting from channel zero (e.g., active channels 8 through 48 would not be possible but 0 to 48 would be).

F MODE READOUT SCHEMES

With the hardware switch S1 located on the bottom edge of an 1872A/75A module switched towards the "F" position, an 1872A/75A TDC is said to be in F mode. In the F mode all the features relating to the internal buffer are enabled. There are a number a different possible readout schemes in F mode, most of which take advantage of the buffer to completely eliminate readout time as a contributor to experimental dead time. However, unless other slaves in the system have similar buffering, this advantage may not be realized.

Thus, in most experimental setups N mode operation should prove adequate. However, the prudent user should look over this section since it illustrates a number of "features" of the module which might prove useful in other applications or may (at worst) cause difficulty if the module is unintentionally set in F mode.

Four different readout schemes will be discussed in the following sub-sections, they are:

1. F Mode - Readout with next COM and CLEARs blocked
2. F Mode - Readout with next COM allowed
3. F Mode - Readout during next Conversion with CLEARs blocked
4. F Mode - Readout during next Conversion

In all F mode readout schemes you are required to increment the REC (Readout Event Counter) in each module following the completion of the readout procedure for that event. Failure to do this will cause the next readout to fetch the same data, not the data for the most recent (uncleared) COM, and will give incorrect responses to SDS operations. Continued failure to increment REC will eventually cause the buffer to overflow, resulting in the module issuing a BUSY response (SS=1) to the next FASTBUS read.

F-Mode - Readout With Next COM and CLEAR Blocked

This readout scheme is referred to as "readout with next COM and CLEAR blocked" since the user is required to disallow all COM and CLEAR signals until data (from the previous "uncleared" COM) has been read out. Figure 4 is a typical timing diagram for this scheme. The functions of the COM and CLEAR signals have been discussed earlier (see Section 3). Notice that once a COM occurs, further COMs must be blocked by the user until either 950 nsec after a CLEAR or the data is read out. The interval labeled MPI is user adjustable (see Section 3) which allows additional time for the arrival of a CLEAR pulse. After the MPI has expired, the module begins the digital conversion process and during this time turns ON the front panel signal CIP.

Once conversion is complete, the module internally increments the CEC and becomes "Not Empty", which enables the module to assert its T-Pin in response to a FASTBUS Sparse Data Scan. Also, readout of the module should begin via standard FASTBUS protocol in either random or block transfer modes. While reading out the data from the module (indicated by the "read" signal in Figure 4), the user must assure in this scheme that no COMs or CLEARs occur. Once all

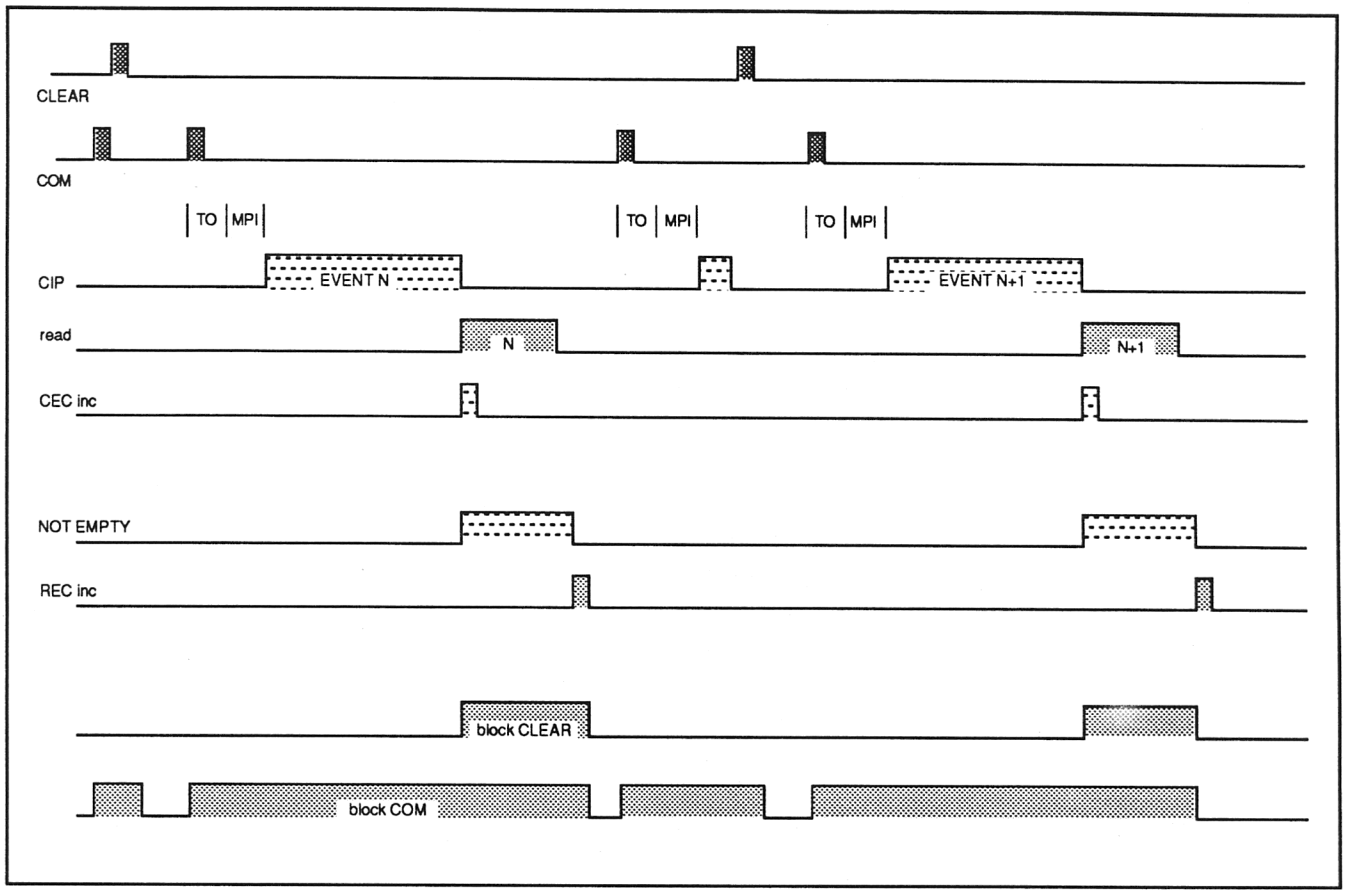


Figure 4
F Mode - Readout with next COM and CLEAR blocked
Timing Diagram

data has been read out of the module, the user MUST increment the REC whereupon the module ceases to be "Not Empty" and the T-Pin response is disabled. As discussed in an earlier section, failure to increment the REC in each module after the event has been read out will give spurious results.

Figures 5 and 6 show the hardware and software logic needed to implement this readout scheme. To ensure the TDC module is properly initialized, the user should CLEAR then RESET the module once after the crate power has been turned on. The Sparse Data Scan shown in the software logic diagram is optional.

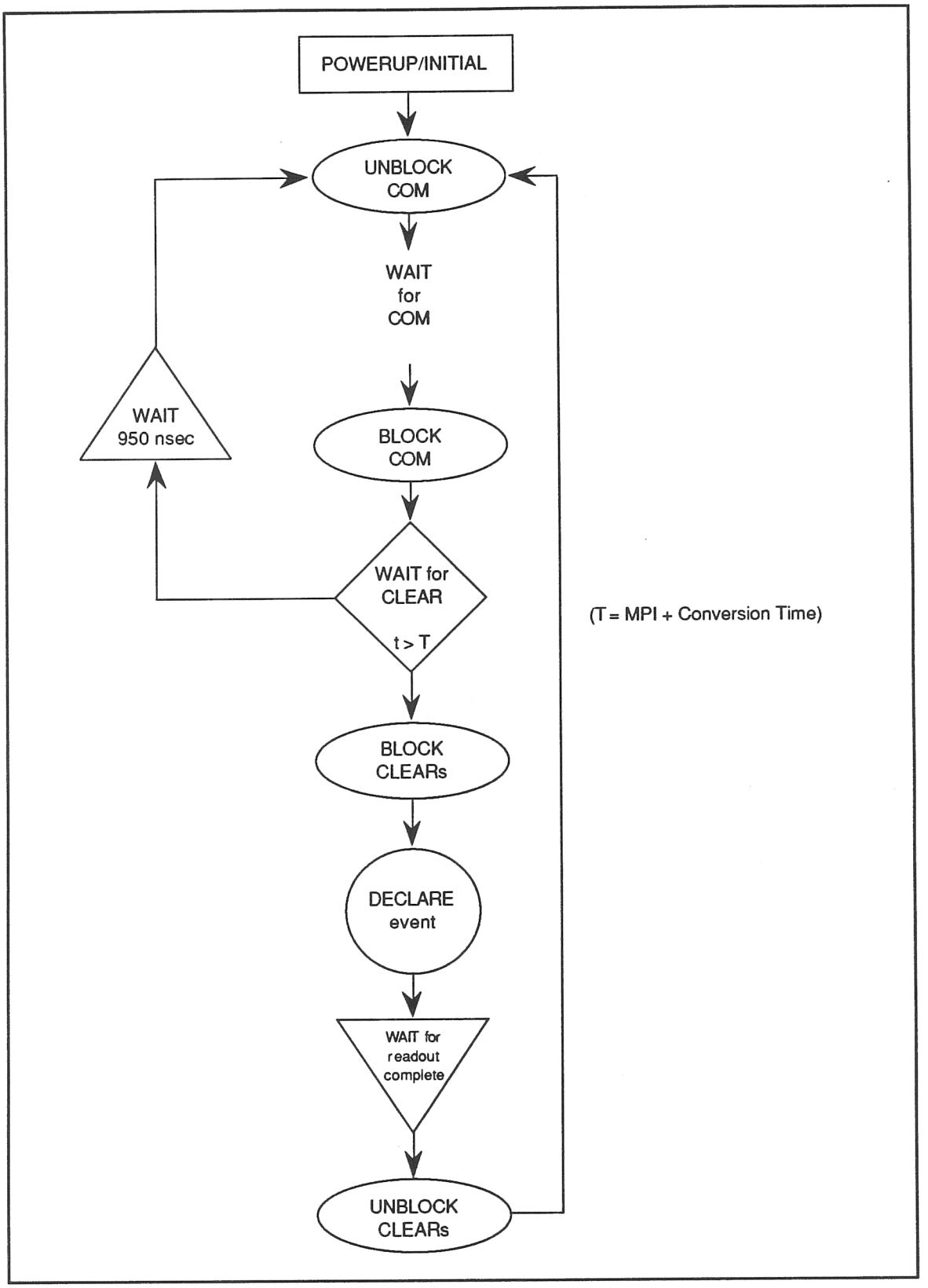


Figure 5
F Mode - Readout with next COM and CLEAR blocked
Hardware Logic

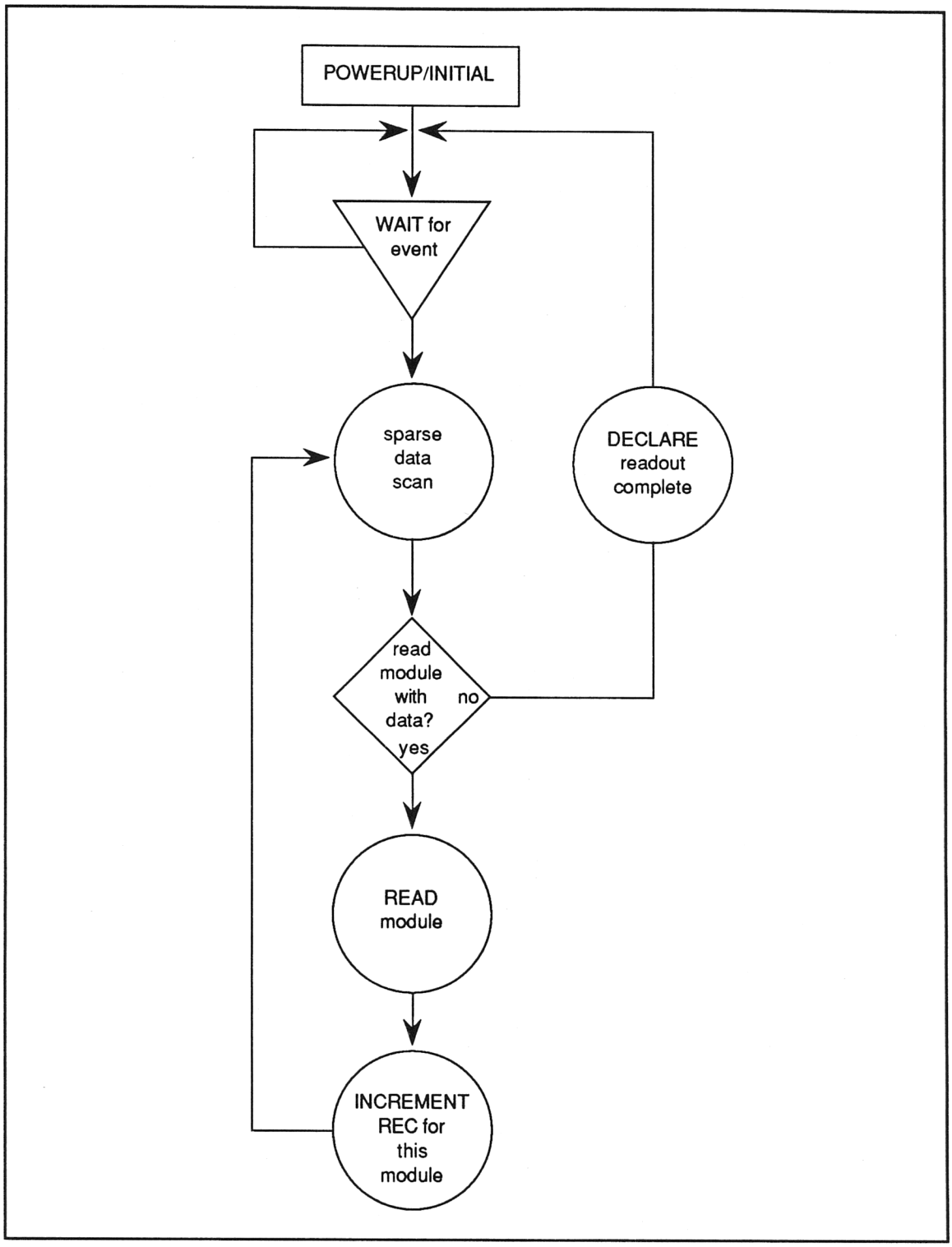


Figure 6
F Mode - Readout with next COM and CLEAR blocked
Software Logic

F Mode - Readout With Next COM Allowed

This readout scheme is referred to as "readout with next COM allowed" since the user may allow COM and CLEAR signals during the readout of the previous event. Figure 7 is a typical timing diagram. This scheme employs the internal buffer of the 1872A/75A.

If data is read out at 10 MHz rate using the FASTBUS block transfer protocol, data from a full crate of TDCs can be readout in less than the conversion time of a single full TDC. This means that data from the previous event will always be read out of the buffer before conversion of the current event is complete. Thus, COMs can be permitted during the readout of the previous event without the possibility of the converted data overflowing the internal buffer. In this scheme the enabling of COMs in parallel with the FASTBUS readout effectively eliminates the readout time as contributor to experimental dead time.

One possible disadvantage in this scheme is that the noise seen by the sensitive analog front end of the TDC may increase due to the FASTBUS backplane activity of reading out the TDCs during the front-end charge collection interval. The extent of this noise is very dependent on crate electronics and other FASTBUS modules in the crate. If excessive noise is experienced with this readout scheme, the user should consider using a readout scheme which only allows data readout during a conversion cycle (discussed in following sections).

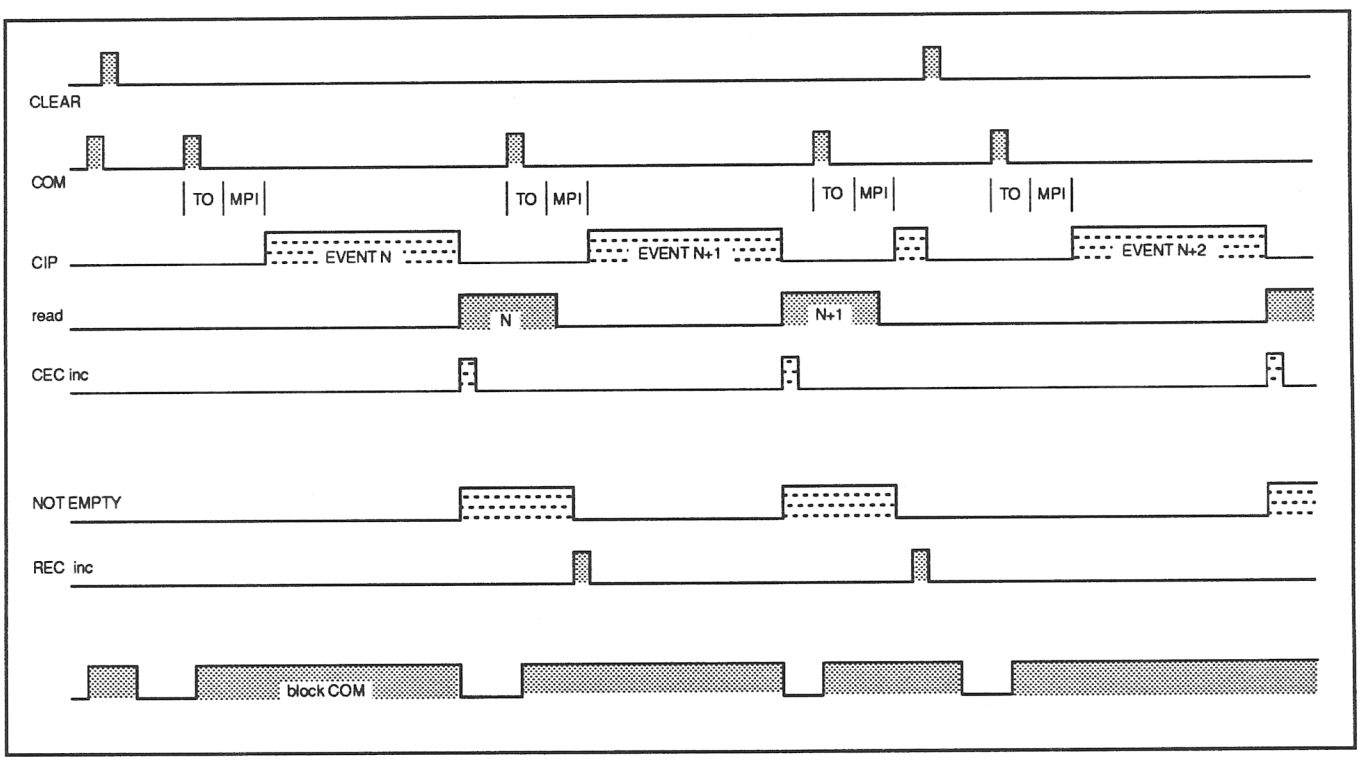


Figure 7
F Mode - Readout with next COM allowed
Timing Diagram

The function of the COM and CLEAR signals has been discussed earlier (see Section 3). Notice that once a COM occurs, further COMs must be blocked by the user until either 950 nsec after a CLEAR or the data is converted. The interval labeled MPI is user adjustable (see Section 3) which allows additional time for the arrival of a CLEAR pulse. After the MPI has expired, the module begins the digital conversion process and during this time turns ON a front-panel signal CIP.

Once conversion is complete the module internally increments the CEC and becomes "Not Empty" which enables the module to assert its T-Pin in response to a FASTBUS Sparse Data Scan. The user may now unblock the COM signal and commence readout of the module via standard FASTBUS protocol for block transfer. Since this scheme depends on the readout time being less than a single module's conversion time (true for 10 MHz readout), it is the user's responsibility to assure that the FASTBUS Master can transfer data at a sufficiently high rate for the number of TDCs to be read out. Once all data has been read out of the module, the user *must* increment the REC whereupon the module ceases to be "Not Empty" and the T-Pin response is disabled. As discussed in an earlier section, failure to increment the REC in each module after the event has been read out will give spurious results.

Figures 8 and 9 show the hardware and software logic needed to implement this readout scheme. To ensure the TDC module is properly initialized, the user should CLEAR then RESET the module once after the crate power has been turned on. The Sparse Data Scan shown in the software logic diagram is optional.

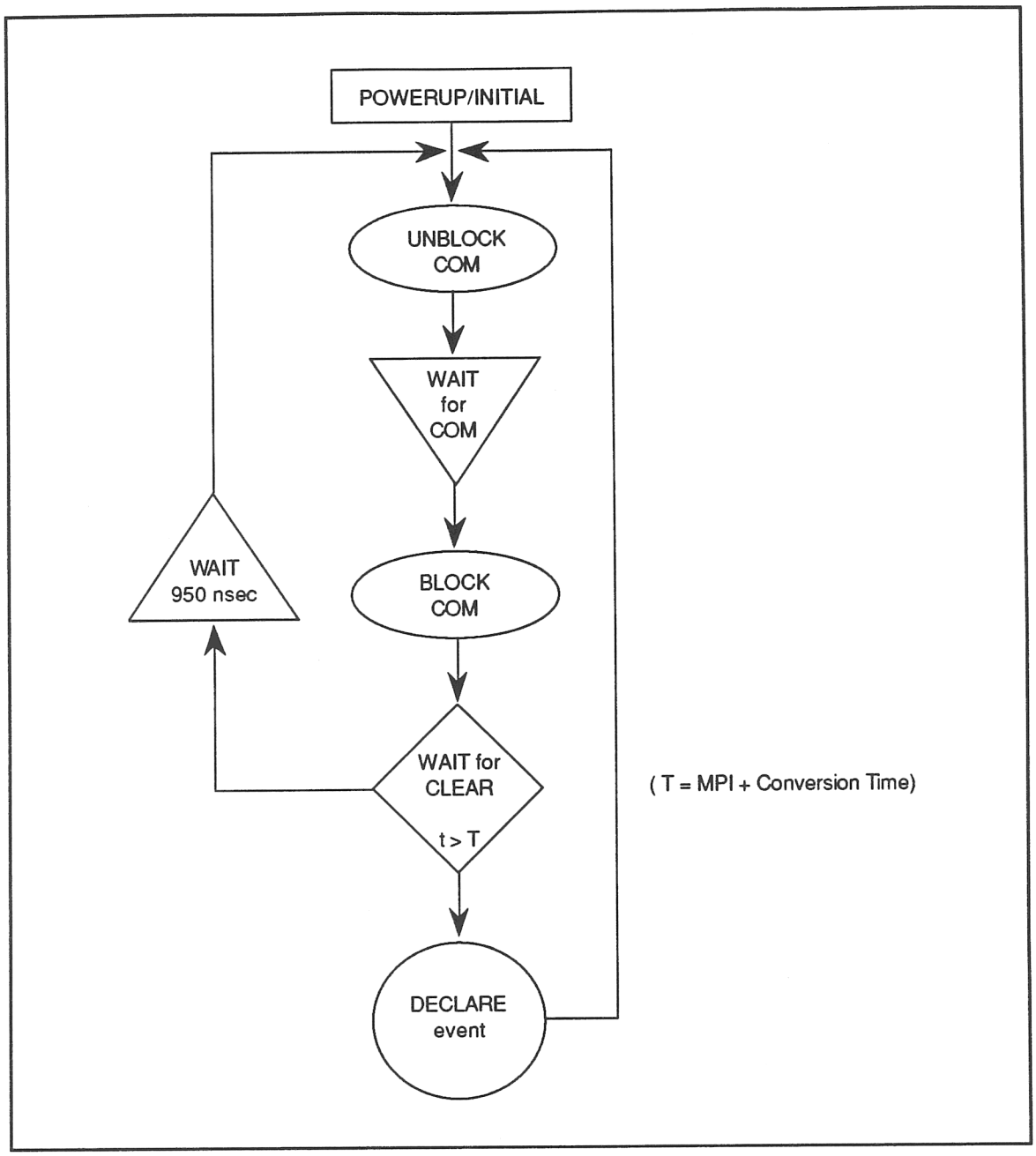


Figure 8
F Mode - Readout with next COM allowed
Hardware Logic

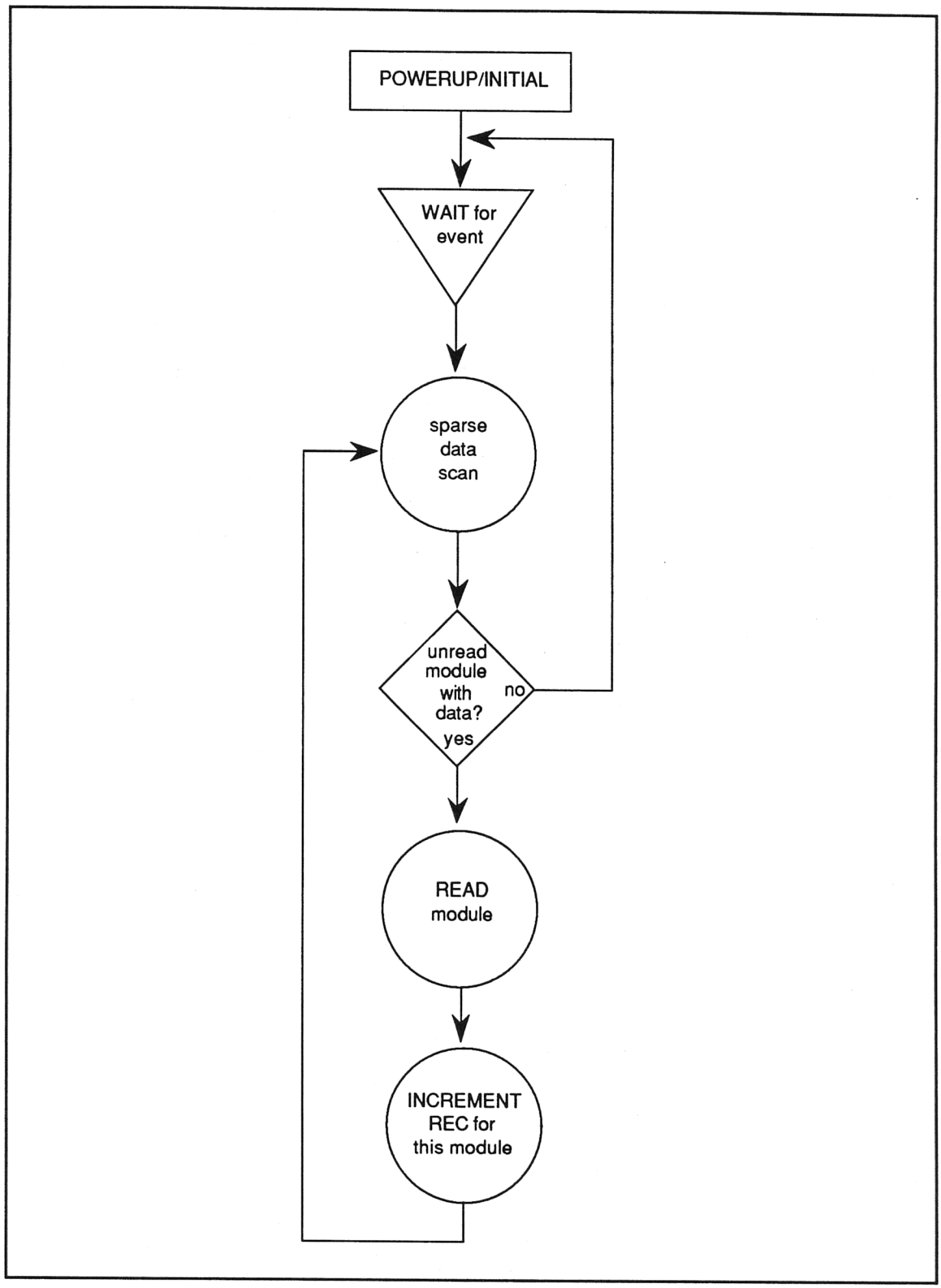


Figure 9
F Mode - Readout with next COM allowed
Software Logic

F Mode - Readout During Next Conversion With CLEARs Blocked

This readout scheme is referred to as "readout during next conversion with CLEAR blocked" since readout of data from an event is delayed until a second event has occurred and the digital conversion of the second event has begun. For illustrative purposes, we will also require in this scheme that all CLEARs are blocked during the conversion time. This constraint is removed in the following sections where its consequences are fully discussed. Figure 10 is a typical timing diagram.

This readout scheme employs the internal buffer of the 1872A/75A. If data is read out at 10 MHz rate using the FASTBUS block transfer protocol, data from a full crate of TDCs can be read out in less than the conversion time of a single full TDC. This means that data from the previous event will always be read out of the buffer before conversion of the current event is complete, (since clears are blocked). In this scheme, the digital conversion of data in parallel with the FASTBUS readout effectively eliminates data readout time as contributor to experimental dead time. Also, this scheme ensures that all FASTBUS backplane activity *does not* occur during the time that the sensitive TDC analog front end is collecting charge. Whether this reduces noise in acquired current integrals is dependent upon the noise environment of the crate.

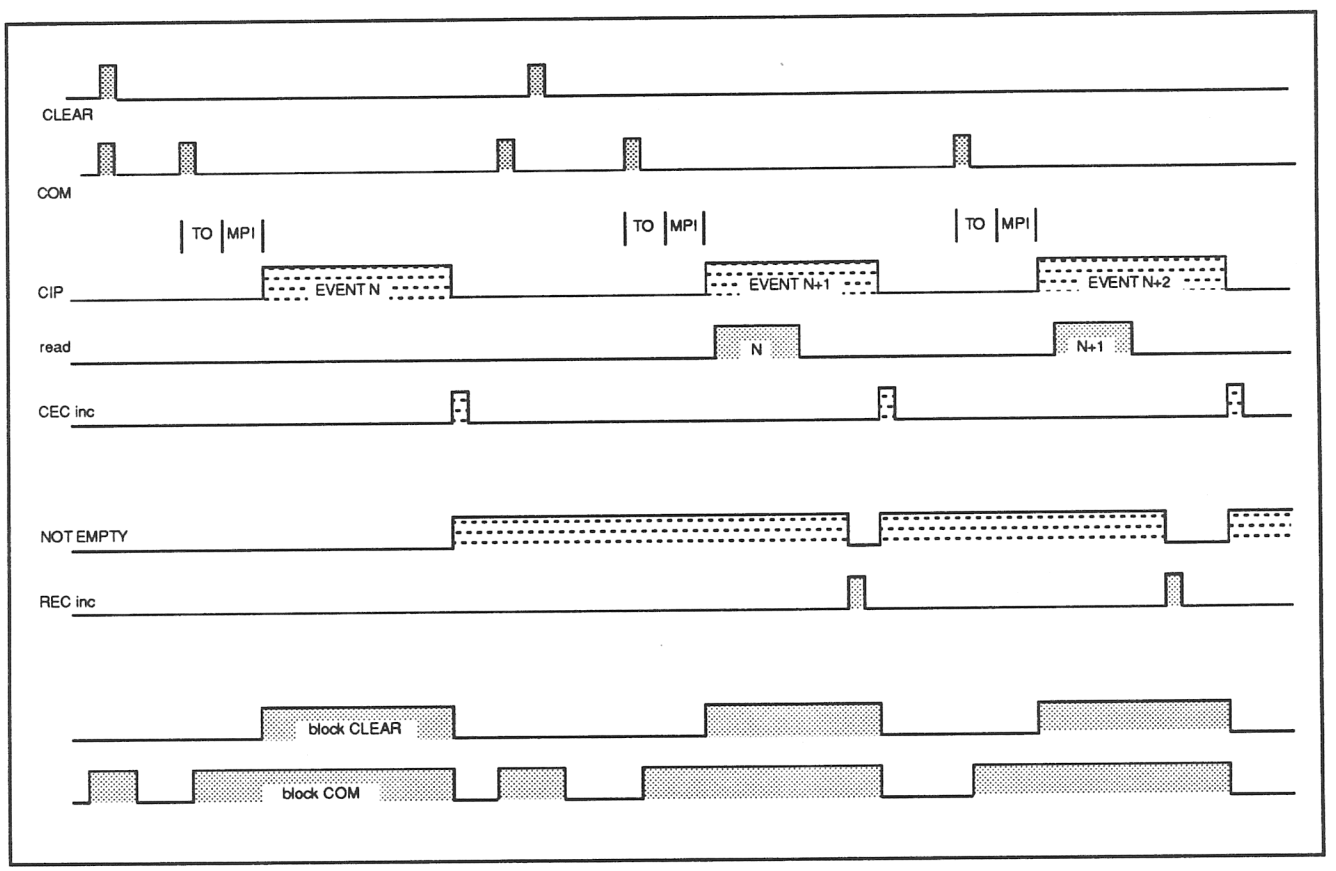


Figure 10
F Mode - Readout during next conversion with CLEAR blocked
Timing Diagram

The function of the COM and CLEAR signals has been discussed earlier (see Section 3). Notice that once a COM occurs, further COMs must be blocked by the user until either 950 nsec after a CLEAR or the data for that COM has been digitally converted. The interval labeled MPI is user adjustable (see Section 3), which allows additional time for the arrival of a clear pulse. After the MPI has expired, the module begins the digital conversion process and during this time turns ON the front-panel signal CIP. In this scheme, the user should ensure that all CLEARs are blocked during the conversion process.

Once conversion is complete the module internally increments the CEC and becomes "Not Empty" which enables the module to assert its T-Pin in response to a FASTBUS Sparse Data Scan. However, readout of this data should not commence until the conversion of the *following* event. The user may now unblock the COM and CLEAR signals and commence readout of the module via standard FASTBUS protocol for block transfer. Since this scheme depends on the readout time being less than a single module's conversion time (true for 10 MHz readout), it is the user's responsibility to ensure that the FASTBUS Master can transfer data at a sufficiently high rate for the number of TDCs to be read out.

Once all data has been read out of the module, the user *must* increment the REC where upon the module ceases to be "Not Empty" and the T-Pin response is disabled. As discussed in an earlier section, failure to increment the REC in each module after the event has been read out will give spurious results.

Notice that this readout scheme has the effect of delaying the arrival of data for Event N to the FASTBUS Master until Event N+1 has occurred and its conversion started.

Figures 11 and 12 show the hardware and software logic needed to implement this readout scheme. To ensure the TDC module is properly initialized, the user should CLEAR, then RESET the module once after the crate power has been turned on. Notice that in these logic schemes it is assumed that an external counter is incremented after each event is converted. It is also assumed that the master has access to the value of this counter and the status of the CIP signal, both of which are used to determine if data should be read out of the TDC(s). Certainly, other techniques might be devised to provide the same control function. The Sparse Data Scan shown in the software logic diagram is optional.

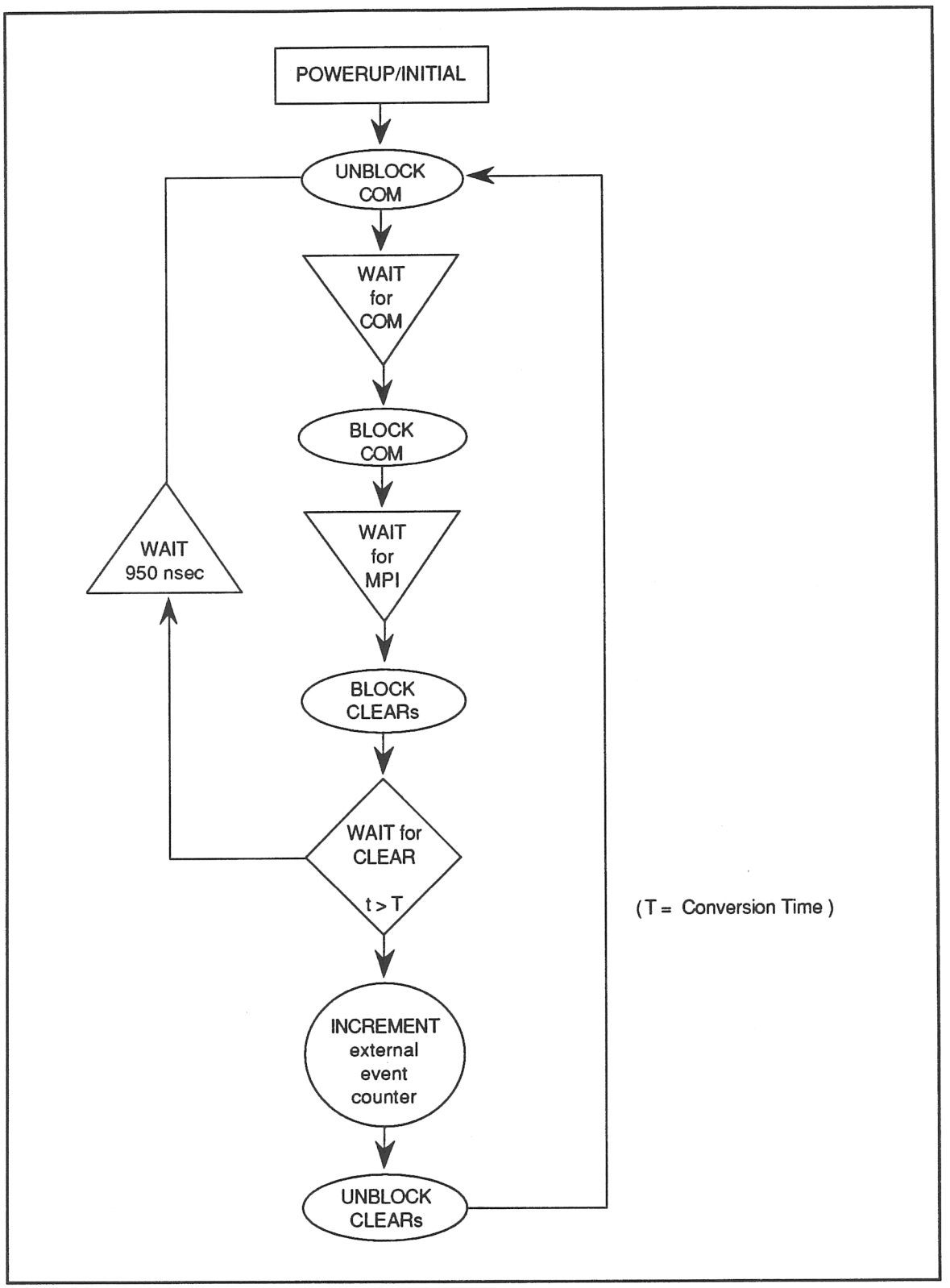


Figure 11
F Mode - Readout during next conversion with CLEAR blocked
Hardware Logic

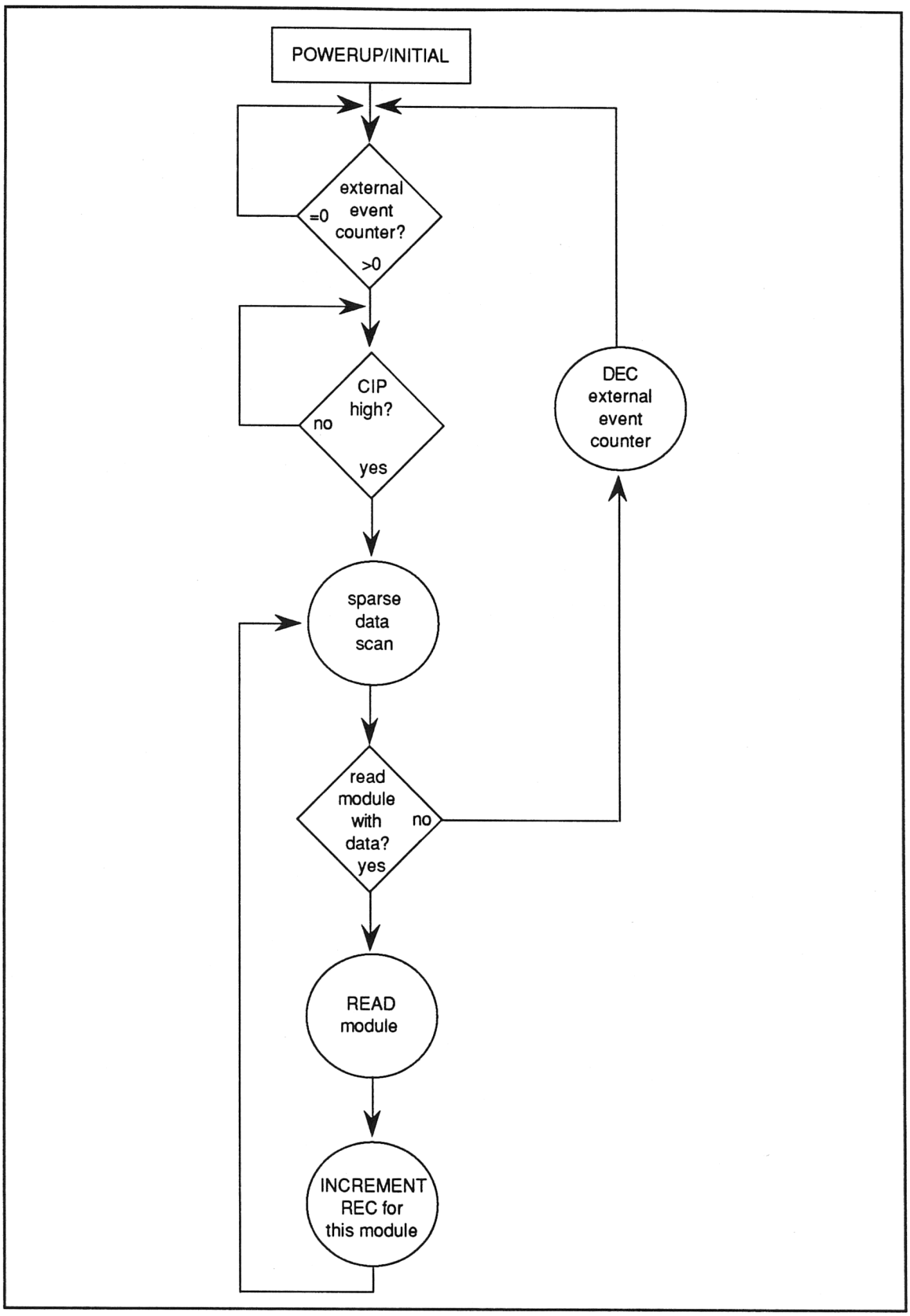


Figure 12
F Mode - Readout during next conversion with CLEAR blocked Software Logic

F Mode - Readout During Next Conversion

This readout scheme is referred to as "readout during next conversion" since readout of data from an event is delayed until a second event has occurred and the digital conversion of the second event has begun. This scheme is the same (in principle) as the previous scheme except that CLEARs are *not* blocked during the conversion time. Figure 13 is a typical timing diagram.

This scheme has all of the advantages and disadvantages of the previous scheme plus on additional "feature". Namely, if a CLEAR occurs during a conversion cycle, the FASTBUS master should cease all readout activities until the next conversion cycle. Thus, readout of an event may spill over into a number of conversion periods as illustrated in Figure 13.

Implementation of "readout during next conversion" is most easily accomplished via enabling the WAIT option (by setting the appropriate bit in CSR0). With WAIT option enabled, an addressed module will assert the FASTBUS WAIT line when a conversion is *not* in progress and the FASTBUS Master actively monitors the WAIT line, stopping all operations upon its assertion. The impact of holding up the Master between conversions should be carefully considered by the user since it may well impact the readout of other types of modules.

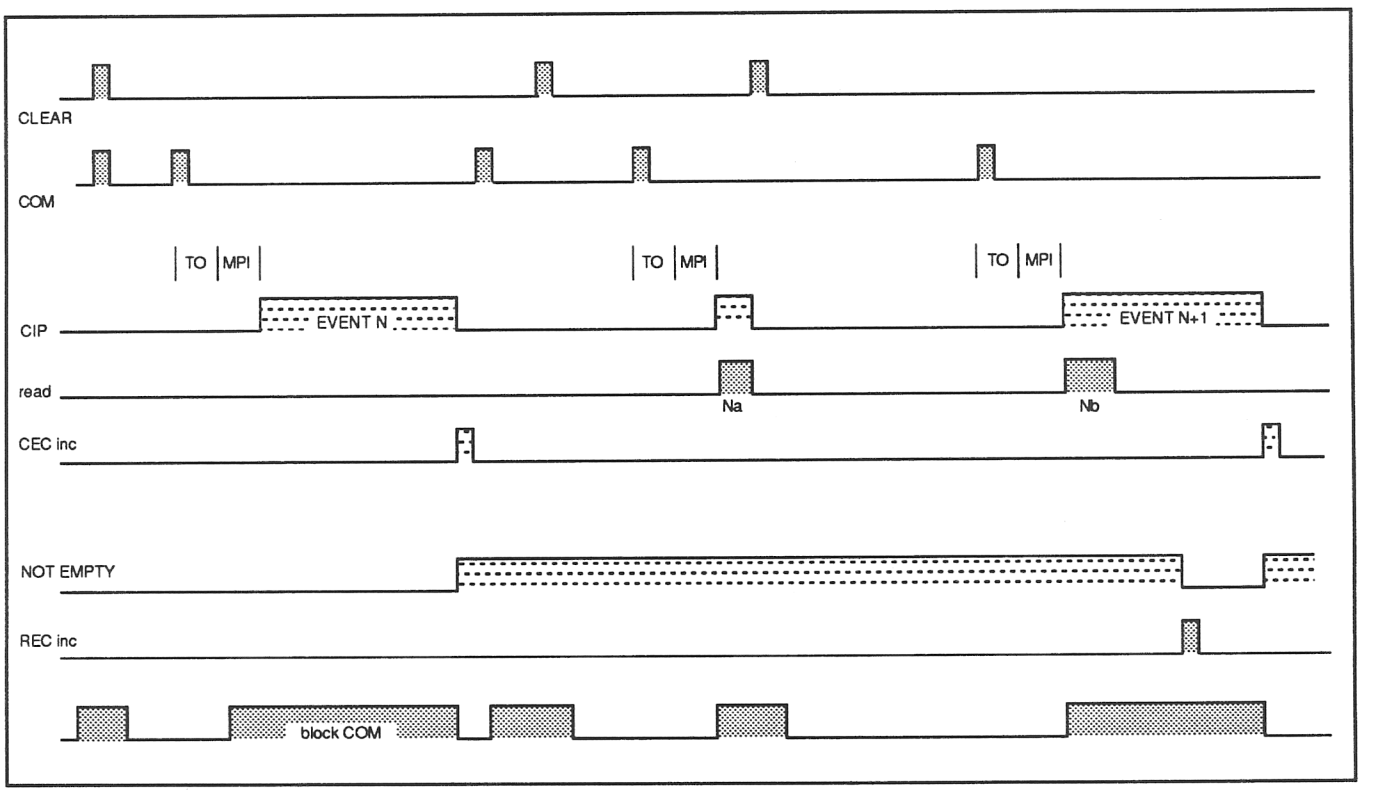


Figure 13
F Mode - Readout during next conversion
Timing Diagram

This readout scheme employs the internal buffer of the 1872A/75A. If data is read out at 10 MHz rate using the FASTBUS block transfer protocol, data from a full crate of TDCs can be read out in less than the conversion time of a single full TDC. This means that data from the previous event will always be read out of the buffer before conversion of a complete event. In this scheme, the digital conversion of data in parallel with the FASTBUS readout effectively eliminates data readout time as contributor to experimental dead time. Also, this scheme ensures that all FASTBUS backplane activity *does not* occur during the time the sensitive TDC analog front end is collecting charge. Whether this reduces noise in acquired current integrals is dependent upon the noise environment of the crate.

The function of the COM and CLEAR signals has been discussed earlier (see Section 3). Notice that once a COM occurs, further COMs must be blocked by the user until either 950 nsec after a CLEAR or the data for that COM has been digitally converted. The interval labeled MPI is user adjustable (see Section 3) which allows additional time for the arrival of a CLEAR pulse. After the MPI has expired, the module begins the digital conversion process and during this time turns ON the front-panel signal CIP.

Once conversion is complete the module internally increments the CEC and becomes "Not Empty" which enables the module to assert its T-Pin in response to a FASTBUS Sparse Data Scan. However, readout of this data should not commence until the conversion of the *following* event. The user may now unblock the COM signal and commence readout of the module via standard FASTBUS protocol for block transfer. Since this scheme depends on the readout time being less than a single module's conversion time (true for 10 MHz readout), it is the user's responsibility to assure that the FASTBUS Master can transfer data at a sufficiently high rate for the number of TDCs to be read out.

Once all data has been read out of the module, the user *must* increment the REC where upon the module ceases to be "Not Empty" and the T-Pin response is disabled. As discussed in an earlier section, failure to increment the REC in each module after the event has been read out will give spurious results.

Figures 14 and 15 show the hardware and software logic needed to implement this readout scheme. To ensure that the TDC module is properly initialized, the user should CLEAR, then RESET the module once after the crate power has been turned on. Notice that in these logic schemes it is assumed that an external counter is incremented after each event is converted.

It is assumed that the master has access to the value of this counter and the status of the CIP signal, both of which are used to determine if data should be read out of the TDC(s). Certainly, other techniques might be devised to provide the same control function. Since the CLEARs can occur at any time in this scheme, the WAIT option is assumed to be enabled on all modules as discussed above and the FASTBUS Master is obligated to cease operations upon the assertion of WAIT. The Sparse Data Scan shown in the software logic diagram is optional.

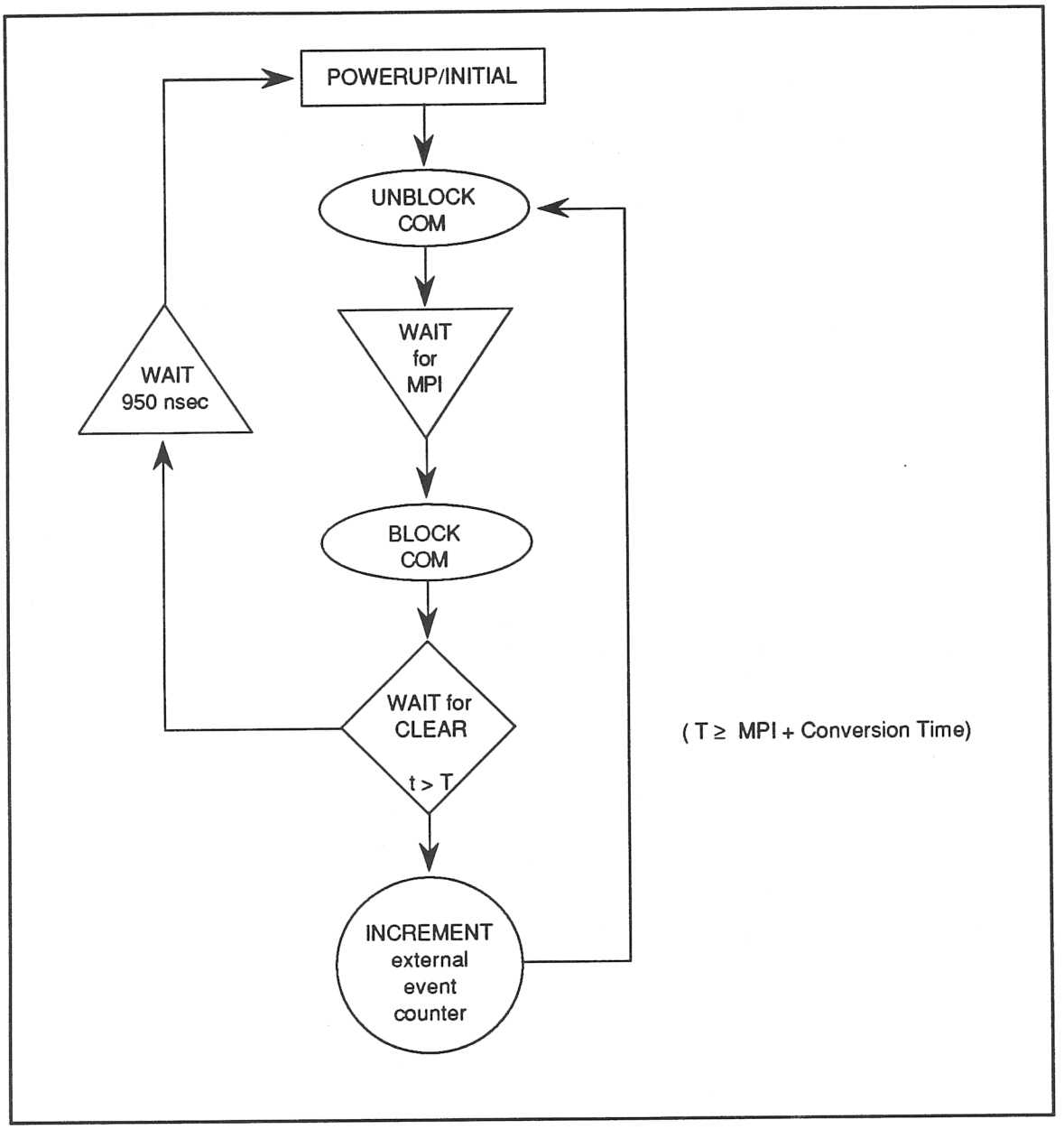


Figure 14
F Mode - Readout during next conversion
Hardware Logic

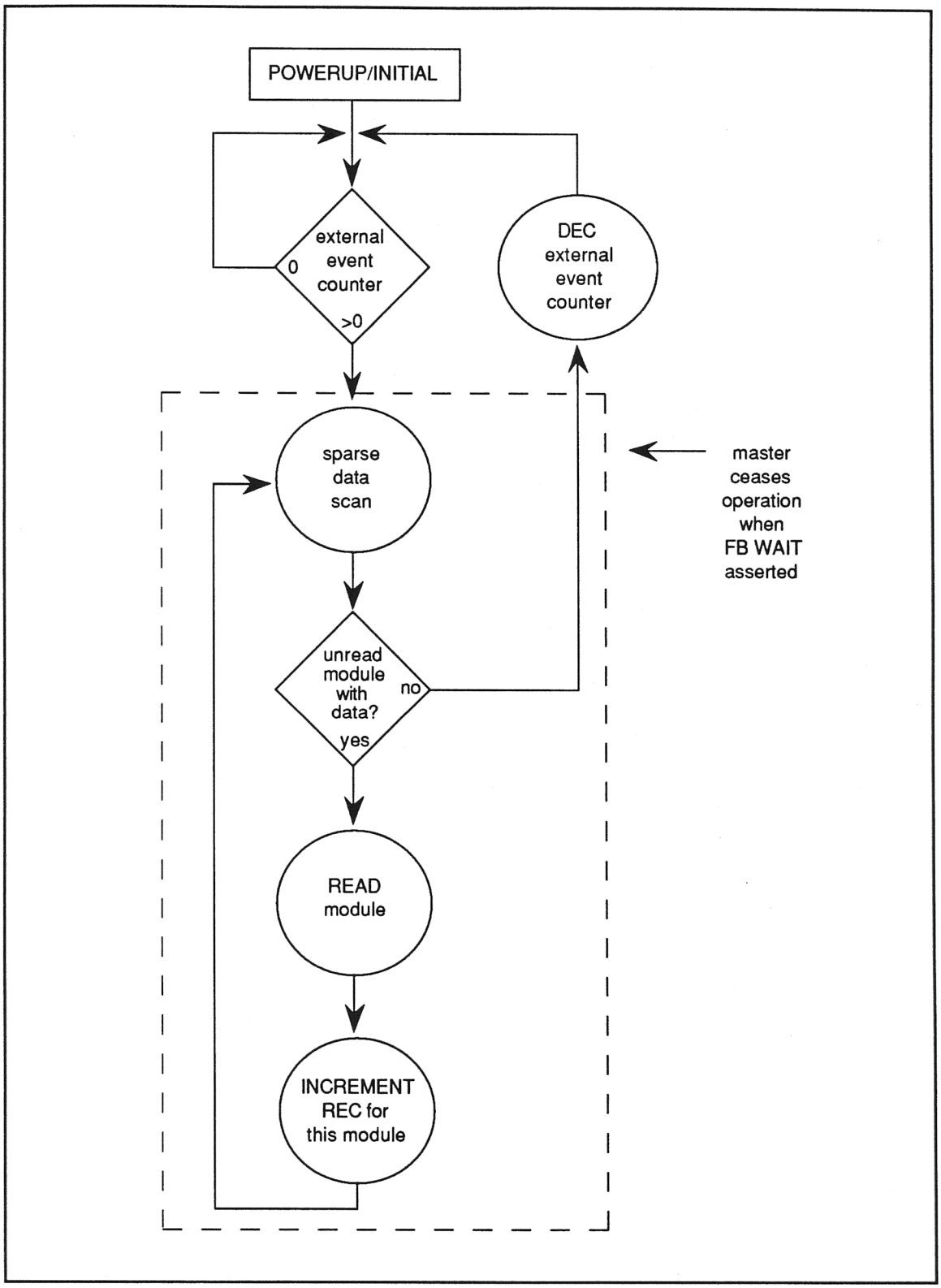


Figure 15
F Mode - Readout during next conversion
Software Logic

MIQ401 - INPUT MONOLITHIC CIRCUITRY

The MIQ401 Input Monolithic is a proprietary integrated circuit designed at LeCroy. It is a 4-channel integrate, hold and multiplex chip. The chip has four analog inputs and three analog outputs. The input signals are integrated for the duration of the gate control signal. The result is held on capacitors internal to the chip for up to a millisecond with no significant droop. At any time after the chip gate is off, any one of the channels may be multiplexed to the common analog output pins to be routed to a common analog-to-digital converter circuit. The output channel is selected by one of the four strobe control lines (STROBE0 to STROBE3). To facilitate the use of many chips, a chip select control line (CS) is provided on the chip. An equivalent circuit diagram of the MIQ401 chip is shown in Figure 16 (see *"A 4-Channel Charge Multiplexer Monolithic Integrated Circuit (QMUX) for Use in Large Scale ADC Systems"*, J. J. Mueller, L. B. Levit and H. Petersen, presented at the 1985 Nuclear Science Symposium, San Francisco, CA, October 1985 and published in IEEE Transactions in Nuclear Science, 33, No. 1, 1986, p. 897-902).

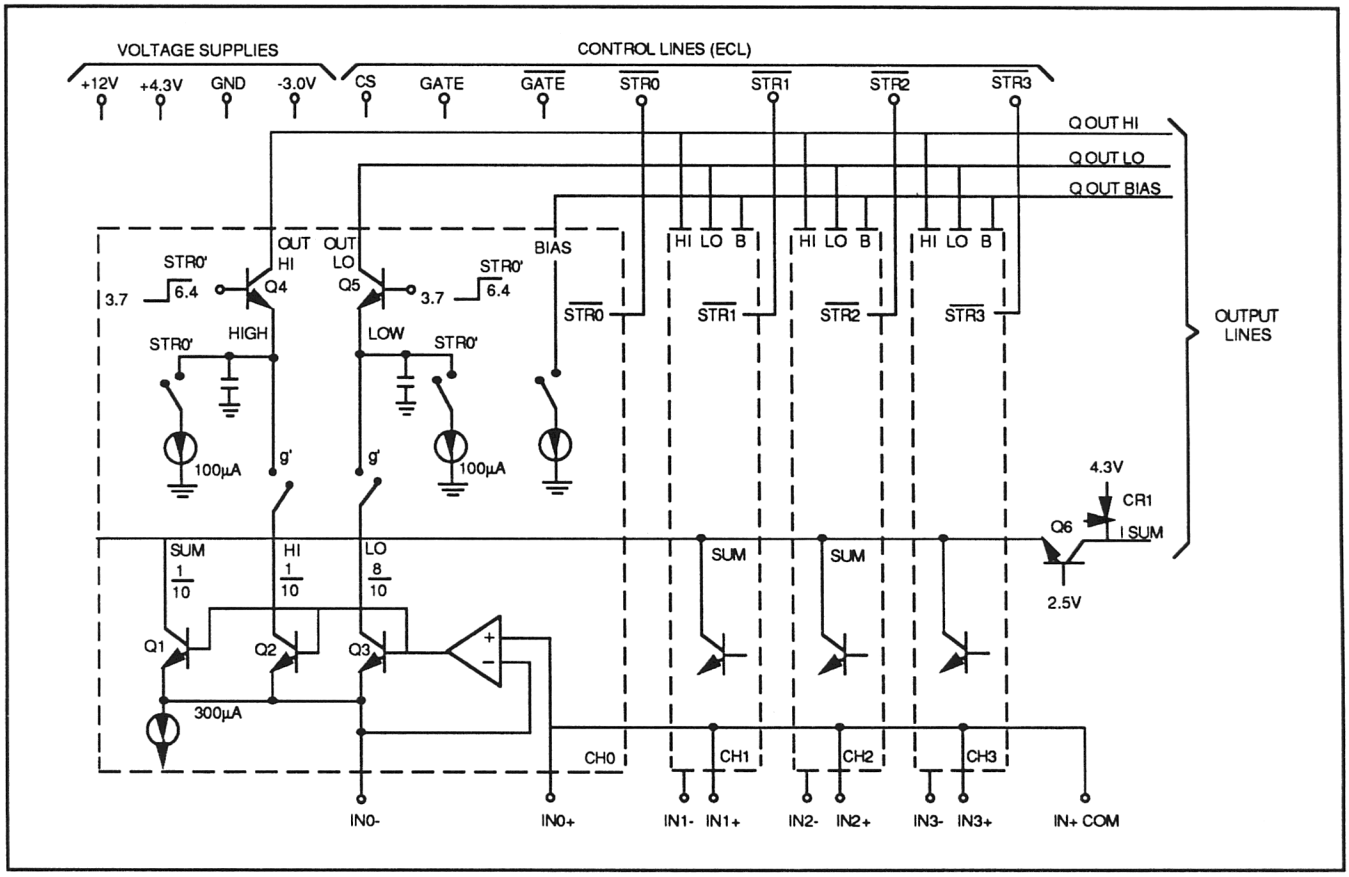


Figure 16
MIQ401 Equivalent Circuit

Each channel input has an amplifier which is used to provide a current sensitive, virtual ground inverting input and a voltage sensitive non-inverting input. The amplifier drives the inverting input to follow the voltage seen on the non-inverting input. The inverting input can source up to 30 mA and sink up to 0.2 mA in order to follow the non-inverting input and still meet the linearity specification. The designer ensures that an overshoot on the unipolar input pulse does not exceed the 0.2 mA limit, to avoid a non-linear measurement.

The input signal for each channel is split inside the MIQ401 into three parts in the ratio 8:1:1. 1/10 of the input of all 4 channels is summed together before any gating and routed to the ISUM pin to be used for fast triggering. The other 8/10 signal and 1/10 signal are gated and integrated on separate internal capacitors of the same size. When the capacitor receiving 8/10 (low range) of the signal is in overflow, the capacitor receiving only 1/10 (high range) of the signal is only 1/8 full scale. When the module is in autoranging mode it checks to see if the low range is in overflow. If it is, it selects the high range output (Q_OUT_HI) to be digitized. Otherwise, the low range output (Q_OUT_LO) is digitized. By this technique a dynamic range of 15 bits is achieved using 12-bit resolution digitizing. A bias current also is output along with the signal current. This is done to insure that the signal charge is output very quickly (to within 12-bit accuracy in 600 nsec). A bias current output (Q_OUT_BIAS) which may be used to subtract the bias current coming out with the signal, also is supplied. When this output is used to make the correction, negligible temperature dependence will result.

TIME-TO-CHARGE CONVERSION

In the 1872A/75A, the normal QMUX inverting inputs are connected to a switchable current source. The current is jumper selectable according to the desired resolution (2 mA maximum). The non-inverting inputs are grounded. Prior to a COM, the current is switched off. Arrival of the COM closes the gate switch and 35 nsec later, switches on the current to the inverting inputs of all QMUXes. Arrival of a hit switches off the current to the hit channel and integration steps. A full scale timeout switches off the current to all channels and then opens the gate switch.

MULTIPLEXING AND CONVERSION

A conversion cycle is triggered after a fixed delay time following the trailing edge of the TIMEOUT (usually about 10 μsec). This delay time, MPI, may be adjusted via a time port (R14) under the side cover. Alternatively, the module may be programmed via CSR#0 to accept the start conversion signal from the FASTBUS backplane (pin B51, ECL, triggered on high to low transition). Since the conversion timing is all synchronized with the module's clock, and the stop is presumably asynchronous, the actual start of the conversion cycle will vary randomly within a 50 nsec window with respect to the STOP trailing edge (see Figure 17).

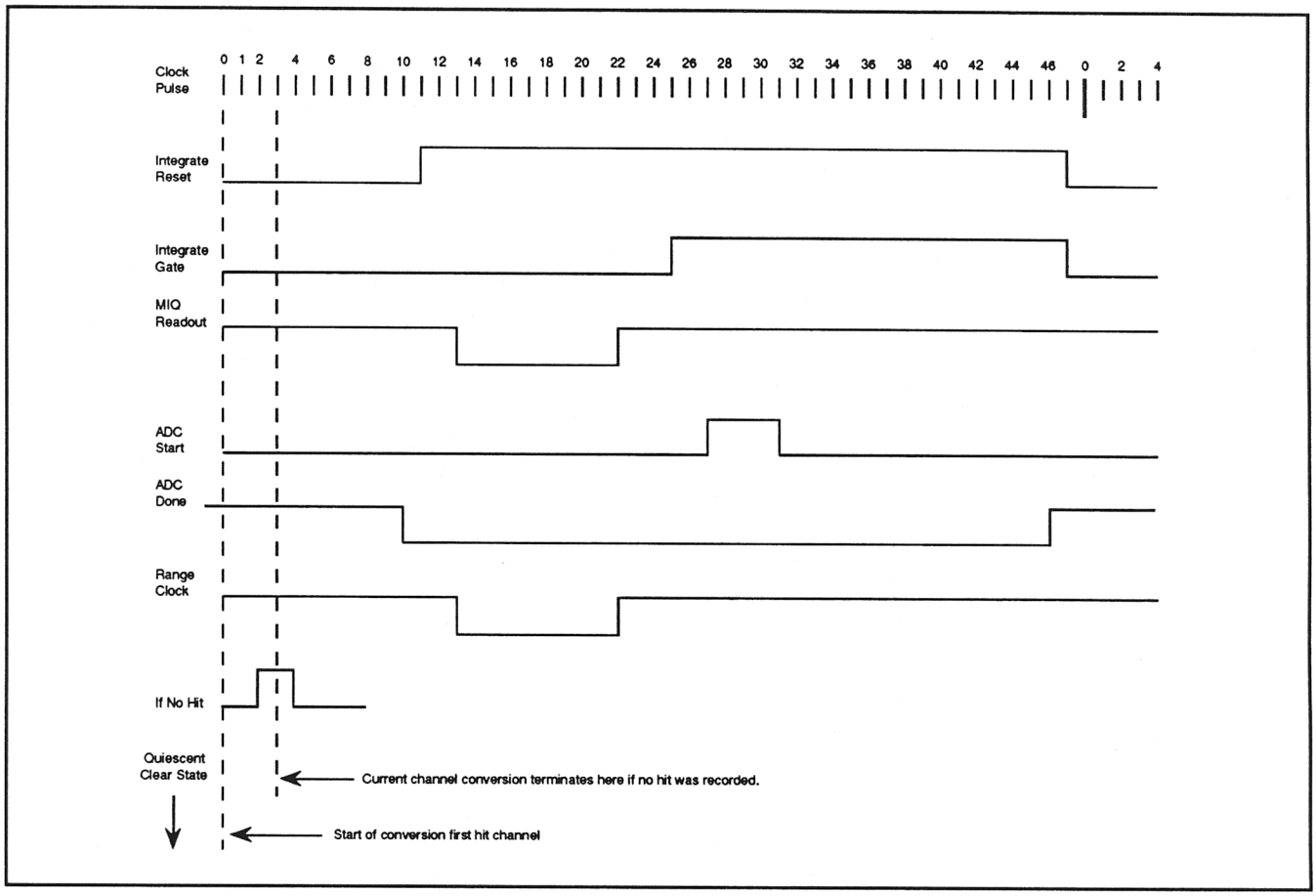


Figure 17
1872A/1875A Timing Diagram

The hit channels are converted sequentially. There are three common output buses to which the analog outputs of all 16 MIQ401s are connected. The three buses are the Q_OUT_LO, Q_OUT_HI, and Q_OUT_BIAS buses. Charge from a low ranged channel is read out via the Q_OUT_LO bus, along with a bias current of approximately 100 μA. Similarly, the high range charge is accessed via the Q_OUT_HI bus with a bias current of the same value. A bias current alone, which is well matched to the bias current used for strobing out the charge for the high and low ranges, is read via the Q_OUT_BIAS bus.

The converter circuit consists of the following circuit blocks:

Q_OUT BUS INTERFACE

This is the input to the converter. It takes the signals in off the three charge buses and outputs to the three integrators. The main function of this circuit is to provide a low input impedance into the converter in order to get the charge off of the highly capacitive bus as quickly as possible. That is, it isolates the capacitance of the buses from the remainder of the conversion circuit — in particular, the feedback loop of the integrators. It also defines the voltage of the output buses since the outputs of the MIQ401s are all open collectors. Clearing is effectively the simultaneous strobing out of all 64 channels, and therefore may cause very large instantaneous currents to be fed into the charge buses. This circuit handles the current surge produced by clearing.

INTEGRATORS

The current outputs to the charge buses are integrated by three high speed precision integrators, one for each bus. It is here that the charge integrated by the front end is finally converted to a voltage. The Low Range Integrator and High Range Integrator integrate the currents seen on the Q_OUT_LO and Q_OUT_HI buses respectively. The Bias Integrator takes the bias current put on the Q_OUT_BIAS bus by the MIQ401, converts it to a voltage and then uses capacitors to convert the voltage back into charge. This charge is injected into the input of the low and high range integrators to effectively subtract the bias current from the integrated high and low range integrals.

The integrators also act to hold the resultant voltage steady during digitizing, thus eliminating the need for a sample-and-hold before the ADC. To aid in this function and to eliminate noise that might be generated on the charge bus, the input to each integrator is gated off with a FET switch after the integration period.

Immediately before strobe-out of the next channel, the integrators are reset with FET switches. The use of monolithic quad FETs and the bias integrator helps in cancelling out effects of the charge injected by the gate drivers of the hold and reset FETs. The integration period for the integrators overlaps both edges of the control pulses going to the front-end MIQ401s, so the net injected charge due to the control pulses is negligible.

RANGE SELECT (1875A only)

In autorange mode (controlled by CSR0) a comparator monitors the output of the low range integrator. If the output voltage of the low range integrator is sensed to be above the crossover point (which can be set by a potentiometer) then the high range integrator output will be connected to the ADC. The low range integrator output is connected to the ADC in default.

In fixed mode, either the low or the high range integrator is connected to the ADC while all 64 channels are digitized. The range selected during fixed mode is controlled via CSR0. For a single event in fixed mode, therefore, all channels *must be digitized* with the same range.

The range bit from this circuit is latched into the TDC result register with the data, for storage in the data memory for readout by user.

3X AMPLIFIER AND LEVEL SHIFTER

This circuit supplies an additional gain of three to the voltage from the selected integrator. It eliminates the DC offset that exists on the integrator outputs and gives a signal voltage which ranges between 0 and 5 V, (the input range to the ADC chip). This amplifier output also acts as a buffer to the ADC input.

CALIBRATION

The 1872A/75A is adjusted to at the factory for nominal 25 psec/50 psec/ 100 psec resolutions.

R24 can be used to make small adjustments to the current source feeding the MIQ401 integrating capacitors. This consequently adjusts resolution independent of pedestal.

R38 adjusts the pedestal of both the low and high ranges, and has some effect on the gain.

The suggested techniques for more precise adjustment is to adjust R38 for high range pedestal first, without disturbing the gain. Then adjust the gain, or resolution, to the desired values using R24.

6 ADDITIONAL INFORMATION

BACKPLANE AUXILIARY CONNECTOR (AFC - Aux. FASTBUS Connector)

Fast Control Signals

Both buffered differential COM and CLEAR signals are routed to the upper rear panel connector (AFC) for event control synchronization of trigger electronics. Also provided is a so-called PC strobe (PCSTR) which is a buffered version of the FASTBUS backplane TR4 line. This is an uncommitted control line which may be used for unique trigger control functions.

User CSR Data Bus

Address, data and control lines are provided for user-implemented CSR registers on the AFC. Addressing is provided for sixteen 8-bit read/write registers. The FASTBUS addresses for these registers range from $C0000000_{16}$ to $C0000000F_{16}$. The signals are listed below.

D<7:0>	Eight user CSR data lines
A<3:0>	Four decoded user CSR address lines
W/R*	Read/write, direction of transfer
WR_STRB	Write strobe supplied to AFC
NA	Not available. User should return this high when the addressed register is not implemented.

In order to access these registers after addressing the module to CSR Space the user must then write the required Secondary Address (MS=2). The Secondary Address selects the user CSR register which will be accessed on successive random data cycles. When these registers are read back, the data are contained in the low order 8 bits. The Geographical Address of the module is contained in the high order 5 bits.

AFC Voltages

All voltages on the module are fed to the AFC via the Auxiliary FASTBUS connector. There are ground, -2, -5.2, +5, -15, and +15 pins.

AFC T-Pin Assert Broadcast

The 1872A/75A modules implement a Broadcast mode in which all modules that have a "trigger" should assert the T-pin. The Broadcast code for this is ED_{16}.

If the user wishes to use this option he must pull down the TRIG (A53) pin on the AFC if a valid trigger condition exists. If this line is low the module will assert the T-pin on this broadcast. When this line is not used it floats high in the module, pulled up by a 5.1 kΩ resistor.

TRIGGER OUTPUTS

The 64 trigger outputs are terminated on-board by 2.2K to -5.2 V. This causes correct levels on the lines for slow testing. However, in order to properly terminate these lines, when used, a 100 Ω termination to -2 V for each line is required on the trigger card. The 2.2K may be left connected.

The trigger outputs are active low ECL signals. For channels with data, they go true (low) at the beginning of the MPI and are valid for the duration of the MPI. After the MPI the trigger outputs will begin changing and are no longer valid.

FRONT PANEL DIMENSIONS

Figure 19 shows the pertinent dimensions for the front panel of the 1872A/75A module, which may be helpful to a user who wishes to build his own input paddle cards.

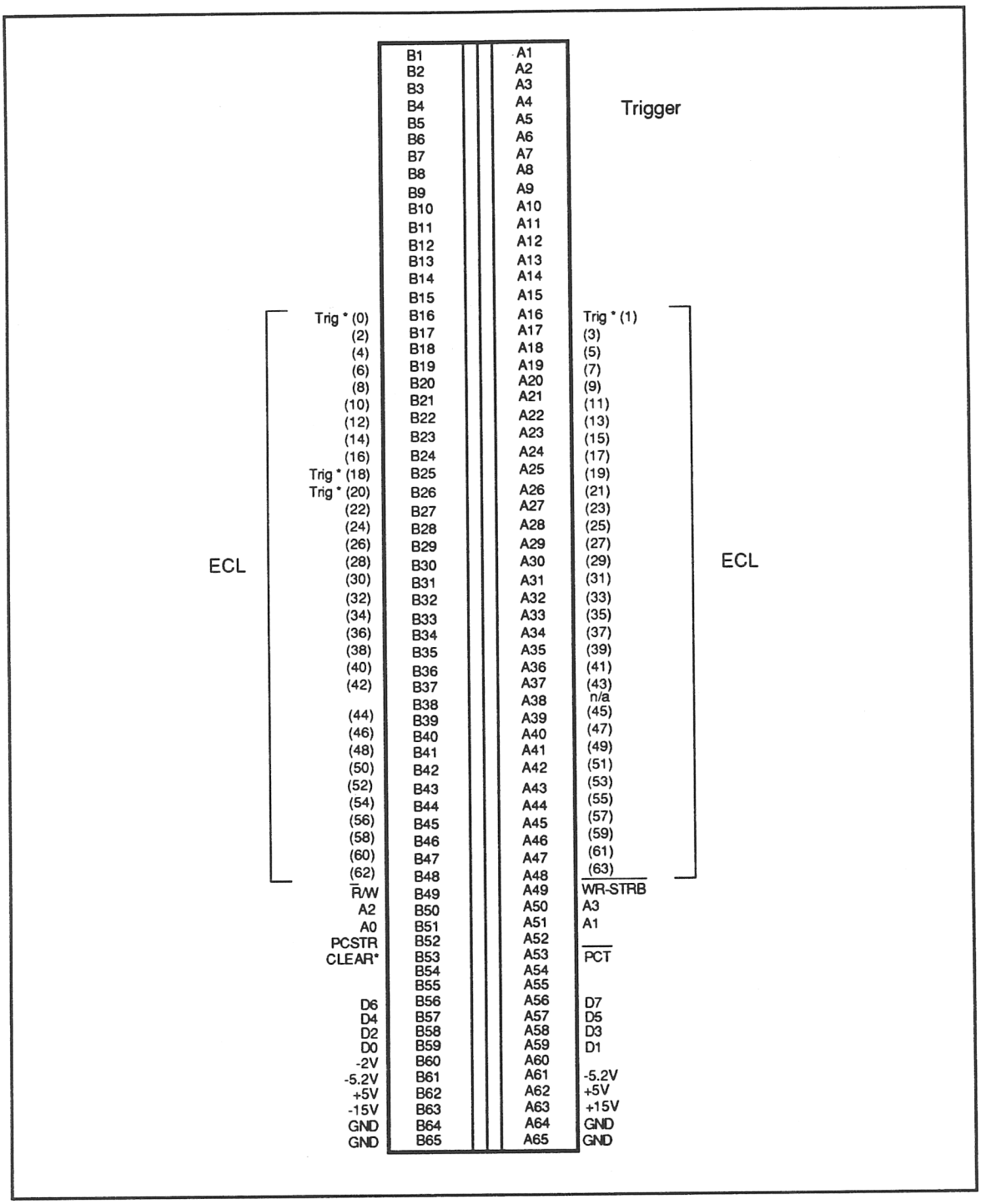


Figure 18
1872A/75A Auxiliary Connector

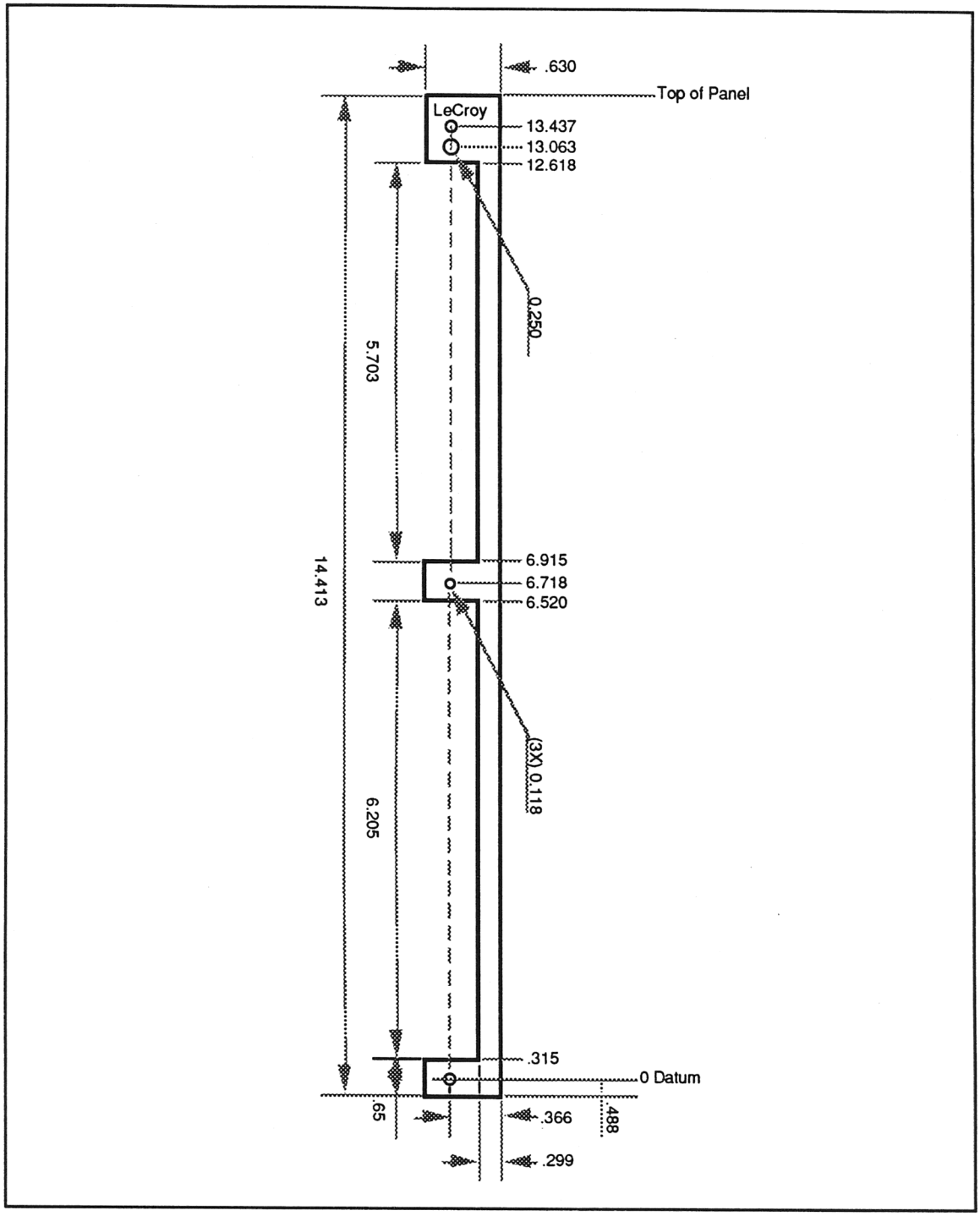


Figure 19
1872A/75A Front Panel

INDEX

Acquisition Timeout 3-3
Active Channel Depth 4-19
AFC T-Pin Assert Broadcast 6-1
AFC T-Pin Assert CD 4-17
AFC Voltages 6-2
Analog Inputs 3-1
Ancillary Logic 3-1
Autorange 4-1
Auxiliary Connector 6-1, 6-2
Auxiliary Function Card (AFC) 4-10, 6-1

Bit Type Definitions 4-6

Calibration 5-5
Chapter Organization 4-1
Checkout Using the Test Pulse and the LeCroy Model 1810 CAT 4-4
Clear 3-3, 4-6, 4-7
Coax Cables 3-1
COM 3-2
Control Bits 4-7
Control Signal Inputs 3-2
Conversion Event Counter (CEC) 4-15, 4-18
Conversion in Progress (CIP) and Wait 4-16
Crate Master 3-1
CSR0 4-6
CSR0 Read 4-8
CSR0 Write 4-6
CSR1 4-18

Data Word 4-9
DEC DR11-W 3-1
Depth Field 4-19
Digital Clear 4-6, 4-7
Disable Autorange 4-6, 4-7
Disable Test Pulse 4-6, 4-7
Disable Wait 4-6, 4-7

Enable Autorange 4-6, 4-7
Enable Test Pulser 4-6, 4-7
Enable Wait 4-6, 4-7
Equipment Needed 3-1
Event Number 4-9

F Mode Operation 4-15
F Mode Readout Schemes 4-20, 4-24, 4-28, 4-32
Fast Control Signals 6-1
FASTBUS 2-1
FASTBUS Backplane 3-2, 3-3
FASTBUS Backplane TR4 Line 6-1
FASTBUS Backplane UR0 and UR1 4-3
FASTBUS Broadcast Functions 4-17
FASTBUS Line TR5 3-2
FASTBUS Specification 4-17
FET Switch 5-4
FIFO 4-15, 4-16
Front Panel Dimensions 6-1, 6-3
Full and Empty Conditions 4-15

General Broadcast 4-10, 4-17

Hits 3-3

Increment Event Counter 4-6, 4-7
Initial Checkout 4-1
Integrators 5-3
Internal Gate 4-7
Internal Data Buffer 4-15
Internal Test Pulsing and Readout 4-2

LIFT 3-1, 4-1

MDB DRV11-2 3-1
Measure Pause Interval (MPI) 3-3
MIQ401 - Input Monolithic 5-1, 5-2, 5-3
MPI 3-3
MPI Status 4-8
Multiplexing and Conversion 5-2

N Mode Compatibility with 1882/5N 4-10
N Mode Operation 4-10
N Mode Readout Scheme 4-11
N vs F Operating Modes 4-1
New Features 2-1

Other Features 2-1
Output Data Word 4-9
Overview 2-1

Pattern Select 09 4-17
Power-up 4-8
Power-up State 4-19
Power-up Status 4-8
Processor Interface 3-1
Pulsed Bits 4-7

Q_OUT Bus Interface 5-3

Range (1/0 = high/low) 2-1, 4-6, 4-8
Range Select 4-6, 5-4
Range Status 4-8
Read the Module ID and Mode 4-2
Readout Event Counter (REC) 4-15, 4-18
Reread 4-6, 4-7
Reread Function 4-6, 4-7
Reset 4-6, 4-7

S1 4-10
SDS Broadcast 4-15
Set COM 4-6
Set COM Backplane 4-6
Set MPI Internal 4-6
Set Range High, Low 4-6
Slave Status Responses 4-16
Sparse Data Scan (SDS) 4-10, 4-17, 4-18
SS=1 4-16
SS=2 4-16
SS=6 4-16
Standard Input Scheme 3-1

T-Pin 4-11
T-Pin Response 4-10
TDC Channel Number 4-9
TDC Geographical Address 4-9
TDC Pattern Select 9D 4-17
TDC Sparse Data Scan 9D 4-17
Test Pulser 4-7
Test Pulser Status 4-8
Time-to-Charge Conversion 5-2
TR (+) TR2 (-) Lines 3-2
TR0 Line 3-3
Trigger Outputs 3-3, 6-1
Twisted Pair Cables 3-1

Unpacking and Inspection 1-1
User CSR Data Bus 6-1
Using the Test Pulser 4-3

Wait 4-7
Wait Status 4-8
Warranty 1-1
Writing to FASTBUS Register CSR1 4-18

TECHNICAL INFORMATION

(PARTS LIST, SCHEMATICS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
1875A-COM	1875A + 1872A COMMON TDC BOARD	1
721875001	FRONT PANEL 1875A	1

End of report. 2 Details encountered.

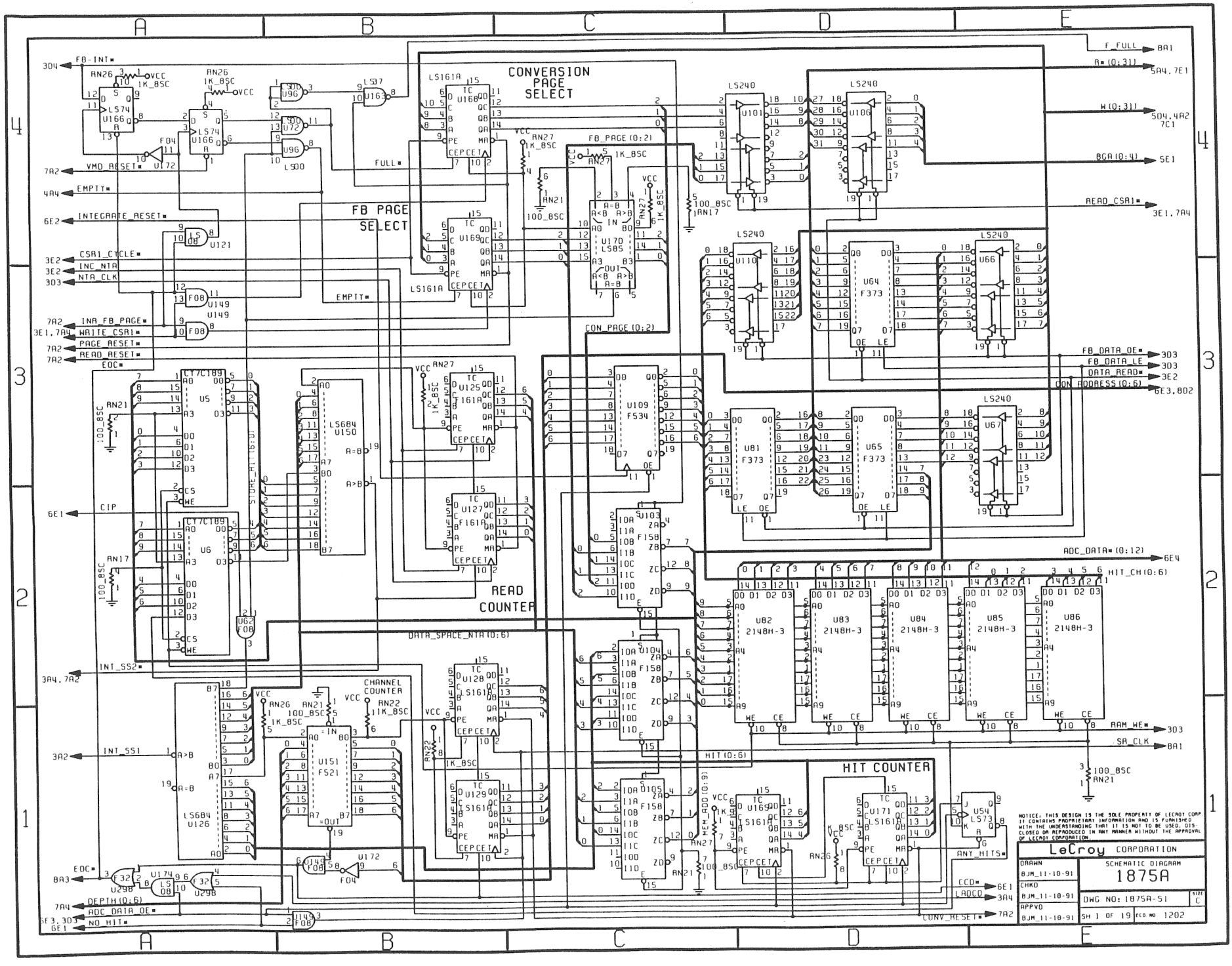
PART NUMBER	DESCRIPTION REMARK	QTY PER
106433100	CAP CERA MONO 10PF	7
106433101	CAP CERA MONO 100PF	6
106433150	CAP CERA MONO 15PF	1
106433181	CAP CERA MONO 180PF	1
106433271	CAP CERA MONO 270PF	2
106433561	CAP CERA MONO 560PF	64
106435102	CAP CERA MONO .001UF	67
106435103	CAP CERA MONO .01UF	67
106438104	CAP CERA MONO .1UF	258
116001910	CAP DIP MICA 1% 91 PF	6
141264476	CAP TANT DIP 10V 47 UF	39
141854685	CAP TANT DIP 6.8 UF	34
146424106	CAP MINI ALUM 20% 10 UF	52
161030000	RES COMP ZERO OHMS	1
161225047	RES CARBON FILM 4.7 OHMS	3
161225100	RES CARBON FILM 10 OHMS	6
161225101	RES CARBON FILM 100 OHMS	19
161225102	RES CARBON FILM 1 K	16
161225103	RES CARBON FILM 10 K	6
161225104	RES CARBON FILM 100 K	3
161225105	RES CARBON FILM 1 MEG	2
161225204	RES CARBON FILM 200 K	1
161225222	RES CARBON FILM 2.2 K	7
161225302	RES CARBON FILM 3 K	1
161225331	RES CARBON FILM 330 OHMS	16
161225391	RES CARBON FILM 390 OHMS	2
161225432	RES CARBON FILM 4.3 K	2
161225472	RES CARBON FILM 4.7 K	1
161225510	RES CARBON FILM 51 OHMS	11
161225511	RES CARBON FILM 510 OHMS	2
161225562	RES CARBON FILM 5.6 K	5
161225750	RES CARBON FILM 75 OHMS	4
161225751	RES CARBON FILM 750 OHMS	4
161335911	RES CARBON FILM 910 OHMS	1
161445750	RES CARBON FILM 75 OHMS	1
168139325	RES RN55E .1% 196 OHMS	3
168139373	RES RN55E .1% 619 OHMS	3
168139393	RES RN55E .1% 1.0 K	2
168139439	RES RN55E .1% 3.01 K	1
168139560	RES RN55E .1% 4.99 K	67
168531201	RES PREC RN55D 10.0 OHMS	2
168531341	RES PREC RN55D 287 OHMS	3
168531345	RES PREC RN55D 316 OHMS	1
168531362	RES PREC RN55D 475 OHMS	1
168531417	RES PREC RN55D 1.78 K	5
168531425	RES PREC RN55D 2.15 K	1
168531472	RES PREC RN55D 6.65 K	1
168531489	RES PREC RN55D 10.0 K	2
168531492	RES PREC RN55D 10.7 K	1
168531493	RES PREC RN55D 11.0 K	1
168531497	RES PREC RN55D 12.1 K	3
168531501	RES PREC RN55D 13.3 K	1

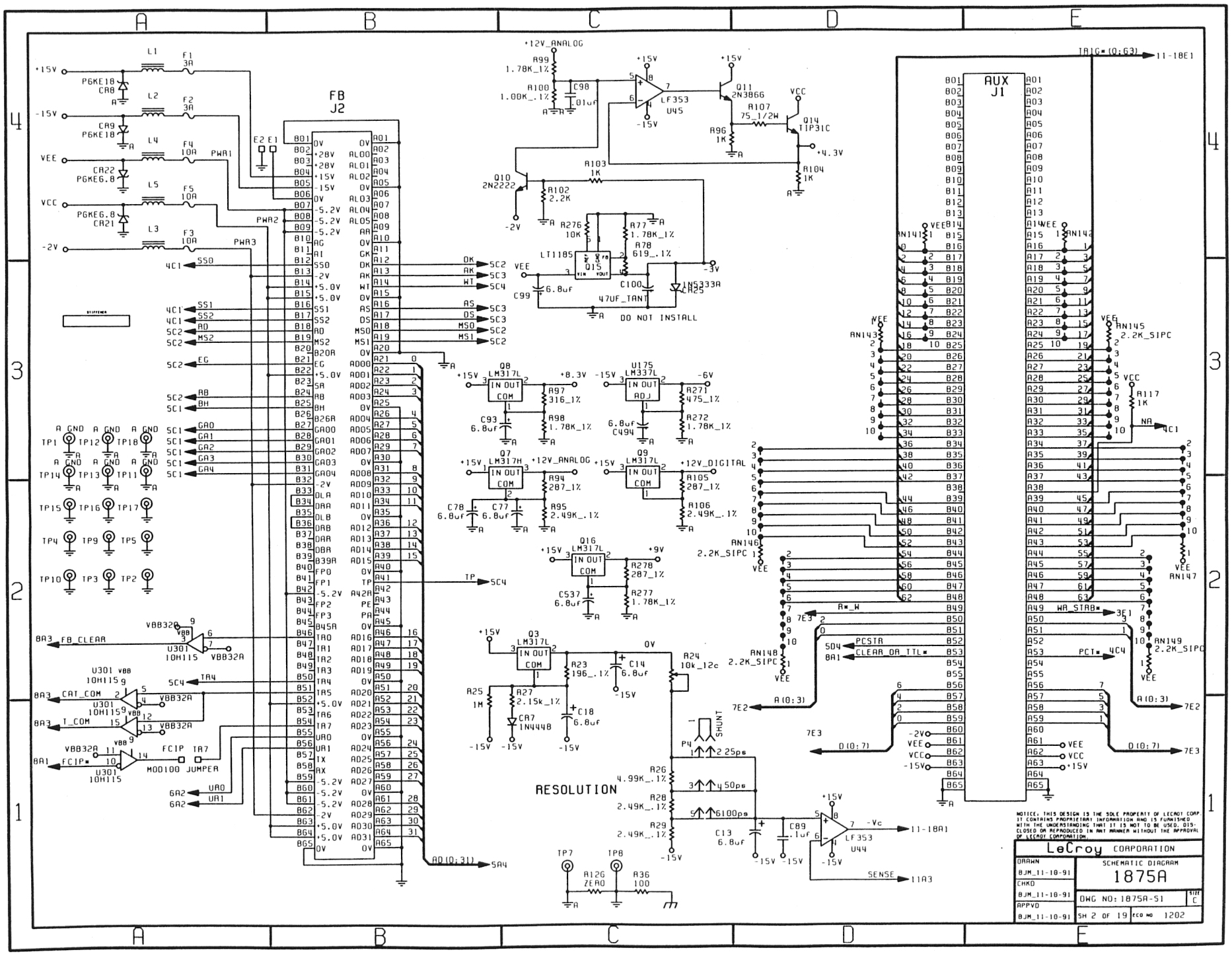
PART NUMBER	DESCRIPTION REMARK	QTY PER
168531511	RES PREC RN55D 16.9 K	1
168531518	RES PREC RN55D 20.0 K	3
168531521	RES PREC RN55D 21.5 K	1
168531529	RES PREC RN55D 26.1 K	2
168531535	RES PREC RN55D 30.1 K	1
168531537	RES PREC RN55D 31.6 K	1
168531542	RES PREC RN55D 35.7 K	4
168531547	RES PREC RN55D 40.2 K	1
168539431	RES PREC FILM .1% 2.49 K	6
180247102	RES VARI CERMET 1 K	3
180247103	RES VARI CERMET 10 K	2
181457504	RES VARI CERMET 500 K	1
190042101	RESISTOR NETWORK 100 OHMS	4
190042102	RESISTOR NETWORK 1 K	4
190042222	RESISTOR NETWORK 2.2 K	8
190052221	RESISTOR NETWORK 220 OHMS	1
190642101	RESISTOR NETWORK 100 OHMS	33
190642560	RESISTOR NETWORK 56 OHMS	2
190662101	RESISTOR NETWORK 100 OHMS	1
190662560	RESISTOR NETWORK 56 OHMS	44
190832100	RESISTOR NETWORK 10 OHM	17
190832101	RESISTOR NETWORK 100 OHMS	16
190842101	RESISTOR NETWORK 100 OHMS	31
190842102	RES NETWORK 1 K	9
200031028	IC 2-INPUT NAND SN74LS00N	6
200031049	IC D-TYP FLOP SN74LS74N	5
200031073	IC 2-IN POS OR SN74LS32N	2
200031074	IC POS-NAND BUF SN74LS37N	1
200031086	IC 2-INPUT AND SN74LS08N	4
200031088	IC J-K FLOP SN74LS73N	4
200041026	IC 4-BIT CTR SN74LS161N	6
200041027	IC QUAD SEL/MP SN74LS157N	1
200041033	IC D-TYP FLOP SN74LS174N	1
200041043	IC 4-BIT MAGNIT SN74LS85N	1
200041044	IC MULTIVIBR SN74LS123N	1
200041062	IC DEC/DEMULTP SN74LS138N	3
200071001	IC 8 X BUFFER SN74LS240	10
200071005	IC D-TYP FLOP SN74LS273N	2
200071007	IC BUFFER SN74LS244N	1
200071534	IC D-TYP FLOP 74LS534N	2
200330000	IC 2-INPUT NAND 74F00	2
200330002	IC 2-IN NOR GATE 74F02	2
200330004	IC FAST HEX INV 74F04	2
200330008	IC 2-INPUT AND GATE 74F08	2
200330020	IC 4-IN NAND GATE 74F20	2
200330032	IC 2-INPUT OR 74F32	4
200330086	IC EX-OR GATE 74F86	1
200330260	IC 5-IN NOR GATE 74LS260	3
200340074	IC D-TYPE POS FLOP 74F74	4
200340130	IC DUAL LATCH MC10H130	1
200340138	IC 1-OF-8 DECODER 74F138	1
200340211	IC 3-IN/3-OUT NOR 10H211	2

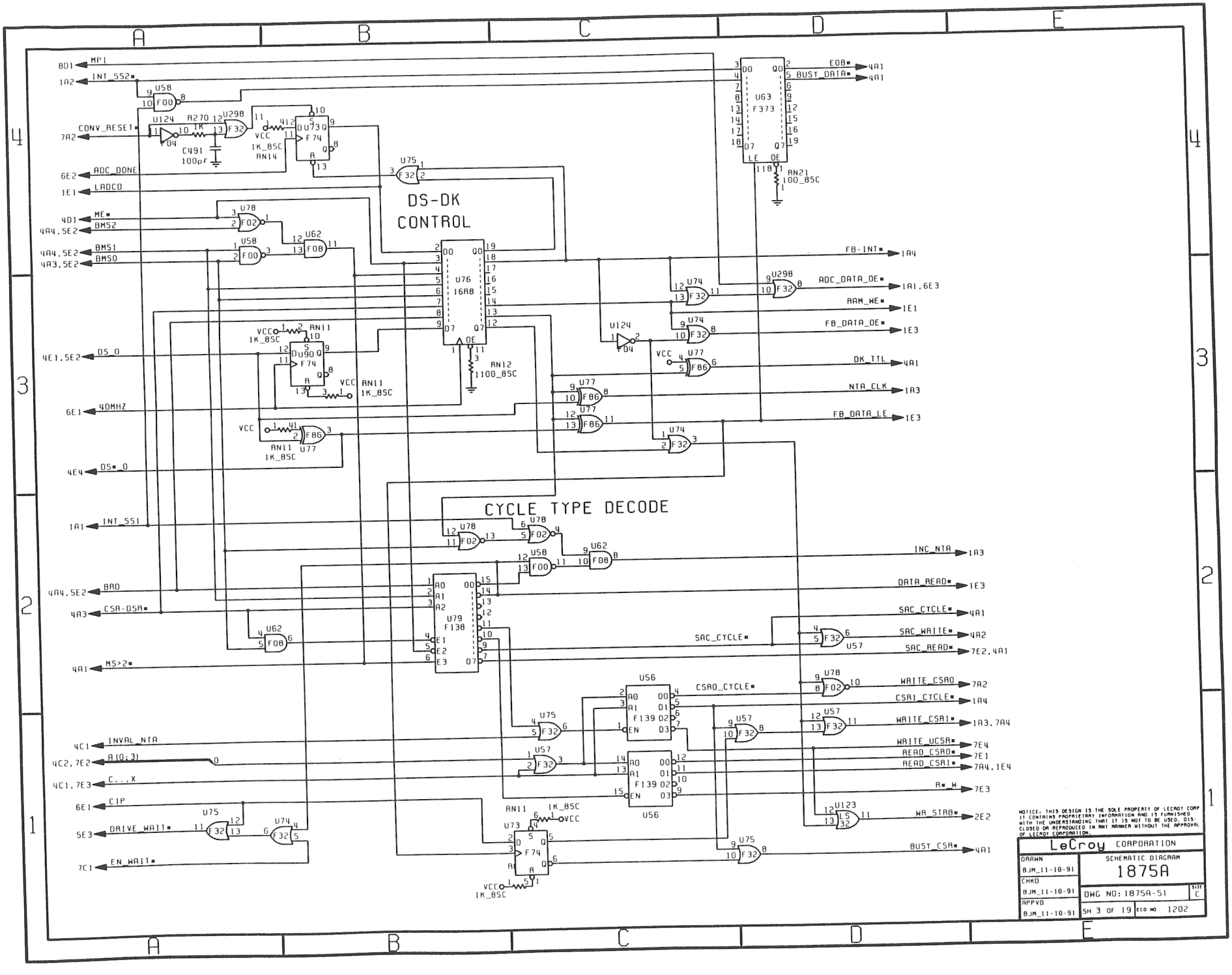
PART NUMBER	DESCRIPTION REMARK	QTY PER
200341210	IC OR GATE 10210	3
200344104	IC QUAD 2-IN NAND 10H104	2
200344131	IC DUAL D M-S FLOP 10H131	33
200370534	IC FAST D FLOP 74F534	1
200371273	IC OCTAL D-FLOP 74F273	1
200440002	IC MONOST MULTIVIB 96LS02	2
200441161	IC 4-BIT COUNTER 74F161	4
200570521	IC 8BIT COMPARATOR 74F521	2
200570684	IC 8BIT MAGN COMP 74LS684	2
200670373	IC LATCH 74F373PC	5
204042001	IC 4-5 OR/NOR GT MC10109P	1
204042007	IC QUAD TRANSL MC10124P	15
204042008	IC QUAD TRANSL MC10125P	11
204042015	IC LINE RECEIVER MC10114P	24
204042016	IC 2-INPUT OR/NOR F10101P	2
205242189	IC 64-BIT STAT RAM CY7C189	2
205260148	IC 1024X4 BIT RAM 2148H-3	5
205680341	IC 8-BIT SHIFT REG 100341	8
205740016	IC PAL 16L8	1
205751168	IC PAL 16L8D	1
205759016	IC 16-IN AND-OR 16R8D	1
207244124	IC QUAD TTL-MECL 10H124	3
207244125	IC QUAD MECL-TTL 10H125	2
207280750	IC MONO A/D CONVERTER 671KD750	1
207340139	IC DECODER/DEMUX 74F139	1
207340158	IC FAST 2-IN MPX 74F158	3
207444115	IC QUAD LINE RCVR 10H115	2
207444116	IC TRIPL LINE RCVR 10H116	2
208011004	IC TIMER NE555	1
208033001	IC TRANS ARRAY CA3046	1
208043000	IC 4X FET SWITCH SD5000	3
208110353	IC DUAL OP AMP LF353N	3
208160586	IC VOLT REFERENCE AD586JQ	1
208212843	IC CBFET OP AMP AD843JN	5
208230102	IC DUAL DIFF AMPLIFIER 3102	32
208510317	IC ADJ +V REG 317LZ	4
208590185	IC LOW DROPOUT NEG REG LT1185CT	1
208590317	IC ADJ +V REG 317H	1
208590337	IC VOLT REG NEG ADJ LM337	1
208610360	IC HI-SPEED VOLT COMP 360	1
229020055	TRANS VOLT SUPPR P6KE6.8	2
229020145	TRANS VOLT SUPPR P6KE18	2
230110005	DIODE SWITCHING 1N4448	11
253010800	DIODE SCHOTTKY HP2800	2
256432212	DIODE LED (YEL) TIL211-1	1
270110001	TRANSISTOR NPN PN2369A	4
270110003	TRANSISTOR NPN PN2222A	3
270140001	TRANSISTOR NPN 2N3866	1
271130002	TRANSISTOR NPN PWR TIP31C	1
275170906	TRANSISTOR PNP 2N3906	1
280170104	TRANSISTOR FET N VN0104N3	1
290142020	DELAY LINE 20 NS	1

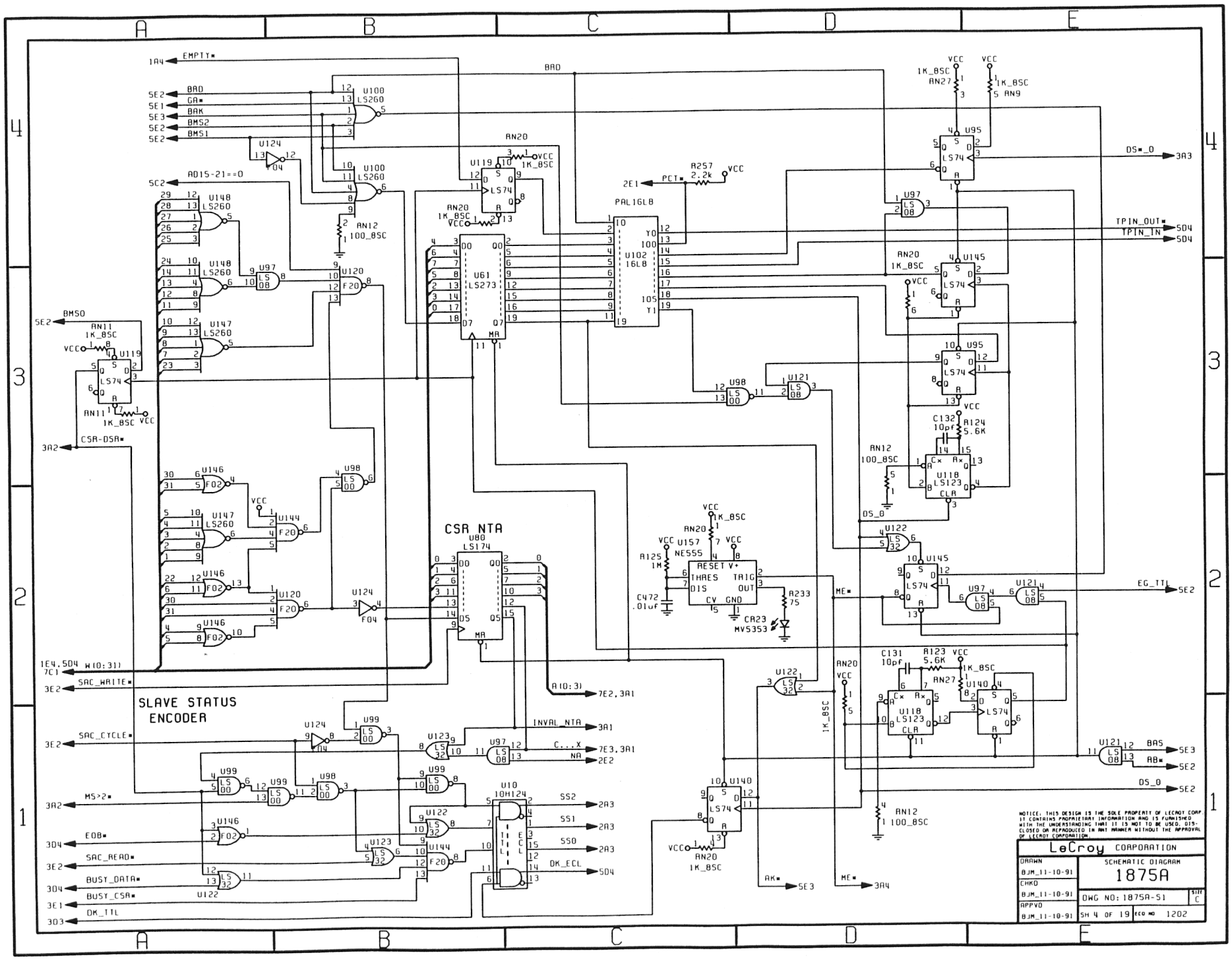
PART NUMBER	DESCRIPTION REMARK	QTY PER
300050001	CHOKE FERRITE SINGLE LEAD	5
309040040	CRYSTAL OSCILLATOR 40MHZ	1
377101006	LABEL TEMP MONITOR 150F	1
400030016	SOCKET IC SOLD TAIL DIP-16	3
400321014	SOCKET IC SOLD TAIL DIP-14	1
400331020	SOCKET IC SOLD TAIL DIP-20	3
400810024	TERMINAL CARRIER DIP-24	16
403119234	HDR DBL ROW RT ANGL 34	4
403181002	HDR SINGL ROW STRAIGHT 2	3
403181003	HDR SINGL ROW 3	18
405764116	SOCKET SINGLE WIRE 16-POS	2
405764121	SOCKET SINGLE WIRE 21-POS	2
419111003	SWITCH SLIDE (SINGLE)SPST	1
433220001	FUSE PICO II 125V 10 AMP	3
433220002	FUSE PICO II 125V 3 AMP	2
454370002	SHUNT 2 POS	16
454713006	HDR SOLD TAIL/MALE 6	1
454720130	HDR SOLD TAIL/FEM 130	2
468099008	TEST POINT W/GLASS INSULATOR	18
500120002	TRANSIPAD "LARGE"	2
505070002	HEAT SINK FOR TO-220	1
519230002	SNAP RIVET NYLON	1
524440020	STANDOFF SWAGED 4-40X.360	6
540303002	SIDE COVER FASTBUS (LEFT)	1
540305001	MOUNTING BLOCK FASTBUS #1	3
540307020	STIFFENER FOR FASTBUS	1
555083374	THUMB NUT(CUSTOM).374 DIA	2
559440004	SCREW 4-40 SLOTTED 1/4"	12
559440005	SCREW SLOT PAN 4-40X5/16	3
560440014	SCREW PHILIPS 4-40X7/8	2
567440004	SCREW FLAT PHIL 4-40X1/4	9
568440003	SCREW FLAT PHIL 4-40X3/16	1
575201006	WASHER FLAT TEFLON #4	3
597000100	SHIPPING CARTON (FASTBUS PAD)	1
711872101	PC BOARD PREASS'Y 1872A	1
MIQ401	QUAD QMUX	16
MVL407	MULTI-CH MONO DISC	1

End of report. 193 Details encountered.


CONVERSION PAGE SELECT
FB PAGE SELECT
READ COUNTER
CHANNEL COUNTER
HIT COUNTER
F_FULL
A=(0:31)
W(0:31)
BCA(0:4)
READ_CSR1=
FB_DATA_OE=
FB_DATA_LE
DATA_READ=
CON_ADDRESS(0:6)
ADC_DATA=(0:12)
HIT_CH(0:6)
RAM_WE=
SR_CLK
ANY_HITS
CCD=
LADCO
CONV_RESET=
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 1 OF 19
ECO NO 1202


FB
J2
AUX
J1
RESOLUTION
DO NOT INSTALL
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DRAWN
BJM_11-10-91
CHKD
BJM_11-10-91
APPVD
BJM_11-10-91
DWG NO: 1875A-S1
SIZE C
SH 2 OF 19
ECO NO 1202


DS-DK CONTROL
CYCLE TYPE DECODE
MPI
INT_SS2*
CONV_RESET*
ADC_DONE
LADCD
ME*
BMS2
BMS1
BMS0
DS_0
40MHZ
DS*_0
INT_SS1
BRD
CSR-DSR*
MS>2*
INVAL_NTA
A(0:3)
C...X
CIP
DRIVE_WAIT*
EN_WAIT*
EOB*
BUSY_DATA*
FB-INT*
ADC_DATA_OE*
RAM_WE*
FB_DATA_OE*
DK_TTL
NTA_CLK
FB_DATA_LE
INC_NTA
DATA_READ*
SAC_CYCLE*
SAC_WRITE*
SAC_READ*
CSR0_CYCLE*
WRITE_CSR0
CSR1_CYCLE*
WRITE_CSR1*
WRITE_UCSR*
READ_CSR0*
READ_CSR1*
R*_W
WR_STRB*
BUSY_CSR*
U76 16R8
U79 F138
U56 F139
U63 F373
U123 LS32
U124 F04
U90 F74
U73 F74
U75 F32
U74 F32
U77 F86
U78 F02
U58 F00
U62 F08
U57 F32
U298 F32
RN11 1K_8SC
RN12 1100_8SC
RN14 1K_8SC
RN21 100_8SC
C491 100pf
R270 1K
VCC
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 3 OF 19
ECO NO 1202



SLAVE STATUS ENCODER
CSR NTA
U80 LS174
U61 LS273
PAL16L8
U102 16L8
U10 10H124
U157 NE555
U118 LS123
U95 LS74
U100 LS260
U148 LS260
U147 LS260
U146 F02
U144 F20
U120 F20
U124 F04
U97 LS08
U98 LS00
U121 LS08
U122 LS32
U145 LS74
U140 LS74
U99 LS00
U123 LS32
U119 LS74
U124 F04
EMPTY*
BRD
GA*
BAK
BMS2
BMS1
AD15-21==0
BMS0
CSR-DSR*
W(0:31)
SAC_WRITE*
SAC_CYCLE*
MS>2*
EOB*
SAC_READ*
BUSY_DATA*
BUSY_CSR*
DK_TTL
A(0:3)
INVAL_NTA
C...X
NA
SS2
SS1
SS0
DK_ECL
PCT*
DS*_0
TPIN_OUT*
TPIN_IN
DS_0
EG_TTL
ME*
AK*
BAS
RB*
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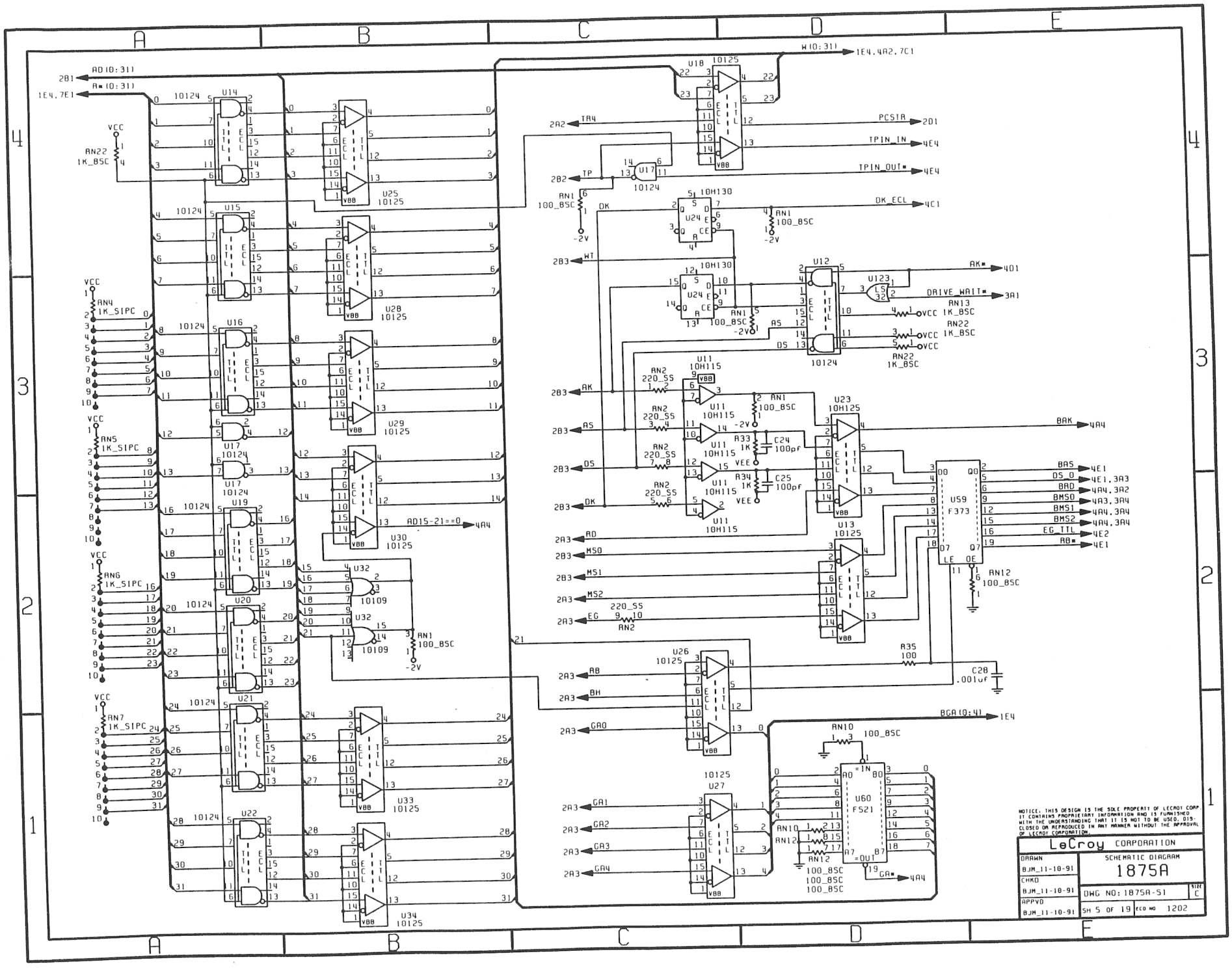
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 4 OF 19
ECO NO 1202



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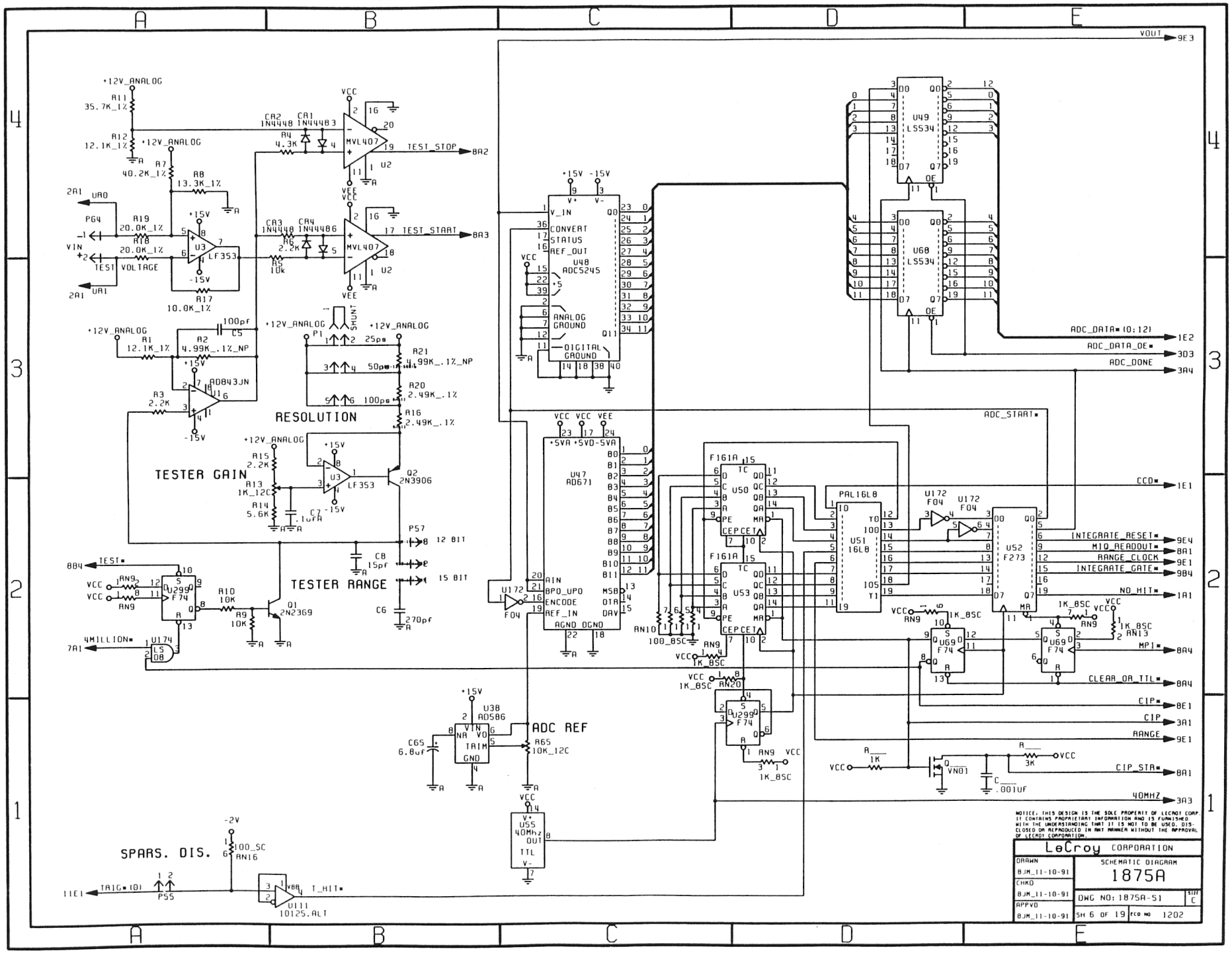
LeCroy CORPORATION

DRAWN BJM_11-10-91	SCHEMATIC DIAGRAM 1875A
CHKD BJM_11-10-91	DWG NO: 1875A-S1 SIZE C
APPVD BJM_11-10-91	SH 5 OF 19 ECO NO 1202



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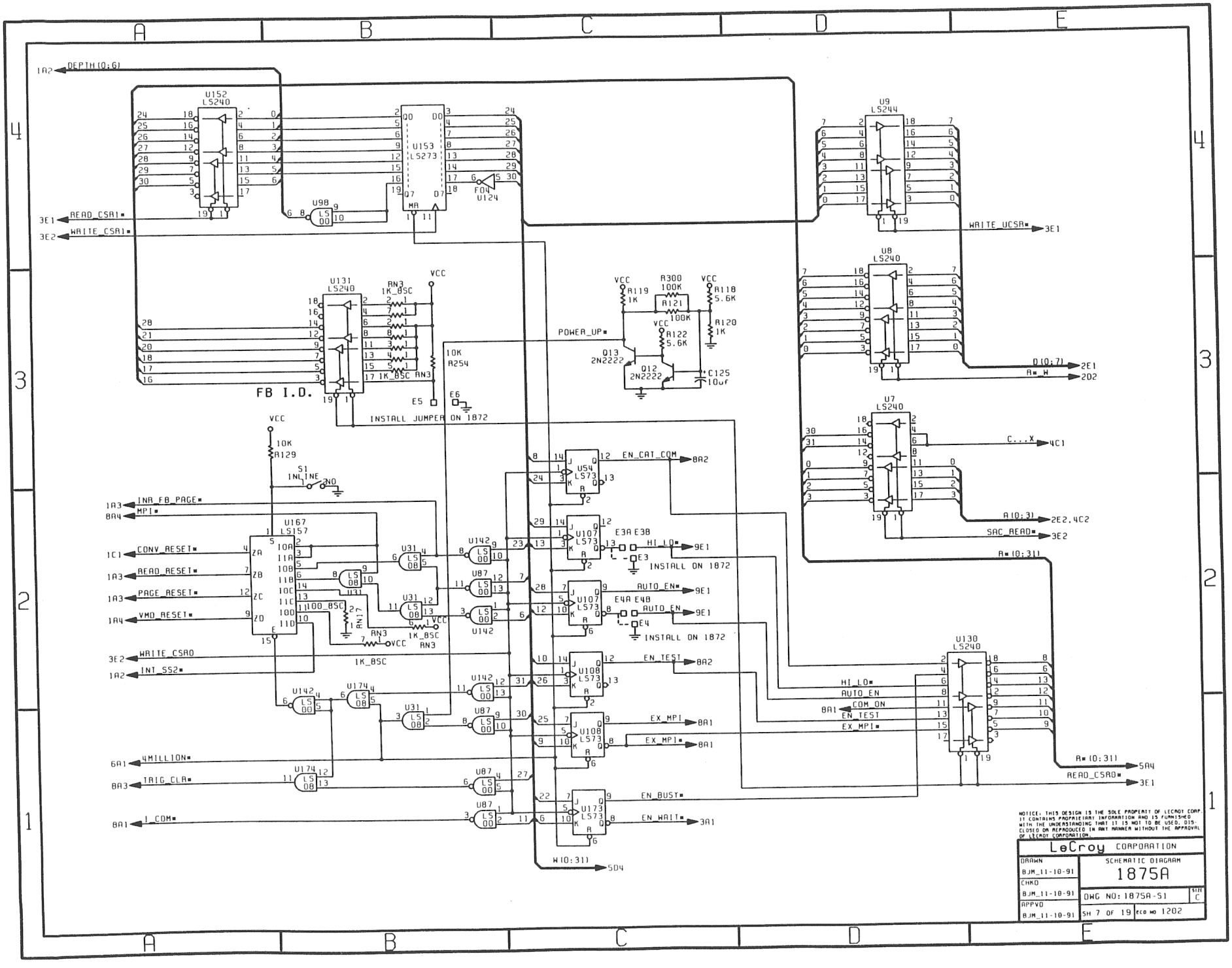
LeCroy CORPORATION		
DRAWN BJM_11-10-91	SCHEMATIC DIAGRAM	
CHKD BJM_11-10-91	1875A	
APPVD BJM_11-10-91	DWG NO: 1875A-S1	SIZE C
	SH 6 OF 19	ECO NO 1202


DEPTH(0:6)
U152 LS240
U153 LS273
U98 LS00
READ_CSR1*
WRITE_CSR1*
U131 LS240
RN3 1K_BSC
FB I.D.
INSTALL JUMPER ON 1872
VCC
10K R254
R300 100K
R119 1K
R121 100K
R118 5.6K
R120 1K
R122 5.6K
POWER_UP*
Q13 2N2222
Q12 2N2222
C125 10uf
U9 LS244
WRITE_UCSR*
U8 LS240
D(0:7)
R*_W
U7 LS240
C...X
A(0:3)
SAC_READ*
A*(0:31)
10K R129
S1 IN_LINE
INA_FB_PAGE*
MPI*
U167 LS157
CONV_RESET*
READ_RESET*
PAGE_RESET*
VMO_RESET*
100_BSC
WRITE_CSR0
INT_SS2*
U54 LS73
EN_CAT_COM
U107 LS73
HI_LO*
AUTO_EN*
AUTO_EN
INSTALL ON 1872
U108 LS73
EN_TEST
EX_MPI*
U173 LS73
EN_BUST*
EN_WAIT*
W(0:31)
U130 LS240
COM_ON
READ_CSR0*
4MILLION*
TRIG_CLA*
I_COM*
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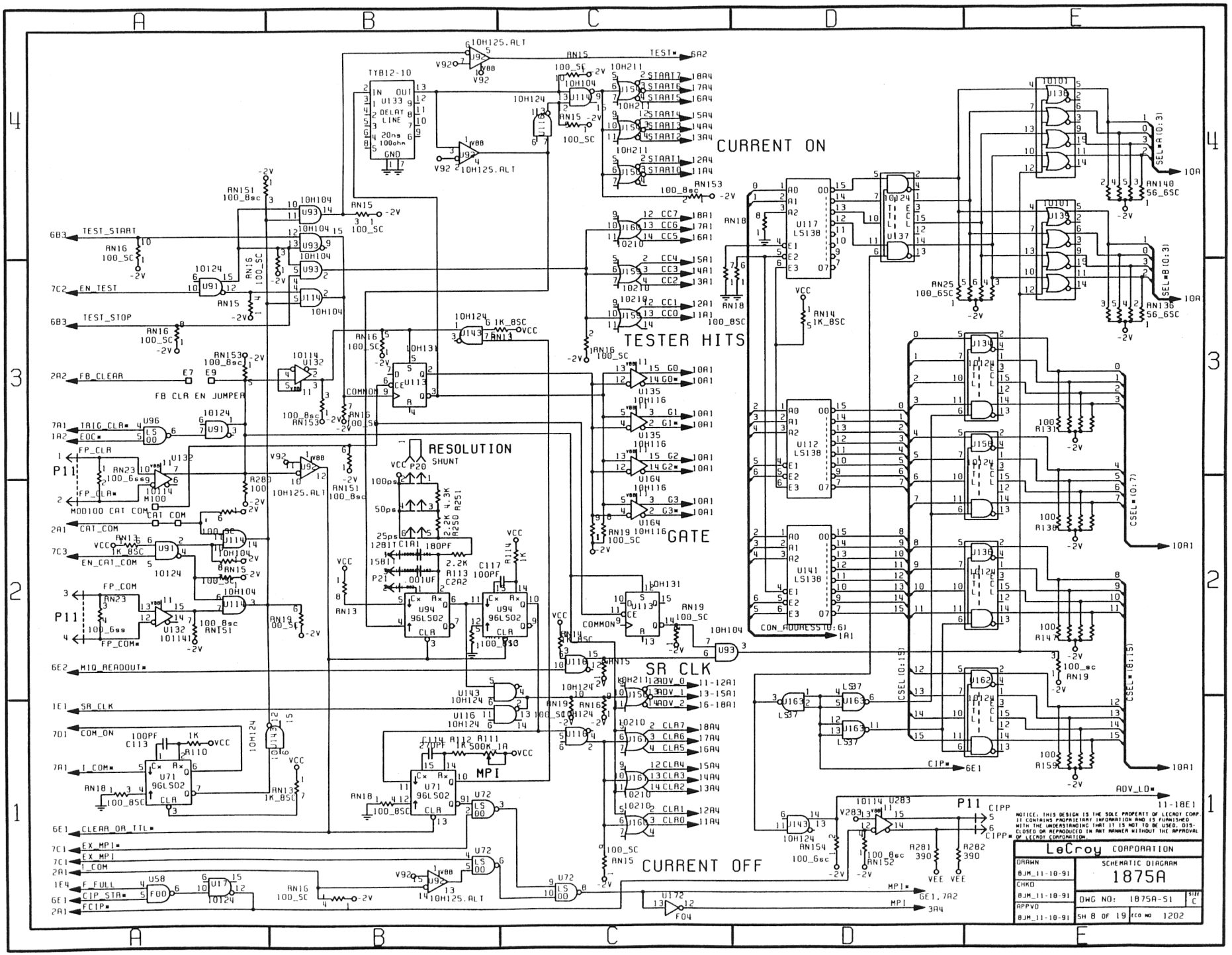
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 7 OF 19
ECO NO 1202


CURRENT ON
TESTER HITS
GATE
SR CLK
CURRENT OFF
RESOLUTION
SHUNT
MPI
TEST_START
EN_TEST
TEST_STOP
FB_CLEAR
FB CLR EN JUMPER
TRIG_CLR
EOC
FP_CLR
MOD100 CAT COM
CAT_COM
EN_CAT_COM
FP_COM
MIQ_READOUT
SR_CLK
COM_ON
I_COM
CLEAR_OR_TTL
EX_MPI
I_COM
F_FULL
CIP_STR
FCIP
TEST
CON_ADDRESS(0:6)
CSEL(0:15)
CSEL(8:15)
CSEL(0:7)
SEL(0:3)
SEL(0:3)
ADV_LD
CIP
MPI
TYB12-10
U133
DELAY LINE
20ns
100ohm
GND
U117
LS138
U112
LS138
U141
LS138
U94
96LS02
U71
96LS02
U72
LS00
U172
F04
P11
P20
P21
VCC
VEE
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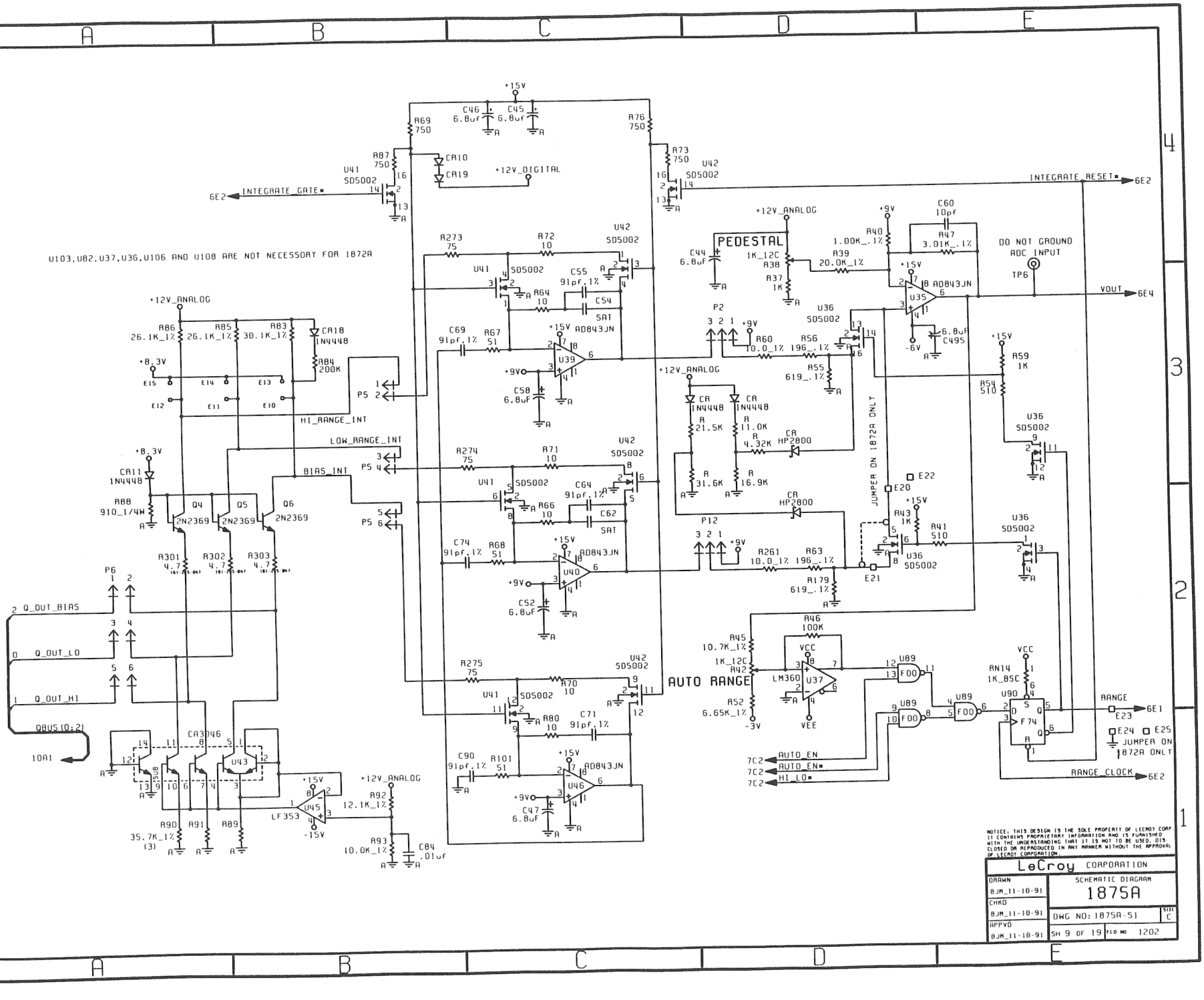
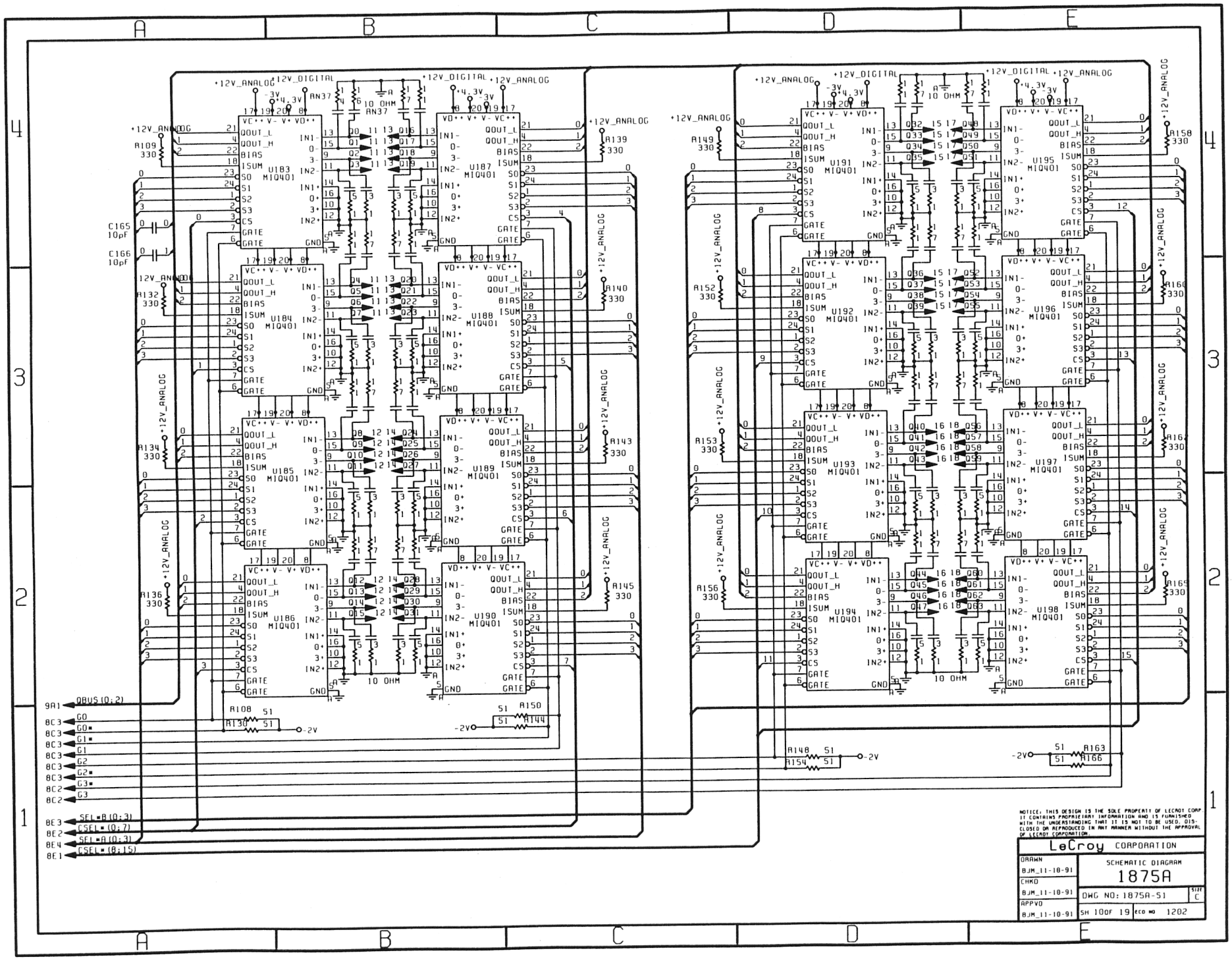
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 8 OF 19
ECO NO 1202


U103,U82,U37,U36,U106 AND U108 ARE NOT NECESSORY FOR 1872A
+15V
+12V_DIGITAL
+12V_ANALOG
+9V
-6V
+8.3V
INTEGRATE_GATE=
INTEGRATE_RESET=
PEDESTAL
DO NOT GROUND ADC INPUT
TP6
VOUT
HI_RANGE_INT
LOW_RANGE_INT
BIAS_INT
JUMPER ON 1872A ONLY
AUTO RANGE
AUTO_EN
AUTO_EN=
HI_LO=
RANGE
RANGE_CLOCK
Q_OUT_BIAS
Q_OUT_LO
Q_OUT_HI
QBUS(0:2)
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
DWG NO: 1875A-S1
SIZE C
SH 9 OF 19
ECO NO 1202


+12V_ANALOG
+12V_DIGITAL
-3V
+4.3V
-2V
U183 MIQ401
U184 MIQ401
U185 MIQ401
U186 MIQ401
U187 MIQ401
U188 MIQ401
U189 MIQ401
U190 MIQ401
U191 MIQ401
U192 MIQ401
U193 MIQ401
U194 MIQ401
U195 MIQ401
U196 MIQ401
U197 MIQ401
U198 MIQ401
10 OHM
AN37
C165 10pF
C166 10pF
DBUS(0:2)
G0
G0*
G1*
G1
G2
G2*
G3*
G3
SEL*A(0:3)
CSEL*(0:7)
SEL*A(0:3)
CSEL*(8:15)
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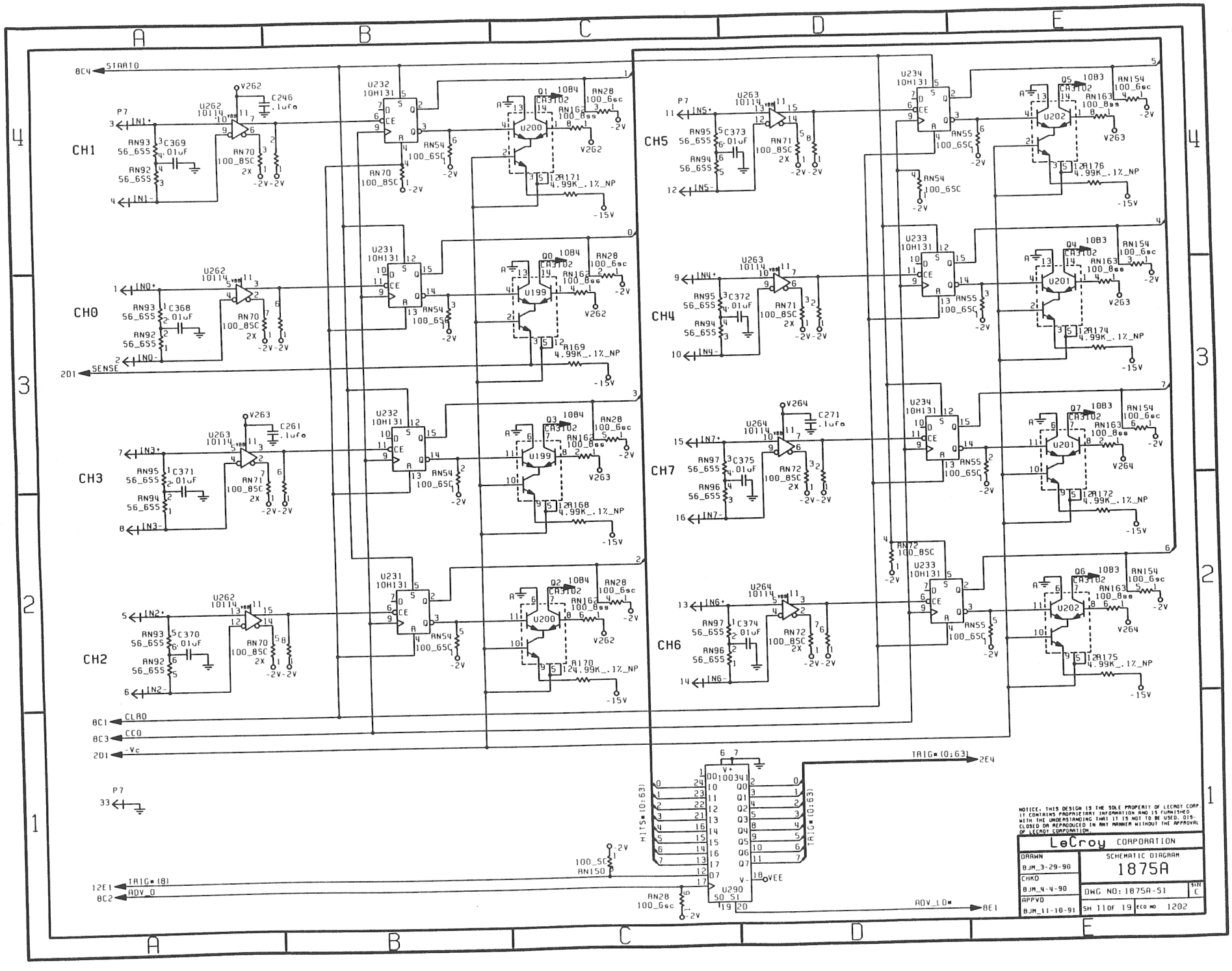
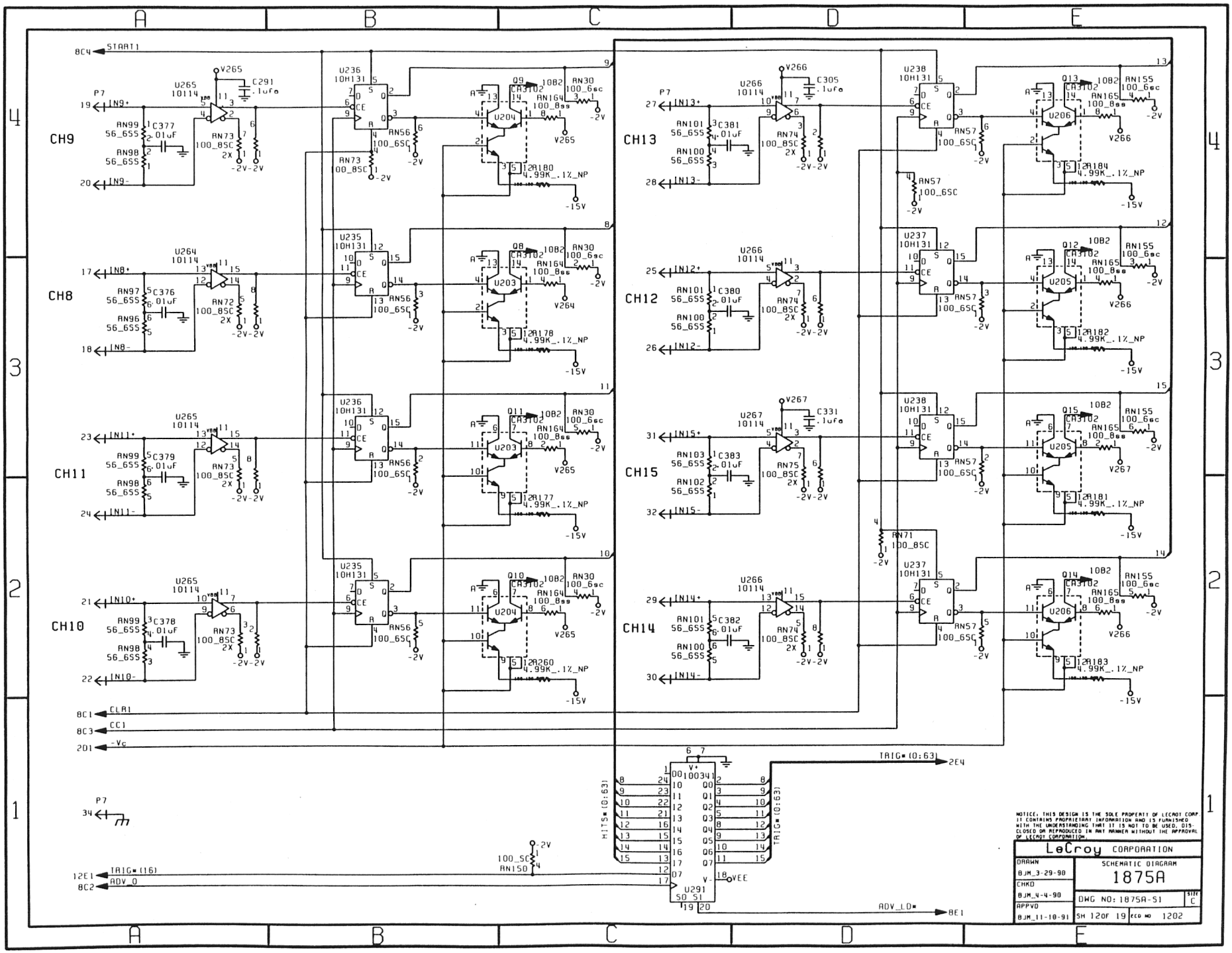
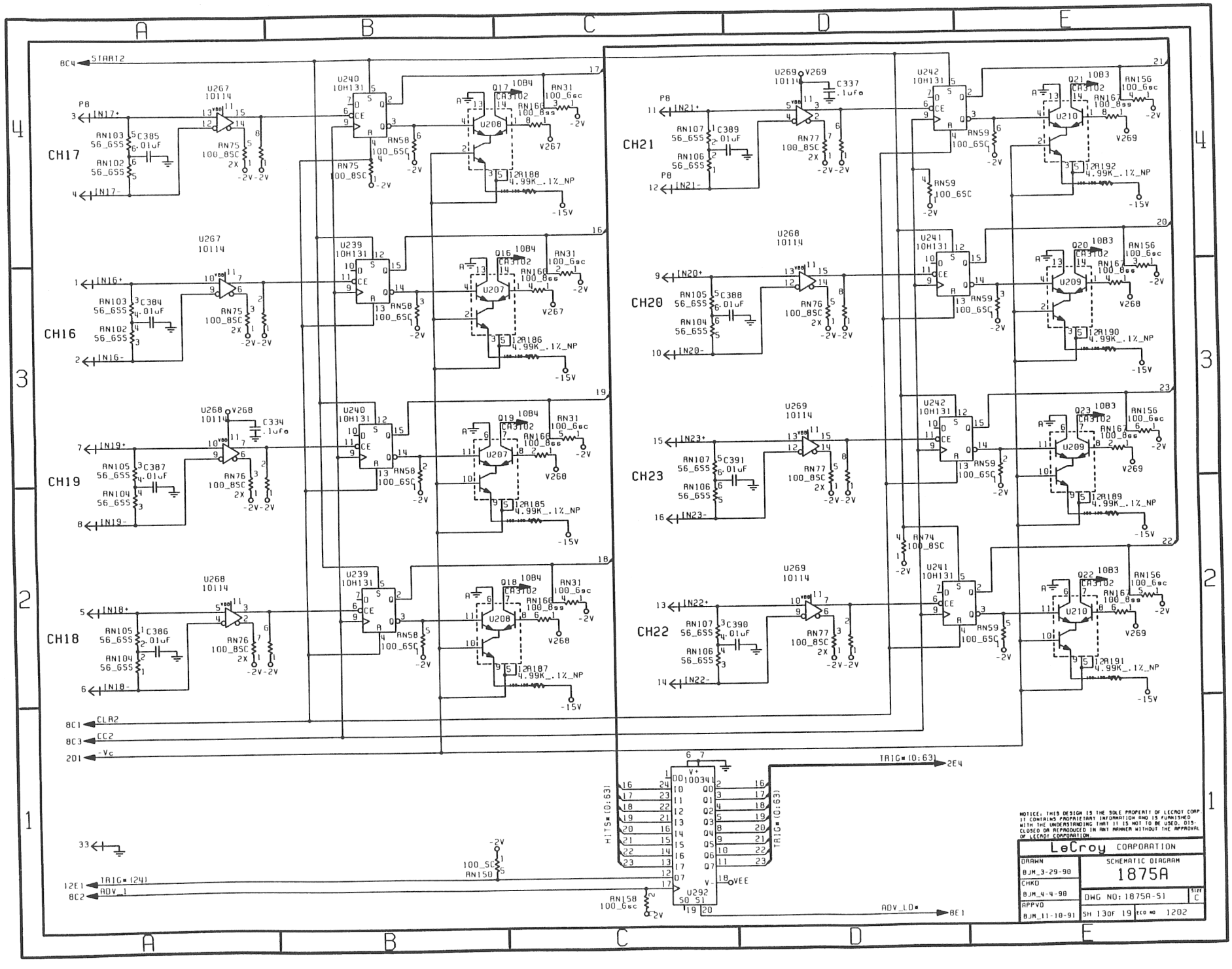
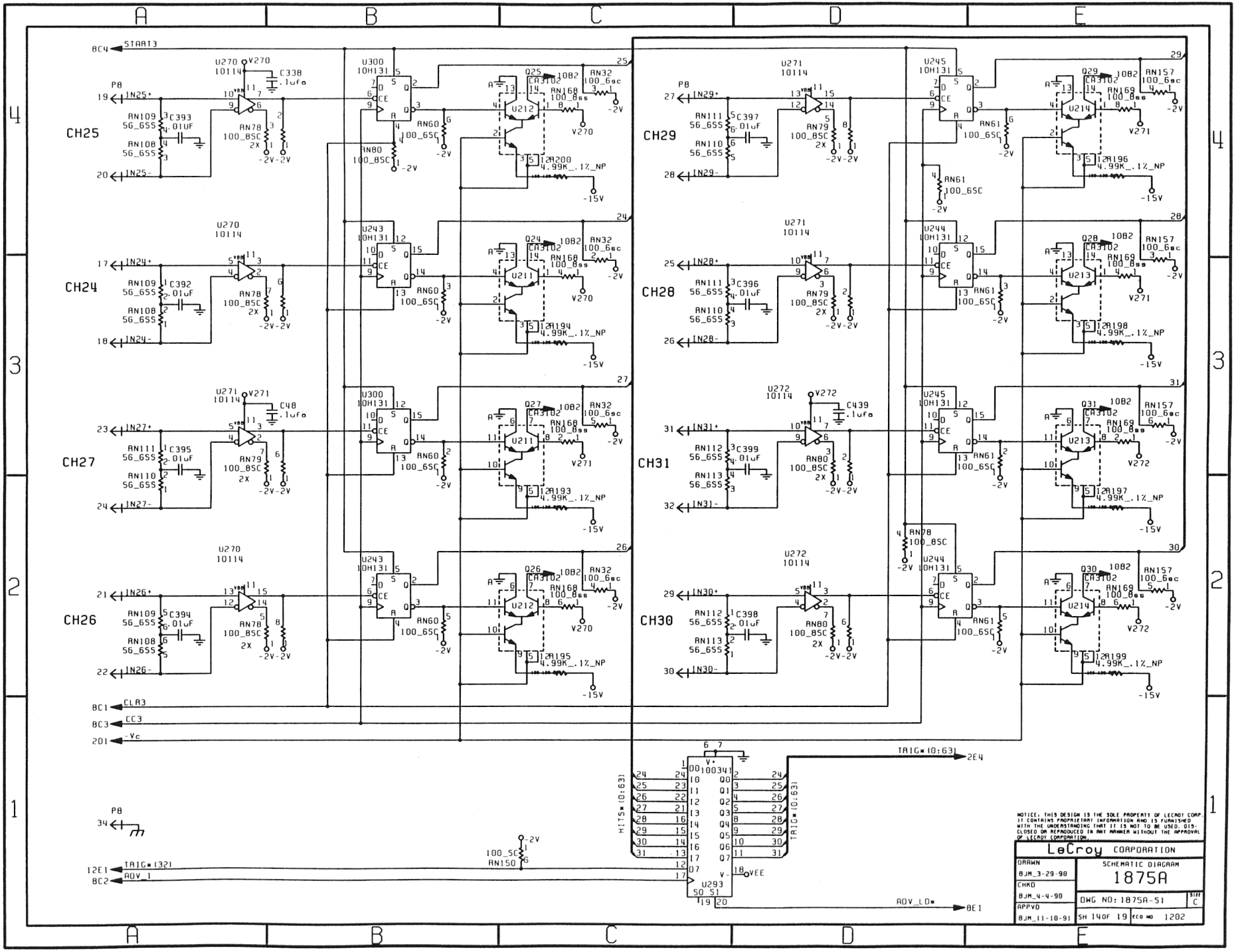
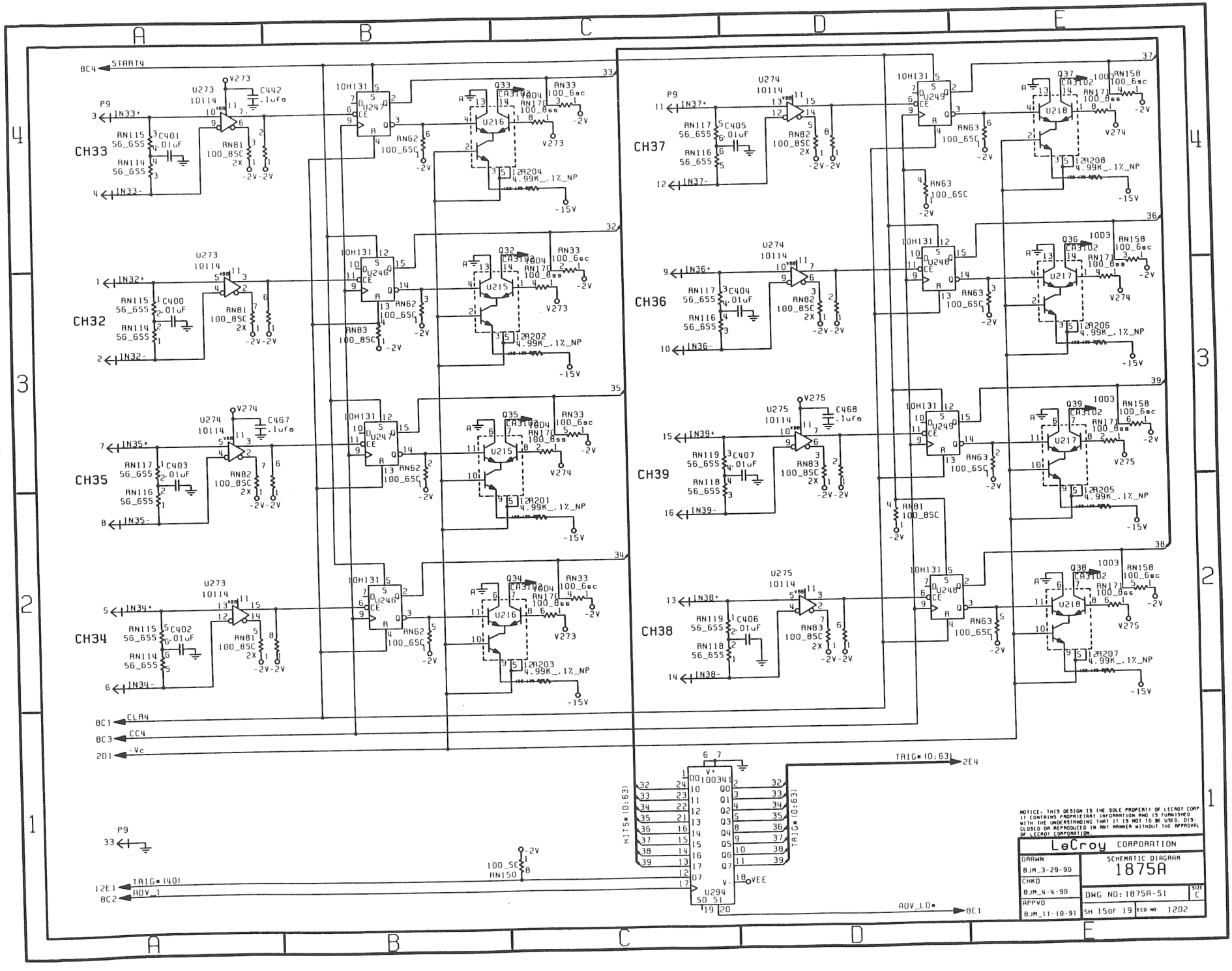
LeCroy CORPORATION
DRAWN BJM_11-10-91
CHKD BJM_11-10-91
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-51
SIZE C
SH 10OF 19
ECO NO 1202

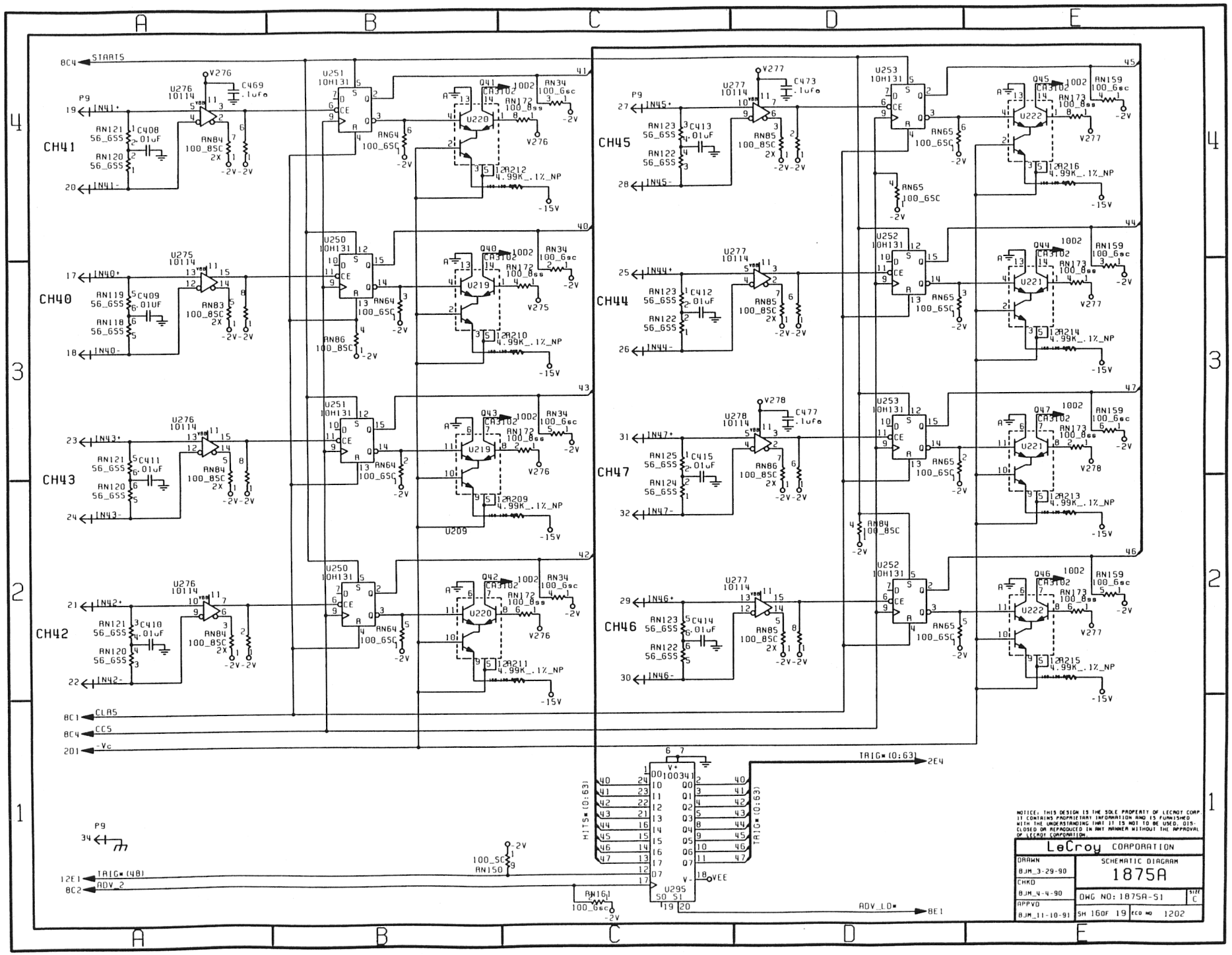

CH1
CH0
CH3
CH2
CH5
CH4
CH7
CH6
START0
SENSE
CLR0
CC0
-Vc
ADV_0
ADV_LD=
TRIG=(0:63)
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-51
DRAWN BJM 3-29-90
CHKD BJM 4-4-90
APPVD BJM 11-10-91
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP
IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED
WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DIS-
CLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL
OF LECROY CORPORATION.


CH9
CH8
CH11
CH10
CH13
CH12
CH15
CH14
START1
CLR1
CC1
-Vc
TRIG* (0:63)
ADV_0
ADV_LD*
HITS* (0:63)
TRIG* (0:63)
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DRAWN
BJM_3-29-90
CHKD
BJM_4-4-90
APPVD
BJM_11-18-91
DWG NO: 1875A-S1
SH 12 OF 19
ECO NO 1202


CH17
CH16
CH19
CH18
CH21
CH20
CH23
CH22
START2
CLR2
CC2
-Vc
TRIG=(24)
ADV_1
TRIG=(0:63)
ADV_LD=
HITS=(0:63)
VEE
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 13 OF 19
ECO NO 1202


CH25
CH24
CH27
CH26
CH29
CH28
CH31
CH30
8C4 START3
8C1 CLR3
8C3 CC3
20I -Vc
12E1 TRIG*(32)
8C2 ADV_1
TRIG*(0:63) 2E4
ADV_LD* 8E1
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-18-91
DWG NO: 1875A-S1
SIZE C
SH 14OF 19
ECO NO 1202
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.


CH33
CH32
CH35
CH34
CH37
CH36
CH39
CH38
START4
CLR4
CC4
-Vc
TRIG=(0:63)
ADV_LD=
HITS=(0:63)
TRIG=(40)
ADV_1
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 15 OF 19
ECO NO 1202


8C4 START5
CH41
CH40
CH43
CH42
CH45
CH44
CH47
CH46
U276 10114
U275 10114
U251 10H131
U250 10H131
U253 10H131
U252 10H131
U277 10114
U278 10114
Q41 CA3102
Q40 CA3102
Q43 CA3102
Q42 CA3102
Q45 CA3102
Q44 CA3102
Q47 CA3102
Q46 CA3102
C469 .1ufa
C408 .01uF
C409 .01uF
C411 .01uF
C410 .01uF
C473 .1ufa
C413 .01uF
C412 .01uF
C415 .01uF
C414 .01uF
C477 .1ufa
RN121 56_6SS
RN120 56_6SS
RN119 56_6SS
RN118 56_6SS
RN123 56_6SS
RN122 56_6SS
RN125 56_6SS
RN124 56_6SS
RN84 100_8SC 2X
RN83 100_8SC 2X
RN85 100_8SC 2X
RN86 100_8SC 2X
RN64 100_6SC
RN65 100_6SC
RN34 100_6sc
RN172 100_8ss
RN173 100_8ss
RN159 100_6sc
RN150 100_5C
RN161 100_6sc
R209 4.99K_.1%_NP
R210 4.99K_.1%_NP
R211 4.99K_.1%_NP
R212 4.99K_.1%_NP
R213 4.99K_.1%_NP
R214 4.99K_.1%_NP
R215 4.99K_.1%_NP
R216 4.99K_.1%_NP
V276
V275
V276
V277
V278
V277
V277
V277
-15V
-2V
-2V-2V
U209
U295 SO_S1
U100341
HIT5*(0:63)
TRIG*(0:63)
TRIG*(0:63) 2E4
ADV_LD* 8E1
TRIG*(48) 12E1
ADV_2 8C2
CLR5 8C1
CC5 8C4
-Vc 2D1
P9
IN41+
IN41-
IN40+
IN40-
IN43+
IN43-
IN42+
IN42-
IN45+
IN45-
IN44+
IN44-
IN47+
IN47-
IN46+
IN46-
41
40
43
42
45
44
47
46
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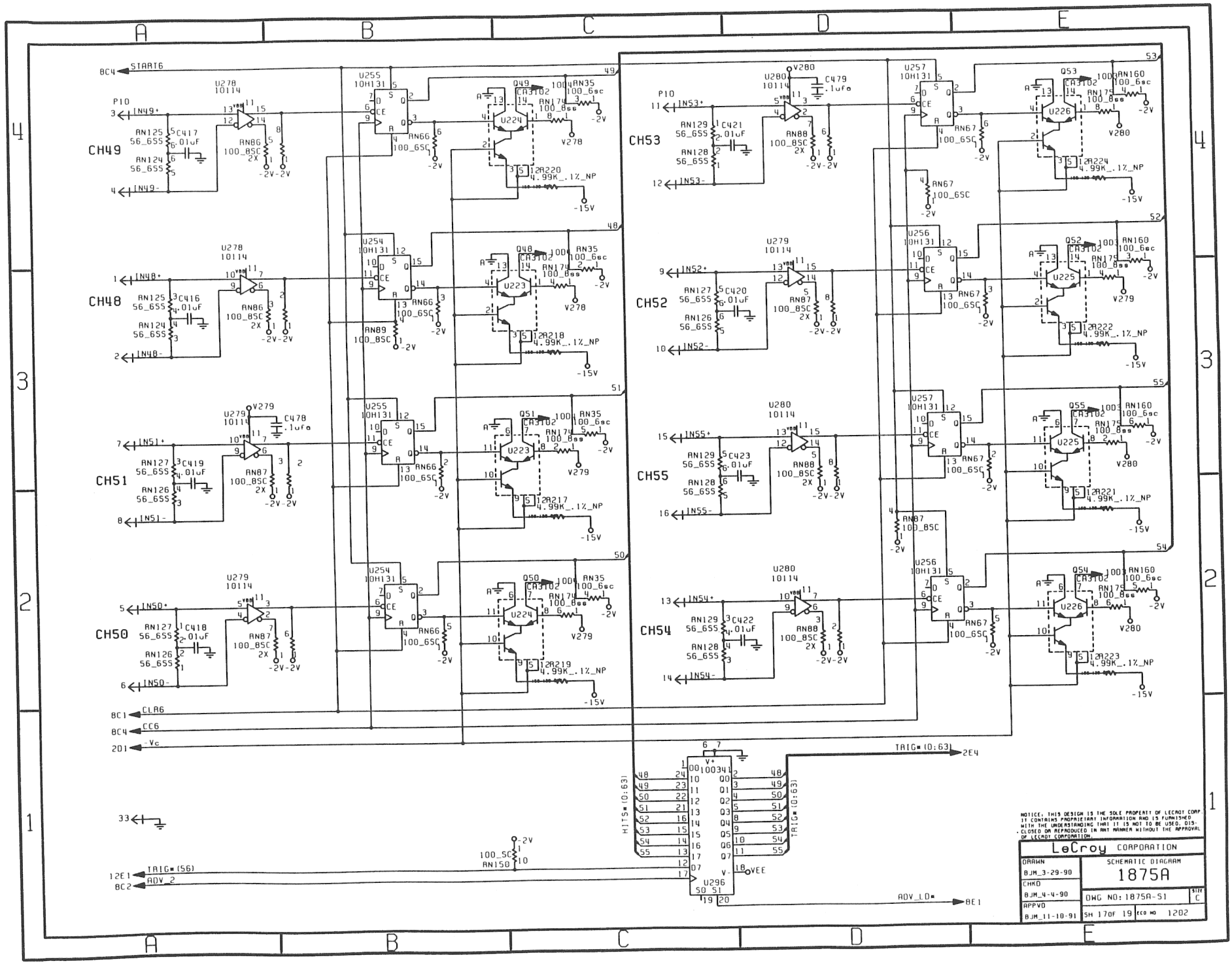
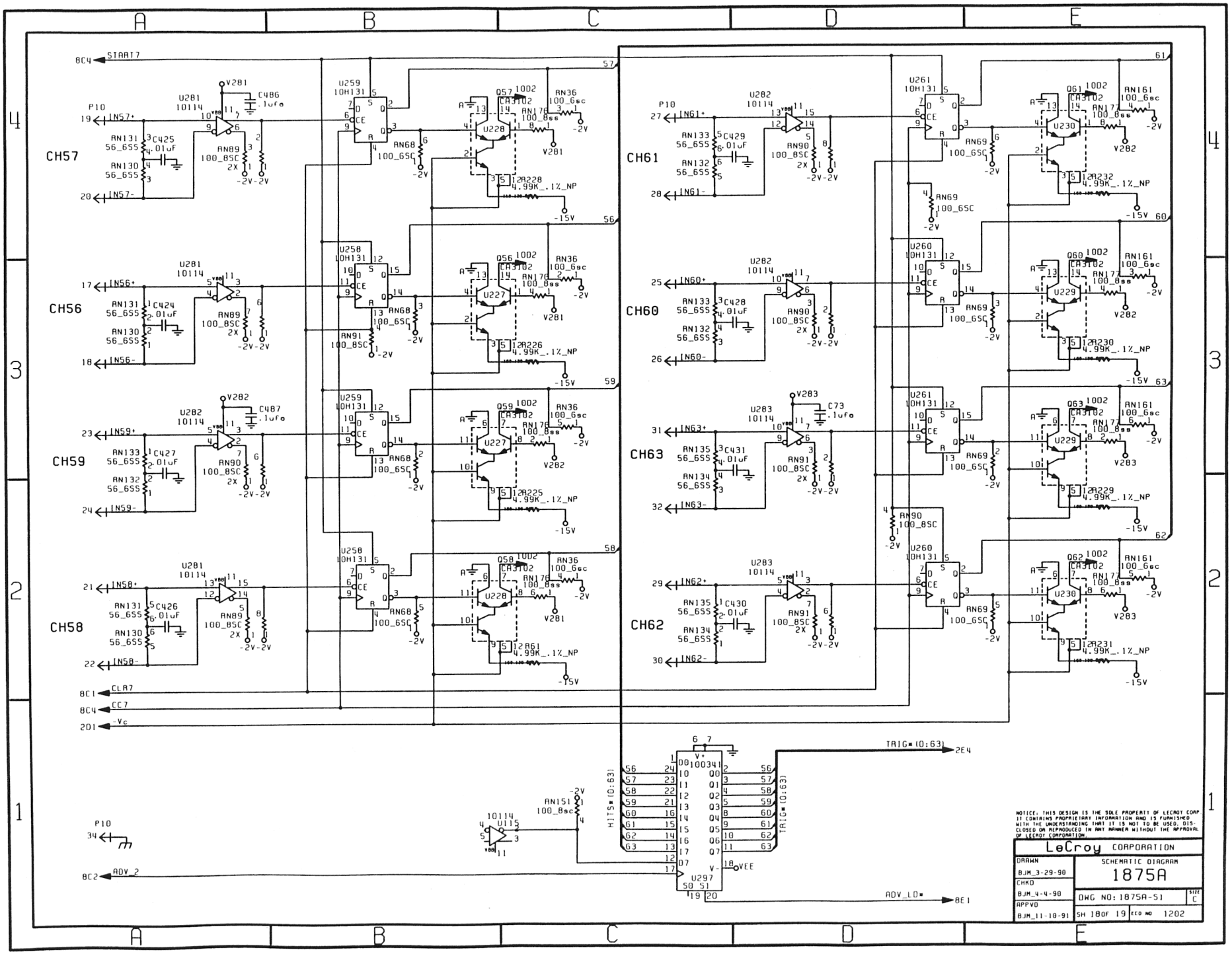
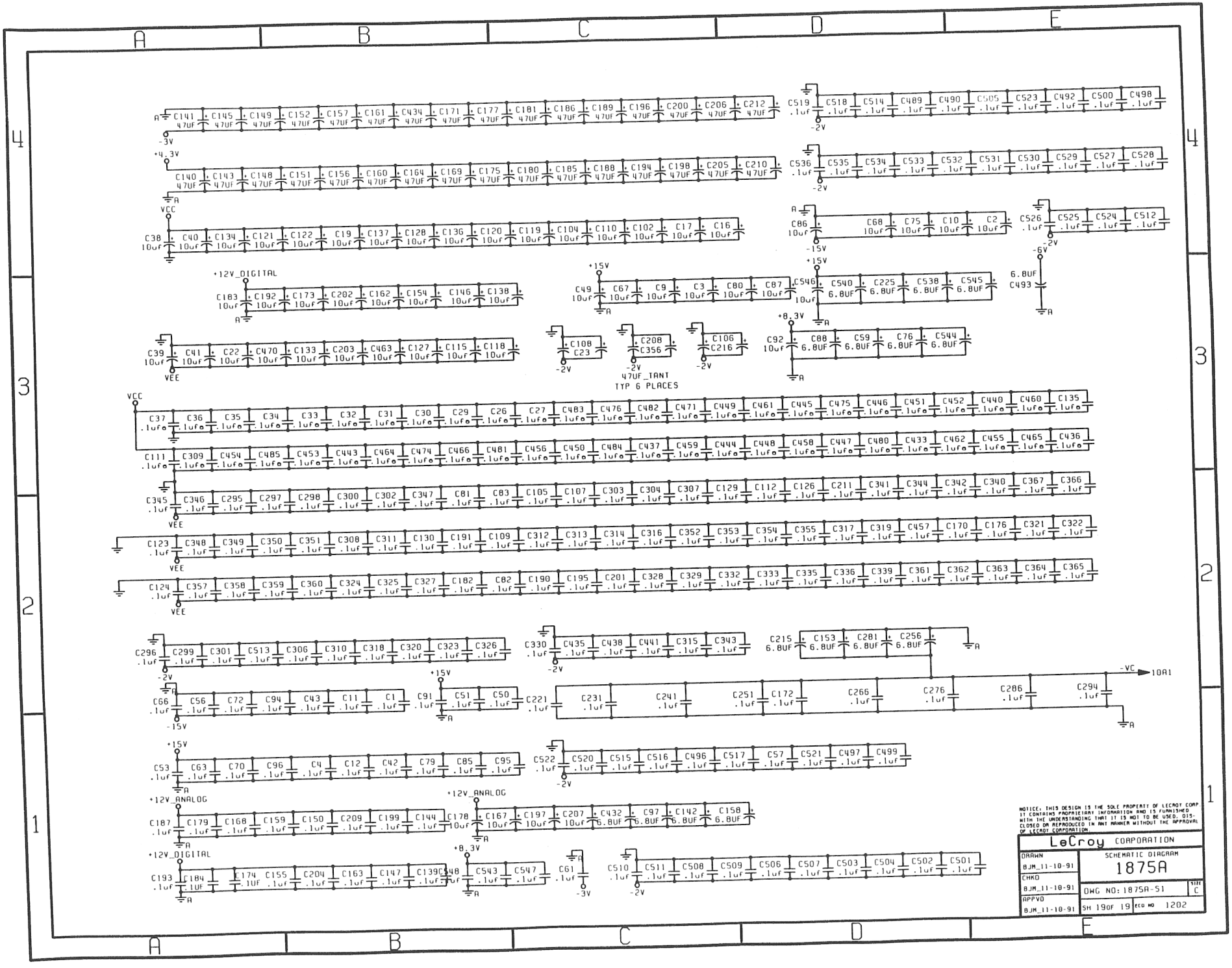
LeCroy CORPORATION
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 16OF 19
ECO NO 1202


CH49
CH48
CH51
CH50
CH53
CH52
CH55
CH54
START6
CLR6
CC6
-Vc
TRIG=(0:63)
HITS=(0:63)
TRIG=(56)
ADV_2
ADV_LD=
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-18-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 17 OF 19
ECO NO 1202


CH57
CH56
CH59
CH58
CH61
CH60
CH63
CH62
START
CLR7
CC7
-Vc
ADV_2
TRIG*(0:63)
ADV_LD*
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
SCHEMATIC DIAGRAM
1875A
DRAWN BJM_3-29-90
CHKD BJM_4-4-90
APPVD BJM_11-10-91
DWG NO: 1875A-S1
SIZE C
SH 18OF 19
ECO NO 1202


A
B
C
D
E
1
2
3
4
-3V
+4.3V
VCC
VEE
+12V_DIGITAL
+15V
-15V
-2V
-6V
+8.3V
47UF_TANT
TYP 6 PLACES
+12V_ANALOG
-VC
10A1
NOTICE: THIS DESIGN IS THE SOLE PROPERTY OF LECROY CORP. IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED, DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LECROY CORPORATION.
LeCroy CORPORATION
DRAWN
BJM_11-10-91
CHKD
BJM_11-10-91
APPVD
BJM_11-10-91
SCHEMATIC DIAGRAM
1875A
DWG NO: 1875A-S1
SIZE C
SH 19OF 19
ECO NO 1202