

SPECIFICATIONS

Models 1878/1879

96 CHANNEL PIPELINE TDC

Inputs:

Phase Latch Accuracy:
Least Count

(Phase Latch):
Model 1878

Model 1879

(Time Bin Size):

Model 1878
Model 1879

TDC Range:

Model 1878
Model 1879

Long Term Stability:

Full Scale:

Double Pulse Resolution:

Common Stop Trigger:

Sync Input:

Channel-to-Channel Matching:

Gain:

Pedestal:

Differential Non-Linearity:

Integral Non-Linearity:

Pedestal Stability:

Fast Clear Response Time:

AS-AK Handshake Time:

DS-DK Handshake Time:

Digital Clear:

Conversion Time:

96 ECL differential line receivers. Input impedance $110 \Omega \pm 10\%$. Minimum pulse width 10 nsec fwhm (must be >1 time bin width). Input swing ≥ 400 mV, differential. ± 200 psec or $\pm 10\%$ of time bin size, whichever is greater

2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31.5 nsec with Model 1810 (half time bin size).

1, 2, 4 or 8 nsec, CSR selected in stand alone mode. 1 to 15.5 nsec with Model 1810 (half time bin size).

4, 8, 16 or 32 nsec, CSR selected in stand alone mode. 4 to 63 nsec with Model 1810.

2, 4, 8 or 16 nsec, CSR selected in stand alone mode. 2 to 31 nsec with Model 1810.

9 bits, 8 + Phase Latch

10 bits, 9 + Phase Latch

$\pm 0.02\%$

1, 2, 4 or 8 μ sec, $\pm 0.01\%$, CSR selected in stand alone mode. 1 to 16 μ sec with 1810.

3-15 bins programmable, Compacting Mode. 3 bins, "All True Data" Mode.

From the Model 1810 CAT Module via TR line or from front panel differential ECL input. CSR selected.

Differential ECL two pin input. Terminated in 100Ω Minimum width 10 nsec. Quenches the Acquisition Oscillator for the duration of the input width. Acquisition Oscillator is active and stable after a time equal to 4 times the Sync pulse width. Synchronism is achieved with respect to the trailing edge of the Sync pulse. Sync accuracy: 0.1 time bins at start up. See Long Term Stability spec above. Recommended width: $(8 \pm \frac{1}{2})/f$. Here f is the Acquisition Oscillator frequency, i.e., input to the divide down circuit.

$< \pm 0.01\%$ card-to-card

$< \pm 4$ nsec channel-to-channel

< 1 nsec, typical

$< \pm 0.5$ nsec or ± 0.25 LSB, whichever is greater

< 100 psec/ $^{\circ}$ C, 1 nsec long term

< 10 nsec. Must be performed during MPI. 50 nsec minimum width

30 nsec, typical

80 nsec, typical

1.6 μ sec

412 μ sec + approximately 50 nsec per hit

GENERAL

Power Requirements:

5 mA at 15 V

7.2 A at +5 V (Model 1879, 8.5 A)

4.2 A at -5.2 V

2.0 A at -2 V (Model 1879, 3.3 A)

50 mA at -15 V

Packaging:

Single width FASTBUS module in conformance with FASTBUS Specification dated December, 1983.

FASTBUS CONTROL

Implemented Addressing Modes:

Geographical, Secondary, Broadcast

Implemented Broadcast Functions:

Code	Significance
(01) _h *	General Broadcast Select
(09) _h	Sparse Data Scan (SDS)
(09) _h	Pattern Select
(0D) _h	All Device Scan
(AD) _h	TDC SDS
(BD) _h	AFC SDS

Comments

The TDC modules are selected and respond to subsequent data cycles.

TDC modules containing time data assert their "T pin" on the following read data cycle. TDC's seeing their T pin asserted on the following write data cycle become selected to respond to subsequent data cycles.

All TDC modules assert their T pin on the following read data cycle.

Unique sparse data scan for only 1878 and 1879 modules. Follows standard SDS (see above).

All TDC modules with AFC's requiring service assert their T pins.

Slave Status Responses
to Data Cycles:

SS	Significance
0	Valid action.
1	Busy. The module is in the encoding mode and will not respond to data space read or write transactions.
3	Valid data space read with second event pending encoding.
2	End of data
6	Error. Non-implemented secondary address or invalid mode.
7	Error. Invalid secondary address loaded into internal address register.

*An h subscript denotes a hexadecimal number, i.e., base 16.

CONTROL FUNCTIONS IMPLEMENTED (CSR Space)

Module Identification Code:	Read Only (1032) _h for 1878, (1033) _h for 1879.
Compacting Parameters (Z):	A 4-bit programmable number of leading zeros which must precede a 0 to 1 transition to be recognized as a hit. To account for edge effects, all history before the first time bin is assumed equal (0 or 1) to the first bin. To allow a diagnosis of "stuck" channels, first bin reporting may be enabled via "Enable Bin 1" of CSR0. All True Data mode (Z = 0) reports every true bin.
Readout Depth, active time interval (ATI):	A 5-bit programmable time range for valid data. For 1878, the number of valid time bins is 8(ATI + 1). For 1879, 16(ATI + 1). The valid bins are those corresponding to the earliest times.
Calibration Enable (T _e and T _o):	Two bits enable the TDC to receive the test input via a TR line and apply it to the even and odd TDC channels, respectively.
Common Stop Source:	Selects the source of the Common Stop, either front panel or a TR line.
FREF Source:	Selects either the internal crystal frequency reference or a rear panel low frequency reference, via a TR line (normally supplied from the CAT).
Gain Control:	A 2-bit parameter used to divide down the on board shift register oscillator. The divide down factor is 1, 2, 4 or 8.
Reread:	Resets the memory pointers for event reread.
Stop Inhibit:	Used for disabling the TDC.
Encoding Inhibit:	Used to allow for two event buffering (one in SOS shift registers, one in data memory. If a second event is buffered, SS = 3 responses replace SS = 0 on valid data space reads.
AFC:	Fourteen locations allocated to Auxiliary Functions Card.

AUXILIARY CONNECTOR

(Auxiliary Functions Card Socket)

T0	B1	A1	T1
T2	B2	A2	T3
T4	B3	A3	T5
T6	B4	A4	T7
T8	B5	A5	T9
T10	B6	A6	T11
T12	B7	A7	T13
T14	B8	A8	T15
T16	B9	A9	T17
T18	B10	A10	T19
T20	B11	A11	T21
T22	B12	A12	T23
T24	B13	A13	T25
T26	B14	A14	T27
T28	B15	A15	T29
T30	B16	A16	T31
T32	B17	A17	T33
T34	B18	A18	T35
T36	B19	A19	T37
T38	B20	A20	T39
T40	B21	A21	T41
T42	B22	A22	T43
T44	B23	A23	T45
T46	B24	A24	T47
T48	B25	A25	T49
T50	B26	A26	T51
T52	B27	A27	T53
T54	B28	A28	T55
T56	B29	A29	T57
T58	B30	A30	T59
T60	B31	A31	T61
T62	B32	A32	T63
T64	B33	A33	T65
T66	B34	A34	T67
T68	B35	A35	T69
T70	B36	A36	T71
T72	B37	A37	T73
T74	B38	A38	T75
T76	B39	A39	T77
T78	B40	A40	T79
T80	B41	A41	T81
T82	B42	A42	T83
T84	B43	A43	T85
T86	B44	A44	T87
T88	B45	A45	T89
T90	B46	A46	T91
T92	B47	A47	T93
T94	B48	A48	T95
BRD	B49	A49	UCSRSTRB
A2	B50	A50	A3
A0	B51	A51	A1
TRIG STRB	B52	A52	VALID ADDRESS
FC	B53	A53	PCT
DB10	B54	A54	DB11
DB8	B55	A55	DB9
DB6	B56	A56	DB7
DB4	B57	A57	DB5
DB2	B58	A58	DB3
DB0	B59	A59	DB1
-2V	B60	A60	A.G.
-5.2V	B61	A61	-5.2V
+5V	B62	A62	+5V
-15V	B63	A63	+15V
D.G.	B64	A64	D.G.
D.G.	B65	A65	D.G.

A-210

VIEWED FROM FRONT OF CRATE
(REVERSE FOR REAR VIEW)

Hit Pulses:	96 signals called $\overline{T0}$ to $\overline{TR95}$. Pulse equal in duration to the front panel input pulse duration. TTL, active low signals.
Trigger Strobe:	A signal received by the TDC via the FASTBUS segment from the 1810 CAT module. Normally used by the AFC to define the fiducial time interval.
$\overline{DB0-DB13}$:	A 14-bit bidirectional bus. TTL, active low.
BRD:	Defines direction of data bus $\overline{DB0-DB13}$. When high AFC is in read mode (i.e., being read from the Segment).
Address Lines:	A0-A3; $\overline{UCSRSTRB}$: Addresses A0-A3 in conjunction with the decode AFC address strobe ($\overline{UCSRSTRB}$) allows user implementation of FASTBUS CSR locations C0000002 _h to C000000F _h . Fourteen locations are available for use on the AFC. A0-A3 are latched on TDC card.
Valid Address:	TTL Active low signal to be driven by AFC circuits if an implemented address being accessed on the AFC. Used to generate the proper SS=0 response to FASTBUS; otherwise, SS=6 is generated if Valid Address is not driven low.
Power Supply:	All FASTBUS voltages.
$\overline{PCT}$:	TTL active low signal asserts module t pin (Service Request) in response to a (BD) _h broadcast.
$\overline{FC}$:	TTL active low signal equal in duration to the Fast Clear input applied via the front panel or 1810 CAT module.