

OPERATOR'S MANUAL

MODEL 222 DUAL GATE GENERATOR



Revised
June, 1996

(ECO 1015)



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Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

A T T E N T I O N

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SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

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222 DUAL CHANNEL, MANUAL CONTROL

- Responds to TTL or Fast NIM Inputs
- "OR" Input Permits Extending Gate With External Signal
- Fast NIM (Normal and Complement) and TTL Outputs
- NIM Level Blanking Input
- NIM Level Delayed Output
- Presettable Gate Durations From < 100 nsec to > 11 sec

VERSATILE, PROMPT AND DELAYED GATE GENERATION

The Model 222 Dual Gate and Delay Generator provides two complete delay/gate channels in a single NIM module. The 222 eliminates the common problems exhibited by other gate generators. There is negligible recovery time associated with the unit at any width setting; it may be retriggered immediately after the gate returns to its quiescent state in all ranges. Each channel of this single module can also be used to provide delays and gate outputs and to drive bin gates in its own NIM bin (LeCroy Model 1403) and several external bins. In addition, an OR input for each channel permits the gate and delay interval to be extended by an external input.

The 222 provides a range switch and a screwdriver-adjustable potentiometer to permit continuous adjustment of gate durations from less than 100 nsec to greater than 11 seconds. A front-panel LED remains on when gate output is present, even if extended by the OR input. The approximate gate setting may be easily determined without an oscilloscope by means of the front-panel monitor point, which provides a DC voltage related to the gate duration. A conversion graph is enclosed with the unit. In addition to preset width ranges, the range switch has a "Latch" position to provide a continuous gate controllable by either the "Start" and "Stop" inputs or by the "Start" and "Stop" push-buttons. The push-buttons permit manual operation when the full scale switch is set on "latch", and single-shot presettable operation when the full scale switch is in any other position.

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SPECIFICATIONS

INPUT

START Input: One; responds to both fast NIM-level and TTL-level inputs.

Fast NIM Input Requirements: Greater than -600 mV enables; minimum width 5 nsec; 50 Ω impedance for any input from +100 mV to -5.0 V.

TTL Input Requirements: Greater than +2.5 V enables; minimum width approximately 20 nsec; high impedance for any input from +400 mV to +6 V. (Requires +5 mA at +2.5 V.)

STOP Input: One; characteristics same as for "Start" input. Used when range switch is in Latch position. Can be used in Preset position but will cause a "delayed stop".

Blanking Input: One; requires fast NIM-level inputs (≥ -600 mV) 50 Ω impedance; blanks all outputs which occur during its presence, including the delayed output*. Maximum blanking rate, 80 MHz.

"OR" Input: One; requires fast NIM-level inputs (≥ -600 mV) 50 Ω impedance; extends preset gate duration by the portion of its input signal that occurs after the preset output time.

OUTPUT

Gate Outputs: One standard fast NIM-level output (quiescently 0 V; -750 mV during pulse) of approximately 2 nsec rise time; fall time slightly longer on wide widths. One complementary fast NIM-level output (quiescently -750 mV; 0 V into 50 Ω during pulse). One TTL-level output (quiescently 0 V; $> +2.5$ V into 50 Ω during pulse).

Delayed Output*: Delivers 10 nsec (FWHM) fast NIM-level signal into 50 Ω . Occurs approximately at the trailing edge of the preset or start-stop gate output (including any gate extension due to input "OR"); ≤ 2.5 nsec rise time.

Presettable Gate Durations: Continuous from < 100 nsec to > 11 sec plus latched position; full scale switch determines range. Screwdriver adjustment vernier permits fine adjustment from $\leq 10\%$ to $> 110\%$ of full scale. Front-panel test point gives DC voltage related to gate width (in % of range switch setting). Conversion chart included with module. Output width jitter, approximately 0.05% of setting.

GENERAL

Recovery Time: None; unit may be retriggered immediately after gate output returns to its quiescent state.

Input-Output Delay: 14 nsec.

Manual: Front panel "Start" and "Stop" push-buttons permit manual operation when full scale switch set on "latch", and single-shot presettable operation when full scale switch is in any other position.

Bin Gate Driver: Each channel has one rear panel Lemo-type connector which switch selectively drives external bins in either normal or inverted direction. Logic 1: < 1 V at 200 mA; Logic 0: 0.5 V into high impedance (2 k Ω).

Channel Select Switch: Rear panel 3-position switch (A/B/Off) determines which channel drives the bin in which the Model 222 is located.

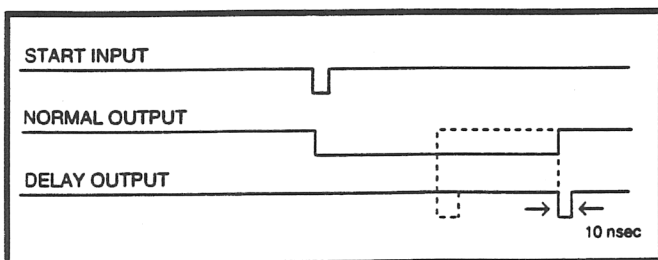
Busy Indicator: Front panel LED remains on when gate output is present, even if extended by "OR" input. Packaging: NIM-standard single width module; Lemo-type connectors.

Current Requirements: 95 mA at +12 V, 180 mA at -12 V, 45 mA at +24 V, 80 mA at -24 V, 235 mA at +6 V (drawn from +12 V if unavailable).

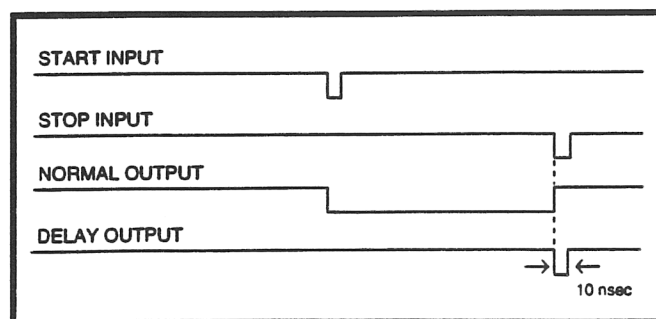
*Blanking of the delayed output may be disabled by factory option.

DUAL GATE GENERATOR TIMING DIAGRAMS

Presettable Width Mode



Latch Mode



SECTION I

SPECIFICATIONS

1.2 Input Characteristics

1.2.1 START and STOP Inputs

The START and STOP inputs respond to either fast NIM* or TTL level inputs. Since the Model 222 input circuit automatically responds to either type of signal, no switch selection or internal change is necessary. A fast NIM input drives an impedance of 50 Ω , however the input is high impedance for TTL levels. A TTL input requires 5 mA at +2.5 V, increasing slightly as the input voltage is increased (i.e., 5.75 mA at +3.5 V). Protection is provided for currents of up to ± 5 A for 1 μ sec by a 47 Ω series-terminating resistor, clamping at 0 V for negative pulses and at +6 V for positive pulses.

It is important to note that the STOP input (or STOP pushbutton) is only intended for use with the FULL SCALE WIDTH switch in the LATCH mode. However, if a Stop is applied while an output is present with the FULL SCALE WIDTH switch set at a finite range, the output pulse will nevertheless be terminated, but only after a short delay.

1.2.2 BLANK Input

The BLANK input responds to fast NIM level* inputs. Input impedance is 50 Ω and input protection extends to at least ± 5 V. The blanking input suppresses only the portion of the Model 222 output pulse occurring during the blanking interval. The delayed output pulse is also suppressed on the standard unit.

1.2.3 OR Input

The OR input responds to fast NIM level* inputs, has a 50 Ω impedance, and is protected to at least ± 5 V. Its specific function is to enable the user to easily extend the preset output width on the basis of external criteria, (e.g., extending an input inhibit to scalars or other data acquisition modules while a computer readout is still in progress).

| | | | | | |
|--------------------|--------|---|-----------|---|--------|
| * Fast NIM Levels: | -12 mA | { | Logical 1 | { | -36 mA |
| TTL Levels: | +2.0 V | { | Logical 1 | { | +5.0 V |

1.3 Output Characteristics

1.3.1 Gate Outputs

General:

The Model 222 provides one standard fast NIM level output (quiescently 0 V, -750 mV during pulse) of approximately 2 nsec risetime, one complementary fast NIM level output (quiescently -750 mV, 0 V during pulse), and one TTL level output (quiescently 0 V, <+2.5 V into 50 Ω during pulse). The falltime of the fast NIM outputs is generally similar to the risetime, except at large output widths where the Model 222 timing stage causes a slight degradation of the falltime.

Gate Durations:

Preset output durations extend from <100 nsec to >11 sec and are determined by a combination of the FULL SCALE WIDTH selector switch and the screwdriver-adjustable vernier. On the BNC version (Model 222N), a lock-in potentiometer replaces the switch and vernier, giving direct visual indication of output width setting. On the LEMO Model 222, a DC level available at the front panel test point gives an indication of the output width setting as a percentage of the FULL SCALE WIDTH switch setting, from approximately 10% to 110%. The conversion chart representing this test point output is shown in Fig. 1.1.

When the output width range selector switch is set in the LATCH position, the output width of the Model 222 is determined by either the START and STOP pushbuttons, or the START and STOP inputs. Once "started", the Model 222 output will stay on indefinitely until "stopped" or until power is turned off.

1.3.2 Delayed Output

The delayed output (DEL) delivers a 10 nsec FWHM (Full Width Half Maximum) fast NIM level signal into 50 Ω . The leading edge of this output occurs shortly before the trailing edge of the normal gate output pulse. In other words, its leading edge occurs a few nsec before the normal gate output is fully completed.

The delayed output is normally suppressed by the BLANK input, but this feature may be disabled by factory option. This output is often useful for creating a "delay and gate generator" using two channels of the Model 222. In this case, either the delayed output or the complementary output of Channel 1 can be fed into the START input of Channel 2 of the Model 222 to create an output pulse of specified width occurring at a time determined by the output width setting of Channel 1. More standard applications involve using the delayed output to trigger a computer readout cycle, as a reset pulse, or as a "flag" pulse to indicate the completion of a data acquisition interval.

1.3.3 Bin Gate Driver Outputs

For Remote Bins:

The Model 222 provides a rear panel LEMO connector output which switch-selectably drives external bins in either the normal or inverted direction. For the normal direction, the Model 222 will clamp 200 mA for a Logical 1 (less than 1 volt). A Logical 0 is a high-impedance open-collector-type output. A 2 k Ω resistor provides pull up to +5.2 V.

NOTE: The NORMAL position disables the driven bin for the duration of the Model 222 output. The INVERTED position enables a normally disabled bin during the gate output interval.

For Driving the Local Bin:

Either Channel 1 or Channel 2 of the Model 222 can drive the bin from which the unit is powered. A rear panel 3-position switch selects which channel, with the third position (OFF) available to disassociate the local bin from the influence of the Model 222. The NORMAL position serves to disable the driven bin for the duration of the Model 222 gate output.

1.4 Recovery Time

With the Model 222, it is possible to get a second gate output immediately after the first gate output. In this respect, no delay period (deadtime) is required before the Model 222 can be retriggered. This feature is made possible by the OR'ing of two internal signals to create one output signal with a width corresponding to the front panel rotary switch setting and vernier.

1.5 BUSY Indicator

The Model 222 provides a front panel LED (light-emitting diode) indication when a gate output is present. This LED lights whenever an output is present, even if extended by an OR input. Because no mechanism is provided to slow down the turning on and off of the LED for each gate output, at short output widths or high rates, the LED will appear to the eye as a steady "on" condition.

1.6 Packaging

The Model 222 is packaged in a standard NIM module conforming to the standards outlined in AEC-NIM Report TID 20893, Rev. 3. The LEMO connector version has a #1 front panel width, while the BNC version utilizes a #2 width due to the size of the front panel lock-in potentiometer and the BNC connectors.

1.7 Current Requirements

The Model 222 dissipates 7.5 watts and requires the following NIM voltages and currents:

-24 V at 80 mA
-12 V at 160 mA
+ 6 V at 235 mA*
+12 V at 95 mA*
+24 V at 45 mA

* It is important to note that the Model 222 will automatically draw an additional 235 mA from the +12 V supply if +6 V is unavailable. For this reason, a +6 V NIM bin is NOT necessary to power the Model 222. When only the +12 V supply is a %%%

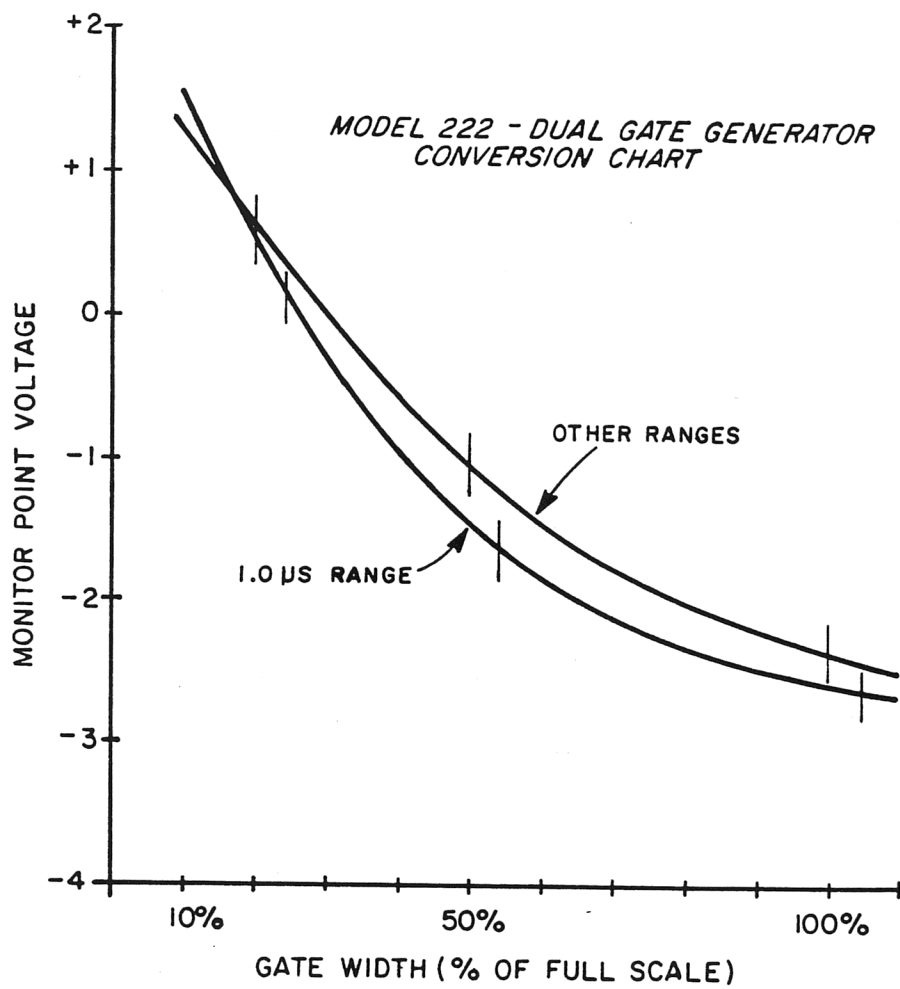


Figure 1.1

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

The Model 222 is a two-channel NIM module. It can be divided into three major sections:

The Start-Stop, Latch and OR'ing stages
The Ramp and Ramp Level Detector stages
The Output and Blanking stages

Each of these will be discussed briefly. The reader should refer to the circuit schematic (located in the rear pocket of this manual), the functional block diagram (Figure 2.1) and the timing waveform diagrams (Figure 2.2).

2.2 START-STOP, Latch and OR'ing Stages

The Start and Stop input stages are identical. Each is composed of a special input stage capable of accepting a low-impedance NIM input (-500 mV into 50 Ω) or a high-impedance TTL input (+2.5 V at 5 mA) using the same input connector. This is accomplished by requiring the input NPN transistor to provide a low-impedance path for negative signals and routing the input current of the negative input signal to the inverting input of the MC10115 receiver, causing it to go low. The same effect is accomplished with a positive input pulse, which turns off the input PNP transistor, enabling the 2 k Ω resistor on the MC10115 to pull the input low. A third method of causing a Start or Stop is via the respective pushbutton which, when depressed, causes circuit operation similar to that for the positive input.

When the inverting input of either the Start or Stop receivers (MC10115) is pulled more negative than the non-inverting input, the output will go high. Even for slow marginal inputs, the output is fast due to both AC and DC positive feedback to the non-inverting input.

From this point on, the Start differs from the Stop. The Start is first differentiated and the resulting "leading-edge" pulse is shaped by an emitter-coupled logic (ECL) receiver (which is inhibited if the Ramp section is already busy). The resulting pulse is then used to set the Latch, (composed of a heavily fed-back section of ECL receiver), by forcing the Latch output positive. (See "Presettable Width Mode" timing diagram in Figure 2.2). This pulse is present for the duration of the Latch and is fed to the Ramp section to start the ramp cycle as well as to provide a prompt input to the final OR stage which is used to drive the output stage.

Once a ramp is generated (see Section 2.3), the Ramp Detector output is fed to the OR along with the Latch output to hold the output stage "on" and inhibit the Start input for the entire ramp duration. At the maximum amplitude of the ramp, the Stop-level Detector (in the

Ramp section) will reset the Latch, but the output of the final OR will still be present until the ramp is totally recovered, at which point the Ramp Detector will return to its quiescent level, removing drive from the output stage.

The STOP input is intended primarily for use in the LATCH mode of operation. In this mode, the Ramp section is disabled, so the output stage follows the Latch output only. (See "Start-Stop Mode" timing diagram in Figure 2.2). A Stop input will reset the Latch previously set by the Start. Therefore, the output stage will be driven only for the time from Start to Stop. If a Stop input is generated when operating in any of the preset modes, it will reset the Latch before the end of the ramp, causing the ramp to be shortened, but because the output stage follows the total ramp duration, the output width will not be promptly terminated, but will be extended by the ramp recovery time (which depends on both the range setting and the amount of preset time which had already elapsed before the Stop was generated).

The input OR stage converts NIM levels to offset ECL levels required to drive directly the final OR stage, independent of the states of the Start-Stop stage, the Latch, the Ramp stage, etc. Thus it provides a final output width equal to the input OR width (or to the overlap of it and the Start-Stop Latch and/or the Ramp Detector).

2.3 Ramp and Ramp Detector Stages

The Ramp stage is composed of a capacitor, C_n ($n=1,2,...,8$, as selected by the FULL SCALE WIDTH switch), resistor $R1^n$ (paralleled by $R2$ on the 1.0 μsec range), and a 10 mA current source (transistor Q15). The current source is quiescently on, causing the ramp to be clamped at about +3 V by the 1N702 zener diode and the base-emitter drop of Q2. When the Start-Stop Latch is set by a Start pulse, the Q15 current source is disabled and the ramp begins to discharge toward -3 V at a rate determined by $R1$ (15 k Ω , or 7.5 k Ω when paralleled by $R2$ on 1.0 μsec range) and C_n , which is determined by the FULL SCALE WIDTH switch setting. (See "Presettable Width Mode" timing diagram in Figure 2.2).

As soon as the current source is turned off, the integrated circuit comparator used as the Ramp Detector is enabled because the collector of Q15 goes to zero. When the ramp reaches the voltage level set by the 2 k Ω front panel vernier width potentiometer, the Stop-level Detector comparator I.C. resets the Start-Stop Latch. This enables the current source and the ramp is returned to its quiescent level at a rate determined primarily by the 10 mA of the current source and the value of C_n . When the ramp reaches the clamp level determined by transistor Q2, the current is shunted to Q2 collector, the Ramp Detector turns off, the output drive to the ECL final OR and the inhibit to the Start stages are removed, and the unit can be retriggered.

2.4 Output and Blanking Stages

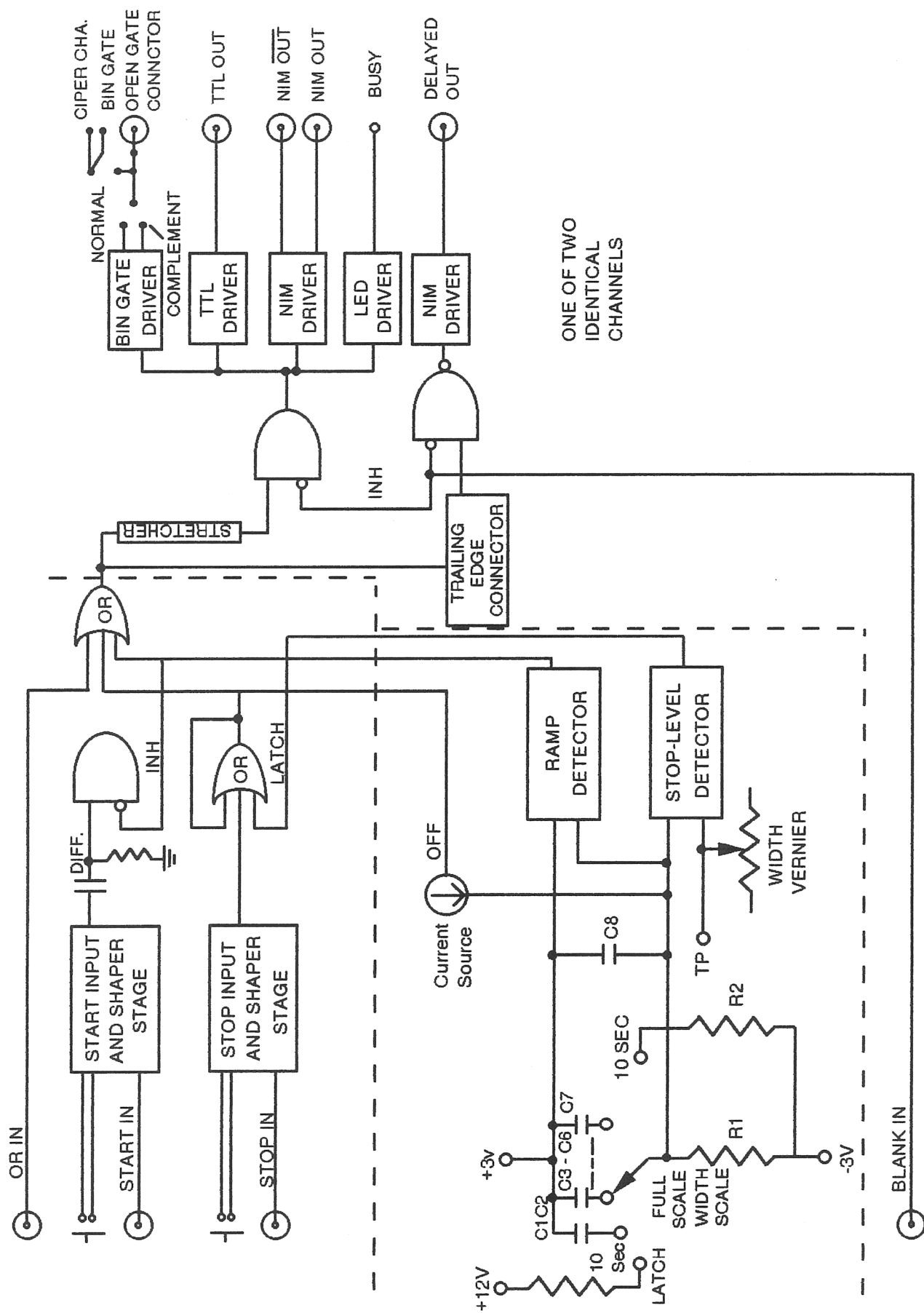
The NIM driver output stage is a 16 mA differential stage operating

from the output OR (with a 5 nsec stretcher stage) via a 1N706 zener diode to provide level shifting. Both the normal and complementary outputs are made available and they are individually clamped at -1 V if no output load is present.

The TTL and Bin Gate output stages and the BUSY LED driver are driven from a stage the same as above except that the collectors are referenced to positive voltages. The TTL stage uses a double emitter-follower to provide stiff drive for either logic level. The Bin Gate output uses one of two switch-selectable, stiff, clamp-to-ground inverting transistors. One provides a normal level to inhibit modules on the bin gate bus for the duration of the output. The other provides an inverted level to inhibit quiescently and to enable only during the output duration. The Busy driver holds the BUSY LED on for the duration of the output, stretching short pulses enough to provide a visual indication.

The Delayed Output stage is also similar to the NIM driver stage, except that only the normal output (quiescently zero, -16 mA during pulse) is available and the stage is driven from a trailing-edge differentiator-shaper stage to generate a 10 nsec wide pulse.

The Blanking input converts a NIM level input to a proper level to disable the three differential stages, and therefore all outputs and the BUSY LED, for the duration of the Blanking input.



FUNCTIONAL BLOCK DIAGRAM MODEL 222 DUAL GATE GENERATOR

Figure 2.1

MODEL 222 DUAL GATE GENERATOR TIMING DIAGRAMS

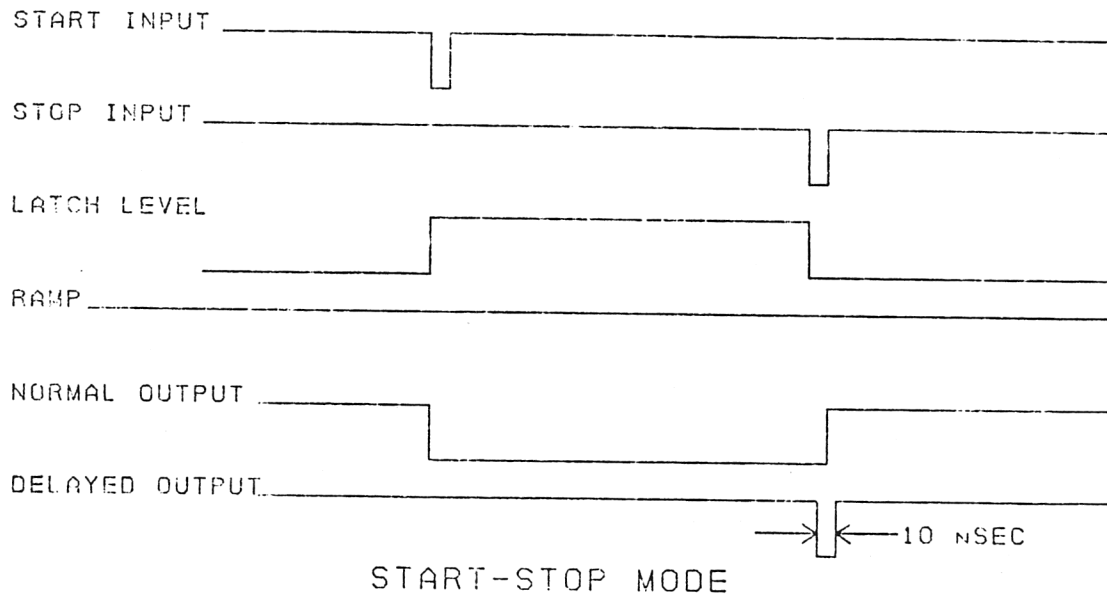
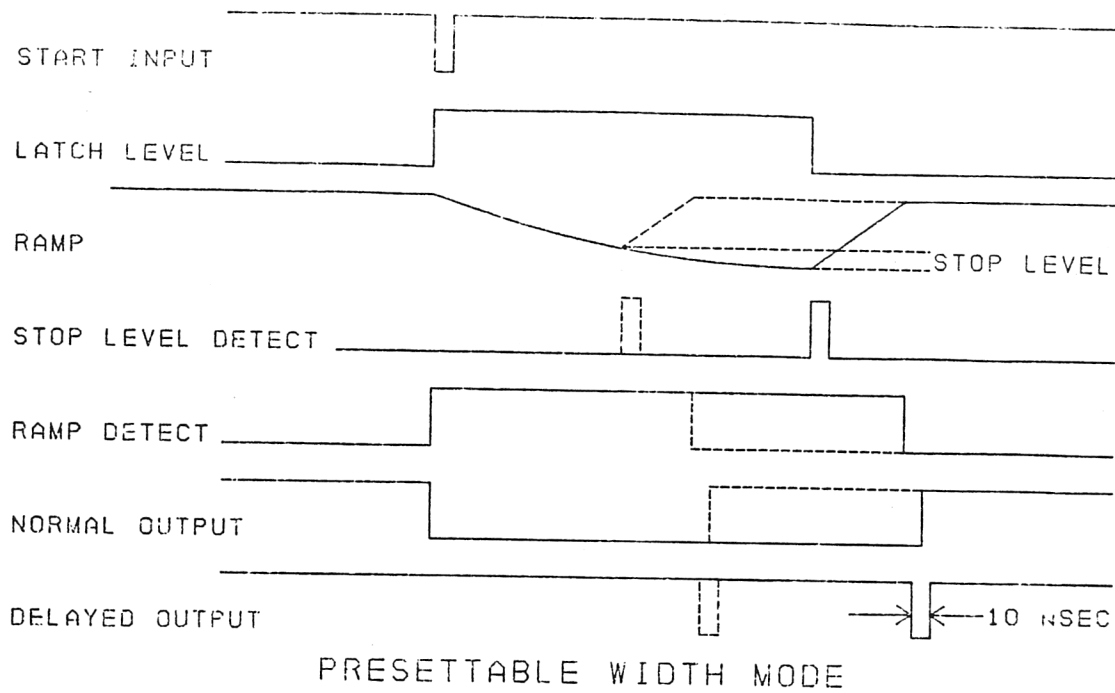


Figure 2.2

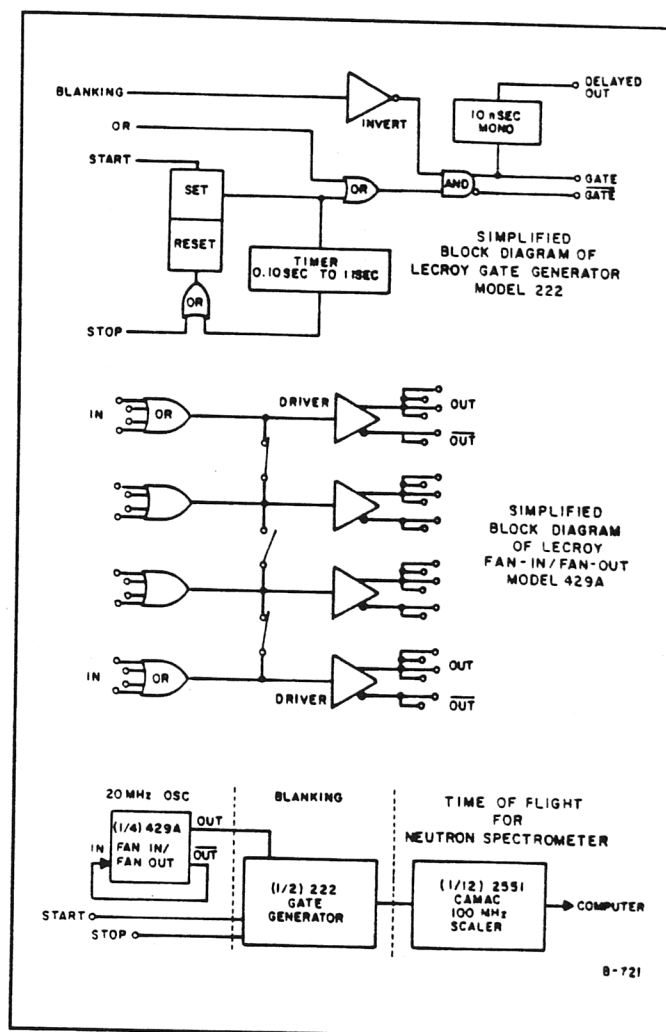
AN-4

A SIMPLE TIMING SCHEME USING A CAMAC GATE GENERATOR AND SCALER

The LeCroy Models 222, gate generator, and Model 2551, scaler, may be used together to form a time digitizer capable of 20 nsec resolution for times as long as 200 msec. If a signal is applied to the start input of the Model 222 and a second signal is applied to the stop input, the Model 222 puts out a gate pulse of duration equal to the time between the start and the stop input pulses or the preset gate time, whichever is smaller. In this way, a gate equal to the time of interest is generated with a provision for overflow. This feature is often necessary when no stop pulses are to be expected.

The blanking input of the Model 222 sets the output of the module to a logical zero state for the duration of the blanking signal. The minimum pulse width to which the blanking input will respond is 10 nsec. Thus, a 50 MHz clock may be applied to this input. In this case, the output of the Model 222 when used as described above will be a 50 MHz pulse train for the duration of the time to be measured. These pulses may be counted by a LeCroy Model 2551 12-channel CAMAC scaler.

Such a system consisting of one Model 2551 and 12 Model 222s may be used for a variety of applications including neutron time-to-flight spectroscopy. The common start (stop) signals and the clock signals may be fanned out using a Model 429A in the 2 x 8 mode.



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TECHNICAL INFORMATION
(PARTS LIST, SCHEMATICS)

XENTIS V4.5
BMPSS
INPMS
BMRES

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222 PARTS LIST
LeCroy-Company Confidential Data

PAGE 1
25-MAR-1998
MANUALBOM.XCF;13

| PART NUMBER | DESCRIPTION REMARK | QTY PER |
|-------------|---------------------------|---------|
| 102145503 | CAP CERA DISC 25V .05 UF | 2 |
| 102245103 | CAP CERA DISC 25V .01 UF | 25 |
| 102444101 | CAP CERA DISC 100V 100 PF | 2 |
| 102444330 | CAP CERA DISC 1000V 33 PF | 12 |
| 102745511 | CAP CERA DISC 500V 510 PF | 2 |
| 102944033 | CAP CERA DISC 1KV 3.3 PF | 2 |
| 102944075 | CAP CERA DISC 1KV 7.5 PF | 4 |
| 102944100 | CAP CERA DISC 1KV 10 PF | 8 |
| 116515100 | CAP DIP MICA DM10 10 PF | 2 |
| 116515330 | CAP DIP MICA DM10 33 PF | 2 |
| 116515331 | CAP DIP MICA DM10 330 PF | 2 |
| | PUT IN IC BOX. | |
| 116515470 | CAP DIP MICA DM10 47 PF | 2 |
| 116545332 | CAP DIP MICA DM19 3300 PF | 2 |
| | PUT IN IC BOX. | |
| 140173337 | CAP TANT METAL CAN 330 UF | 2 |
| | PUT IN IC BOX. | |
| 140243336 | CAP TANT METAL CASE 33 UF | 2 |
| | PUT IN IC BOX. | |
| 140323335 | CAP TANT METAL CAN 3.3 UF | 2 |
| | PUT IN IC BOX. | |
| 140523334 | CAP TANT METAL CAN .33 UF | 2 |
| | PUT IN IC BOX. | |
| 140623333 | CAP TANT METAL CAN.033 UF | 2 |
| | PUT IN IC BOX | |
| 142824685 | CAP TANT DIP CASE 6.8 UF | 8 |
| 147147090 | CAP ALUM METAL CAN 90 UF | 1 |
| 147447050 | CAP ALUM METAL CAN 50 UF | 2 |
| 161335101 | RES CARBON FILM 100 OHMS | 10 |
| 161335102 | RES CARBON FILM 1 K | 26 |
| | PUT IN IC BOX. | |
| 161335103 | RES CARBON FILM 10 K | 8 |
| 161335104 | RES CARBON FILM 100 K | 4 |
| 161335111 | RES CARBON FILM 110 OHMS | 2 |
| 161335123 | RES CARBON FILM 12 K | 2 |
| 161335133 | RES CARBON FILM 13 K | 1 |
| 161335152 | RES CARBON FILM 1.5 K | 2 |
| 161335153 | RES CARBON FILM 15 K | 4 |
| | PUT IN IC BOX. | |
| 161335163 | RES COMP 1/4W 5% 16 K | 1 |
| 161335200 | RES CARBON FILM 20 OHMS | 2 |
| 161335201 | RES CARBON FILM 200 OHMS | 4 |
| 161335202 | RES CARBON FILM 2 K | 36 |
| 161335203 | RES CARBON FILM 20 K | 2 |
| 161335221 | RES CARBON FILM 220 OHMS | 2 |
| 161335242 | RES CARBON FILM 2.4 K | 4 |
| 161335301 | RES CARBON FILM 300 OHMS | 4 |
| 161335332 | RES CARBON FILM 3.3 K | 2 |
| 161335333 | RES CARBON FILM 33 K | 1 |
| 161335391 | RES CARBON FILM 390 OHMS | 2 |
| 161335392 | RES CARBON FILM 3.9 K | 2 |
| 161335393 | RES CARBON FILM 39 K | 1 |

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BMPSS
INPMS
BMRES

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| PART NUMBER | DESCRIPTION REMARK | QTY PER |
|-------------|------------------------------------|---------|
| 161335470 | RES CARBON FILM 47 OHMS | 8 |
| 161335472 | RES CARBON FILM 4.7 K | 4 |
| 161335510 | RES CARBON FILM 51 OHMS | 6 |
| 161335511 | RES CARBON FILM 510 OHMS | 8 |
| 161335512 | RES CARBON FILM 5.1 K | 2 |
| 161335681 | RES CARBON FILM 680 OHMS | 2 |
| 161335751 | RES CARBON FILM 750 OHMS | 4 |
| 161335911 | RES CARBON FILM 910 OHMS | 2 |
| 161445271 | RES CARBON FILM 270 OHMS | 1 |
| 161445470 | RES CARBON FILM 47 OHMS | 2 |
| 161555151 | RES COMP 1W 5% 150 OHMS | 1 |
| 161665150 | RES COMP 2W 5% 15 OHMS | 1 |
| 182527202 | RES VARI CERMET 2 K | 2 |
| 204042003 | IC LINE RECEIVER MC10115P | 2 |
| 204042004 | IC 2-3-2-IN GATE MC10105P | 2 |
| 208011003 | IC SINGLE OP AMP LM301AN | 1 |
| 208011004 | IC TIMER NE555 | 2 |
| 208031003 | IC VOLT COMPARATOR NE521A | 2 |
| 230110005 | DIODE SWITCHING 1N4448 | 33 |
| 235010005 | DIODE RECTIFIER 1N4005 | 1 |
| 240225702 | DIODE ZENER 2.7V 1N5986A | 2 |
| 240225703 | DIODE ZENER 3.6V 1N5989A | 2 |
| 240225705 | DIODE ZENER 4.7V 1N5992A | 2 |
| 240225706 | DIODE ZENER 5.6V 1N5994A | 2 |
| 240225707 | DIODE ZENER 6.8V 1N5996A | 4 |
| | SEND TO RSD PROD. FOR MATCHING. | |
| 253010835 | DIODE SCHOTTKY HP2835 | 22 |
| 256010102 | DIODE LED (RED) DIFF LENS | 2 |
| 270110001 | TRANSISTOR NPN PN2369A | 2 |
| 270110004 | TRANSISTOR NPN 2N4013 | 4 |
| 270140001 | TRANSISTOR NPN 2N3866 | 2 |
| 270170001 | TRANSISTOR NPN 2N5770 | 26 |
| 270190001 | TRANSISTOR NPN PWR 2N3054 | 1 |
| 275140545 | TRANSISTOR HF PNP MRF545 | 2 |
| 275170002 | TRANSISTOR PNP 2N5771 | 10 |
| 275170003 | TRANSISTOR PNP A441 | 2 |
| 300010001 | BEAD SHIELDING FERRITE | 14 |
| 300020001 | BEAD SHIELDING "1/2" SIZE | 3 |
| 300050001 | CHOKE FERRITE SINGLE LEAD | 3 |
| 400010008 | SOCKET IC SOLD TAIL DIP-8 | 3 |
| 400020014 | SOCKET IC SOLD TAIL DIP-14 | 2 |
| 400030016 | SOCKET IC SOLD TAIL DIP-16 | 4 |
| 402030000 | CONN CO-AX LEMO | 18 |
| 402030002 | SPANNER NUT SMALL OD LEMO | 18 |
| 402030003 | GROUND LUG NONLOCK LEMO | 8 |
| 405112001 | CONNECTOR BLOCK (PIN) | 1 |
| 405212002 | GUIDE PIN (MALE) | 1 |
| 405213001 | GUIDE PIN (MALE) | 1 |
| 405312001 | GUIDE PIN (FEMALE) | 2 |
| 405410016 | CONNECTOR PIN (MALE) | 7 |
| 405613001 | CONNECTOR HOOD | 1 |

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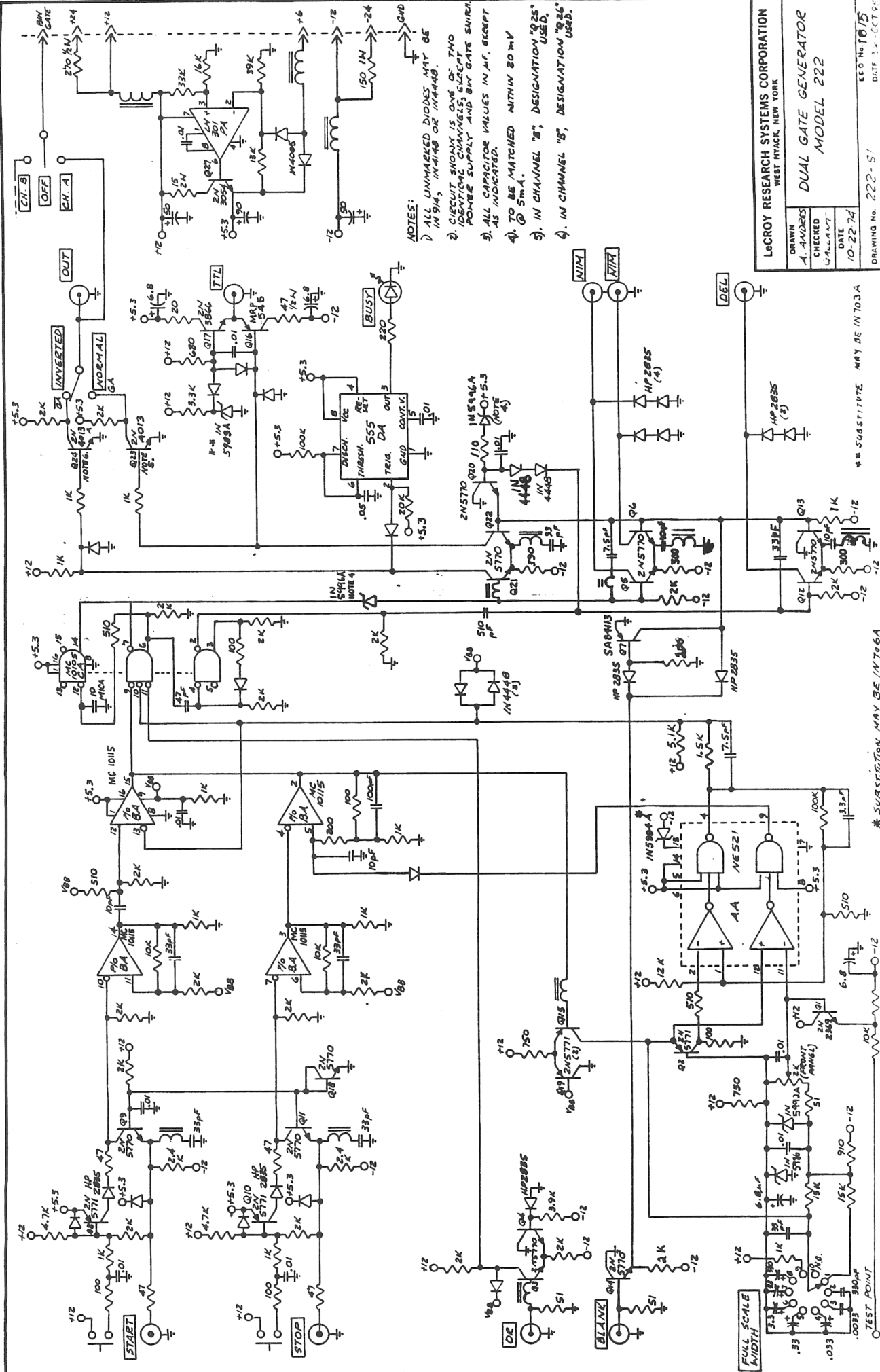
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| PART NUMBER | DESCRIPTION REMARK | QTY PER |
|-------------|---------------------------|---------|
| 410112102 | SWITCH TOGGLE SPDT | 2 |
| 410112203 | SWITCH TOGGLE SPDT | 1 |
| 412111002 | SWITCH ROTARY 1P10T | 2 |
| 416110001 | SWITCH PUSHBUTTON NO SPST | 4 |
| 468911001 | TEST POINT (JACK) WHT | 2 |
| 500120002 | TRANSIPAD "LARGE" | 4 |
| 519110002 | BUSHING LED BLK MP 52 | 2 |
| 520000510 | STANDOFF GLASS 8MM | 50 |
| 521400022 | SPACER ROUND #4 11/16 | 2 |
| 521400024 | SPACER ROUND #4 3/4 | 2 |
| 536142004 | KNOB ASSY, 3-PIECE BLACK | 2 |
| 540103102 | SIDE COVER NIM LEFT | 1 |
| 540103103 | SIDE COVER NIM RIGHT | 1 |
| 540105001 | BRACKET NIM WRAP SIZE #1 | 2 |
| 540109100 | SWITCH HOLE PATTERN COVER | 1 |
| 555611001 | CAPTIVE SCREW 6-32 | 2 |
| 555621002 | CAPTIVE SCREW RETAINER | 2 |
| 560440005 | SCREW PHILIPS 4-40X5/16 | 6 |
| 560440014 | SCREW PHILIPS 4-40X7/8 | 2 |
| 567256004 | SCREW FLAT PHIL 2-56X1/4 | 4 |
| 568440003 | SCREW FLAT PHIL 4-40X3/16 | 10 |
| 577400001 | WASHER SHAKEPROOF SIZE 4 | 4 |
| 580440001 | NUT HEX STANDARD 4-40 | 2 |
| 585141237 | RIVET "POP" ALU 1/8X.237 | 2 |
| 590001022 | WIRE TEFLON 7/30 BLK 22 | 2 |
| 590111022 | WIRE TEFLON 7/30 BRN 22 | 1 |
| 590221022 | WIRE TEFLON 7/30 RED 22 | 1 |
| 590331022 | WIRE TEFLON 7/30 ORA 22 | 1 |
| 590441022 | WIRE TEFLON 7/30 YEL 22 | 1 |
| 590551022 | WIRE TEFLON 7/30 GRN 22 | 1 |
| 590881022 | WIRE TEFLON 7/30 GRAY 22 | 1 |
| 590991022 | WIRE TEFLON 7/30 WHT 22 | 8 |
| 591101022 | WIRE BUS TIN-COPP AWG 22 | 1 |
| 594120001 | TIEWRAP | 3 |
| 595003018 | SLEEVING SHRINK BLK 3/32" | 1 |
| 595003104 | SLEEVING SHRINK BLK 3/8" | 1 |
| 595901022 | SLEEVING TEFLON AWG 22 | 2 |
| 710222013 | PC BD PREASS'Y 222 | 1 |
| 720222013 | FRONT PNL PREASS'Y 222 | 1 |
| 740222013 | WRAPAROUND NIM 1 222 | 1 |

End of report.

144 Details encountered.



- NOTES:
1. ALL UNMARKED DIODES MAY BE IN 9K, IN 4K OR IN 4K40.
 2. CIRCUIT SHOWN IS ONE OF TWO IDENTICAL CHANNELS, EXCEPT POWER SUPPLY AND BAY GATE SWIRL AS INDICATED.
 3. ALL CAPACITOR VALUES IN μ F, EXCEPT AS NOTED.
 4. TO BE MATCHED WITHIN 20 mV.
 5. IN CHANNEL "B", DESIGNATION "Q25" USED.
 6. IN CHANNEL "B", DESIGNATION "Q26" USED.

| | | | |
|---|----------------------------------|--------------------|---------------|
| LECROY RESEARCH SYSTEMS CORPORATION WEST HYDE PARK, NEW YORK | | | |
| DRAWN A. ANDERS | DUAL GATE GENERATOR MODEL 222 | | |
| CHECKED A. ANDERS | DATE 10-22-74 | DRAWING NO. 222-51 | |
| REVISION 10/15 | | | DATE 10-22-74 |

*** SUBSTITUTION MAY BE IN 703A

*** SUBSTITUTION MAY BE IN 706A

FULL SCALE
WIDTH
TEST POINT