TECHNICAL DATA

LeCroy

2277 DIGITAL COUNTER TIME-TO-DIGITAL CONVERTER

- 1 nsec LSB
- 16-Bit Range, 65 μsec Full Scale
- 32 Channels Per CAMAC Module
- Common START or STOP
- Multihit Capability, 16 Measurements (Hits)/Channel
- Leading and/or Trailing Edge, Allows Pulse Width Measurements
- 20 nsec Double Edge Resolution
- Zero Pedestal
- Chip Level Zero Suppression

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TDCs FOR HIGH RATE EXPERIMENTS

The 32-channel, CAMAC-based Model 2277 Digital Counter Time-to-Digital Converter (TDC) has been designed for a wide variety of timing applications. The module features a 16-bit dynamic range, 1 nsec LSB (750 psec R.M.S.) and a 16 element pipeline. The double edge resolution is below 20 nsec. The module is ideal for time measurements of drift chambers, time projection chambers or other detectors requiring time interval measurements with high accuracy.

The Model 2277 can be operated in either a COMMON STOP or COMMON START mode. At the end of the acquisition period, the time elapsed between each hit and the COMMON STOP or START along with the address of the associated channel may be read out via CAMAC. The data is automatically zero suppressed. A trigger port with prompt outputs is also provided.

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The Model 2277 Digital Counter TDC is a CAMAC instrument for the measurement of multiple time intervals, accurate to 1 nanosecond for time ranges up to 65 microseconds.

The times are measured with respect to a common reference time mark or "COMMON HIT", which can occur before or after the individual time signal (also called "HIT") inputs to be measured. This common reference concept is appropriate when the relative times between one input channel and any other input channel is of interest, since they are both measured with respect to a common time. It is also appropriate for absolute time measurements between the individual signal inputs and the reference itself.

Because many experiments will need many time measurements, the 2277 has incorporated a large number of independent signal channels (however, single measurements are just as appropriate). In addition, each individual input channel has a FIFO type buffer attached to it such that up to 16 hits can be recorded on the channel with respect to the common hit.

The 2277 inputs are an edge sensitive design. Consequently the polarity of the logic signal inputs is selectable. The module will record the time of the rising, falling, or both signal edges.

COMMON START AND COMMON STOP MODES

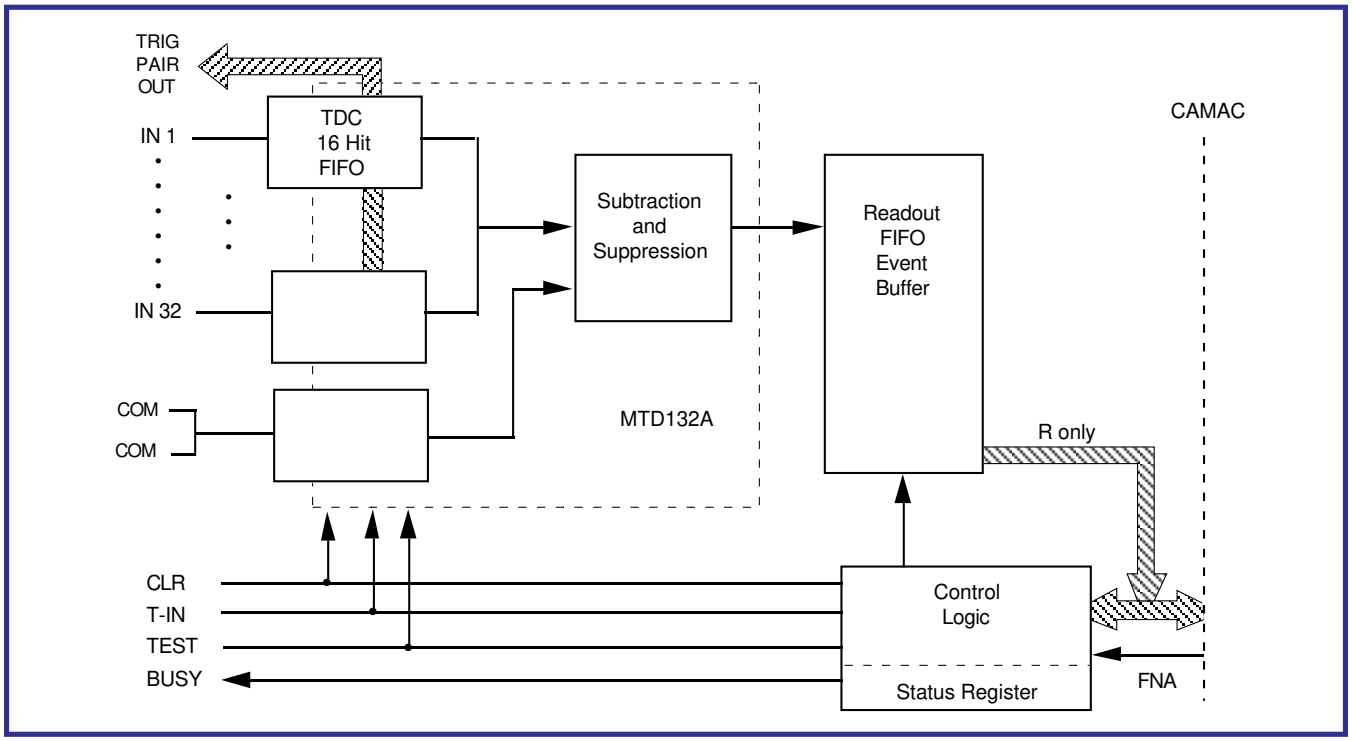
When the common reference time precedes the signal times, the 2277 is operating in a "COMMON START" mode. Alternatively, if the inputs precede the reference the "COMMON STOP" mode is used. Of course, by adding delays to the common or individual signals either mode can be used.

Common start mode is typically preferred in synchronous situations, such as colliding beam accelerators or pulsed laser experiments, when the time interval to be measured can be associated in time with a causal effect. In common start mode, a time window for the measurements must also be provided to terminate the measuring process. This can be internally generated in the 2277 or supplied from an external source via a front-panel input.

Common stop mode is better suited to continuous beam or randomly occurring events when a trigger decision is required.

OPERATION OF THE TDC

The 2277 must be configured and operated from CAMAC. The configuration of the module is determined by the status register. The data value stored in the register is decoded as a bit pattern (see Table 1). The bit pattern permits the mode selection, internal time window duration, edge sensitivity, test features and trigger output type. Once the status register is configured time measurement can be made.



Model 2277 Block Diagram

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The actual measurements are a combination of front panel signals and CAMAC commands. A typical operation sequence begins with a CAMAC Clear command or pulse on the CLR input. This readies the module for data taking. The registration of individual hits and common hits begins automatically. At the completion of the measurement, (a time-out in common start mode from the internal timer or front-panel T-IN input, or the arrival of a hit in common stop mode) the embedded data processor takes over. This processor primarily does two things. It combines the individual hit marks and the common mark to produce the time data desired, and it suppresses data which results in a zero or overflow condition. The accumulated data is passed to a readout FIFO in the 2277. During this process a BUSY signal is output from the front panel. The busy condition can also be monitored by CAMAC.

The data can now be read through CAMAC to the host computer. Readout is accomplished with a single CAMAC function code. The channel number associated with each data value is passed along with it. In fact, readout can begin as soon as the embedded processor has transferred the first word into the 2277 readout FIFO. In this way, "conversion" time and data transfer time can overlap, resulting in reduced dead time and increased data throughput. The readout is complete when both Busy and CAMAC Q are returned as zero.

If for some reason the data is not read, it can be cleared. This restarts the data acquisition cycle again.

TEST FEATURES

The 2277 contains an internal pulse generator so that signals can be injected to verify the behavior of each channel. The internal tester is controlled by the status register. In addition, there is a front panel TEST input so an external pulse generator can be used.

ADDITIONAL FEATURES AND APPLICATIONS

Prompt hit information is presented at the front panel TRIG PAIR OUT port for inclusion in first level trigger decisions. The input channels are paired and OR'd together. A hit on either channel of the pair produces a pulse or latched output bit. These outputs are designed to match the LeCroy ECLine programmable trigger logic standard.

By capturing both the leading and trailing edge time information, the 2277 can be used in a time-over-threshold technique to simultaneously determine time and charge from a given detector element. This low cost technique avoids many of the traditional problems of using ADCs and TDCs together.

This TDC is based on the LeCroy MTD132A Monolithic Time Digitizer chip. The 2277 is essentially identical to the Model 1176 VME TDC and is similar to the Model 1876 FASTBUS TDC. For this reason the 2277 is an ideal testbed for chamber developments.

SPECIFICATIONS

GENERAL

Channels: 32, differential ECL inputs with a recommended minimum width of 15 nsec. Impedance 112 Ω. Unused inputs/outputs are allowed to float.
COMMON START/STOP: Front-panel ECL 2-pin connectors; 112 Ω terminating resistors.
Range: 16 bits.
Full Scale: 65.535 µsec.
Sensitivity (Resolution): 1 nsec least count, (750 psec R.M.S.).
Double Edge Resolution: < 20 nsec.
Long Term Stability: 10 ppm/year.
Integral Non-Linearity: None (0%).
Differential Non-Linearity: < ±20%.
Digital Clear: 100 nsec.
Buffering: 4.3 µsec + 533 nsec per hit.
Data Format: 16 bits data, 1 bit edge polarity, 5 bits channel address.
Power: -24 V at 150 mA; -6 V at 1.65 A; +6 V at 1.7 A; +24 V at 22 mA.
Mechanical: #1 CAMAC Module according to IEEE-583 Standard.
Weight: 1.5 lbs. (0.7 kg).

FRONT PANEL LEDS

N:	Red LED indicates accessing module.
MODE:	Bicolor LED. Green indicates COMMON START. Red indicates COMMON STOP.
HIT:	Yellow LED indicates whether any channel received a hit.
COM HIT:	Green LED indicates whether a COMMON START/STOP was received.

INPUT SIGNALS

All inputs are differential ECL signal standard.

IN 0-31:	32 channel inputs.
COM:	2 bridged connectors.
CLR:	Clear; resets module - aborts conversion.

T-IN: Time out; terminates COMMON START acquisition window.

TEST: Used to provide test pulses to the odd and even numbered channels.

OUTPUT SIGNALS

TRIG PAIR OUT: 16 outputs - pairwise OR'd channels.

$\overline{\text{BUSY}}$: Indicates front end disabled due to buffering and readout.

CAMAC COMMANDS

F(0)•A(0): Read Data. Q = 1 if valid data. Q = 0 if FIFO is empty.

F(1)•A(0): Read Status Register.

F(8)•A(0): Test LAM. Q = 1 if LAM is set.

F(9)•A(0): Clear. F(9) does not affect status register.

F(10)•A(0): Clear LAM.

F(17)•A(0): Write Status Register.

F(24)•A(0): Disable LAM.

F(25)•A(0): Test Cycle.

F(26)•A(0): Enable LAM.

F(27)•A(0): Test "Buffering in Progress". Q = 1 if true.

F(27)•A(1): Test Busy. Q = 1 if Busy is true.

Notes

1. Any CAMAC command must be accompanied by a valid N (Station Number).
2. An X = 1 response is generated for any valid CAMAC command.
3. A LAM is generated when the module is ready for readout (when the buffering is computed).

STATUS REGISTER BIT CONFIGURATIONS

BIT(S)	CONTROL FUNCTION	PATTERN	VALUE
16	MODE	0	COMMON STOP
		1	COMMON START
15, 14, 13 Controlled	COMMON START TIMEOUT	000	Front Panel
		001	1024 nsec
		010	2048 nsec
		011	4096 nsec
		100	8192 nsec
		101	16384 nsec
		110	32768 nsec
		111	65536 nsec
12	HIT LEADING EDGE RECORDING	0	DISABLE
		1	ENABLE
11	HIT TRAILING EDGE RECORDING	0	DISABLE
		1	ENABLE
10	EVEN CHANNEL TEST INPUT	0	DISABLE
		1	ENABLE
9	ODD CHANNEL TEST INPUT	0	DISABLE
		1	ENABLE
8	TRIGGER MODE	0	PULSE
		1	LATCH
4, 3	TESTER HIT DURATION	00	128 nsec
		01	256 nsec
		10	1024 nsec
		11	2048 nsec
2, 1	TESTER HIT BURST	00	1 hit
		01	2 hits
		10	4 hits
		11	8 hits

Table 1

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