OPERATOR'S MANUAL

MODEL 3001
QVT MULTICHANNEL
ANALYZER

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LeCroy

Innovators in Instrumentation

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CAUTION

INSTALLATION

Nim Bin power should be turned off during insertion or removal of modules to avoid possible damage caused my momentary misalignment of contacts.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation, packaged separately, should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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LeCroy is committed to providing state–of–the–art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up–to–date circuitry.

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All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department in your area.

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2 PRODUCT DESCRIPTION

GENERAL

The Model 3001 is a multichannel analyzer that can histogram any one of three parameters: charge (area), voltage (peak), and time (start/stop). The 10-bit ADC used for the Q (charge) mode has a sensitivity of 0.25 pC/channel, directly compatible with photomultiplier anodes pulses, thus obviating the need for a charge-sensitive preamplifier. In the Q mode, the input current is integrated for a duration ranging from 20 nsec to 1 μsec. A front-panel-adjustable internal gate is generated by either an internal or an external trigger, or an external gate pulse may be directly applied to the MCA. Operating in the Internal mode, the Model 3001 is a standalone device, possessing an internal discriminator of 1 mV minimum threshold. The Q input is terminated in 50 Ω and all analog circuitry is DC-coupled, thus eliminating the need for DC restoration instrumentation. The front-panel layout is shown in Figure 1.

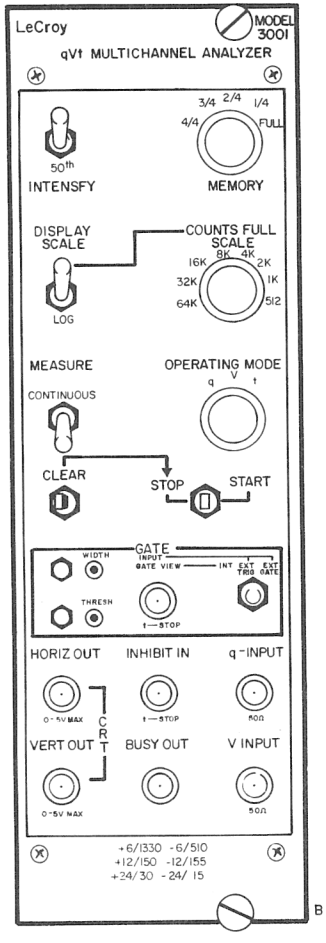

Figure 1
Front Panel Layout

The 10-bit TDC used for the T (time) mode of the Model 3001 digitizes time intervals by the start-stop technique and stores their spectra. Full-scale time intervals are 102 nsec and 1024 nsec, offering respective resolutions of 100 psec/channel and 1 nsec/channel. The start and stop inputs are leading edge triggered, responding to fast NIM (negative) signals. Uses of the T mode include time of flight, counter timing, and delay measurement, β-γ time correlation spectra, and drift chamber calibration.

In the V (voltage) mode, the output of any voltage source, e.g., a charge-sensitive preamplifier, may be analyzed. The maximum (peak) voltage of signals >50 nsec risetime applied to the input during the gating interval is digitized, thus making external stretching circuits unnecessary. The full-scale input in the V mode is +1 V (+10 V is switch selectable), offering a resolution of 1 mV (10 mV) consistent with that of a Si(Li) detector. The internal gate may be extended to 5 μsec in this mode.

Each of the 1024 channels has a count capacity of 16 bits (65,535). The contents may be displayed in log/linear fashion on any X-Y oscilloscope. The display is active on a time-available basis, thus affording display during data accumulation. A front-panel switch selects intensification of every 10th or 50th channel. Data may be accumulated and displayed in selected 256-channel quadrants or in the full 1024-channel memory. In addition to both an internal and external trigger capability with variable gate width, the 3001 provides external gate and inhibit inputs, which are also used as start and stop inputs in the time mode.

Rear-panel digital outputs are supplied to allow for data transfer to interface options including a readout device (e.g., printer) or a CAMAC Dataway. The output connector may also be used to load or increment any one of the 16-bit words in memory. This feature allows the 3001 to be used as an additional 1024 words of memory and to act as a histogram display module.

SPECIFICATIONS

Analysis Modes:

Q: Current integrating (charge sensitive); integration interval 20 nsec to 1 μsec; full scale, 256 pC ±10%; sensitivity, 0.25 pC/channel.

V: Peak voltage; input signal risetime, ≥50 nsec; full scale, +1 V or +10 V ±10%, internal switch selectable; resolution, 1 mV or 10 mV/channel; external gate width, 100 nsec minimum to 1 μsec or, switch selectable, 5 μsec maximum.

T: Time interval (Start/Stop); full scale internally switch-selectable, 102 or 1024* nsec ±10%; resolution, 100 psec and 1 nsec respectively.

Number of Channels: 1024 (10 bits); 256 (8 bits) in quadrants; overflow counts are stored in the last address of the selected memory segment.

Memory Size: 16 bits - 1 per channel (65,535 counts).

Digitizing Time: 12 μsec +0.05 μsec/channel.

Temperature Stability: ±.03% of full scale/°C.

Long-Term Stability: ±0.2% of full scale/week, maximum.

Integral Non-linearity: ±0.25% of reading ±2 channels.

Display: 100 sweeps/sec.

Channel Intensification: Every 10th or 50th channel, front-panel selectable.

Physical Characteristics

Packaging: #2 width, RF-shielded NIM-standard module.

Voltages Used: ±24 V, ±12 V (Note: a rear-panel switch permits operation from ±6 V (if available) instead of ±12 V.)

* Range 120 to 1120 nsec.

Current Requirements:

+24 V at 24 mA	−24 V at 125 mA
+12 V at 6 mA	−12 V at 127 mA
+6 V at 1.35 A	− 6 V at 510 mA

Note: ±6 V requirements add to ±12 V requirements when ±6 V option is unused.

CONTROLS AND CONNECTORS

Operating Mode: One of the three analysis modes (Q, V, or T) is selectable by a 3-position switch.

Trigger Mode: A 3-position switch selects internal trigger operation (INT), External Trigger operation (EXT TRIG), or operation via an externally-applied gate pulse (EXT GATE).

Gate Width: Front-panel multiturn gate width control for Internal and External Trigger mode operation with range of 20 nsec to 1 μsec (5 μsec switch-selectable in longer time range). Setting stability ±1% or 1 nsec, whichever is greater. Output monitors permit switch-selectable viewing of internal gate pulse for precise adjustment. Lower level discriminator triggers internal gate.

Threshold: Front-panel screwdriver-adjustable potentiometer determines threshold setting in internal trigger (INT) mode. Range, −1 mV to −15 mV in Q mode, +1 mV to +15 mV in V mode. Front-panel monitor point gives output voltage equal to 1000× actual threshold setting. Threshold stability <0.2%/°C over 20°C to 60°C operating range.

Memory Select: Full-1/4-2/4-3/4-4/4 In the Full position, all 1024 channels accept and display input data.

In the 1/4 position, the first quadrant (256 channels) accepts and displays input data. Full-scale range settings remain the same (i.e., 256 pC, +1 V, and 102 or 1024 nsec); similarly 2/4, 3/4, 4/4.

Clear: Front-panel spring-return toggle clears all memory and register. Start/Stop switch must be simultaneously placed in stop position.

Start/Stop: Front-panel 2-position, spring-return toggle switch. Start position initiates new measurement cycle after a Stop or Clear. Stop position stops measurement cycle.

Continuous/Stop at Overflow: A 2-position switch either permits continuous data collection and display or limits each channel to a full scale capacity.

Display LIN/LOG: Selects linear or logarithmic display.

Intensify: Either every 10th or every 50th channel is intensified on the display, determined by a front-panel 2-position switch.

Vertical Gain: In LIN (linear) mode, an 8-position switch selects a maximum number of counts to be displayed per channel, between 512 and 65K.

Front-Panel Inputs

Q Input: Analog input; 50 Ω impedance; DC coupled. Accepts input charge of 0 to 256 pC. Voltage range 0 to −1 V. Protected to ±100 V.

V Input: Analog input 50 Ω impedance (93 Ω optional). Accepts input voltage of 0 to +1 V (with switch selection 0 to 10 V range). Protected to ±100 V.

Gate Input/Output: One common front-panel connector; functionally controlled by trigger mode switch; requires −600 mV signal into 50 Ω.

In External Gate, the internal gate is triggered by the leading edge of the fast NIM signal applied to this connector (minimum trigger width, 10 nsec).

In the time mode, the leading edge of Start input begins the start-stop time measurement; minimum pulse width, 10 nsec. External trigger mode only.

Inhibit/Stop: One common front-panel connector; requires −600 mV into 50 Ω.

In the Q and V modes conversion is inhibited by application of a NIM inhibit signal. This level must be established before, and persist at least 20 nsec after the leading edge of the gate trigger. Inhibit is ignored after conversion is begun.

In the time mode, leading edge of stop pulse terminates the interval measurement; minimum pulse width, 10 nsec.

Front-Panel Outputs

Threshold Test Point: Reads 1000× preset threshold value in Internal mode operation.

Internal Gate View: Internally generated gate is available for oscilloscope monitoring on the Gate Connector when Internal Trigger is selected. Amplitude: −100 mV.

Internal Gate Test Point: Internally-generated gate is available for oscilloscope monitoring when Internal or External Trigger mode is selected. Amplitude: −200 mV.

Busy: TTL low level output during conversion time.

Horizontal Out: Horizontal deflection voltage for CRT proportional to channel number; 0-5 V for full or quadrant display. Minimum load impedance 1 kΩ.

Vertical Out: Vertical deflection voltage for CRT proportional to number of counts. Linearity ±0.2% of full scale. Full-scale output of 5 V corresponds to 200 dB/V in the log mode. Minimum load impedance 1 kΩ.

Rear-Panel Outputs

Connector Type: 44-contact card-edge connector; mates with AMP 5682358-2 (hood number 530087-4).

Memory Overflow (22): A high TTL level* indicates channel overflow. Available during memory load only.

External Enable (4): Low TTL level enables external functions accessed by the rear connector.

External Memory Address Latch (R): The trailing edge of a positive-going TTL* pulse of minimum duration 200 nsec latches the address applied to the 10 Memory Address lines (A,B,C,D,E,F,H,J,K,L) corresponding to 2^0 to 2^9 respectively.

Memory Enable (21): TTL high level* causes the contents of the memory address latches in lines A-L to be loaded into the internal incrementing register. A low level permits loading of the 16-External Data Input levels into the 16-External Data Input levels** into the Incrementing Register as follows.

Pin	6: 2^0	Pin	10: 2^4	Pin	14: 2^8	Pin	18: 2^{12}
	5: 2^1		9: 2^5		13: 2^9		17: 2^{13}
	7: 2^2		11: 2^6		15: 2^{10}		19: 2^{14}
	8: 2^3		12: 2^7		16: 2^{11}		20: 2^{15}

External Load (N): A low TTL level latches the Internal Incrementing Register. Data must be quiescent during load interval. Minimum duration 200 nsec.

External Read/Write (M): Causes data to be read from the memory to the Internal Incrementing Register or written in memory from the Internal Incrementing Register. Low for read, high for write.*

Incrementing Register (P): Leading edge of positive going TTL level causes the contents of the incrementing register to be incremented by 1.

*TTL levels: Low -0.8 V; High -2.0 V.

3 INSTALLATION

POWER SELECTION

The Model 3001 utilizes ±6 V, ±12 V, and ±24 V. Because some NIM bins do not supply ±6 V, internal supplies, operating off of the ±12 V supplies have been incorporated in the QVT. A rear-panel switch selects this feature. Note that the current required for the ±6 V sections is then drawn from the ±12 V supplies.

INSTALLATION

The Model 3001 may be installed in any position in the NIM power bin. Bin power should be turned off during insertion or removal of the instrument.

DISPLAY CONNECTION

The Horizontal Out and Vertical Out connectors of the Model 3001 supply 0 to +5.0 V. Intensification of every 10th or 50th channel is selected by the Intensification switch. Channel intensification is accomplished by pausing. Any oscilloscope capable of X-Y operation may be used. The oscilloscope should be used with unterminated (high impedance) inputs to use the 0 to +5.0 V calibration of the 3001's outputs.

4 OPERATING INSTRUCTIONS

GENERAL

Select Display Mode

The Display Scale switch selects the mode of display. On the LIN position, the display is linear with a full scale (+5.0 V) as set by the Counts Full Scale switch. In the LOG position, the display is logarithmic the +5.0 V corresponding to LOG 65.5 K counts. In the LOG display mode, the Counts Full Scale switch is inactive.

Accumulation and Memory Clear

After the Start/Stop switch is placed in the Start position, the Model 3001 will accept data. It will remain live until it receives a Stop command. When the Measure switch is in the Stop At Overflow position, the analyzer generates a Stop when the content of any channel exceeds the capacity of the memory. (If the Measure switch is in Continue, the analyzer memory will overflow but will continue acquisition). A Stop command is also generated when the Start/Stop switch is placed in the Stop position.

The memory display of the 3001 remains active at all times. A slight flicker is discernible only at very high input rates. The portion of memory in use (full or quadrant) will be cleared (set to zero) by moving the Clear switch to the right (Clear position) and simultaneously moving the Start/Stop switch to the left (Stop position). This is a protection feature to guard against inadvertent clear of the memory.

Memory Control

The Memory switch allows the user to select the part of the memory he wishes to use. In the Full position, the entire 1024 channels are used for both histogramming and display. In the 2/4 position only channels 256 to 511 (Quadrant 2) are used, etc. When the analyzer is operated in the quadrant mode, the Clear operation effects only the quadrant in use.

OPERATING MODES

The Operating Mode switch selects the Q, V, or T mode. It allows the operating controls, inputs, and outputs, to have varying functions. Those described above, however, are independent of the Operating Mode. Operation of the 3001 in each of the three modes will be discussed below.

Q Mode

The Q Mode is intended for analysis of photomultiplier anode signals without amplifying or shaping. Analog-to-digital conversion is performed on the quantity of charge received at the Q-Input within a well defined time interval. A gate pulse (internally or externally generated) activates a linear gate and allows the current at the Q-Input to be integrate on a capacitor. Thus the analog "pulse height" is stored for ADC. The input imped-

ance of the Q–Input is 50 Ω. This mode exhibits best stability when driven from source impedances >1 kΩ such as a photomultiplier.

Q Mode Gating

An internal gate generator may be used to generate gates in the Q Mode. This generator may be triggered either by an internal discriminator operating on the analog input signal (Internal Mode) or by an externally applied NIM logic pulse on the Gate Input (Event Trigger Mode). An externally applied NIM pulse derived from external logic may be applied as the gate pulse (External Gate Mode).

Gate Width Control

The gate generator is a triggerable monostable whose output may be adjusted by a 22–turn front–panel Gate Width potentiometer. Fully counter–clockwise, this control sets a gate width of approximately 20 nsec and fully clockwise, it sets a width of >1 μsec. The actual gate width can be determined by viewing the NIM gate pulse at the test point adjacent to the Gate Width potentiometer. In the Internal mode, the Gate Input/Gate View connector serves as an output of the gate pulse with an amplitude of approximately –100 mV. The test point and Gate View outputs supply gate pulses whenever the gate generator is triggered.

Internal Gate Trigger

In the Internal Gate trigger mode, an internal discriminator on the analog signal is used to trigger the gate generator. The discriminator level is set by the 22–turn Threshold potentiometer. Set full counter–clockwise, a threshold of approximately –1 mV is obtained. Fully clockwise, the threshold is approximately –20 mV. The test point adjacent to the input Threshold potentiometer gives a voltage approximately 1000× the threshold. No connection should be made to the Input of the module when measuring the threshold.

In Internal Gate trigger mode, the Gate Input/Gate View connector serves as monitor output giving a –100 mV output (into 50 Ω) each time the 3001 gate generator is fired. The Inhibit In connector allows the output of the internal discriminator to be inhibited. A NIM pulse of 10 nsec minimum duration should be applied simultaneously with the leading edge of the analog input pulse at the Q–Input to inhibit. The Gate Inhibit inputs are ignored after conversion has begun.

External Gate Trigger

Operation in the External Trigger Mode is intended for applications in which a somewhat more extensive trigger is required. In this mode, a NIM pulse applied to the Gate Input is used to trigger the internal gate generator. The Inhibit In input accepts

NIM pulses which may be used to veto the trigger. The internal discriminator is therefore defeated in this mode. The leading edge of the gate trigger pulse should occur 3 nsec after the leading edge of the analog input at the Q–Input connector.

A NIM inhibit pulse of minimum 10 nsec duration should be applied simultaneously with the leading edge of the Gate Trigger pulse in order to inhibit conversion. The Gate and Inhibit inputs are ignored after conversion is begun.

External Gate Application

In the External Gate Mode, the 3001 accepts an external gate pulse rather than employing the internal gate generator. In fact, the Width setting has no effect on performance in this mode. The integration time in this mode is equal to the width of the gate pulse. Gates as short as 10 nsec may be used. Because of internal delays, the leading edge of a NIM pulse must be applied to the Gate Input 3 nsec after the leading edge of the Q–Input analog pulse.

Note that this requires 5 nsec of additional signal delay as compared with Model 2249A operation. The Inhibit Input requires a NIM pulse of 10 nsec minimum duration in order to inhibit the gate pulse. The leading edge of the Inhibit pulse should be coincident with the leading edge of the gate pulse. After conversion has begun, the Gate and Inhibit inputs are ignored.

Q Mode Input Signals

The Q Input is terminated in 50 Ω. Because of the high speed nature of this mode, attention should be paid to proper impedance matching throughout the system. The reflections caused by impedance mismatches will cause a loss of resolution.

The Q Input accepts negative analog signals. Signals as large as −20 mA (1 V into 50 Ω) are handled linearly. Larger signals cause a gradual deviation from linearity. Input signals of 2 V, for example, register approximately 10% lower than 1 V signals of twice the duration. The input is protected against ±100 V transients of duration ≤1 μsec. Although such transitions will not cause circuit damage, they may, however cause the data in the analyzer to become disturbed.

Q Mode Slope and Pedestal

The action of the charge sensitive ADC in the Model 3001 is to produce a digital output, related to the input charge Q by the relationship:

$$q = S(N-N_0) \qquad (N \geq N_0)$$

Here S is the slope, approximately 0.25 pC/count or 1 pC/count in the full or quadrant modes respectively. N_0 is the pedestal or the channel number obtained for a conversion with no Q signal. Pedestal also depends upon the output impedance of the signal source. Although S is fixed, N_0 is not.

Increasing the gate width will cause an increase in the pedestal. A trimmer capacitor mounted on the analog board adjacent to the QT100M hybrid affords pedestal adjustment over a range of approximately 50 counts.

In general, a pedestal >0 counts is advantageous in that it allows the experimenter to be aware of the origin of his histogram. This is of particular significance for the Model 3001 in that it maintains linearity even in the first few channels above pedestal.

V Mode

The V Mode is intended for analysis of the output of voltage sources such as spectroscopy amplifiers or Mossbauer velocity drives. Analog-to-digital conversion is performed upon the maximum voltage within the gating interval. The input impedance of the V Input is either 50 Ω or 93 Ω. Because the V Input is intended for slower signals, the gate timing is less critical.

V Mode Gating

An internal gate generator may be used to generate gates in the V Mode. This generator may be triggered either by an internal discriminator on the analog input signal (Internal Mode) or by an externally applied NIM logic pulse on the Gate Input (External Trigger). An externally applied NIM pulse derived from external logic may be applied as the gate pulse (External Trigger Gate).

Gate Generator

The gate generator may be adjusted by a 22-turn front-panel Gate Width potentiometer. Fully counter-clockwise, this control sets a gate width of approximately 20 nsec and fully clockwise, it sets a width >1 μsec. The minimum gate width for V Mode operation is 100 nsec. The actual gate width can be determined by viewing the NIM gate pulse at the test point adjacent to the Gate Width potentiometer. In the Internal mode, the Gate Input Gate View connector serves as an output of the gate pulse with an amplitude of approximately −100 mV. The test point and Gate View outputs supply gate pulses whenever the gate generator is triggered.

Internal Gate Trigger

In the Internal Gate trigger mode, an internal discriminator on the analog signal is used to trigger the gate generator. The discriminator level is set by the 22-turn Threshold potentiometer. Set fully counter-clockwise, a threshold of approximately +1 mV is obtained. Fully clockwise, the threshold is approximately +20 mV. The test point adjacent to the input Threshold potentiometer gives a voltage approximately 1000× the threshold. No connection should be made to the Q Input.

In this mode, the Gate Input/Gate View connector serves as a gate view output giving a −100 mV amplitude gate output (into 50 Ω) each time the Model 3001 gate generator is fired. The Inhibit In connector allows the output of the internal discriminator to be inhibited. The Inhibit pulse, a NIM pulse, should overlap the gate for proper operation. The Gate Inhibit inputs are ignored after conversion is begun.

External Gate Trigger

Operation of the External Trigger Mode is intended for applications in which a somewhat more extensive trigger is required. In this mode, a NIM pulse applied to the Gate Input is used to trigger the internal gate generator. The Inhibit In input accepts NIM pulses which maybe used to veto the trigger. The internal discriminator is therefore defeated in this mode. The leading edge of the gate trigger pulse should be coincident in time with the leading edge of the analog input at the V-Input connector.

A NIM inhibit pulse of minimum 10 nsec duration should be applied simultaneously with the leading edge of the Gate Trigger pulse in order to inhibit conversion. The Gate and Inhibit inputs are ignored after conversion is begun.

External Gate Application

In the External Gate Mode, the 3001 accepts an external gate pulse rather than employing the internal gate generator. In fact, the Width setting has no effect on performance in this mode. The peak search time in this mode is equal to the width of the gate pulse. Gates as short as 100 nsec may be used. Because of internal delays, the leading edge of a NIM pulse applied to the Gate Input should be coincident with the leading edge of the V Input analog pulse. The Inhibit Input pulse will veto a gate pulse if a NIM level is present coincident with the leading edge of a gate pulse and persists for at least 10 nsec.

V Mode Input Signals

The V Input is terminated in 93 Ω and accepts input signals of 50 nsec risetime or greater. Generally, Gaussian shaped pulses are used as analog inputs, but the 3001 allows other shapes also. For example, a ramp input may be used. If no peak is ob-

tained during the gating interval, the maximum voltage will be analyzed.

The V Input accepts positive analog signals. The range of the ADC for this mode allows signals to 1 V. Larger signals give an off-scale result and are treated as a full scale (ch 1024) signal. The input is protected against ±100 V transients of ≤1 μsec duration. Although such transients will not cause circuit damage, they may, however, cause the date in the analyzer to become disturbed.

V Mode Slope and Pedestal

The action of the peak sensing ADC in the Model 3001 is to produce a digital output, N, related to largest voltage in the gate interval by the following relationship:

$$V = S(N-N_0) \qquad (N > N_0)$$

Here S is the slope, approximately 1 mV/count or 4 mV/count in the full or quadrant modes respectively. N_0 is the pedestal or the channel number obtained for a conversion with the V Input open. Although S is fixed, N_0 is not. Increasing the gate width will effect the pedestal in the V Mode only slightly.

T Mode

In the T Mode, the Gate switch must be in the External Trigger position. In this mode, the Gate Trigger input is the T Start input and the Inhibit input is the T Stop input. The time between the T Start and T Stop pulses is digitized without the use of a time-to-amplitude converter (TAC).

A side-panel switch is used to select the full scale time. Two ranges are available: 100 nsec full scale (0 to 100 nsec) and 1 μsec full scale (100 nsec to 1100 nsec). Two spare switch positions are supplied to allow selection of alternate conversion gains. Full scale time may range from 100 nsec minimum to 7 μsec maximum. Selection of resistance values R for alternate gains is based on the following relationships:

$$R(\text{in } k\Omega) \simeq 1.97 \cdot 10^{10} \cdot \text{conversion gain (in nsec/count)}$$

The allowed range of conversion gain is from 0.1 nsec/count to 6 nsec/count. This results in a minimum value for R of 1.97 kΩ and a maximum value of 118 kΩ.

A pedestal of approximately 14% of full scale must be provided externally because of the inherent negative pedestal of the system. The required external time pedestal can be calculated in the following way:

> Pedestal (in nsec) $\simeq$ 140 $\times$ conversion gain (in nsec/count)
>
> Example: conversion gain = 6 nsec/count
> required pedestal = 840 nsec

Therefore, at the selected gain of 6 nsec/count the measuring range for T will extend from approximately .84 µsec to 6.84 µsec.

At any time of operation, only one time range should be selected. The following diagram illustrates positions for alternate conversion gain components. Access to the PC board illustrated in Figure 2 is gained by sliding back the right hand side cover having the cutout that exposes the T Mode range select switch. For best results use a 1% resistor value. A second resistor position is provided in each of the two alternate gain locations for a fine trim of the gain if desired.

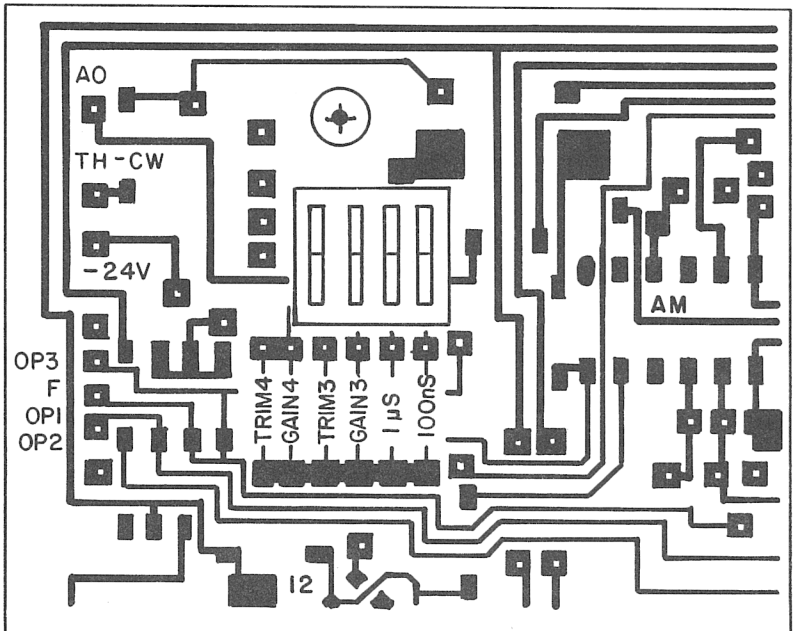

Figure 2
Location of T Mode Range Selection Switch

EXTERNAL CONTROL

The following is a list of signals provided at the QVT rear-panel connector. Usage in the LeCroy Model 2301 CAMAC interface and the Model 3157 printer interface (discontinued) is indicated.

Digital Input/Output

The digital connector, (J2) on the 3001 is a 44-contact edge-connector which mates with AMP connector number 582358-2. The contacts are named A through Z (excluding G, I, O and Q) and 1 through 22. The extreme contacts, A, Z, 1 and 22 are labeled on the board. All signals are TTL standard. Read-out, writing in and histogramming may be performed through this connector. The details and definitions of each of the 44 input or output requirements are described in the next section.

A block diagram of the memory and register section of the 3001 is shown in Figure 3.

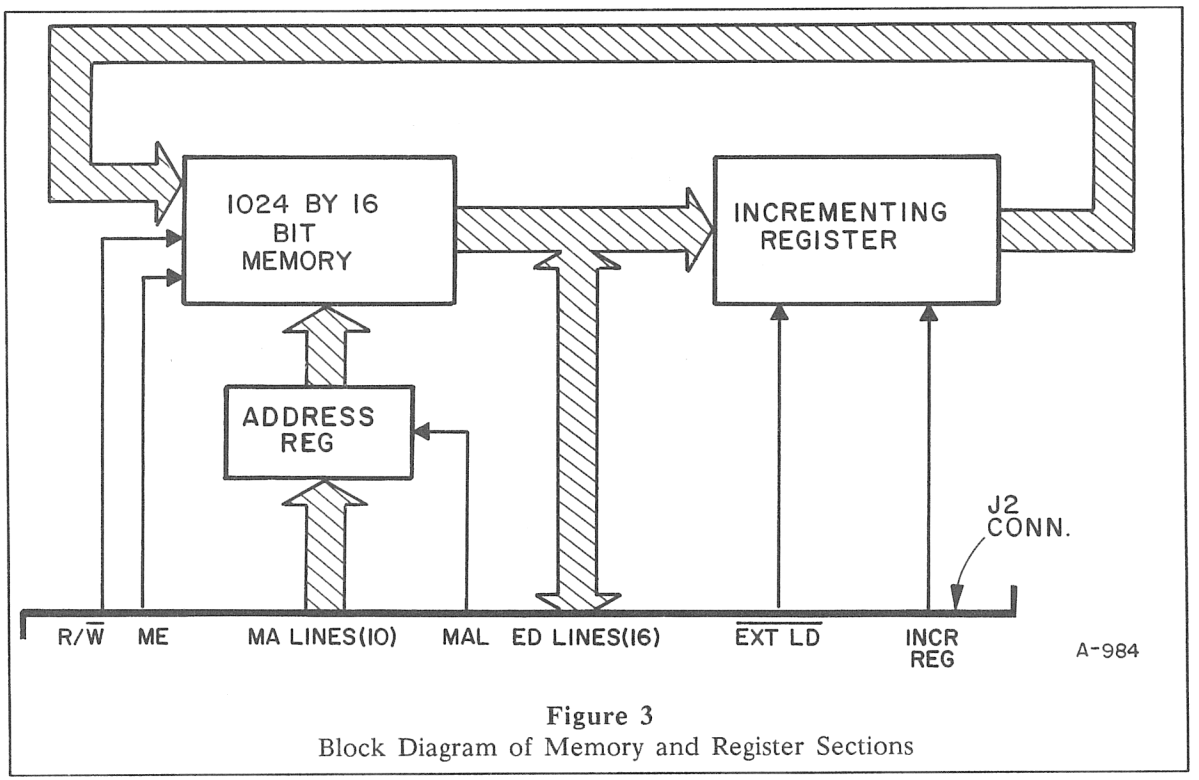

Figure 3
Block Diagram of Memory and Register Sections

Data may be read or written into any channel of the 3001 by latching an address into the Memory Address Latch and supplying the appropriate strobes.

A pedestal of approximately 14% of full scale must be provided externally because of the inherent negative pedestal of the system. The required external time pedestal can be calculated in the following way:

Pedestal (in nsec) $\simeq$ 140 $\times$ conversion gain (in nsec/count)

Example: conversion gain = 6 nsec/count
required pedestal = 840 nsec

Therefore, at the selected gain of 6 nsec/count the measuring range for T will extend from approximately .84 μsec to 6.84 μsec.

At any time of operation, only one time range should be selected. The following diagram illustrates positions for alternate conversion gain components. Access to the PC board illustrated in Figure 2 is gained by sliding back the right hand side cover having the cutout that exposes the T Mode range select switch. For best results use a 1% resistor value. A second resistor position is provided in each of the two alternate gain locations for a fine trim of the gain if desired.

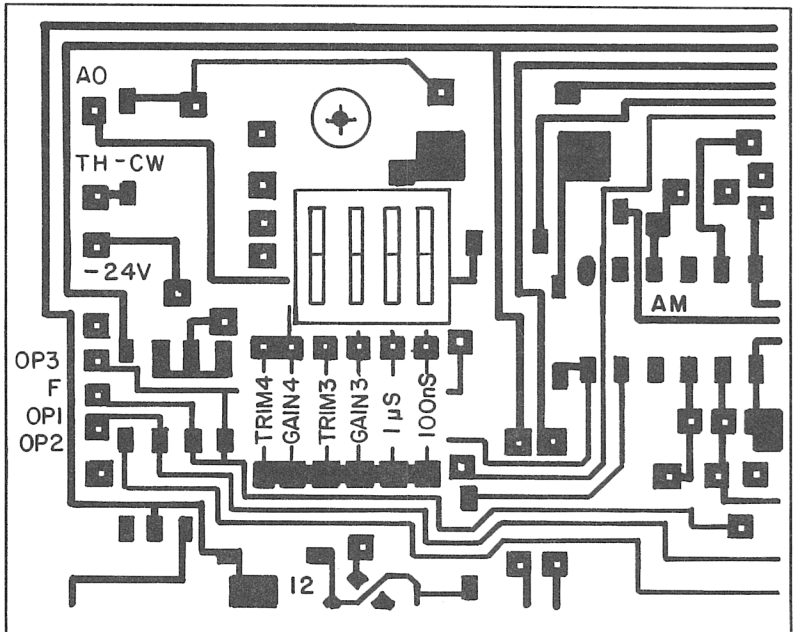

Figure 2
Location of T Mode Range Selection Switch

EXTERNAL CONTROL

The following is a list of signals provided at the QVT rear-panel connector. Usage in the LeCroy Model 2301 CAMAC interface and the Model 3157 printer interface (discontinued) is indicated.

Digital Input/Output

The digital connector, (J2) on the 3001 is a 44-contact edge-connector which mates with AMP connector number 582358-2. The contacts are named A through Z (excluding G, I, O and Q) and 1 through 22. The extreme contacts, A, Z, 1 and 22 are labeled on the board. All signals are TTL standard. Read-out, writing in and histogramming may be performed through this connector. The details and definitions of each of the 44 input or output requirements are described in the next section.

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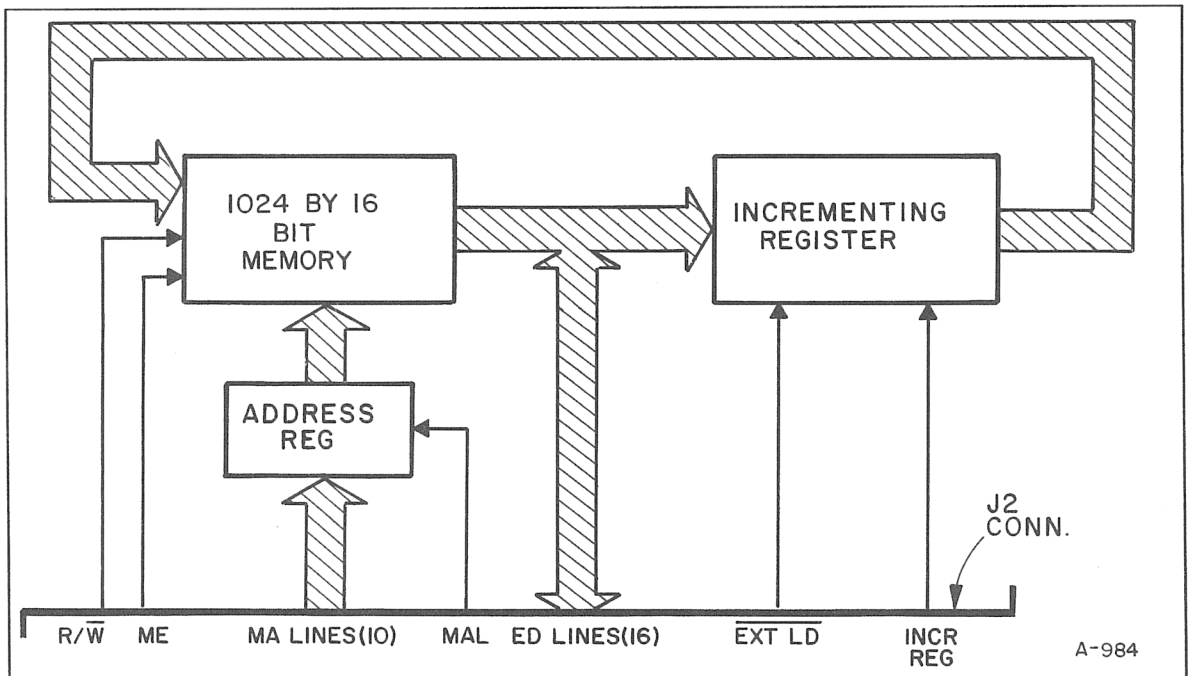


Figure 3
Block Diagram of Memory and Register Sections

Data may be read or written into any channel of the 3001 by latching an address into the Memory Address Latch and supplying the appropriate strobes.

Latching Into the Memory Address Latch

In order to read out or write into the memory of the 3001, it is necessary to latch an address into the Memory Address Latch. The procedure is shown in Figure 4. The memory address lines should be driven from either an open collector or tri-state source activated by a low level on the external line.

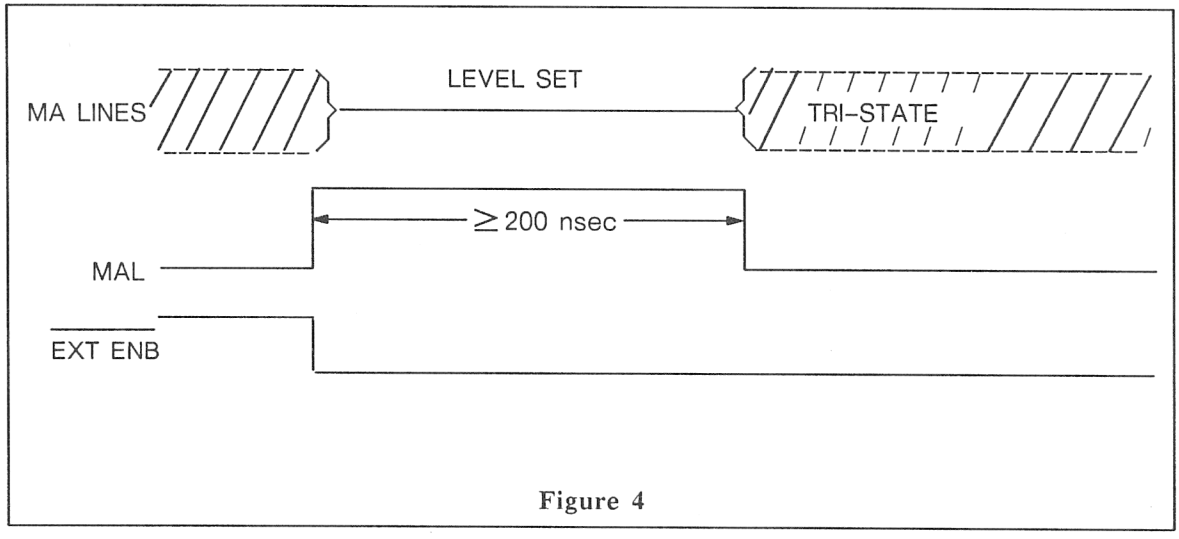


Figure 4

Writing Into the Model 3001

In order to write into the Model 3001, data must also be latched into the Incrementing Register by the EXT LD pulse. Data levels may be set on the ED lines only after the memory is disabled (ME low).

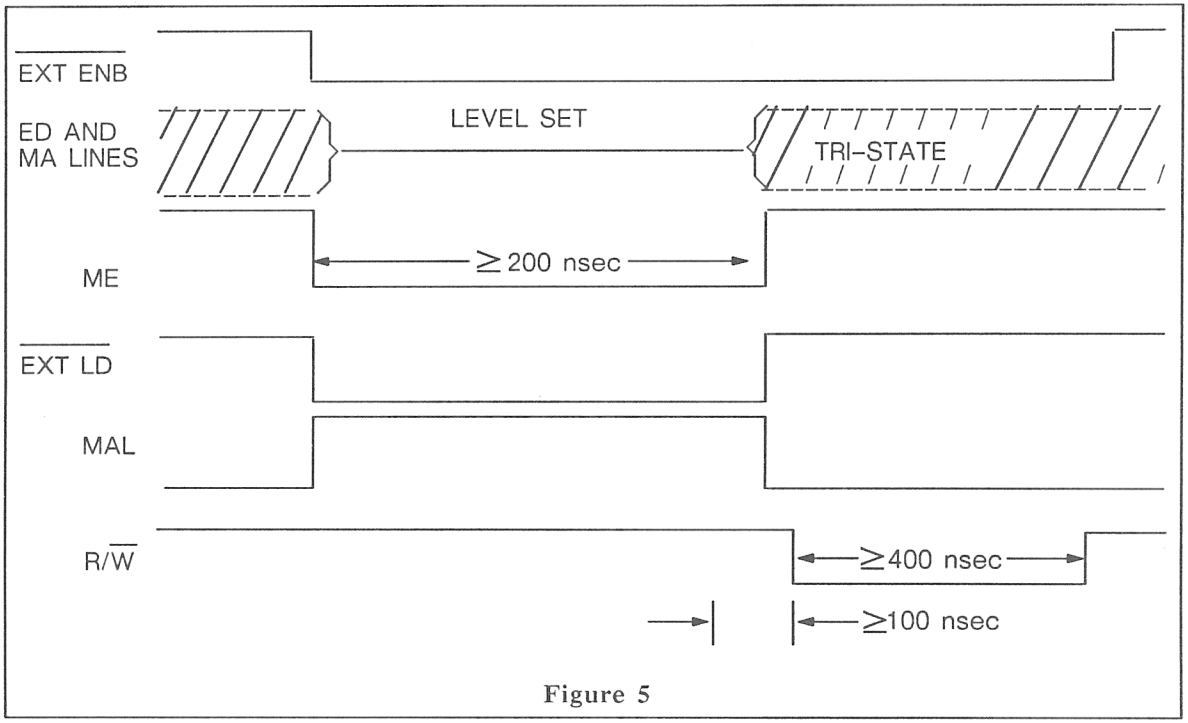


Figure 5

J2 Connector Contact Usage

Signal	2031	3157	Designation	Pin #	Characteristic
Memory Address	X	X	MA-0	A	Least significant bit of memory address, a positive true TTL level. When used as input address, data must be supplied by an open collector or Tri-state driver. Internal 2 k Ω pull-up resistors are provided in the MCA. The transmission of address must be enabled only when the EXT.EN. is low. Address is read into the Address Register on negative going transition of MAL (pin R). The line serves as a memory address output when EXT.EN. is high. Logic is positive true. The line will drive one low power TTL load.
Memory Address	X	X	MA-1	B	As above but 2^1 bit
Memory Address	X	X	MA-2	C	As above but 2^2 bit
Memory Address	X	X	MA-3	D	As above but 2^3 bit
Memory Address	X	X	MA-4	E	As above but 2^4 bit
Memory Address	X	X	MA-5	F	As above but 2^5 bit
Memory Address	X	X	MA-6	G	As above but 2^6 bit
Memory Address	X	X	MA-7	J	As above but 2^7 bit
Memory Address	X	X	MA-8	K	As above but 2^8 bit
Memory Address	X	X	MA-9	L	As above but 2^9 bit

J2 Connector Contact Usage

Signal	2031	3157	Designation	Pin #	Characteristic
External Enable	X	X	$\overline{\text{ENT.EN.}}$	4	Low TTL compatible level disables internal control thus enabling external memory control functions.
Memory Enable	X		ME	21	TTL low disables (Tri-State) the memory output and prevents it from being written into. TTL high enables memory input or output. Low level permits loading of external data into the incrementing register Input data must be quiescent and ME should be low until External Load is returned to high state. External Load must be high during write interval.
External Load	X	X	$\overline{\text{EXT LD}}$	N	External data (ED00 to ED15) is loaded into the Incrementing Register by trailing edge of a low going TTL compatible pulse, 200 nsec minimum duration. Data must be quiescent during load interval. (See Note).
Increment Register	X		$\overline{\text{INCR REG}}$	P	The contents of MCA's Incrementing Register is incremented by 1 by the positive going transition of the Increment Register pulse, a TTL compatible, 200 nsec minimum width pulse. When unused, must be a TTL high during $\overline{\text{EXT ENB}}$ (see Note on next page).

J2 Connector Contact Usage

Signal	2031	3157	Designation	Pin #	Characteristic
External Read/Write	X		R/$\overline{W}$	M	The contents of the Incrementing Register are written into the memory of minimum duration 600 nsec. The R/$\overline{W}$ must be high for reading. Read or write operations require ME high level. (See Note).
External Memory Address Latch	X	X	MAL	R	The data applied to the ten MA lines, A-L, are latched on the trailing edge of a TTL compatible positive 200 nsec minimum duration pulse. Address data must be quiescent at least 200 nsec prior to the latching edge (See Note).
External Data Input/ Data Output	X		ED00	6	The least significant bit (2^0) of external data. Coding is TTL high true. Data source must be from either an open-collector or Tri-state source. Input of external data is permitted when ME is in Low State. No internal pull-up resistors are supplied. Data are loaded into the Incrementing Register by an EXT LD pulse. The 16 ED lines serve as memory data output when ME is in the High State. Outputs will drive one standard TTL load. Length of interconnecting data cables should be limited to 6 feet.

NOTE: The signals $\overline{\text{EXT LD}}$, $\overline{\text{INC REG}}$, R/$\overline{W}$ and MAL can be applied only during the interval that $\overline{\text{EXT ENB}}$ is low.

J2 Connector Contact Usage

Signal	2031	3157	Designation	Pin #	Characteristic
External Data Input/ Data Output	X		ED01	5	As above but 2^1 bit
" "	X		ED02	7	As above but 2^2 bit
" "	X		ED03	8	As above but 2^3 bit
" "	X		ED04	10	As above but 2^4 bit
" "	X		ED05	9	As above but 2^5 bit
" "	X		ED06	11	As above but 2^6 bit
" "	X		ED07	12	As above but 2^7 bit
" "	X		ED08	14	As above but 2^8 bit
" "	X		ED09	13	As above but 2^9 bit
" "	X		ED10	15	As above but 2^{10} bit
" "	X		ED11	16	As above but 2^{11} bit
" "	X		ED12	18	As above but 2^{12} bit
" "	X		ED13	17	As above but 2^{13} bit
" "	X		ED14	19	As above but 2^{14} bit
" "	X		ED15	20	As above but 2^{15} bit
Memory Overflow	X		MO/F	22	A high level output indicates an overflow in the 16th bit of the memory.
Clock Inhibit		X	CK INH	1	A high TTL inhibits internal clock halting operation used to generate an intensified display marker provided inhibit is synchronous with display sweep.

J2 Connector Contact Usage

Signal	2031	3157	Designation	Pin #	Characteristic
ADC Data	X		SEL	S	Active Low TTL signal of 200 nsec duration indicates ADC data is present on pins A to L.
Clear QVT	X		CLR	T	TTL low level of 100 msec minimum duration clears the QVT. EXT.EN. not required.
Start QVT	X		START	U	TTL low of 2 µsec minimum duration starts the QVT. $\overline{\text{EXT.EN.}}$ not required.
Stop QVT	X		STOP	V	TTL low of 2 µ sec minimum duration stops the QVT. EXT.EN not required.
Display Clock	X		DCLK	W	TTL level display 50 kHz, 400 nsec wide clock pulses available when clock inhibit is low.
Display Reset		X	DR	X	TTL low of 500 nsec duration indicates that the display sweep has begun.
Decrement Register		X	$\overline{\text{DREG}}$	Y	Positive going TTL edge decrements Incrementing Register. Internal pull-up is provided.
Zero Register		X	$\overline{\text{ZREG}}$	Z	A TTL low of 500 nsec duration indicates the data in the Incrementing Register is zero.
QVT Status	X		STATUS	2	A TTL output indicating the state of the QVT. Low for stopped, high for started.
Common	X	X	GND	3	Signal common.

5 THEORY OF OPERATION

ANALOG FRONT END

The operation of the 3001 is shown by the block diagram in Figure 6. The ADC employed is a run-down type consisting of three separate front ends, one of which is selected to gate clock pulses to a scaler. The three front ends are the hybrid circuits QT100M, VT100B and QT100T used for the Q, V, and T modes respectively.

The QT100M and QT100T are charge-to-time converters consisting of "virtual ground" inputs (Pin 16) capable of current amplifying the input pulse received during the time that a gate is applied to Pin 15. Full scale charge is about 300 pC and 1500 pC for the QT100M and QT100T respectively. When a gate pulse is received by either of these hybrids, an internal capacitor is charged and a run-down is begun. For the duration of the run-down, a TTL clamp-to-ground is present at Pin 9. This "T output" width is proportional to the amount of charge transferred to the capacitor.

The VT100 has an identical pin configuration to that of the QT100 described above. The input is also a "virtual ground" but it is non-integrating. An amount of charge proportional to the maximum input current applied during the gating interval is stored on the internal capacitor. Run-down is identical to that of the QT100's. Full scale is -10 mA.

In the Q Mode, the QT100M is biased on by applying +50 mV to Pin 8. In the V and T modes, it is biased off by applying -200 mV to Pin 8. In the Q Mode, a gate may be generated either internally or applied from an external source. The Q Input is connected directly to the Internal Discriminator, an LD604LG hybrid, and then via a 25.5 nsec 50 Ω delay cable to a 50 Ω termination at the QT100M. Since the input impedance of the LD604LG is very high, the Q Input performs as a low reflection transmission line well terminated at the QT100M. In the INT gate mode, the LD604LG is used to generate a gate trigger, for the internal gate generator circuit. The purpose of the delay line is to compensate for the propagation delay through the LD604LG and gate circuitry.

In the T mode an amount of charge proportional to the gate width is deposited in the QT100T. A constant current source based upon the -24 V NIM supply is used. A side-panel switch selects a series resistance, thus determining the full scale time. Two spare switch positions are available. Pads are available for both fixed and trim resistors. The gate applied to QT100T is based upon the T Start and T Stop input pulses. The T Start clocks the Start flip flop. The clock for the Start flip flop is kept high by the busy level (derived from the Busy Generator). Similarly, the Stop flip flop is clocked by a signal

derived from the T Stop input. Its circuitry is activated by the Start flip flop. The transistors Q11 and Q12 are used to form the gate pulse applied to the QT100T.

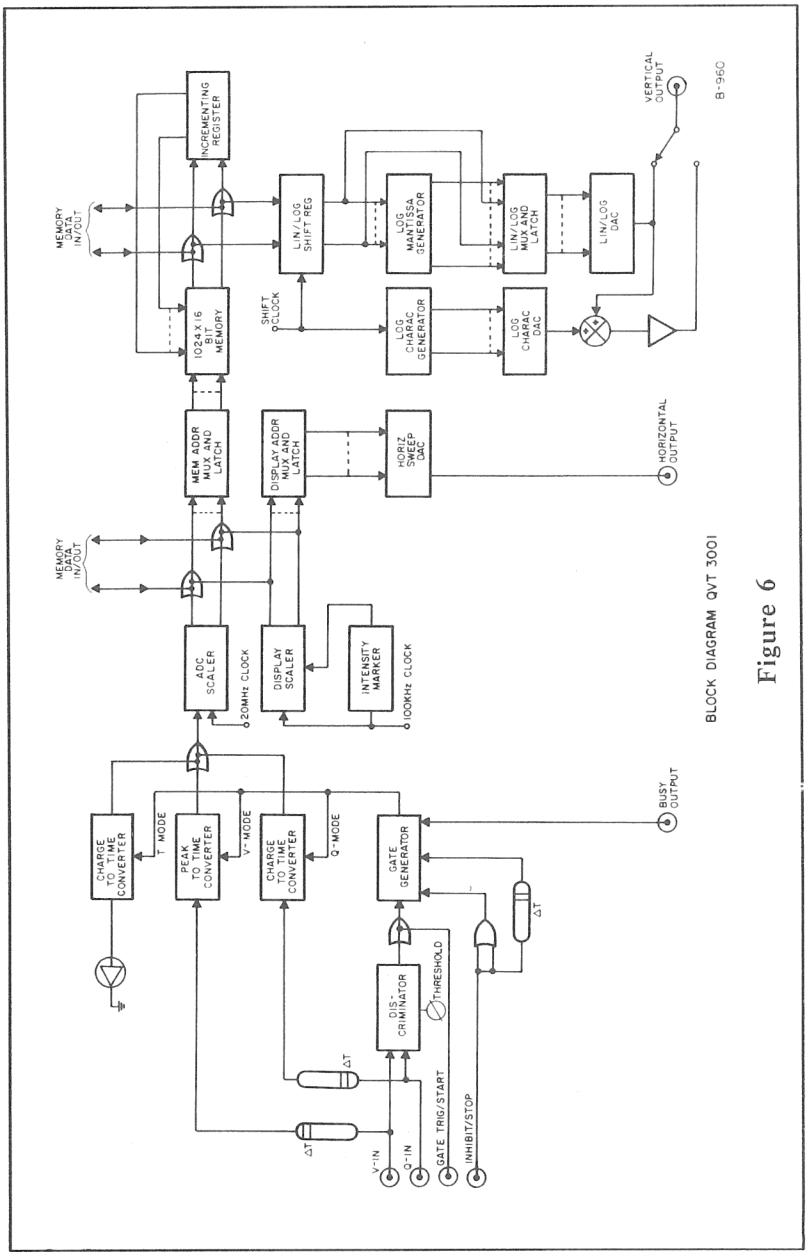


Figure 6

DIGITAL SECTION

The master clock employed in the 3001 is based upon a 20 MHz LC oscillator. The circuit was designed to allow rapid startup and shut down gating. When conversion is initiated, the clock is stopped and remains off until the 7 μsec Wait Monostable completes its cycle. The clock may also be inhibited by the user through the pad labeled CI located between TP and TQ, a TTL high inhibits.

When a conversion is in process, Channel A of the dual 11-bit 20 MHz scaler, Model SC100, is used. The output of the hybrid front end is used to gate the master clock. Thus, after a conversion is completed,the binary data (address) is available at the SC100 outputs.

The scaler address is latched into the Memory Address Latch. In the quadrant mode, the word is shifted right 2 bits and the 2 most significant bits are determined by the Memory switch. The word in the Memory Address Latch addresses the memory which is normally in a READ state. The resulting data word is latched into the Incrementing Register, incremented by 1 and replaced in the Memory in the same address as given by the Memory Address Latch.

DISPLAY SECTION

The Display is active except when an analog signal is being received or the results of a conversion are being entered in the Memory. The clock continuously cycles Channel B of the SC100 through 1024 counts. The resulting addresses latched into the Memory Address Latch are supplied to the Horizontal Sweep DAC and to the Memory. In the quadrant mode, the memory address is shifted right as in the digital section discussed above. The data read from Memory and latched into the Data Scaler are processed either by an 8-bit linear or 16-bit logarithmic vertical DAC. Display mode is selected by the Display Scale switch. In the linear mode, data is shifted right in accordance with the setting of the Counts Full Scale switch and presented to the IN/Mantissa DAC. In the logarithmic mode, the "characteristic" is generated by counting the number of shifts left required to obtain left justified logic "1". The remaining data are used to generate a mantissa using a programmed read-only memory. The analog mantissa is generated by the 8-bit LIN/Mantissa DAC and the analog characteristic is generated by the 8-bit "characteristic".

6 ADDITIONAL INFORMATION

A simplified method for calibrating Q mode pedestal and gain using standard lab equipment.

GENERAL

The inherent 51 Ω termination of the Model 3001 Q input allows one to obtain a well-defined amount of charge from the area of a well defined pulse, given by the relation Q = (V/51) t.

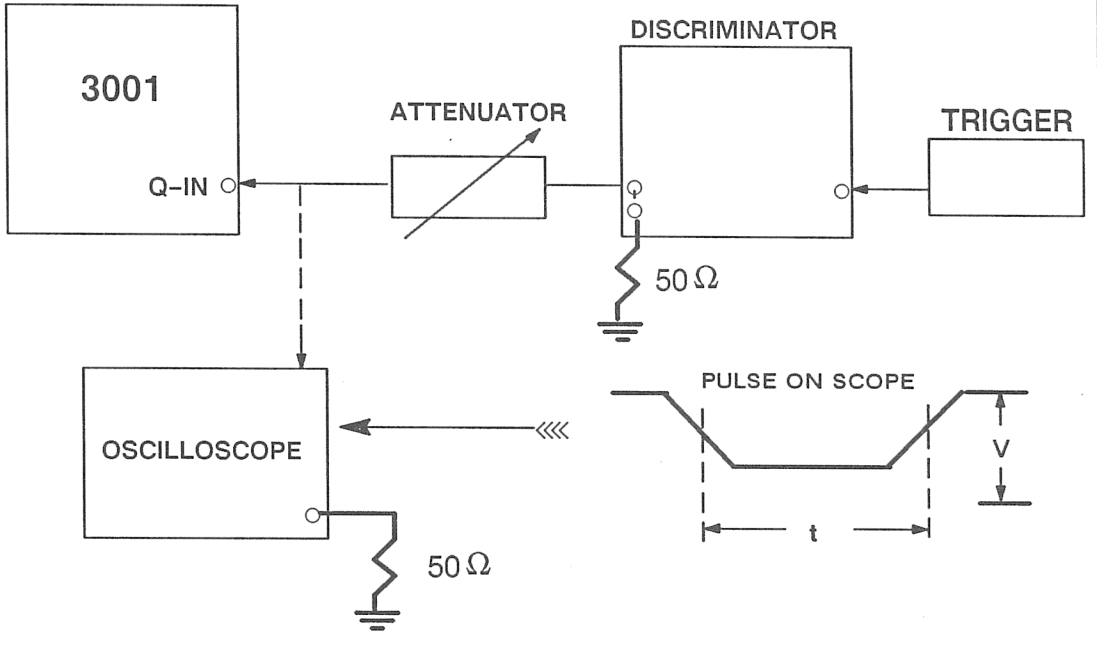


Figure 7
Block Diagram of 30001 Q Mode
Full-Scale Calibration

Test Equipment

Attenuator: Variable gain such as LeCroy 8102
Discriminator: LeCroy Models 623B, 821, or 4608C, etc.
Trigger: Instapulser IP-1.
Oscilloscope: Textronix 475 or 485 or equivalent.

Procedure

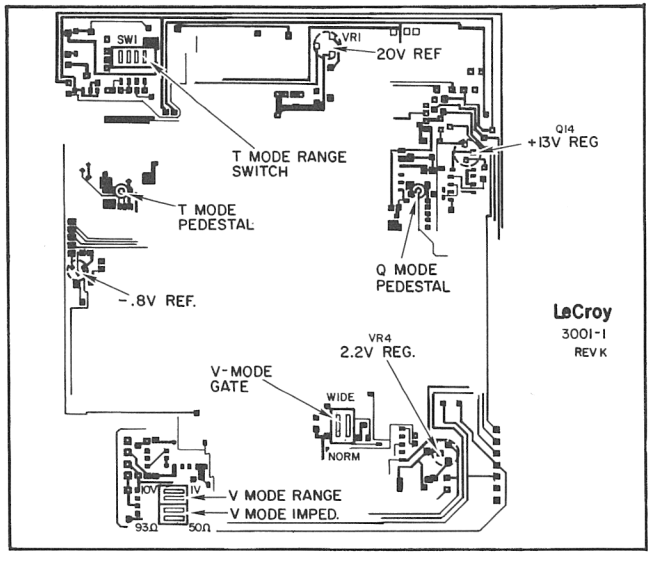
1. Set the Model 3001 gate width to 150 nsec using a NIM input pulse and with the gate switch in EXT TRIG position.

2. Terminate the scope input (50 Ω) and with the calibration set up as shown in the block diagram, select and set the Q input pulse.

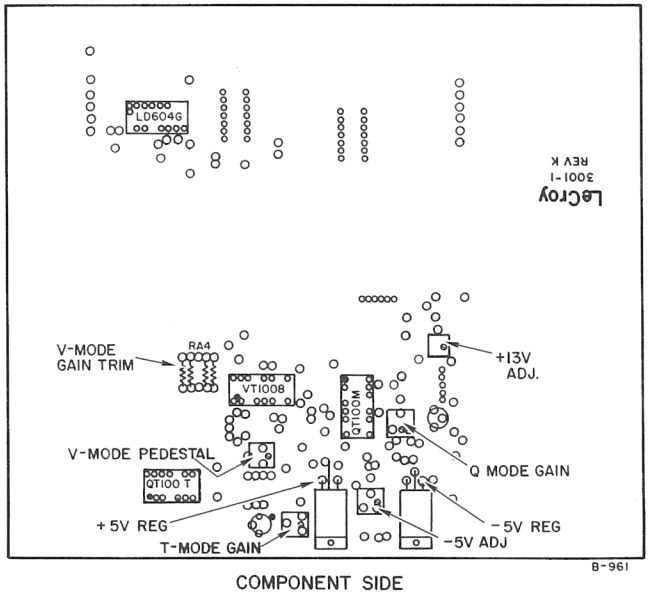
   For a pedestal of 30, a charge of 243 pc is required to obtain a peak in channel 1000 (based on 0.25 pc/channel sensitivity). One therefore obtains the relation t=(12.368)/V(nsec). From it t can be determined if V is selected *(Note: V must be between 02. and 0.5 V)*. Actually, the above value of t must be corrected by increasing its value by about 8–10%.

   Example: Let V=0.30 V which gives t=41 nsec and the corrected t is 45 nsec. This value of t is used for the calibration pulse.
3. Terminate the Q Input with 50 Ω and switch the channel intensification (i.e. INTENSIFY) to 10th. *(Note: The NIM input pulse is still connected to the GATE INPUT)*.
4. On the scope, select the XY Mode and adjust the Q Mode pedestal to channel 30 via the 6–20 pF trim capacitor on pin 16 of QT–100M.
5. Remove the terminator from the Q Input and connect the output of the attenuator to it. Set gate switch to INT, INTENSIFY to 50th and adjust Q Mode gain* or counts in channel 1000.
6. Repeat steps (4) and (5) until pedestal and pulse occur in channels 30 and 1000 respectively.

   *The Q Mode gain is set with the 200 Ω pot at pin 12 of QT100M (see Figure 8). *(Note: Gain should be checked with unit in NIM bin since gain setting may be affected by extension cable)*.



SOLDER SIDE



COMPONENT SIDE

Figure 8
Location of Various Controls including those for Q-Mode Gain Adjustment

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