OPERATOR'S MANUAL

MODEL 3304

FERA SYSTEM MANAGER

PRELIMINARY



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GENERAL INFORMATION

PURPOSE	This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.
UNPACKING AND INSPECTION	It is recommended that the shipment be thoroughly inspected immedi- ately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.
WARRANTY	LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original pur- chaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.
	In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.
	The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.
	This warranty is in lieu of all other warranties, express or implied, includ- ing but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in con- tract, or otherwise.
PRODUCT ASSISTANCE	Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.
MAINTENANCE AGREEMENTS	LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES	LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.
SOFTWARE LICENSING AGREEMENT	Software products are licensed for a single machine. Under this license you may:
	Copy the software for backup or modification purposes in support of your use of the software on a single machine.
	Modify the software and/or merge it into another program for your use on a single machine.
	Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.
SERVICE PROCEDURE	Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578- 6030.

OPERATING INSTRUCTIONS

GENERAL		RA™ is a data acquisition sy nsists of the following module	stem for medium sized experiments. It
		Model 4300B Model 4303+4300B	ADC (charge) TDC
		Model 4301	Driver
		Model 4302	Memory
		Model 3304	System Manager
		detailed description of the sys n Note AN-4004A.	tem architecture can be found in Applica-
		System Manager (FSM) provides all automatic operation of the FERA system. Figure 1. In particular, it manages:	
	1.	The handling of Gate and S conversion and readout.	tart signals by a Busy signal during
	2.		n normal operation mode as well as after erval to avoid hang-ups of the system.
	3.	conversion and transfer tim LeCroy Model 3341 Spectro	e ECLbus readout to allow different es of FERA-compatible units (e.g., oscopy Grade Charge Integrating ADC, Grade Peak Sensing ADC and Model FDC).
	4.	The generation of 4 event reexperiment.	ates to monitor and control the

- 5. The hardware-driven, memory-switching mode with two memory modules, Model 4302, working alternately to minimize deadtime.
- 6. The event-by-event mode for memory readout after each event.

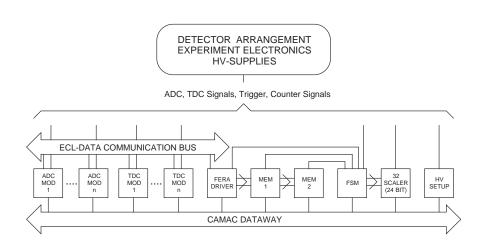


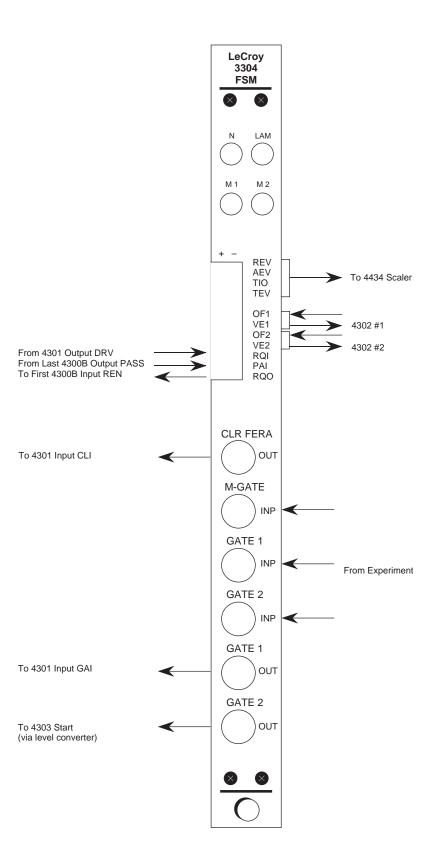
Figure 1

Gate Management	In general, the experiment:	following signals have	e to be supplied as inputs from the	
	Master Gate Gate 1 Gate 2	(M-GATE INP) (GATE1 INP) (GATE2 INP)	start event cycle Gate ADC or Start TDC	
1 and 2 and starts the timeout coun			r Gate signal enables the inputs Gate er. An incoming Gate signal is fed and at the same time, the Gate input	
		hat a minimum delay ate and Gate 1 or 2.	of 40 nsec is required between	
	The inhibit of the gate inputs is removed when an ECLbus data transfer is completed or when a timeout occurred. Only then a new cycle can be started via the Master Gate input.			
Counting Rates	From the Gate signal management, the following information is derived to generate different counting rates:			
	Total Events (TEV): total number of events offered by the experiment (corresponds to number of Master Gate signals).			
	Accepted Events (AEV): number of registered events with competed ECLbus transfer (number of PASS signals).			
	Rejected Events (REV): number of events during module BUSY, i.e., Gate inputs Inhibit (from Master Gate to data transfer completed or during overflow of both memories).			
	Timeout Detected (TIO): number of Clear signals generated by the FSM after timeouts.			
	•	end of a measureme	LeCroy Model 4434 Scaler and be nt run for statistical and normaliza-	
FERA Clear	signal of the la (PAI input). Ad PASS does no	st ADC, which reports ditionally, the FSM itse	iated in Buffer mode by the PASS data transfer complete to the FSM elf produces a Clear signal, if a grammed timeout interval. Therefore, ed.	
	Following conversion and/or zero suppression times, there is a fixed delay of 2 μsec between system Clear and remove Inhibit of the FSM Gate inputs.			
Readout Delay The ECL-commandbus signal REQ reports that data are ready for ECL port readout. This signal is the logical OR ADC requests; timing differences are compensated by a the Driver Model 4301, which can be manually adjusted 500 nsec. This interval may not be sufficient if additional ible units from other manufacturers with considerably lor		nal is the logical OR of the individual e compensated by a delay interval in e manually adjusted between 150- ufficient if additional FERA compat-		

	times, are added to the system (e.g., LeCroy Model 3351 with up to 25 $\mu sec).$
	To handle this configuration, it is possible to delay the Readout Request signal in the FSM, in programmable steps of 100 nsec. Only after this period does the RQO signal from the FSM to the first ADC start the transfer of the data via ECLbus.
Memory Switching Mode	By using the Overflow and Veto signals of two memories Model 4302, the FSM completely controls a hardware driven automatic and continuous double buffer operation. In this mode, data are written into one memory, while the other is read out via CAMAC block transfer or is ready to take data. No software control is necessary, thus dead time is minimized. The selection and switching of the memories is organized by bits 1, 2, and 3 of the status register. A further 2 bits only readable, indicate the memory, which is currently active. The LAM on Overflow finally allows data readout without any special software effort.
	At high data rates, both memories may report an overflow, because CAMAC readout of one unit has not yet completed, whereas the second one has already filled again with data. In such a case, the FSM internally generates a Memory Full signal and inhibits the Gate 1 and 2 inputs, until one memory becomes available again.
	In cases where FERA is part of a more complex data acquisition system, which has to be read out after each event, it is possible to switch on the event-by-event mode by setting status register bit 6 equal to 1.

SYSTEM INTEGRATION

Cabling



Signal Description	Master Gate (M-GATE): Input, Lemo type connector accepting NIM signals (50 Ohm). Typically Master Trigger from the experiment.
	Gate 1 (GATE1 INP): Input, Lemo type connector accepting NIM signal (50 Ohm), e.g., ADC gate input.
	Gate 2 (GATE2 INP): Input, Lemo type connector accepting NIM signals (50 Ohm), e.g., TDC start input.
	Gate 1 (GATE1 OUT): Output, Lemo type connector; produces NIM signals, e.g., gate for 4300B.
	Gate 2 (GATE2 OUT): Output, Lemo type connector; produces NIM signals, e.g., gate for 4303.
	Clear (CLR FERA): Output, Lemo type connector; produces NIM signals. Connect to CLI input of 4301.
	Readout Request Input (RQI): Input, 2-pin connector accepting diff. ECL signals (100 Ohms). Connect to REQ output of 4301.
	Pass Input (PAI): Input, 2 pin connector accepting diff. ECL signals (100 Ohms). Connect to PASS output of last 4300B.
	Readout Request Output (RQO): Output, 2-pin connector accepting diff. ECL signals (100 Ohms). Connect to REN input of first 4300B.
	Overflow Memory #1 (OF1): Input, 2-pin connector accepting diff. ECL signals (100 Ohm). Connect to OVF output of 4302 #1.
	Overflow Memory #2 (OF2): Input, 2-pin connector accepting diff. ECL signals (100 Ohm). Connect to OVF output of 4302 #2.
	Veto Memory #1 (VE1): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to VETO input of 4302 #1.
	Veto Memory #2 (VE2): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to VETO input of 4302 #2.
	Total Events (TEV): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to 4434 input.
	Accepted Events (AEV): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to 4434 input.
	Rejected Events (REV): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to 4434 input.
	Timeout Detected (TIO): Output, 2-pin connector producing diff. ECL signals (100 Ohm). Connect to 4434 input.

LED Indicators	N: Module addressed.		
	LAM: LAM from	Memory #1 or #2 (if enabled).	
	M1: Memory #1 active.		
	M2: Memory #2 active.		
CAMAC COMMANDS AND FUNCTION CODES	F(0)•A(0):	Read Status Register; X=1, Q=1.	
		R1 - acquisition started R2 - memory #1 ready R3 - memory #2 ready	
		R4 - memory #1 active	
		R5 - memory #2 active R6 - single event mode on, off	
	F(16)•A(0):	Write Status Register; X=1, Q=1. W1 - start acquisition, enable memory #1, free master gate	
		W2 - set memory #1 ready W3 - set memory #2 ready	
		W6 - enable single event mode	
	F(16)•A(1):	Set Timeout-Counter; X=1, Q=1. W1W16 (timeout=value*100 nsec).	
	F(16)•A(2):	Set Readout-Delay-Counter; X=1, Q=1. W1W16 (delay=value*100 nsec).	
	F(8)•A(0):	Test LAM #1; X=1, Q=1 if L=1.	
	F(8)•A(1):	Test LAM #2; X=1, Q=1 if L=1.	
	F(10)•A(0):	Test and Clear LAM #1; X=1, Q=1 if L=1.	
	F(10)•A(1):	Test and Clear LAM #2; X=1, Q=1 if L=1.	
	F(24)•A(0):	Disable LAM; X=1, Q=1.	
	F(26)•A(0):	Enable LAM; X=1, Q=1.	
	F(9)•A(0):	Reset Module; X=1, Q=1. - memory #1, #2 ready - acquisition stop - single event mode off - clear LAM #1, LAM #2 - disable LAM	
	l:	Inhibit Acquisition	
	C or Z:	Reset Module.	
	L:	Buffer Mode: on overflow of memory #1 or #2. Single event mode: following each ECL port readout.	