OPERATOR'S MANUAL

MODEL 3341

CAMAC 8-INPUT CHARGE ADC

LeCroy

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CAUTION

POWER REQUIREMENTS

The Model 3341 requires both +12 V and -12 V in addition to +6 V, -6 V, +24 V and -24 V supplies for proper operation.

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

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LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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GENERAL

The Model 3341 QADC incorporates 8 analog memories used to simultaneously store 8 charge signals to be analyzed.

The analog memories outputs are routed, through an analog multiplexer, to a fast analog-to-digital converter (3 μsec) featuring offset control and two thresholds: a lower (LLD) and an upper (ULD) threshold. This makes it possible to assign different threshold and offset (zero energy intercept) values to each measuring channel.

A "Parameters Memory" contains the LLD, ULD and OFFSET values of each single channel, as well as the common threshold value. A 6-bit register (STATUS REGISTER) allows different data acquisition and readout modes of the 8 measuring channels. Data may be read out either via CAMAC or via the ECL Data Bus, depending upon the programming of the Status Register.

Both the Status Register and Parameters Memory must be previously loaded via CAMAC.

If enabled, the ECL Data Bus, located on the front panel, sends analog-to-digital conversion data sequentially in words of 16 bits with differential ECL levels (the first 12 bits are data bits plus 3 subaddress bits, plus the "Overflow" bit, if it exists).

A REQ output signal is generated when the ECL Data Bus is ready to deliver data.

In CAMAC mode, data is always read in 16 bit words in either sequential (Q stop mode) or addressed mode. When data is ready, a LAM signal may be generated and there is Q=1 with the readout function N.F(0) or N.F(2).

The instrument includes provisions for testing the 8 input modules of the 3341 via a CAMAC controlled TEST signal with function N.F(25) A(0). This signal simulates a GATE command and applies a charge corresponding to about 1/2 of the dynamics to the input of each channel. The ADC may be in two states: "Idle" or "Busy", depending on the GATE, CLEAR and internal CLEAR signals. (Internal CLEAR is applied after a conversion if here is no valid data or when data readout is performed in sequential mode.) GATE and CLEAR signals may be sent either via front-panel (ECL Command Bus) or via CAMAC.

After a CLEAR signal the ADC is in the "Idle" state, that is, it is ready to receive a GATE signal (front-panel or test). The Status Register and the Parameters Memory may be loaded only when the module is in the "Idle" state.

The GATE signal (front-panel or test) causes the ADC to go to the "Busy" state, during which no further GATE signal is allowed. Data conversion is enabled approximately 1 μsec after the GATE signal, and at the end of

the conversion time data readout is initiated. At this point, depending on the state of the Status Register and the data converted by the ADC, any of three conditions may occur:

1. Data read out via ECL port only (EEN = 1, see Status Register).
2. Data read out via CAMAC only (EEN = 0).
3. No data to be read. In this case, no data readout is performed.

During the “Busy” state, to disable the ongoing data conversion or to accept further GATE signals, it is necessary to apply a CLEAR signal. The ADC is ready to perform a new data acquisition 1.2 μsec after the CLEAR signal.

Analog Inputs

The 8 analog inputs are designed for negative signals. The input circuit can work with any desired input impedance; it is normally provided with a 50 ohm input for coaxial cable connections, but it may also be supplied with other arrangements, for instance, a 100 ohm input suitable for twisted pair connections.

CLEAR Function

The CLEAR function may be enabled either by an ECL CLEAR command of the front-panel ECL Bus or by CAMAC functions Z, C and N.F(9) A(0) strobed by S2 or by an internal command generated after completion of sequential data readout or at the end of conversion, if no valid data is present.

After a CLEAR signal, the ADC changes to the “Idle” state and is held in this state until the next GATE signal is applied. During the CLEAR signal (duration of about 1.2 μsec) the input GATE is inhibited.

It is recommended to avoid sending new GATE commands in coincidence with the end of the CLEAR signal. This will prevent generation of sliced GATE commands.

External GATE Input

The GATE command should be sent only when the module is in the “Idle” state. It should never be sent in coincidence with the CLEAR signal (at least 1.2 μsec after the CLEAR function has been initialized). The GATE input may be inhibited by line 1 (CAMAC inhibit). A GATE signal activates the following functions:

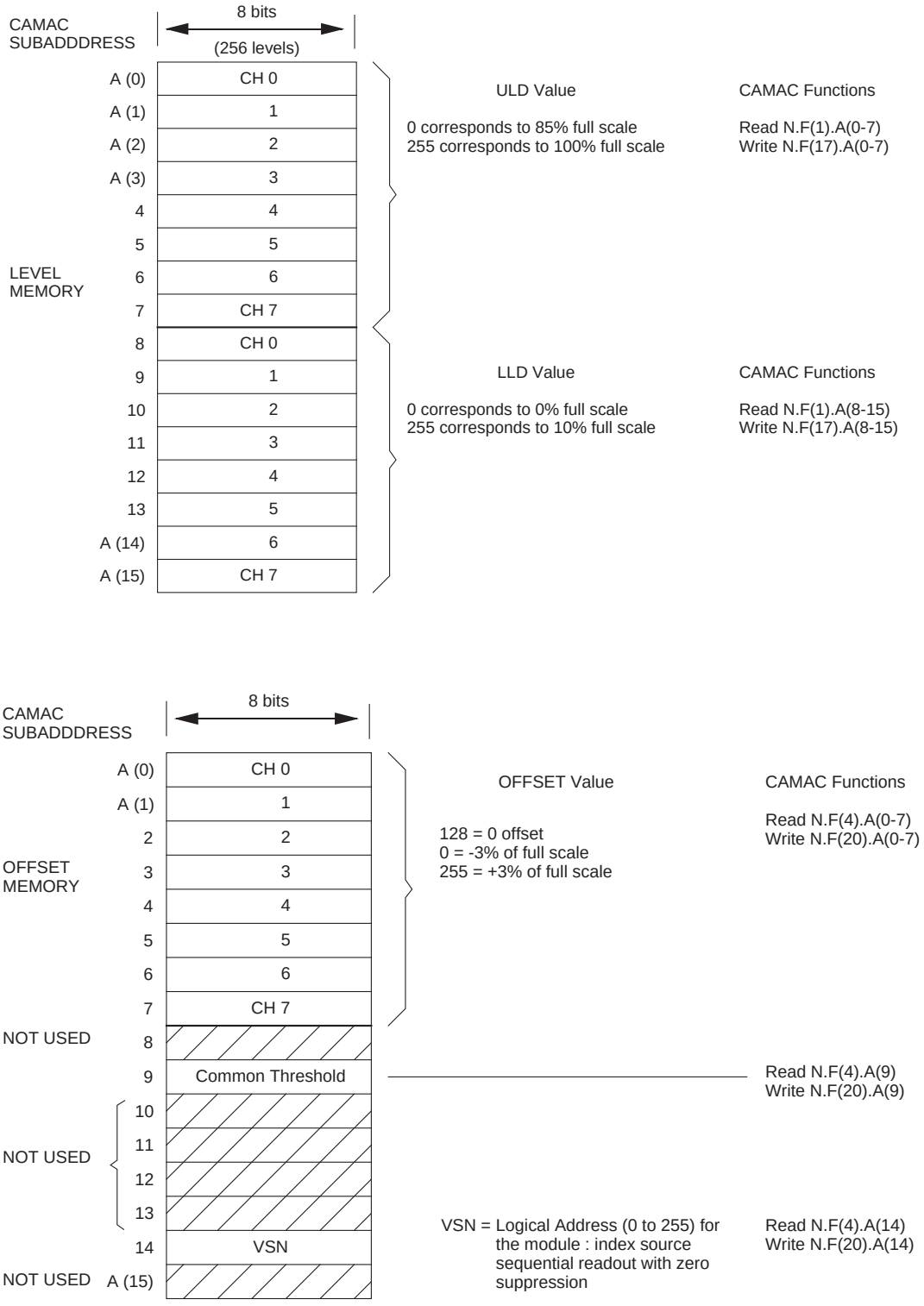
1. Enable the integrator circuit.
2. The end of the GATE signal automatically inhibits the GATE input disabling further GATE signals.

After a 1 μsec time delay it starts conversion causing the ADC to change to the “Busy” state.

ADC Thresholds and Offset Memory

The 3341 includes a Parameters Memory made up of two 16x8 word groups. With the module in the “Idle” state, the threshold values (Low Level Discriminator-LLD; Upper Level Discriminator ULD), as well as the offset, Common Threshold and VSN (Virtual Station Number) values can be loaded into the Parameters Memory. Different threshold (ULD and LLD) and offset values may be assigned to each input; whereas the threshold is common to all the 8 input modules.

A schematic diagram of the ADC Parameters Memory is illustrated in the following drawing.



MODEL 3341 PARAMETERS MEMORY

Test Function

The TEST function is initiated by the CAMAC command N.F(25).A(0) strobed by S2. If accepted, Q is equal to 1.

This function is accepted only when the ADC is in the “Idle” state. It performs the following operations:

1. Applies a specific charge to the analog memories inputs.
2. Generates a GATE signal in coincidence with the pulse peak. During the entire duration of this pulse no signal is allowed on any of the analog inputs, even if the interconnecting cable may remain connected.

The GATE command (front panel) must not be sent while the Test function is in progress.

Overflow

The ADC actual dynamics is 3840 channels (4096-256) (256 channels are reserved for the Sliding Scale Circuit). Data having a content greater than or equal to 3840 is not considered to be valid for measurement. If this data is present, an Overflow indication is generated by the ADC control circuit. Via the Status Register bit (R12) (See Status Register) it is possible to enable the Data Memory to associate the Overflow information with the conversion Data and store it into the DATA WORD at position R16 (see ECL or CAMAC Data Structures).

Status Register

The Status Register is a memory into which the Status Word is loaded. The Status Register is made up of two distinct sections.

The first (low order 8-bit) consists of a word of the Parameters Memory and contains the address number of the module (VSN-Virtual Station Number). This is used to identify the data source during sequential readout with zero suppression mode.

The other section contains the information that determines the data acquisition and readout modes. The Status Register is written by the CAMAC function N.F(20).A(14) strobed by S1 and is readout by-function N.F(4).A(14).

These two functions are accepted only when the module is in the “Idle” state; there is Q response when the functions are accepted.

After switching on the module, the content of the Status Register is undefined. The CAMAC initialization function (Z) sets the 6 Status Register bits (R10 through R16) to the “1” state, but will not affect the VSN register, whose content remains undefined. The other CLEAR signals will not reset the Status Register.

The six functions of the Status Register are as follows:

R16							R9	R8 R1
0	CLE	CSR	CCE	OVF	EEN	SUB	0	VSN

SUB (W10-R10) Channel Subaddress Enable

If enabled (SUB=0), in addition to the ADC data, the binary addresses of the 8 analog memories (0 for the 0 channel, etc.) are loaded into the Data Memory at positions R13, R14, R15. If SUB=1, the value of R13-R14-R15 in the Data Word is always “zero”.

ECL (W11-R11) ECL Bus Enable

If EEN=1, only the ECL Port readout is enabled.
If EEN=0, only CAMAC readout is enabled.

OVF (W12-R12) Overflow Indication Enable

If OVF=0, the Overflow indication, if it exists, is loaded into the Data Memory at position R16.
If OVF=1, the value of R16 in the Data Memory is always “zero”.

CCE (W13-R13) Zero Suppression Enable

CSR (W14-R14) Sequential Readout Enable

These two bits allow 3 different data acquisition and readout modes to be performed.

1. With Zero Suppression CSR = 1 and CCE = 1
   Data conversion takes place only in valid channels (i.e. channels with pulses falling within the LLD-ULD window). These valid channels are readout in sequential mode either via the ECL bus or CAMAC.

2. Without Zero Suppression CSR = 1 and CCE = 0
   All the 8 input channels are converted and read sequentially. Readout may be either via the ECL BUS or CAMAC.

3. Addressed Readout CSR = 0 and CCE = Indifferent
   All the 8 channels are converted and the ADC data is read by CAMAC only in addressed mode with any of two functions N.F(0).A(0-7) or N.F(2).A(0-7). The readout channel is identified by subaddress A: A(0) = channel 0 etc.

CLE (W15-R15) CAMAC LAM Enable

If CLE = 1, the LAM output is enabled to indicate that there is valid data to be read by CAMAC; in the Zero Suppression mode, if no valid data is present, LAM will not be enabled.
If CLE = 0, the LAM output will be disabled.

Note: After the CAMAC initialization (Z) the 6 bits of the Status Register are set to “1”. This means With Zero Suppression mode, ECL readout, SUB and OVF disabled.

ECL Data Bus

The module delivers 16-bit data words with complementary ECL outputs at the ECL Data Bus connector. The maximum readout frequency is 8 MHz. If several modules are connected, the pull-down resistors must be removed in all modules, except for the last module (see Figure 1). When these resistors are mounted, the associated LED indicator is lighted. If several modules are connected, only the positive ECL output is used; the negative output should be connected to ground.

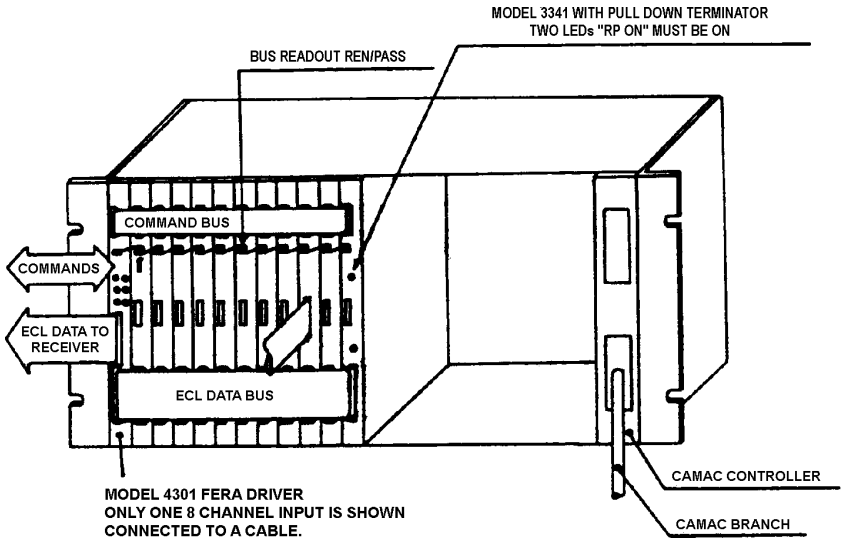


Figure 1

ECL BUS - COMMAND

In addition to the ECL CLEAR and GATE signals, all those signals with ECL levels that control and allow use of the ECL DATA Readout are present at the ECL Bus and REN/PASS connectors.

These signals include:

1. **Busy Output (BUSY)**
   This output is set to the “1” state 1 μsec after the end of the GATE signal and is held to this state until after the end of the readout cycle (ECL Readout or CAMAC Readout). The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL Bus (CLR). The ADC is ready to start a new conversion 1.2 μsec after the end of the BUSY state.

2. **Write Strobe Output (WST)**
   Indicates the time period during which the data word present on the ECL Data Bus can be stored in the external memory. WST is generated a minimum of 10 ns after the data is ready. Its width is higher than 40 ns. The ECL Data Bus data is maintained stable as long as the WST pulse lasts.

3. **Request Output (REQ):**
   Indicates that the module is ready to send data to the ECL Data Bus. The REQ signal is generated at the end of conversion if the bit

related to ECL Readout in the Status Register has been set. The REQ signal remains until after the last data word has been read or a CLEAR command has been given.

4. **Write Acknowledge Input (WAK)**
   This input receives the acknowledge signal indicating that the data present on the ECL Bus has been loaded into memory and the next data word may be sent. The next WST signal is generated at least 50 ns after the WAK signal. Minimum WAK width must be 30 ns.

ECL PORT ENABLE/PASS

1. **Readout Enable Input (REN)**
   The REN signal indicates to the module that it can take control of the ECL Data Bus; REN must be maintained during the entire readout time. The signal enables the ECL Data Bus, WST output and WAK input if the module is ready for data transfer (REQ output ON). If there is no data present (REQ=OFF) the REN signal automatically generates the NEXT signal, which becomes REN for the next module.

2. **Pass Output (PASS)**
   Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has completed data transfer. The PASS output signal is generated by the REN line in the absence of the REQ internal command or, if this command is present, at the end of data readout. The transit time between the REN and PASS output is typically 3 ns (6 ns max) if the module does not include data readout capabilities.

   As previously mentioned for the ECL Data Bus, if several modules are connected, it is necessary to remove the pull-down resistors in all modules, except for the last one. The LED indicator is lighted when the resistors are mounted (see Figure 1).

   The timing sequence of ECL Data transfer is described below.

   1. After data conversion, the ADC module, sends the REQ signal and waits for the REN Readout Enable.

   2. An external driver provides the REN line.

   3. The REN signal clocks the internal flip-flop in the requesting ADC module and inhibits the PASS output. The non-requesting ADCs closer to the driver are disabled by the same REN signal. The non-requesting ADCs far away from the driver do not receive the REN signal because it is stopped in the requesting module (no PASS signal). Moreover, the REN signal sets the WST line high and enables the first data word to transit through the ECL Data Bus. The module remains in this state waiting for the WAK signal. As soon as the WAK signal is received, the WST signal is released and is held to this position for at least 60 ns by an internal protection. During this time the module makes available the next data word which is loaded into the ECL Data Bus with the leading edge of the next WST signal.

4. After the last data word from an ADC has been read, the request REQ signal is removed and the REN signal is routed to the PASS output, thus enabling readout of the next ADC module.

5. If a far off ADC has sent in a request, the common REQ line remains high and data readout from this module is initiated.

6. If a module closer to the driver has data ready, it waits until the REN signal goes low and as soon as this occurs it sends its own REQ signal. (This module was disabled by the REN signal.)

ECL Bus Readout Interrupt

An ongoing ECL Bus readout may be momentarily interrupted in two different ways.

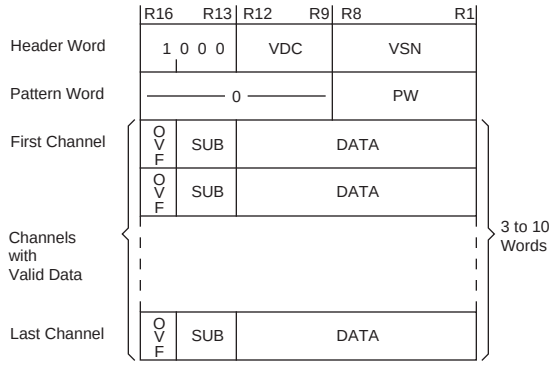
1. By not sending a WAK signal after a WST signal. In this case, the data word on the ECL Data Bus remains until the WAK signal is received.

2. By interrupting the WAK signal, stopping it after the first transition. If this occurs, the WST command is terminated and the next data word is placed on the ECL Data Bus, but it is only upon release of the WAK signal that the next WST will be activated again.

ECL Data Structures

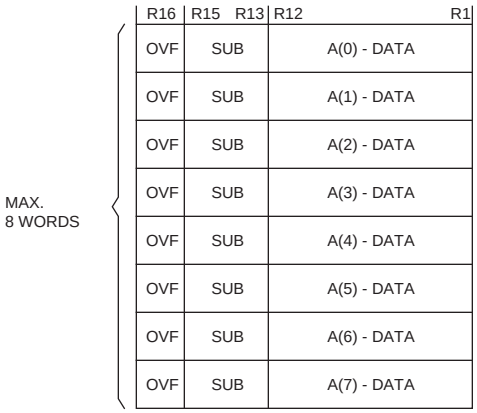
Note: EEN, CSR, and CCE are STATUS WORD bits.

1. EEN=1, CSR=1, CCE=1



Zero suppression is on. Up to 8 data words is to be read. Sequential readout only is possible on ECL BUS. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in S.R. is 0.

2. EEN=1, CSR=1, CCE=0



R16	R15 R13	R12 R1
OVF	SUB	A(0) - DATA
OVF	SUB	A(1) - DATA
OVF	SUB	A(2) - DATA
OVF	SUB	A(3) - DATA
OVF	SUB	A(4) - DATA
OVF	SUB	A(5) - DATA
OVF	SUB	A(6) - DATA
OVF	SUB	A(7) - DATA

Always 8 data words are to be read out. Sequential readout only is possible on ECL BUS. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in S.R. is 0.

CAMAC Commands and Functions

Note: If the module is in BUSY Status (BUSY LED on), only data read-out and clear functions can be executed. Busy is released after clear and when all data is read out. The BUSY line is connected on the Common ECL Bus.

F(0)•A(9): Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be read out.

F(0)•A(0-7): Reads data addressed (CSR=0). Q-response is 1 if there is data to be read out.

F(0)•A(14): Reads Header Word (Q=1 if module is in BUSY status).

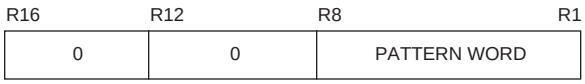
HEADER WORD

R16		R12	R8 R1
1	0	VDC	VSN

Header Word contains an information about the logical address of the module (VSN virtual station number bit 1-8) loaded to STATUS REGISTER, and an information about a number of valid data (VDC valid data counter). Q-response is 1 if there is the data to be read out.

F(0)•A(15): Reads Pattern Word (Q=1 if module is in BUSY Status).

PATTERN WORD



Pattern Word contains a bit muster that shows which channel has a valid data. Bit R1 corresponds to ch. 0.

F(1)•A(0-7): Reads threshold Memory (upper threshold). Q=1 if BUSY=0.

F(1)•A(8-15): Reads threshold Memory (lower threshold). Q=1 if BUSY=0.

F(2)•A(0): Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be read out.

F(2)•A(0-7): Reads data addressed (CSR=0) and clears with F(2)•A(7) strobed on S2. Q-response is 1 if there is the data to be read out.

F(2)•A(14): Reads Header Word in data addressed mode (CSR=0) (Q=1 if module is in BUSY status).

F(2)•A(15): Reads Pattern Word and clears LAM (Q=1 if module is in BUSY status).

F(4)•A(0-7): Reads offset memory (Q=1 if module isn't in BUSY status).

F(4)•A(9): Reads common threshold (Q=1 if module isn't in BUSY status).

F(4)•A(14): Reads Status Word Register (Q=1 if module isn't in BUSY status).

F(8)•A(0): Tests LAM. Q=1 if LAM is set.

F(9)•A(0): Clears ADC and control logic. Doesn't clear memories and status register.

F(10)•A(0): Clears LAM and clears Single Channel mode. Q=1.

F(16)•A(0-7): Single Channel mode (Autotrigger).

F(17)•A(0-7): Writes threshold memory (upper thr.). 8 bits (0-255) correspond to 85-100% full scale. (Q=1 if module isn't in BUSY status).

F(17)•A(8-15): Writes threshold memory (lower thr.). 8 bits (0-255) correspond to 0-10% full scale. (Q=1 if module isn't in BUSY status).

F(20)•A(0-7): Writes offset memory. 8 bits (0-255) correspond to ±3% of full scale; 128 correspond to 0 V. (Q=1 if module isn't in BUSY status).

F(20)•A(9): Write common threshold 8 bit (0-255). (Q=1 if module isn't in BUSY status).

F(20)•A(14): Writes Status Word Register (Q=1 if module isn't in BUSY status).

STATUS WORD

R16				R12			R8	R1
0	CLE	CSR	CCE	OVF	EEN	SUB	0	VSN

R1-R8 (VSN) Logical address of the module.
R10 (SUB) when SUB=0 subaddress enabled (see data structure).
R11 (EEN) when EEN=1, ECL readout enabled (EEN=0 CAMAC enabled).
R12 (OVF) when OVF=0, the overflow bit enabled (see data structure).
R13 (CCE) when CCE=1, zero suppression enabled, only if CSR=1.
R14 (CSR) when CSR=1, CAMAC sequential readout enabled.
R15 (CLE) when CLE=1, CAMAC LAM enabled.

Note: The all bits of S.W.R. are set to 1 by CAMAC Z=init. function.

F(25)•A(0): Test function (Q=1 if module isn't in BUSY status).

Z: Initialize; clears the module and sets the Status Register bits 9-16 to 1. Does not clear the memory.

C: Clears the Module. Does not clear the Status Register and memory.

I: Inhibits the GATE input.

X: X response is generated for all valid functions.

Q: Q response is generated when the function can be executed.

L: LAM set, if enabled, after the end of conversion and if there is valid Data to be read.

The Status Word Register CLE, CSR, CCE, OVF, EEN, SUB bits, VSN - virtual station number and Parameters Memory must be written before acquisition begins.

CAMAC Readout

CAMAC Readout may be performed in either "sequential" mode or "addressed" mode, depending upon the state of the CSR bit of the Status Register.

CSR = 1: Enables Sequential Readout: at the end of the conversion cycle the first data word is available on the CAMAC Dataway. The Q response is given as long as there is data to be read. After the last data

word has been read, the internal CLEAR signal causes the ADC to go to the “Idle” state. Data is read with functions N.F(0).A(0) or N.F2.A(0). On completion of the readout of each single data word (at the end of S2) the address of the ADC Data Memory is incremented and the next data word is sent.

CSR = 0: Enables Addressed Readout: at the end of the conversion cycle, the various channels can be read by addressing the channel to be read via CAMAC with Subaddress A. Readout functions are N.F(0).A(0-7) or N.F.(2).A(0-7). With function N.F(0).A(0-7) the Q response is given each time a data word is read and the module is maintained enabled to send the requested data until a CLEAR function is released. With function N.F(2).A(0-7) the Q response is given each time a data word is read but the CLEAR function is automatically generated by Subaddress 7 [N.F(2).A(7)] strobed by S2.

LAM Handling

The LAM (Look-at-Me) is activated when the related bit of the Status Register is set to “1”. It is activated as soon as data is ready for CAMAC readout. During “Sequential Readout” the LAM is reset after the last data word has been read.

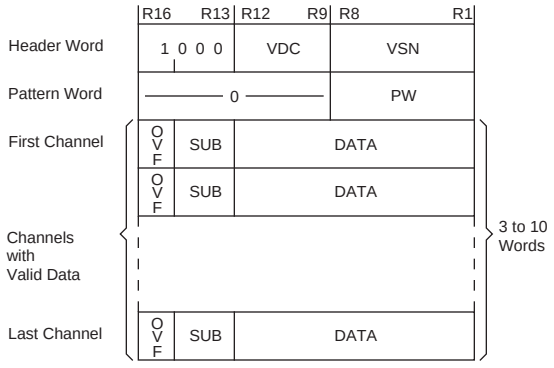
Function N.F(8).A(0) is used to test the state of the LAM. Q = 1 if the LAM is present.

The LAM may also be cleared by the following functions ECL/CLEAR front panel, Z, C, N.F(9).A(0) strobed by S2.

CAMAC Data Structures

Note: EEN, CSR and CCE are Status Word bits.

1. Read Data F(0)•A(0), F(2)•A(0), EEN=0, CSR=1, CCE=1



Zero suppression is on. Up to 8 data words are to be read. Sequential readout is on. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in S.R. is 0.

2. Read Data F(0)•A(0), F(2)•A(0), EEN=0, CSR=1, CCT=0.

MAX.
8 WORDS

R16	R15 R13	R12 R1
OVF	SUB	A(0) - DATA
OVF	SUB	A(1) - DATA
OVF	SUB	A(2) - DATA
OVF	SUB	A(3) - DATA
OVF	SUB	A(4) - DATA
OVF	SUB	A(5) - DATA
OVF	SUB	A(6) - DATA
OVF	SUB	A(7) - DATA

Always data words are to be readout. Sequential readout is on.
HW can be read with F(0)•A(14) or F(2)•A(14).
PW can be read with F(0)•A(15) or F(2)•A(15).

Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is 0.
Subaddress bits are enabled when SUB bit in S.R. is 0.

3. Read data F(6)•A(0-7), F(2)•A(0-7), EEN=0, CSR=0, CCE=X

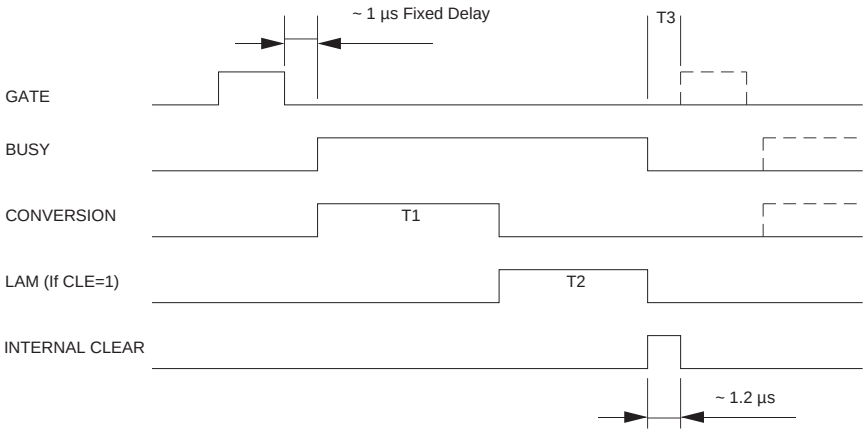
MAX.
8 WORDS

R16	R15 R13	R12 R1
OVF	SUB	A(0) - DATA
OVF	SUB	A(1) - DATA
OVF	SUB	A(2) - DATA
OVF	SUB	A(3) - DATA
OVF	SUB	A(4) - DATA
OVF	SUB	A(5) - DATA
OVF	SUB	A(6) - DATA
OVF	SUB	A(7) - DATA

CAMAC Addressed (random) readout. Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is 0. Subaddress bits are enabled when SUB bit in Status Register is 0.

Readout Timing Diagram

Figures 2 and 3 show the readout timing sequence via CAMAC and via ECLbus.



T1	depends on CSR and CCE status		
	CSR=1 and CCE=1	T1=N•4 µs	(N=number of valid channels)
	CSR=1 and CCE=0 or CSR=0 and CCE=X	T1=32 µs	
T2	depends on CSR and CCE status		
	CSR=1 and CCE=1	T2=(2+N)•t	(N=number of valid channels)
	CSR=1 and CCE=0	T2=8•t	
	CSR=0 and CCE=X	T2 with function N.F(0).A(0-7) terminates upon release of the CLEAR function; with function N.F(2).A(0-7) terminates with function N.F(2).A(7) strobed by S2	
T3	protection time : next gate must follow the end of LAM for at least 1.2 µs		

Figure 2: Acquisition and CAMAC Readout Timing. Note: this diagram does not define the logic state of the signals: Low = FALSE, High = TRUE

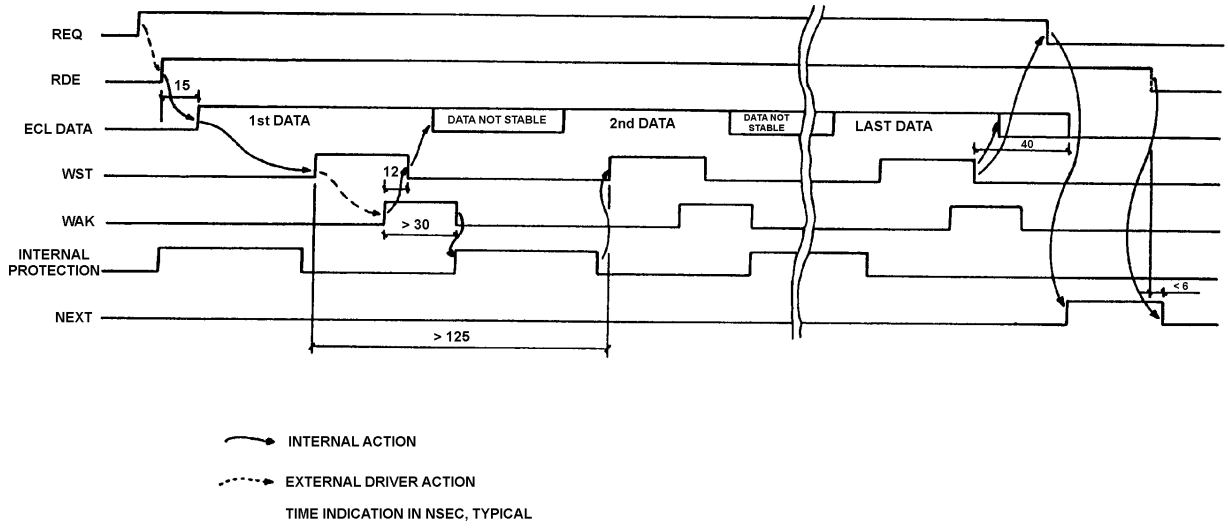


Figure 3: ECL BUS Timing. Note: this diagram does not define the logic state of the signals: Low = FALSE, High = TRUE

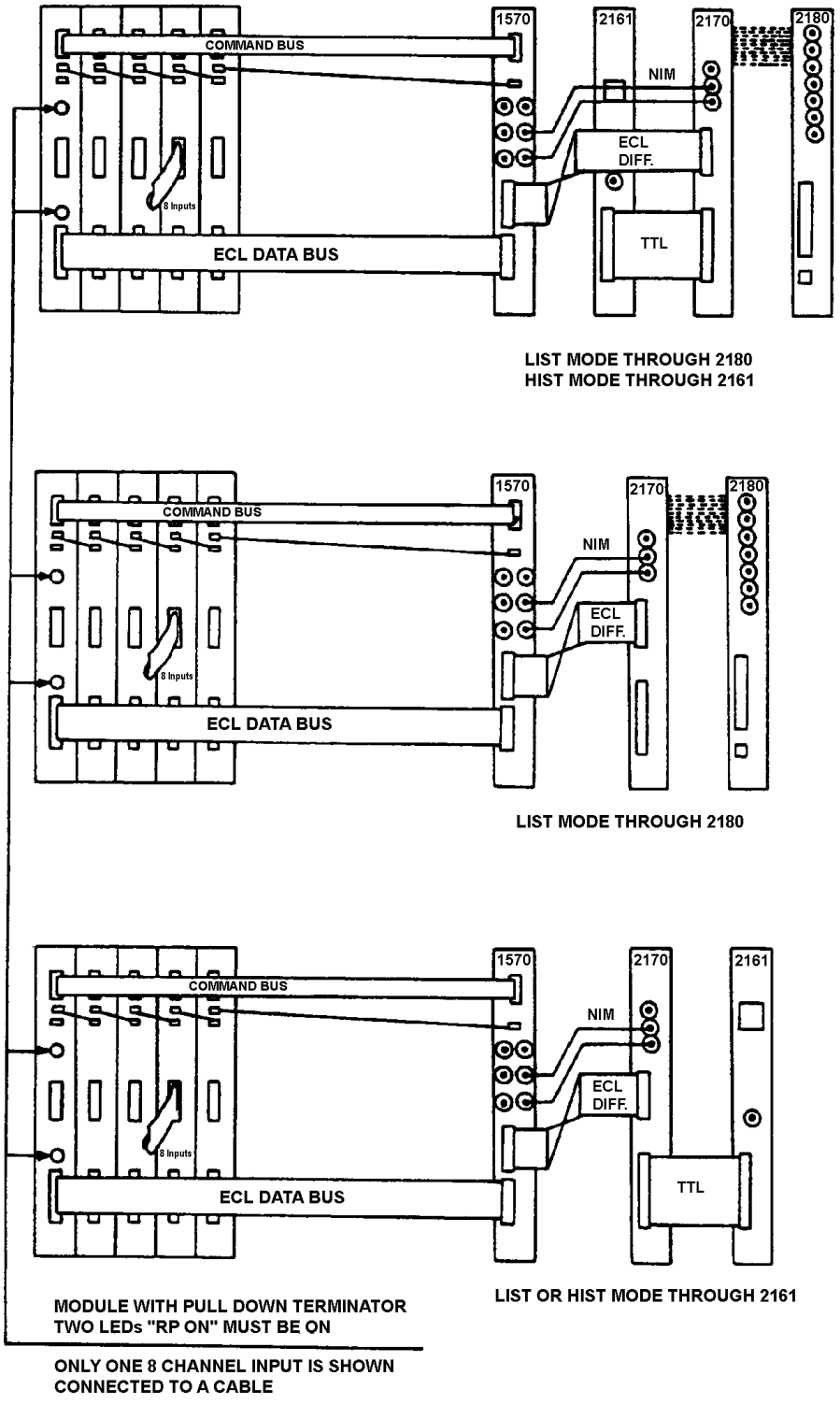


Figure 4: CES System Connection

GENERAL

The Model 3341 module consists of three different printed cards including:

1. A mother board containing the GATE, TEST, and ECL logic circuitry and the TTL ➔ ECL adapting circuitry related to the front-panel Bus. It also accommodates the 8 analog modules.

2. Eight analog modules (Analog memories).

3. A card accommodating the Analog-to-Digital Converter, Thresholds, DACs and the entire logic circuitry of the module.

Description
(see Figures 5 and 6)

In the “Idle” state switches (DMOS) S1 through S4 are in the following condition:

S1 = CLOSED
S2 = OPEN
S3 = OPEN
S4 = CLOSED

1. The cancellation of the direct current (DC) level is accomplished by means of a feed back loop consisting of T1, T2 and OP2, which maintains the current in R1-R2 constant.

2. The common mode rejection (CMRR-Common Mode Rejection Ratio) is accomplished by the differential input, with the result that common mode input signals do not cause any variation in the current in R1-R2.

3. Input signals not accompanied by the GATE pulse are sensed by the comparator FD and cause the control logic to open switch S4 and close S3. In this way, the pulse is rejected and no contribution is added to the stabilization loop.

4. The input GATE signal or a monostable triggered by the TEST Function N.F(25).A(0) initiates the following command sequence:

a) Sets Flip-Flop FF1 and opens-through the control logic-switch S1. This causes the integrator consisting of OP1 and C1 to be set to the “Hold” state. Flip-Flop FF2 regenerates the GATE pulse, which disables comparator FD and opens-through the control logic-switch S4 and closes S2 as long as the GATE lasts. An input pulse applied during the GATE pulse generates a current I given by $V_{in}/(R1+R2)$ that is a charge $Q=I \cdot t$. This charge passes through T_2 - S_2 and after being integrated and memorized on condenser C1, generates an output voltage corresponding to $I \cdot t/C1$. At-the end of data conversion Flip-Flops FF1 and FF2 are reset, thus causing S1 to be closed and C1 to be discharged.

b) The end of the GATE signal inhibits the front-panel GATE input and triggers the "ΔT" monostable (waiting time for multiplexer settling time and LLD-ULD and offset preset).

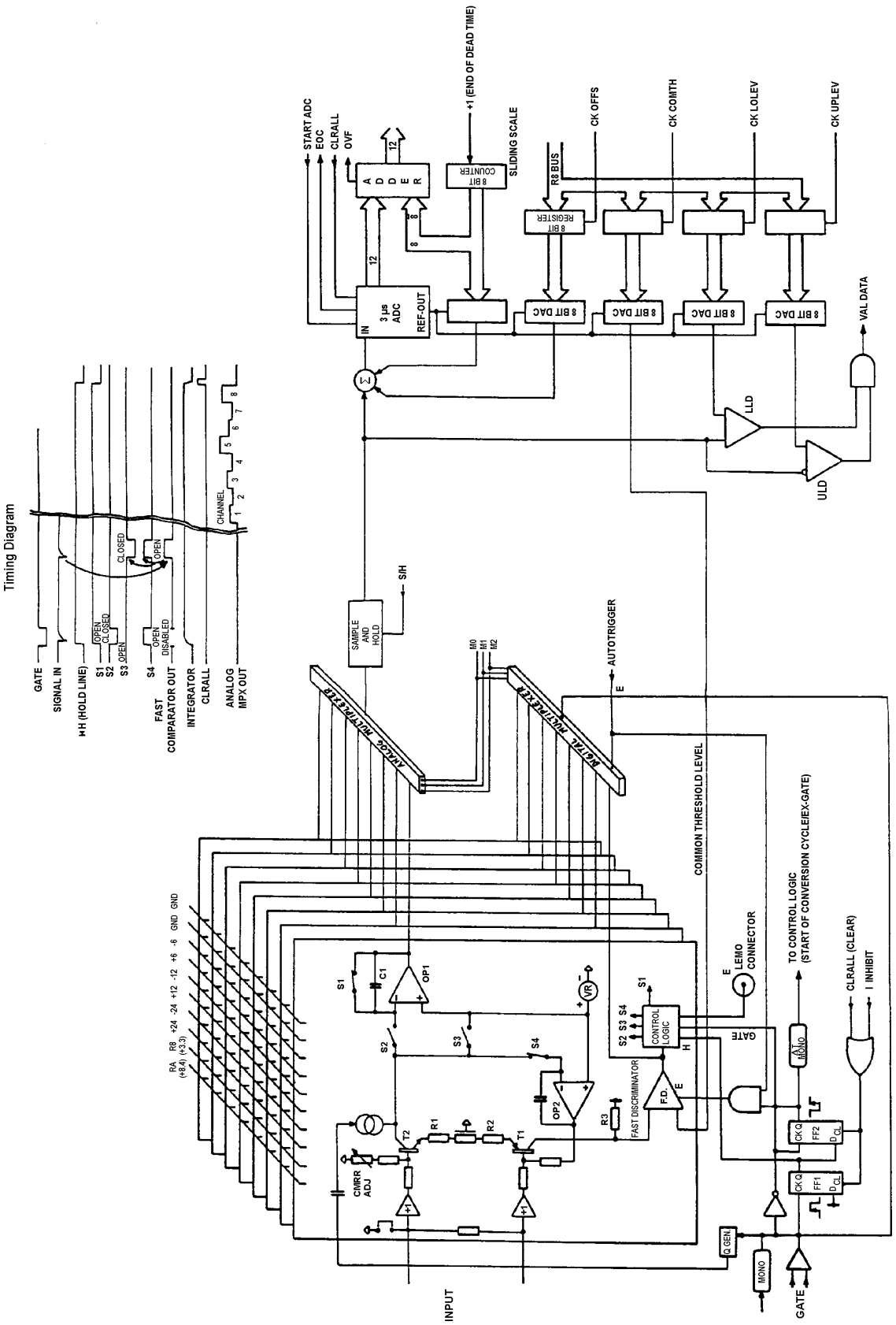


Figure 5: Input Circuit and ADC Block Diagram

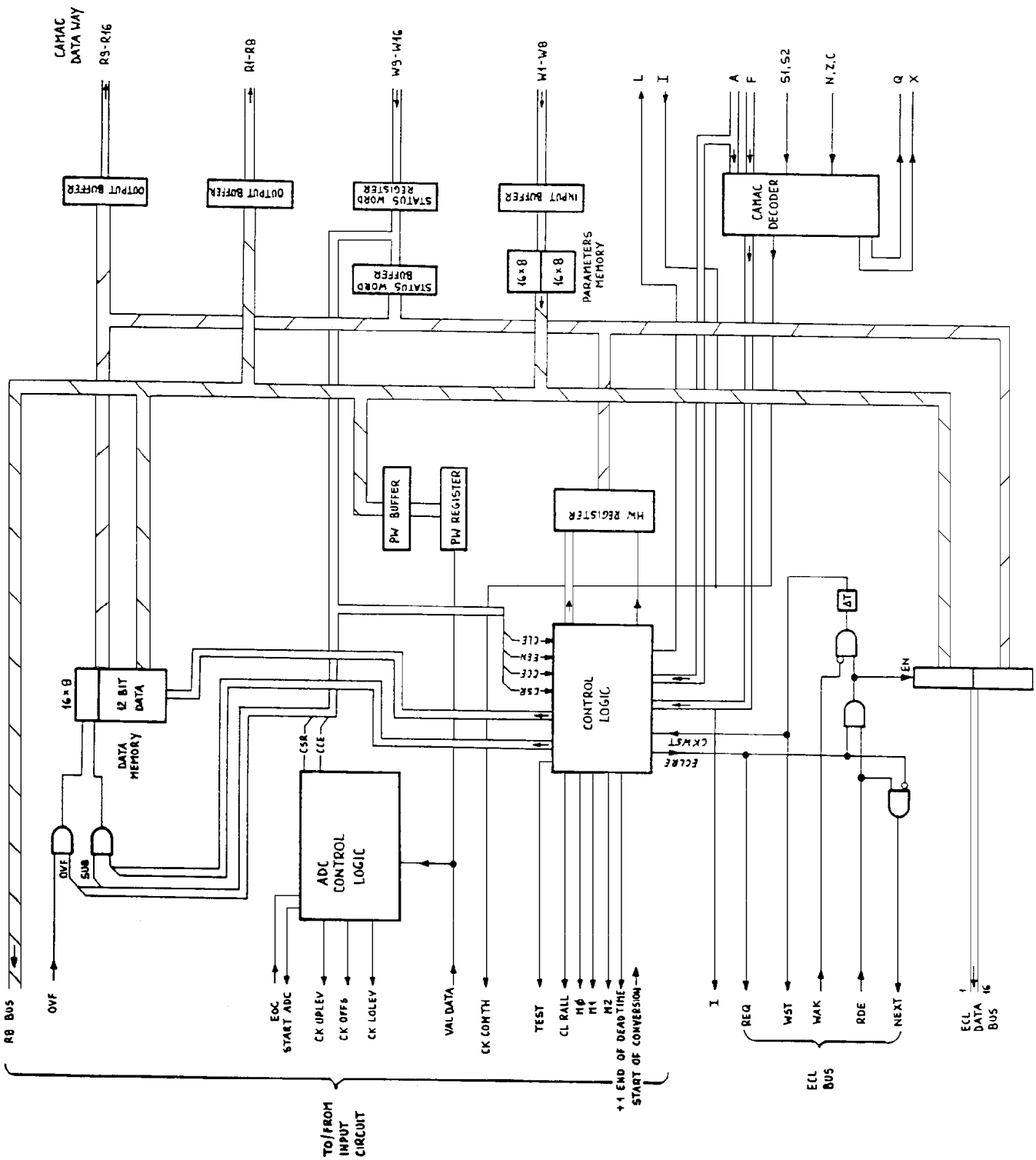


Figure 6: Logic Circuit Block Diagram

c) The end of the "ΔT" monostable sets the “Busy” state and starts conversion. As long as the module is in the “Busy” state all the functions of the CAMAC decoder are disabled, except the readout and CLEAR functions.

The analog outputs of the 8 modules are connected to an analog multiplexer. Three lines (M0, M1 and M2) sequentially select the inputs of the analog multiplexer, whose output is first memorized by a sample and Hold stage and then routed to the ADC.

The ADC used is a successive approximation (SAR) type using the differential linearity correction method (Sliding Scale) devised by Prof. Emilio Gatti.

The values of the Upper Threshold (ULD), Offset and Lower Threshold (LLD) levels of the 8 measurement inputs are stored in the Parameters Memory while the module is in the “Idle” state by the following functions:

N.F(17) . A(0-7) ULD
N.F(17) . A(8-15) LLD
N.F(20) . A(0-7) OFFSET

These values are loaded into the associated registers before each single data conversion by the following commands:

CKUPLEV = loads the value in the upper level register
(0 corresponds to 85%) (255 corresponds to 100%)

CKOFFS = loads the value in the offset register
(0 corresponds to -3%)
(128 corresponds to 0)
(255 corresponds to +3%)

CKLOLEV = loads the value in the lower level register
(0 corresponds to 0%)
(255 corresponds to 10%)

If the module is set for operation in the Zero Suppression Mode data conversion takes place only in the measuring channels whose value is higher than the set LLD level and lower than the ULD level.

If the module is set for operation in the Without Zero Suppression Mode or Addressed Readout Mode, data conversion is performed on all the 8 inputs independently of the threshold values.

Autotrigger Mode (Single Channel Mode)

The “Autotrigger” facility provides a convenient means of setting the threshold common to all the eight input modules in such a way that only the pulses not falling within the GATE are rejected. This prevents discriminator FD from releasing owing to the noise resulting in an incorrect interruption of the stabilization loop.

Comparator FD is continuously activated by the autotrigger line (E).

An input pulse exceeding the preset threshold level is instantly sensed by the collector of transistor T1, and therefore at the input of comparator FD. The output of the comparator is a signal having a length equal to the duration of the input analog signal. The output of the comparator of the input module under examination simulates-through the digital multiplexer – a GATE signal that initiates an operating sequence equivalent to the sequence caused by an external GATE-front-panel signal. (In the autotrigger operating mode, the GATE-front-panel signal is automatically disabled.)

Since the threshold level is common to all the 8 channels, the set threshold value after calibration of all the 8 channels will be the value of the nosiest measuring channel. The Common threshold level is stored into the associated register by the **CKCOMTH** line with the module in the "Idle" state via CAMAC functions:

N.F(20) A(9)	writes common threshold
N.F(4) A(9)	reads common threshold

The autotrigger operating mode is set via CAMAC function N.F(16). A(0-7). Subaddressed (0-7) selects the measuring channel to be investigated. The module is held to this state independently of the internal CLEAR signal or N.F(9). A(0) CAMAC clear. To switch the module to the normal operating mode, it is necessary to release either a Z or C or N.F(10). A(0) command. (This latter command performs two distinct functions: "Clears LAM" in the normal operating mode; "Clears Single Channel Mode" in the Autotrigger mode.)

E Input LEMO Connector

As a logic signal is applied, the measurement of the mean input level is suspended and the cancelling level feedback is maintained for the entire duration of the logic signal.

The maximum allowed duty cycle of the "hold" logic signal is 50%, with duration of the time intervals between adjacent "hold" signals of at least 100 microseconds.

– ECL Input level: FALSE = High (-0.8 V) feedback loop enabled
  TRUE = Low (-1.6 V) feedback loop disabled

– Input Impedance: 50 Ω V_{bb} (-1.2 V)

Analog Inputs, Impedance, Attenuation and Connection

The measuring channels may be preset for either "SINGLE-ENDED" Coaxial cable or "DUAL-ENDED" twisted-pair shielded cable connection.

If Single-Ended connection is used, the input impedance is 50 Ohm and the signal return is connected to ground via a wire jumper. In its standard version the Model 3341 is set for "Single-Ended" input.

If the Dual-Ended connection is chosen, the input resistor should be replaced with a resistor having a value equal to the line impedance (80 ÷ 110 Ohm) and the grounded jumper has to be removed on the signal return.

On changing the input impedance of the module, it is important to keep in mind that charge Q applied to the integrator is given by

$$\frac{V_{in}}{R1 + R2} \cdot t$$

$$Q = \frac{V_{IN}}{R1 + R2} \cdot t$$

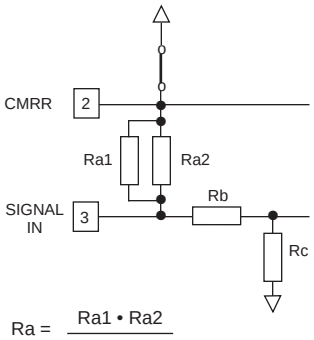
where: $R1 + R2 = 100\ \Omega$
$V_{IN} = i_{IN} \cdot Z_0$

t = length of the input pulse
Z_0 = input impedance of the module

To locate the resistor that determines Zo and the grounded jumper, refer to the component layout in Figure 7.

If it is wished to reduce the input signal, reference should be made to the following indications related to the input stage.

SINGLE-ENDED INPUT

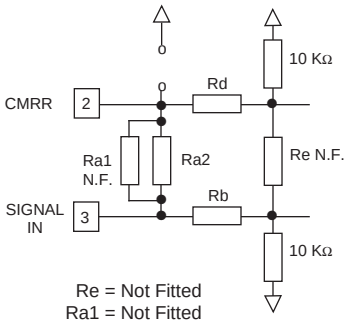


$$Ra = \frac{Ra1 \cdot Ra2}{Ra1 + Ra2}$$

$$Z_0 = \frac{Ra \cdot (Rb + Rc)}{Ra + Rb + Rc}$$

$$ß = \frac{Rb + Rc}{Rc}$$

DUAL-ENDED INPUT



Re = Not Fitted
Ra1 = Not Fitted

$$Z0 = Ra2$$

$$ß = \frac{Rd + Re + Rb}{Re}$$

Where Z0 = Input impedance of the module
ß = Attenuation Factor

To locate the resistors that determines Z_0 and B, refer to the component layout in Figure 7.

Example

Single-Ended	**Dual-Ended**
$Z_0 = 51\ \Omega$	$Z_0 = 100\ \Omega$
ß = 2	ß = 2
Mount Ra_1 = N.F. (Not fitted)	Rb=Rd=25.5 Ω
$Ra_2 = 100\ \Omega$	Re = 51 Ω
Rb = 51 Ω	Ra_2= Not Fitted
Rc = 51 Ω	

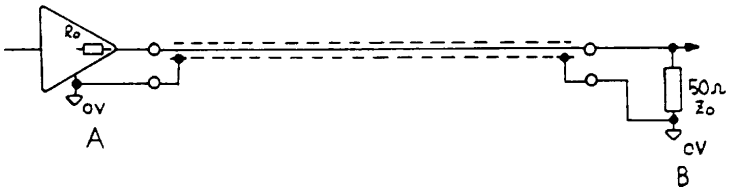
In its standard version the Model 3341 is set for “Single Ended” input:

$Z_0 = 50\ \Omega$
ß = 1 ($Ra_1 = 100\ \Omega$, $Ra_2 = 100\ \Omega$, Rb = 51 Ω , Rc = I0 KΩ)

The choice of the cable to be used for input signal connection depends on the nature and intensity of the electrical interferences present in the environment where the detector and the modules are located.

The advantages and drawbacks associated with some different types of connections are briefly discussed below.

Coaxial Cable - Single-Ended Connection

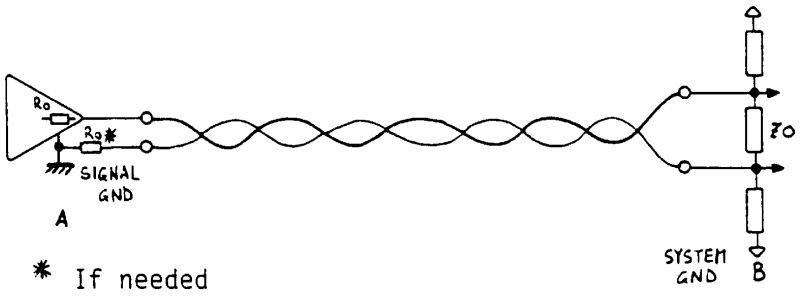


Easy to Perform

Advantages: Provides adequate shielding against radio-frequency signal inductors. Differences in the DC potential between points A and B are compensated by the “Q” module.

Drawbacks: Not differential input; alternate signals between points A and B are not cancelled. The Q module is able to cancel only low frequencies (50 Hz) and not completely.

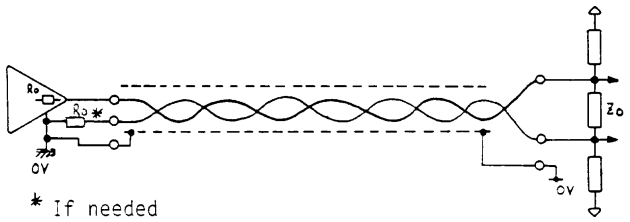
Twisted-pair Cable - Dual-Ended



Advantages: Easy to connect, High CMRR for ground difference signals.

Drawbacks: Extreme sensitivity to signals induced on twisted wires (Radio frequency - 50 Hz Power line, etc.).

Shielded Twisted Pair Cable True Differential Input



Advantages: Ideal to solve all problems outlined above.

Drawbacks: Difficult to connect (3 wires).

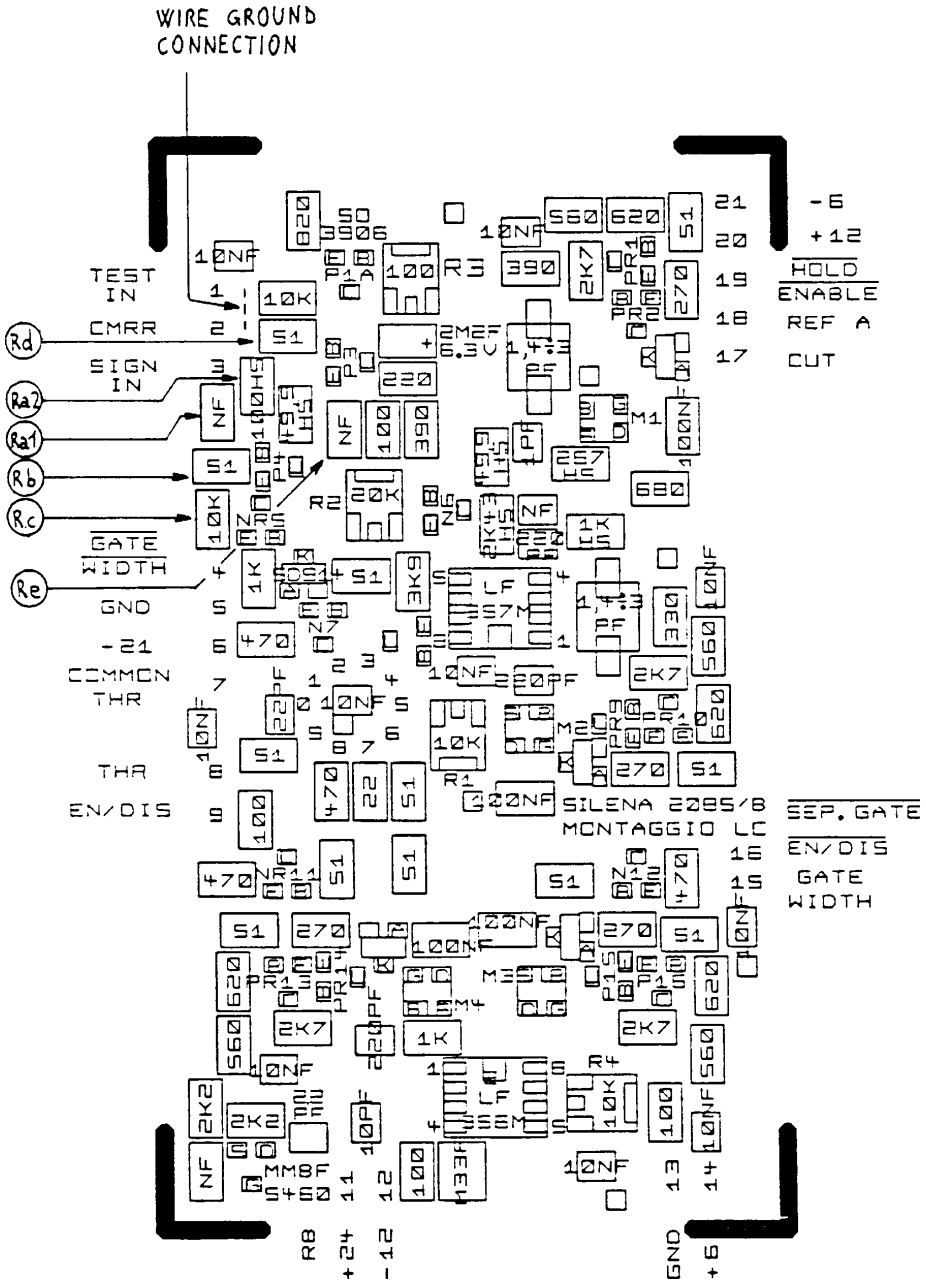


Figure 7