OPERATOR'S MANUAL

MODEL 3351

CAMAC 8-INPUT
PEAK SENSING ADC

LeCroy

Innovators in Instrumentation

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GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

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LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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OPERATING INSTRUCTIONS

GENERAL

The Model 3351 Peak Sensing ADC incorporates 8 analog memories with associated peak detectors and linear gates provided with thresholds featuring a common level adjustable via a CAMAC-programmable 8-bit DAC.

The analog memories outputs are routed, through an analog multiplexer, to a fast analog-to-digital converter (3 μsec) featuring offset control and two thresholds: a lower (LLD) and an upper (ULD) threshold. This makes it possible to assign different threshold and offset (zero energy intercept) values to each measuring channel.

A "Parameters Memory" contains the LLD, ULD and OFFSET values of each single channel, as well as the common threshold value. A 6-bit register (STATUS REGISTER) allows different data acquisition and readout modes of the 8 measuring channels. Data may be read out either via CAMAC or via the ECL Data Bus, depending upon the programming of the Status Register.

Both the Status Register and Parameters Memory must be previously loaded via CAMAC.

If enabled, the ECL Data Bus, located on the front panel, sends analog-to-digital conversion data sequentially in words of 16 bits with differential ECL levels (the first 12 bits are data bits plus 3 subaddress bits, plus the "Overflow" bit, if it exists).

A REQ output signal is generated when the ECL Data Bus is ready to deliver data.

In CAMAC mode, data is always read in 16 bit words in either sequential (Q stop mode) or addressed mode. When data is ready, a LAM signal may be generated and there is Q=1 with the readout function N.F(0) or N.F(2). The instrument includes provisions for testing the 8 input modules of the 3351 ADC via a CAMAC-controlled TEST signal with function N.F(25).A(0). This signal simulates a GATE command and applies a pulse corresponding to about 1/6 of the dynamics to the input of each channel. The ADC may be in any of two states: "Idle" or "Busy", depending on the GATE, CLEAR and internal CLEAR signals. (Internal CLEAR is applied after a conversion if there is no valid data or when data readout is performed in sequential mode).

GATE and CLEAR may be sent either via front-panel (ECL Command Bus) or via CAMAC. After a CLEAR signal, the ADC is in the "Idle" state, that is it is ready to receive a GATE signal (front-panel or test). The Status Register and the Parameters Memory may be loaded only when the module is in the "Idle" state. The GATE signal (front-panel or test) causes the ADC to go to the "Busy" state, during which no further GATE signal is allowed. Data conversion is enabled approximately 1 μsec after the GATE signal, and at the end of the conversion time data readout is

initiated. At this point, depending on the state of the Status Register and the data converted by the ADC, any of three conditions may occur:

1. Data readout via ECL port only (EEN = 1, see Status Register).
2. Data readout via CAMAC only (EEN = 0).
3. No data to be read. In this case, no data readout is performed.

During the “Busy” state, to disable the ongoing data conversion or to accept further GATE signals, it is necessary to apply a CLEAR signal. The ADC is ready to perform a new data acquisition 1.2 μsec after the CLEAR signal.

Analog Inputs

The 8 analog inputs are designed for positive signals. Input impedance is 1 KΩ with respect to the ground. When long-distance cables and short pulse shaping times are used (i.e. 0.5 μsec), it is advisable to replace the 1 KΩ resistor with a resistor corresponding to the impedance of the cable used. A threshold value common to all 8 inputs must be programmed via CAMAC to prevent the input noise associated with the gate signal from generating busy time.

CLEAR Function

The CLEAR function may be enabled either by an ECL CLEAR command of the front-panel ECL Bus or by CAMAC functions, Z, C and N.F(9).A(0) strobed by S2 or by an internal command generated after completion of sequential data readout or at the end of conversion, if no valid data is present.

After a CLEAR signal, the ADC changes to the “Idle” state and is held in this state until the next GATE signal is applied. During the CLEAR signal (duration of about 1.2 μsec) the input GATE is inhibited.

It is recommended to avoid sending new GATE commands in coincidence with the end of the CLEAR signal. This will prevent generation of sliced GATE commands.

External GATE Input

The GATE command should be sent only when the module is in the “Idle” state. It should never be sent in coincidence with the CLEAR signal (at least 1.2 μsec after the CLEAR function has been initialized). The GATE input may be inhibited by line 1 (CAMAC inhibit). A GATE signal activates the following functions:

1. Enable the Peak Detector circuit and hold the peak value.

2. The end of the GATE signal automatically inhibits the GATE input disabling further GATE signals.

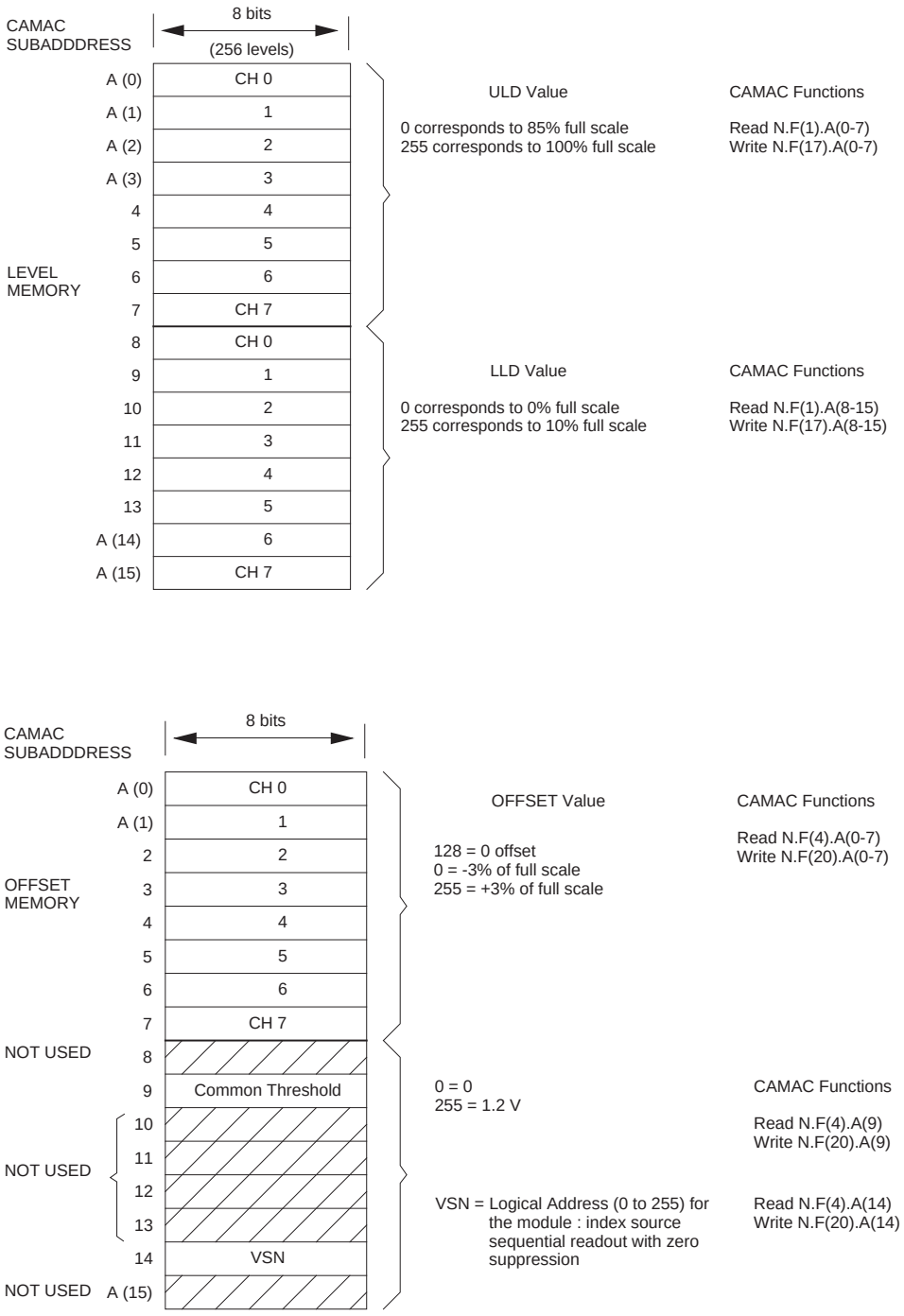
After a 1 μsec time delay it starts conversion, causing the ADC to change to the “Busy” state. For optimum results the GATE signal must be applied delayed with respect to the analog signal, but before the pulse to be measured reaches its peak, and must be maintained at least up to this instant.

ADC Thresholds and Offset Memory

The 3351 ADC includes a Parameters Memory made up of two 16x8 words groups. With the module in the “Idle” state, the threshold values (Low Level Discriminator-LLD; Upper Level Discriminator ULD), as well

as the Offset, Common Threshold and VSN (Virtual Station Number) values can be loaded into the Parameters Memory. Different threshold (ULD and LLD) and offset values may be assigned to each input; whereas the threshold is common to all the 8 input modules.

A schematic diagram of the ADC Parameters Memory is illustrated in the following drawing.



Model 3351 Parameters Memory

Test Function

The TEST function is initiated by the CAMAC command N.F(25).A(0) strobed by S2. If accepted, Q is equal to 1. This function is accepted only when the ADC is in the “Idle” state.

This function performs the following operations:

1. Applies a voltage pulse to the analog memories inputs.

2. Generates a GATE signal in coincidence with the pulse peak. During the entire duration of this pulse no signal is allowed on any of the analog inputs, even if the interconnecting cable may remain connected.

The GATE command (front panel) must not be sent while the Test function is in progress.

Overflow

The ADC actual dynamics is 3840 channels (4096 - 256); 256 channels are reserved for the Sliding Scale Circuit. Data having a content greater than or equal to 3840 is not considered to be valid for measurement. If this data is present, an Overflow indication is generated by the ADC control circuit. Via the Status Register bit (R12) (See Status Register) it is possible to enable the Data Memory to associate the Overflow information with the conversion Data and store it into the DATA WORD at position R16 (see ECL or CAMAC Data Structures).

Status Register

The Status Register is a memory into which the Status Word is loaded. The Status Register is made up of two distinct sections.

The first (low order 8-bit) consists of a word of the Parameters Memory and contains the address number of the module (VSN-Virtual Station Number). This is used to identify the data source during Sequential readout with zero suppression mode.

The other section contains the information that determines the data acquisition and readout modes. The Status Register is written by the CAMAC function N.F(20).A(14) strobed by S1 and is read out by function N.F(4).A(14).

These two functions are accepted only when the module is in the “Idle” state; there is Q response when the functions are accepted. After switching on the module, the content of the Status Register is undefined. The CAMAC initialization function (Z) sets the 6 Status Register bits (R10 through R16) to the “1” state, but will not affect the VSN register, whose content remains undefined. The other CLEAR signals will not reset the Status Register.

R16							R9	R8 R1
0	CLE	CSR	CCE	OVF	EEN	SUB	0	VSN

The six functions of the Status Register are as follows:

SUB (W10-R10) Channel Subaddress Enable

If enabled (SUB=0), in addition to the ADC data, the binary addresses of the 8 analog memories (0 for the 0 channel, etc.) are loaded into the Data Memory at positions R13, R14, R15.
If SUB = 1, the value of R13-R14-R15 in the Data Word is always “zero”.

EEN (W11-R11) ECL Bus Enable

If EEN = 1, only the ECL port readout is enabled.
If EEN = 0, only CAMAC readout is enabled.

OVF (W12-R12) Overflow Indication Enable

If OVF = 0, the Overflow indication, if it exists, is loaded into the Data Memory at position R16.
If OVF = 1, the value of R16 in the Data Memory is always “zero”.

CCE (W13-R13) Zero Suppression Enable

CSR (W14-R14) Sequential Readout Enable

These two bits allow 3 different data acquisition and readout modes to be performed.

1. With Zero Suppression: CSR = 1 and CCE = 1
   Data conversion takes place only in valid channels (i.e. channels with pulses above the Common Threshold and falling within the LLD-ULD window).
   These valid channels are readout in sequential mode either via the ECL bus or CAMAC.

2. Without Zero Suppression: CSR = 1 and CCE = 1
   All the 8 input channels are converted and read sequentially. Readout may be either via the ECL BUS or CAMAC.

3. Addressed Readout: CSR = 0 and CCE = Indifferent
   All the 8 channels are converted and the ADC data is read by CAMAC only in addressed mode with any of two functions N.F(0).A(0-7) or N.F(2).A(0-7). The readout channel is identified by Subaddress A: A(n) , n = channel # (0-7).

CLE (W15-R15) CAMAC LAM Enable

If CLE = 1, the LAM output is enabled to indicate that there is valid data to be read by CAMAC; in the “Zero Suppression” mode, if no valid data is present, LAM will not be enabled. If CLE = 0, the LAM output will be disabled.

Note: After the CAMAC initialization (Z) the 6 bits of the Status Register are set to “1”. This means “With Zero Suppression mode”, ECL readout, SUB and OVF disabled.

ECL Data Bus

The module delivers 16-bit data words with complementary ECL outputs at the ECL Data Bus connector. The maximum readout frequency is 8 MHz. If several modules are connected, the pull-down resistors must be removed in all modules, except for the last module (see Figure 1). When these resistors are mounted, the associated EED indicator is lighted. If several modules are connected, only the positive ECL output is used; the negative output should be connected to ground. See section on ECL Data Structures.

ECL BUS - REN/PASS

In addition to the ECL CLEAR and GATE signals, all those signals with ECL levels that control and allow use of the ECL DATA Readout are present at the ECL Bus and REN/PASS connectors.

These signals include :

1. **Busy Output (BUSY)**
   This output is set to the "1" state 1 μsec after the end of the GATE Signal and is held to this state until after the end of the readout cycle (ECL Readout or CAMAC Readout). The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL Bus (CLR). The ADC is ready to start a new conversion 1.2 μsec after the end of the BUSY state.

2. **Write Strobe Output (WST)**
   Indicates the time period during which the data word present on the ECL Data Bus can be stored in the external memory. WST is generated a minimum of 10 nsec after the data is ready. Its width is higher than 40 nsec. The ECL Data Bus data is maintained stable as long as the WST pulse lasts.

3. **Request Output (REQ):**
   Indicates that the module is ready to send data to the ECL Data Bus. The REQ signal is generated at the end of conversion if the bit related to ECL Readout in the Status Register has been set. The REQ signal remains until after the last data word has been read or a CLEAR command has been given.

4. **Write Acknowledge Input (WAK)**
   This input receives the acknowledge signal indicating that the data present on the ECL Bus has been loaded into memory and the next data word may be sent. The next WST signal is generated at least 50 nsec after the WAK signal. Minimum WAK width must be 30 nsec.

ECL PORT ENABLE/PASS

1. **Readout Enable Input (REN)**
   The REN signal indicates to the module that it can take control of the ECL Data Bus; REN must be maintained during the entire readout time. The signal enables the ECL Data Bus, WST Output and WAK input if the module is ready for data transfer (REQ output ON). If there is no data present (REQ=OFF) the REN signal automatically generates the PASS signal, which becomes REN for the next module.

2. **PASS Output (PASS)**
   Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has completed data transfer. The PASS output

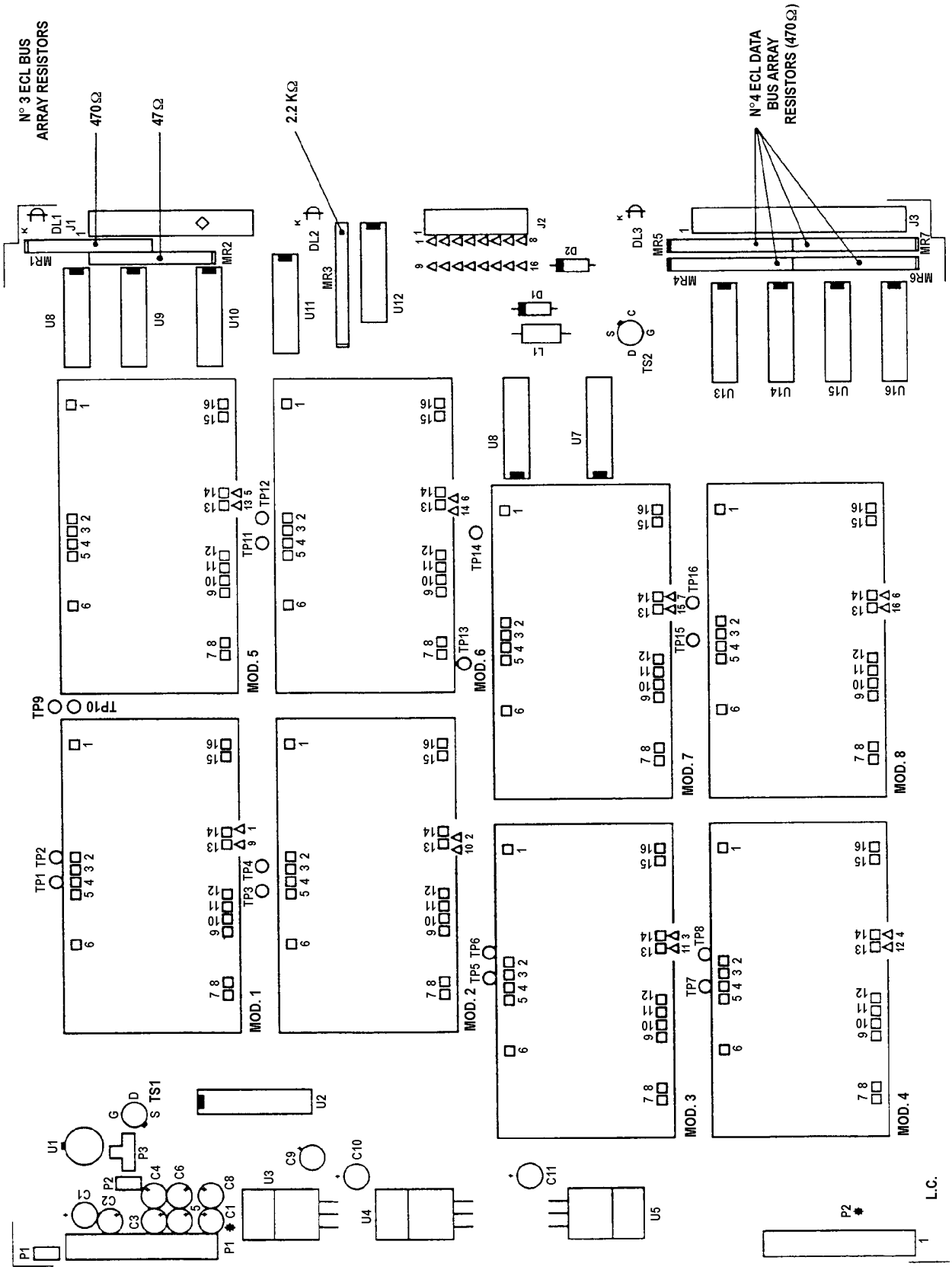


Figure 1: Matching and pull-down resistors position.

signal is generated by the REN line in the absence of the REQ internal command or, if this command is present, at the end of data readout. The transit time between the REN and PASS output is typically 3 nsec (6 nsec max.) if the module does not include data readout capabilities.

As previously mentioned for the ECL Data Bus, if several modules are connected, it is necessary to remove the pull-down resistors in all modules, except for the last one. The LED indicator is lighted when the resistors are mounted. (see Figure 1).

The timing sequence of ECL Data transfer is described in the following:

1. After data conversion, the ADC module sends the REQ signal and waits for the REN Readout Enable.

2. An external driver provides the REN line.

3. The REN signal clocks the internal flip-flop in the requesting ADC module and inhibits the PASS output. The non-requesting ADCs closer to the driver are disabled by the same REN signal. The non-requesting ADCs far away from the driver do not receive the REN signal because it is stopped in the requesting module (no PASS signal). Moreover, the REN signal sets the WST line high and enables the first data word to transit through the ECL Data Bus. The module remains in this state waiting for the WAK signal. As soon as the WAK signal is received, the WST signal is released and is held to this position for at least 60 nsec by an internal protection. During this time the module makes available the next data word, which is loaded into the ECL Data Bus with the leading edge of the next WST signal.

4. After the last data word from an ADC has been read, the request REQ signal is removed and the REN signal is routed to the PASS output, thus enabling readout of the next ADC module.

5. If a far off ADC has sent in a request, the common REQ line remains high and data readout from this module is initiated.

6. If a module closer to the driver has data ready, it waits until the REN signal goes low and as soon as this occurs it sends its own REQ signal. (This module was disabled by the REN signal).

ECL Bus Readout Interrupt

An ongoing ECL Bus readout may be momentarily interrupted in two different ways.

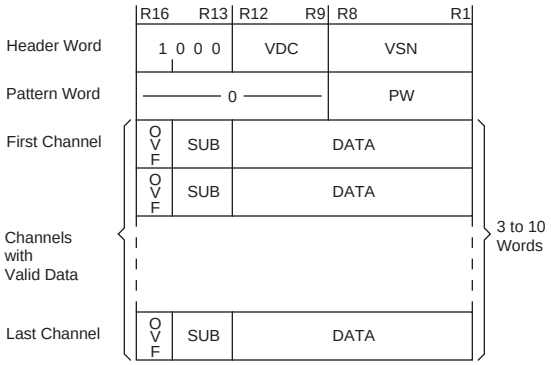
1. By not sending a WAK signal after a WST signal. In this case, the data word on the ECL Data Bus remains until the WAK signal is received.

2. By interrupting the WAK signal, stopping it after the first transition. If this occurs, the WST command is terminated and the next data word is placed on the ECL Data Bus, but it is only upon release of the WAK signal that the next WST will be activated again.

ECL Data Structures

Note: EEN, CSR, and CCE are STATUS WORD bits.

1. EEN = 1, CSR = 1, CCE = 1



Zero suppression is on. Up to 8 data words is to be read. Sequential readout only is possible on ECL BUS. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in Status Register is 0.

2. EEN = 1, CSR = 1, CCE = 0

R16	R15 R13	R12 R1	Offset
OVF	SUB	0-DATA	1
OVF	SUB	1-DATA	2
OVF	SUB	2-DATA	3
OVF	SUB	3-DATA	4
OVF	SUB	4-DATA	5
OVF	SUB	5-DATA	6
OVF	SUB	6-DATA	7
OVF	SUB	7-DATA	8

Always 8 data words are to be readout. Sequential readout only is possible on ECL BUS. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in Status Register is 0.

CAMAC Commands and Functions

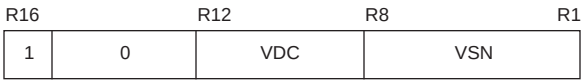
Note: If the module is in BUSY Status (BUSY LED on), only data readout and clear functions can be executed. Busy is released after clear and when all data is readout. The BUSY line is connected on the Common ECL Bus.

F(0)•A(0): Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be readout.

F(0)•A(0-7): Reads data addressed (CSR=0). Q-response is 1 if there is the data to be read out.

F(0)•A(14): Reads Header Word (Q=1 if module is in BUSY status).

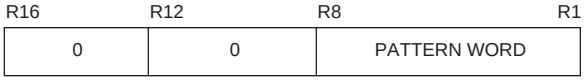
HEADER WORD



Header Word contains an information about the logical address of the module (VSN virtual station number bit 1-8) loaded to STATUS REGISTER, and an information about a number of valid data (VDC valid data counter). Q-response is 1 if there is the data to be readout.

F(0)•A(15): Reads Pattern Word (0=1 if module is in BUSY Status).

PATTERN WORD



Pattern Word contains a bit muster that shows which channel has a valid data. Bit R1 corresponds to ch.0.

F(1)•A(1-7): Reads threshold Memory (upper threshold). Q=1 if BUSY=0.

F(1)•A(8-15): Reads threshold Memory (lower threshold). Q=1 if BUSY=0.

F(2)•A(0): Reads the data memory sequential (CSR=1). Memory address is incremented with S2. Q-response is 1 if there is the data to be read out.

F(2)•A(0-7): Reads data addressed (CSR=0) and clears with F(2)•A(7) strobed on S2. Q-response is 1 if there is the data to be read out.

F(2)•A(14): Reads Header Word in data addressed mode (CSR=0) (Q=1 if module is in BUSY status).

F(2)•A(15): Reads Pattern Word and clears LAM (Q=1 if module in BUSY status).

F(4)•A(0-7): Reads offset memory (Q=1 if module isn't in BUSY status).

F(4)•A(9): Reads common threshold (Q=1 if module isn't in BUSY status).

F(4)•A(14): Reads Status Word Register (Q=1 if module isn't in BUSY status).

F(8)•A(0): Tests LAM. Q=1 if LAM is set.

F(9)•A(0): Clears ADC and control logic. Doesn't clear memories and status register.

F(10)•A(0): Clears LAM. Q=1.

F(16)•A(0-7): Reserved for ADC Model 3341.

F(17)•A(0-7): Writes threshold memory (upper thr. 8 bits 0-255) correspond to 85-100% full scale. (Q=1 if module isn't in BUSY status).

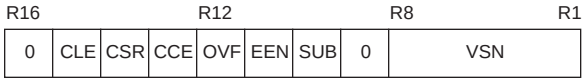
F(17)•A(8-15): Writes threshold memory (lower thr. 8 bits 0-255) correspond to 0-10% full scale. (Q=1 if module isn't in BUSY Status).

F(20)•A(0-7): Writes offset memory, 8 bits (0-255) correspond to ±3% of full scale, 128 correspond to 0 V. (Q=1 if module isn't in BUSY status).

F(20)•A(9): Write common threshold 8 bits (0-255). (Q=1 if module isn't in BUSY status).

F(20)•A(14): Writes Status Word Register (Q=1 if module isn't in BUSY status).

STATUS WORD



R1-R8 (VSN) Logical address of the Module
R10 (SUB) when SUB=0 subaddress enabled (see data structure)
R11 (EEN) when EEN=1, ECL readout enabled (EEN=0 → CAMAC enabled)
R12 (OVF) when OVF=0, the overflow bit enabled (see data structure)
R13 (CCE) when CCE=1, zero suppression enabled, only if CSR=1
R14 (CSR) when CSR=1, CAMAC sequential readout enabled
R15 (CLE) when CLE=1, CAMAC LAM enabled.

Note: The all bits of S.W.R. are set to 1 by CAMAC Z=init. function

F(25)•A(0): Test function (0=1 if module isn't in BUSY status).

Z: Initialize; clears the module and sets the Status Register bits 9-16 to 1. Does not clear the memory.

C: Clears the Module. Does not clear the Status Register and memory.

I: Inhibits the Gate input.

X: X response is generated for all valid functions.

Q: Q response is generated when the function can be executed.

L: LAM set, if enabled, after the end of conversion and if there is valid Data to be read.

The Status Word Register CLE, CSR, CCE, OVF, EEN, SUB bits, VSN - Virtual Station Number and Parameters Memory must be written before acquisition begins.

CAMAC Readout

CAMAC Readout may be performed in either "sequential" mode or "addressed" mode, depending upon the state of the CSR bit of the Status Register.

CSR = 1: Enables Sequential Readout: at the end of the conversion cycle the first data word is available on the CAMAC Dataway. The Q response is given as long as there is data to be read. After the last data word has been read, the internal CLEAR signal causes the ADC to go to the "Idle" state. Data is read with functions N.F(0).A(0) or N.F2.A(0). On completion of the readout of each single data word (at the end of S2) the address of the ADC Data Memory is incremented and the next data word is sent.

CSR = 0: Enables Addressed Readout: at the end of the conversion cycle, the various channels can be read by addressing the channel to be read via CAMAC with Subaddress A. Readout functions are N.F(0).A(0-7) or N.F.(2).A(0-7). With function N.F(0).A(0-7) the Q response is given each time a data word is read and the module is maintained enabled to send the requested data until a CLEAR function is released. With function N.F(2).A(0-7) the Q response is given each time a data word is read but the CLEAR function is automatically generated by Subaddress 7 N.F(2).A(7) strobed by S2.

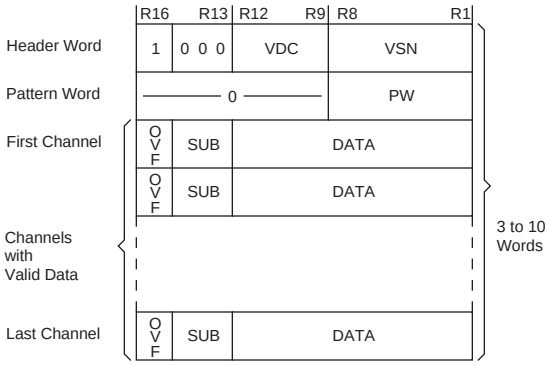
LAM Handling

The LAM (Look-at-me) is activated when the related bit of the Status Register is set to "1". It is activated as soon as data is ready for CAMAC readout. During Sequential Readout the LAM is reset after the last data word has been read. Function N.F(8).A(0) is used to test the state of the LAM. Q = 1 if the LAM is present. The LAM may also be cleared by the following functions: ECL CLEAR front panel, Z, C, N.F(9).A(0) strobed by S2.

CAMAC Data Structures

Note: EEN, CSR and CCE are Status Word bits.

1. Read Data F(0).A(0), F(2).A(0), EEN = 0, CSR = 1, CCE = 1



Zero suppression is on. Up to 8 data words are to be read. Sequential readout is on. Bit 16=OVF (overflow) is enabled when OVF-bit in Status Register is 0. Subaddress bits are enabled when SUB bit in S.R. is 0.

2. Read Data F(0).A(0), F(2).A(0), EEN = 0, CSR = 1, CCE = 0.

R16	R15 R13	R12 R1	Offset
OVF	SUB	1-DATA	1
OVF	SUB	2-DATA	2
OVF	SUB	3-DATA	3
OVF	SUB	4-DATA	4
OVF	SUB	5-DATA	5
OVF	SUB	6-DATA	6
OVF	SUB	7-DATA	7
OVF	SUB	8-DATA	8

Always 8 data words are to be readout. Sequential readout is on.
HW can be read with F(0)•A(14) or F(2)•A(14).
PW can be read with F(0)•A(15) or F(2)•A(15).

Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is 0.
Subaddress bits are enabled when SUB bit in S.R. is 0.

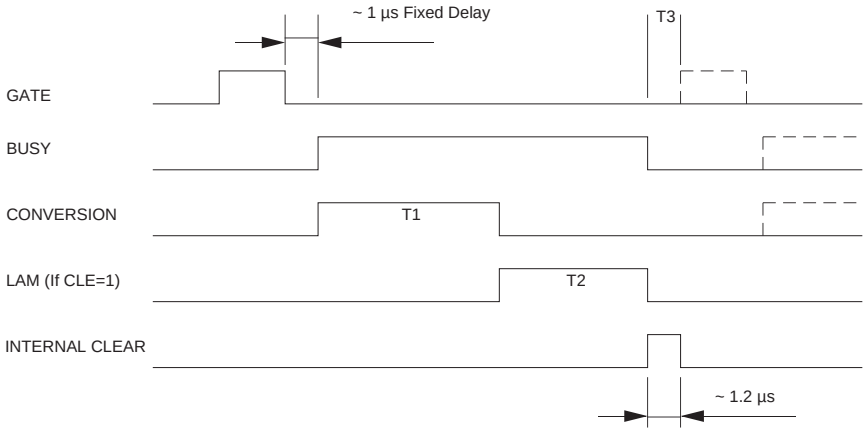
3. Read data F(0).A(0-7), F(2).A(0-7), EEN = 0, CSR = 0, CCE = X

R16	R15 R13	R12 R1	Offset
OVF	SUB	A(0)+DATA	1
OVF	SUB	A(1)-DATA	2
OVF	SUB	A(2)-DATA	3
OVF	SUB	A(3)-DATA	4
OVF	SUB	A(4)-DATA	5
OVF	SUB	A(5)-DATA	6
OVF	SUB	A(6)-DATA	7
OVF	SUB	A(7)-DATA	8

CAMAC Addressed (random) readout. Bit 16=OVF (overflow) is enabled when OVF bit in Status Register is 0. Subaddress bits are enabled when SUB bit in Status Register is 0.

Readout Timing Diagram

Figures 2 and 3 show the readout timing sequence via CAMAC and via ECL BUS.



T1 depends on CSR and CCE status
CSR=1 and CCE=1 T1=N•4 µs (N=number of valid channels)

CSR=1 and CCE=0 or
CSR=0 and CCE=X T1=32 µs

T2 depends on CSR and CCE status
CSR=1 and CCE=1 T2=(2+N)•t (N=number of valid channels)

CSR=1 and CCE=0 T2=8•t
CSR=0 and CCE=X T2 with function N.F(0).A(0-7) terminates upon release of the CLEAR function; with function N.F(2).A(0-7) terminates with function N.F(2).A(7) strobed by S2

T3 protection time : next gate must follow the end of LAM for at least 1.2 µs

Figure 2: Acquisition and CAMAC Readout Timing. Note: this diagram does not define the logic state of the signals: Low = FALSE, High = TRUE

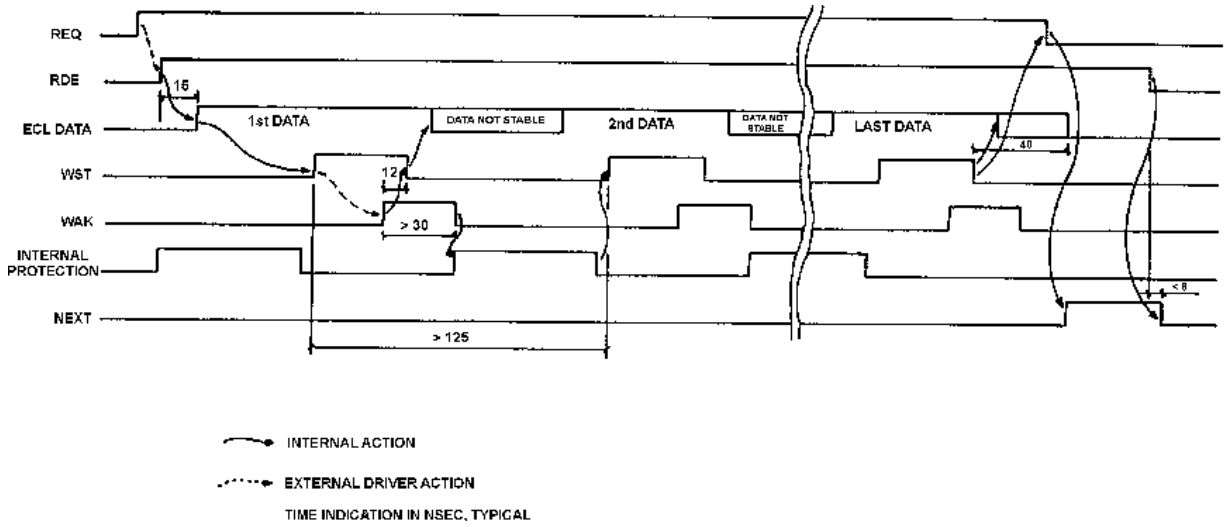


Figure 3: ECL BUS Timing. Note: this diagram does not define the logic state of the signals: Low = FALSE, High = TRUE

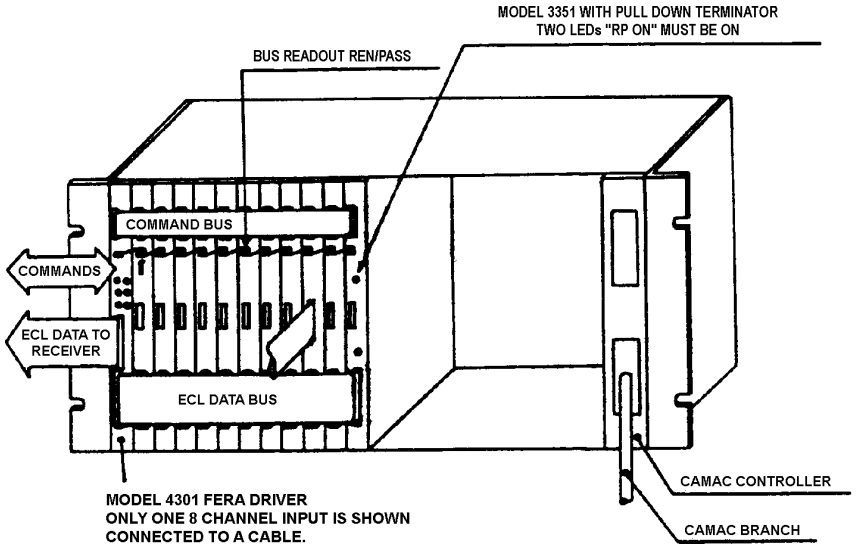


Figure 4: FERA System Connections

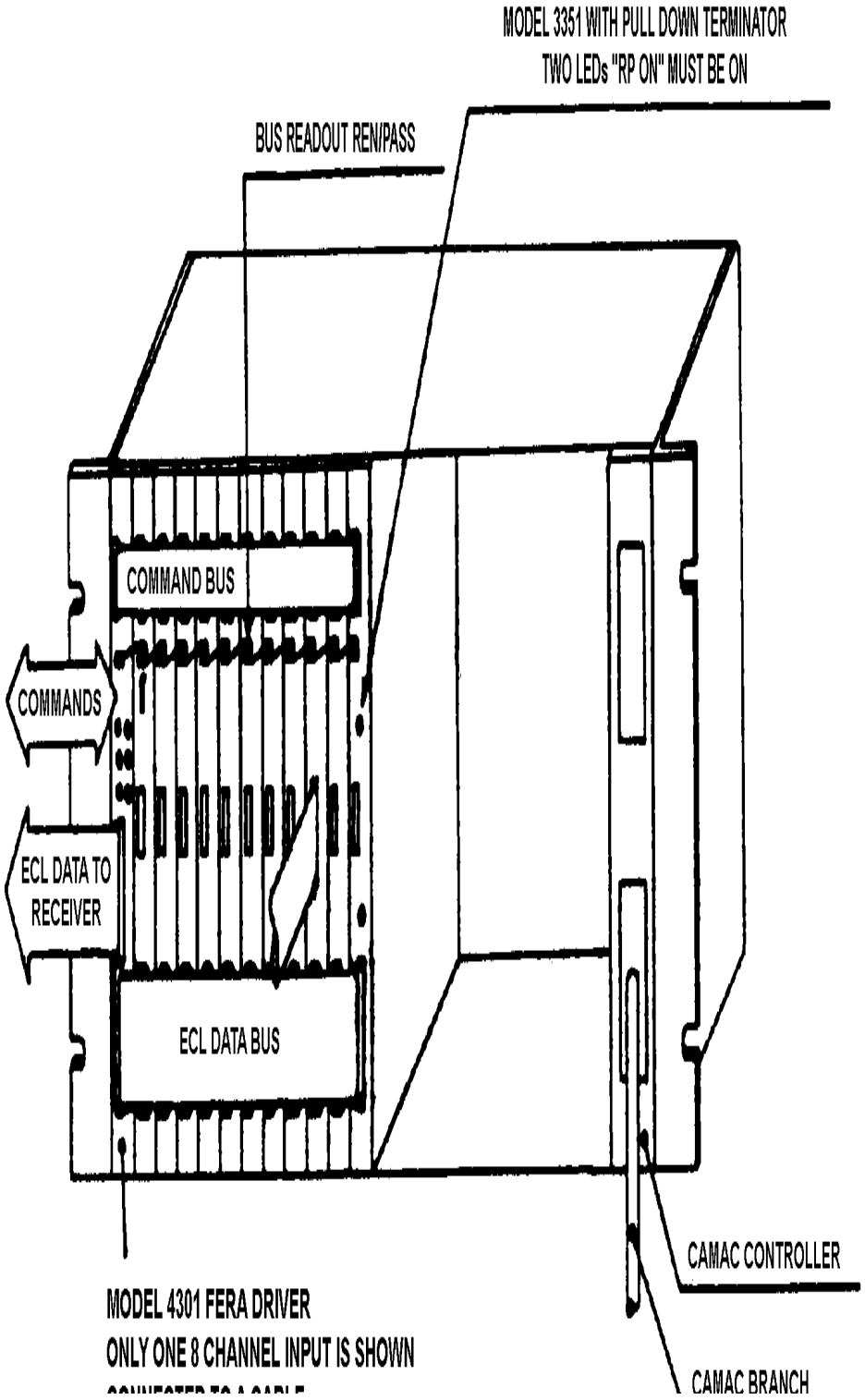


Figure 5: CES System Connection

GENERAL

The 3351 module is made up with three types of printed board:

1. A Mother Board including the GATE, test and ECL logic circuitry and the TTL → ECL adapting circuitry related to the front-panel Bus. This circuit also support the 8 analog modules.

2. Eight analog modules (analog memories).

3. A circuit including the Analog-to-Digital Converter, Thresholds, DAC's and the entire ADC logic circuitry.

Description
(see Figures 6 & 7)

A GATE input signal or a monostable triggered by the TEST function N.F(25).A(0).S2 initiates the following sequence:

1. Enables the peak detector and analog storage of the input pulse.

2. At the end of the GATE signal, inhibits the front panel GATE input and trigger the "ΔT" monostable (waiting time for analog multiplexer setting time and LLD-ULD and offset preset).

3. The end of the "ΔT" monostable sets "BUSY" state and starts conversion. During the "BUSY" state in the CAMAC decoder, all functions except the readout and CLEAR functions are disabled. Storage of the peak value of the input signal is individually performed for each single channel via a module using SMT (Surface Mounting Technology) mounting techniques.

The operating principle is based upon comparison between the input and the output signal of a "Follow and Hold" circuit in order to determine the instant when the signal reaches the peak and then go from the "Follow" state to the "Hold" state. The input signal, after passing through a 4 to 1 attenuator (10 V F.S. to 2.5 V F.S.) and a 1 gain amplifier, is applied to the threshold circuit*.

On overcoming the preset threshold value, flip-flop FF1 is set. This flip-flop activates the comparison (Fast Comparator) between the input signal and the output signal from the "Follow and Hold" circuit. As soon as the input signal goes below the output signal the comparator sets flip-flop FF2. This flip-flop inhibits the input linear GATE and sets the analog memory to the "Hold" position.

The analog outputs from the 8 modules are connected to an analog multiplexer. Three lines (M0, M1 and M2) sequentially select the inputs of both the analog and digital multiplexer (Peak Detector).

*Note: Since the threshold circuit is DC coupled with the input, if a DC level overlaps the signal, the following error conditions will occur:

a) Positive DC level - The threshold is held to the "ON" state and no peak is detected. The result is that the value converted by the ADC will be zero. Corrective action: the value of the Common Threshold should be incremented via CAMAC command

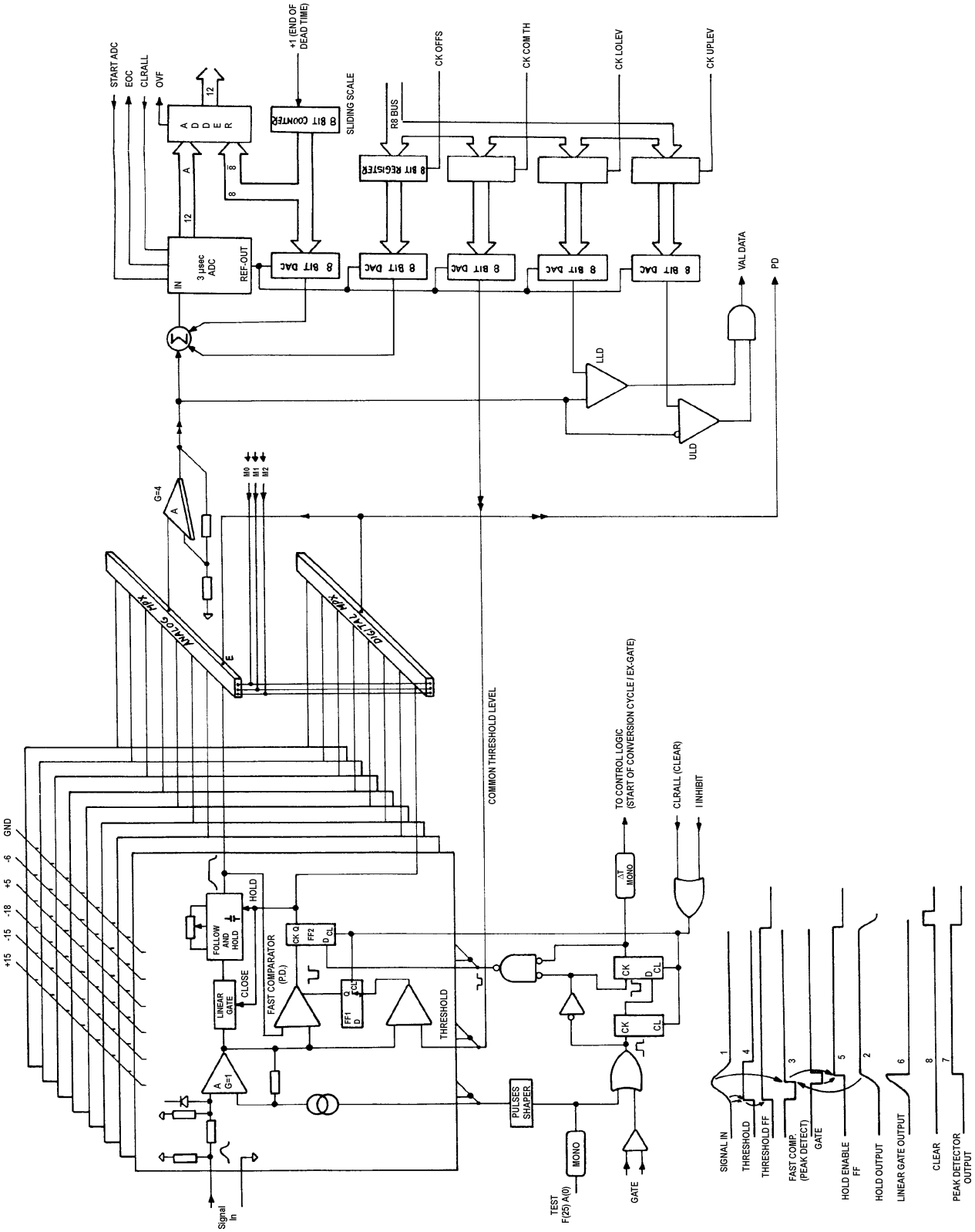


Figure 6: Input Circuit and ADC Block Diagram

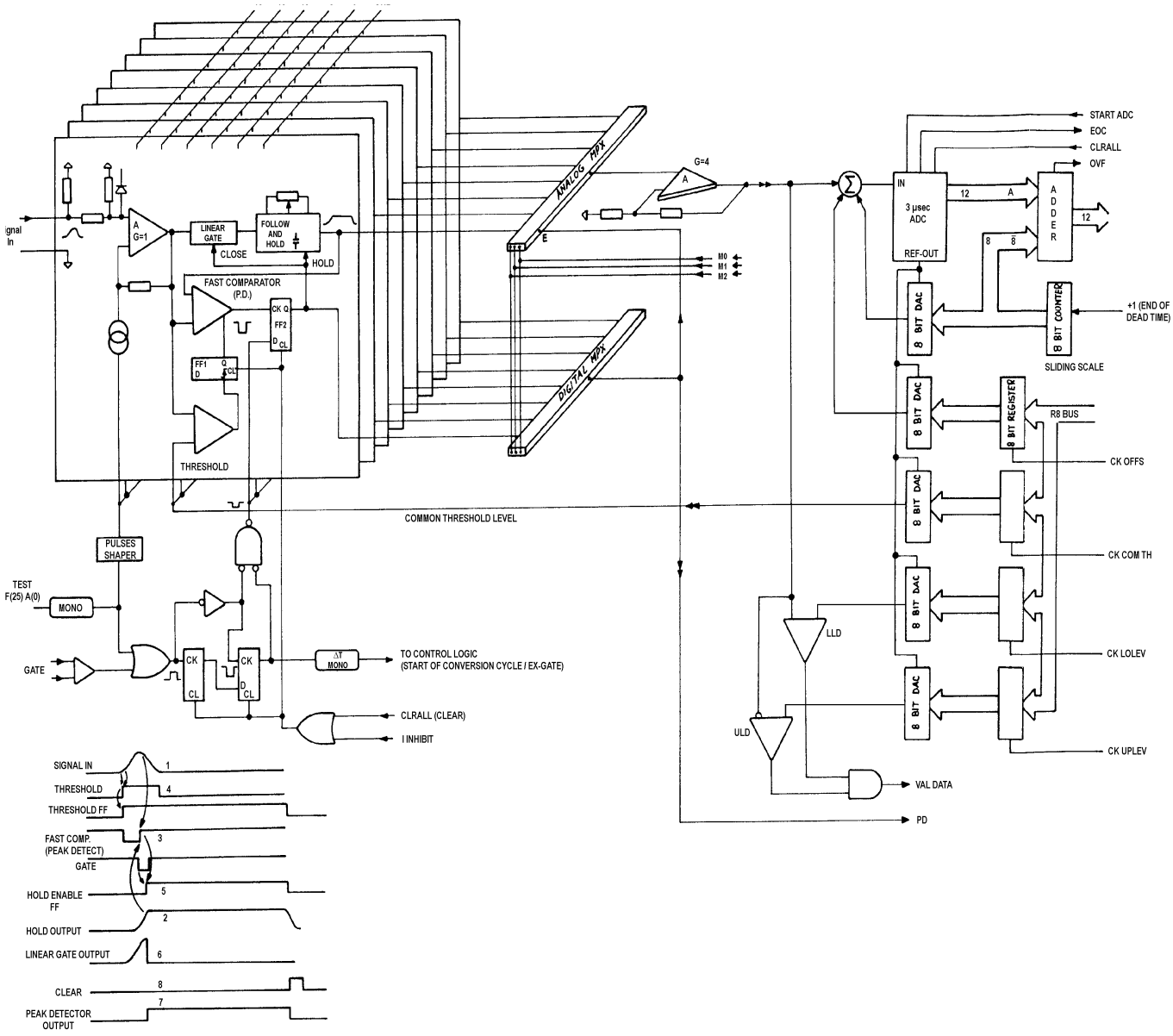


Figure 7: Logic Circuit Block Diagram

b) Negative DC level - The input pulses lying between - VIN (DC) and V THRESHOLD are not accepted. Corrective action: the direct level should be corrected by external control.

Only if PEAK DETECTOR is ON the output from the analog MPX is enabled. After being amplified by 4 (from 2.5 V F.S. to 10 V F.S.) it is routed to the ADC. The ADC used is a successive approximation type (SAR) with correction of the differential linearity using the sliding scale method devised by Prof. E. GATTI.

The Common Threshold level is stored into the associated register through the CKCOMTH line during the “Idle” state via CAMAC function N.F(20).A(9).

The values of the Upper Threshold (ULD), Offset and Lower Threshold (LLD) of the 8 measurement inputs are stored into the Parameter Memory while the module is in the “Idle” state by the following functions:

N.F(17).A(0-7) ULD
N.F(17).A(8-15) LLD
N.F(20).A(0-7) OFFSET

These values are loaded into the associated registers before each single data conversion by the following commands:

CKUPLEV = loads the value in the upper level register 0 corresponds to 85% F.S., 255 corresponds to 100% F.S.

CKOFFS = loads the value in the offset register 0 corresponds to -3% F.S., 128 corresponds to 0, 255 corresponds to +3% F.S.

CKLOLEV = loads the value in the lower level register 0 corresponds to 0% F.S., 255 corresponds to 10% F.S.

If the module is set for operation in “Zero Suppression Mode” data conversion takes place only for the measuring channels with Peak Detector indication, provided that their values are higher than the preset LLD level and lower than the ULD level. If the module is set for operation “Without Zero Suppression Mode” or “Addressed Readout Mode” data conversion takes place on all 8 inputs independently of the Peak Detector and threshold values.

The analog Multiplexer remains inhibited in the presence of inputs without Peak Detector indication with the result that the converted value will be “zero volt” $\pm$ the preset offset value.

Acceptable Signal In and Gating Time

This paragraph provides information regarding acceptable input pulses and the sampling time (Gating Time) to be used to achieve the best results. As mentioned in the technical specifications, the leading edge of the pulse is the main limitation. This should be ≥ 1 μsec and ≤ 8 μsec.

With fast leading edge the main limitation is posed by the “Settling Time” of the “Follow and Hold” circuit, whose response to a fast step is as follows:

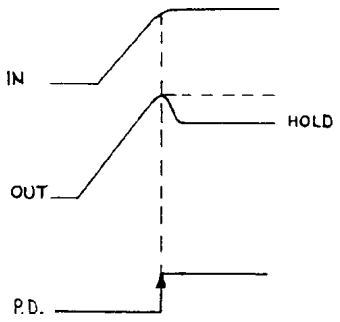


Figure 8

As can be seen, the peak detector is activated on occurrence of the output pulse overshoot with the result that an incorrect peak value is stored. When pulse shaping times are too long, false peak detections may occur due to the gain of the comparator and the noise added to the pulse.

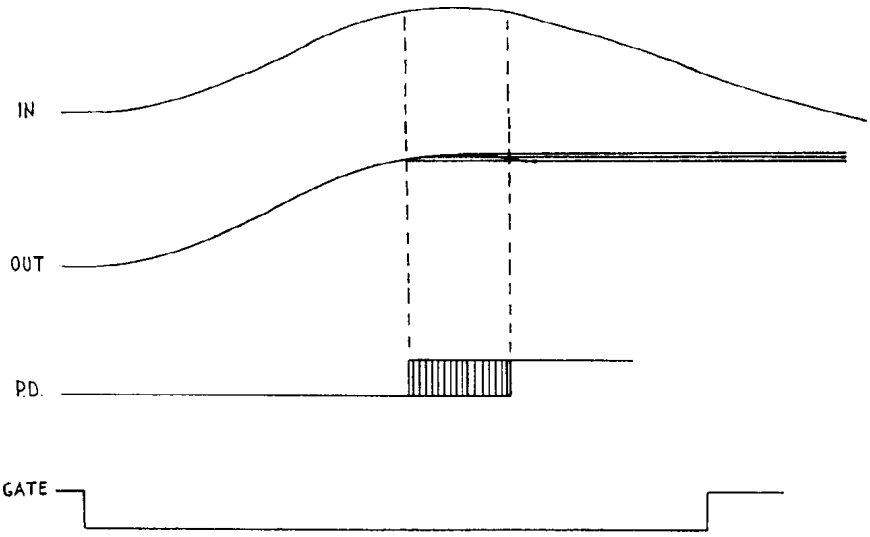


Figure 9

To prevent false peak detections from occurring even with not too long pulse shaping times it is advisable that the gate covers only the peak value.

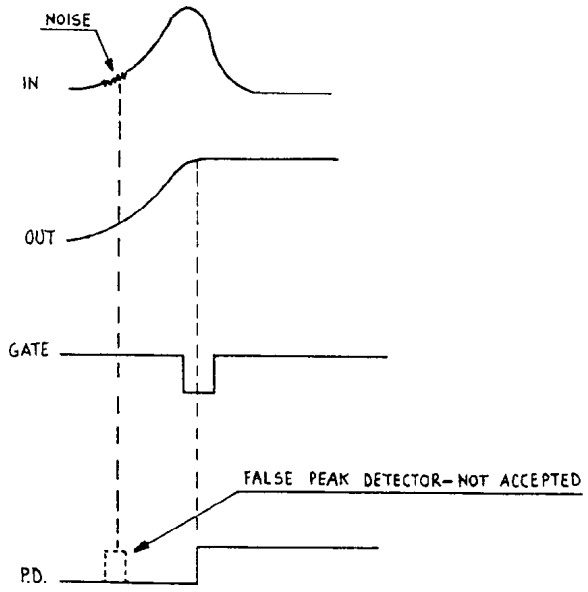


Figure 10

If rectangular-shaping pulses (flat top) are used, proceed as indicated below.

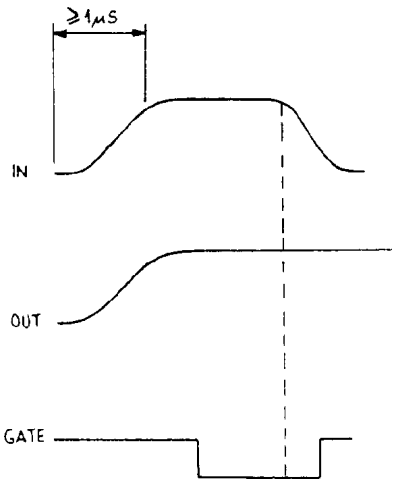


Figure 11

Analog Input Impedance

In the standard version, the input impedance of the measuring channels is 1 KΩ.

If long connecting cables and fast signals (i.e. 0.5 μsec semigaussian shaping time) are used, the cable must be terminated with the impedance of the cable itself; otherwise possible oscillations due to the non-terminated cable may result in remarkable differential non-linearities.

To locate the resistor that determines the input impedance, refer to the electrical diagram of the Input Module (Figure 12) and to the associated component layout (Figure 13).

Example of connection with closing impedance differing from the characteristic impedance of the cable used. The amplitude and frequency of the oscillations change or they disappear depending upon the signal width owing the non-terminated cable which is considered by the shaper-amplifier as a capacity.

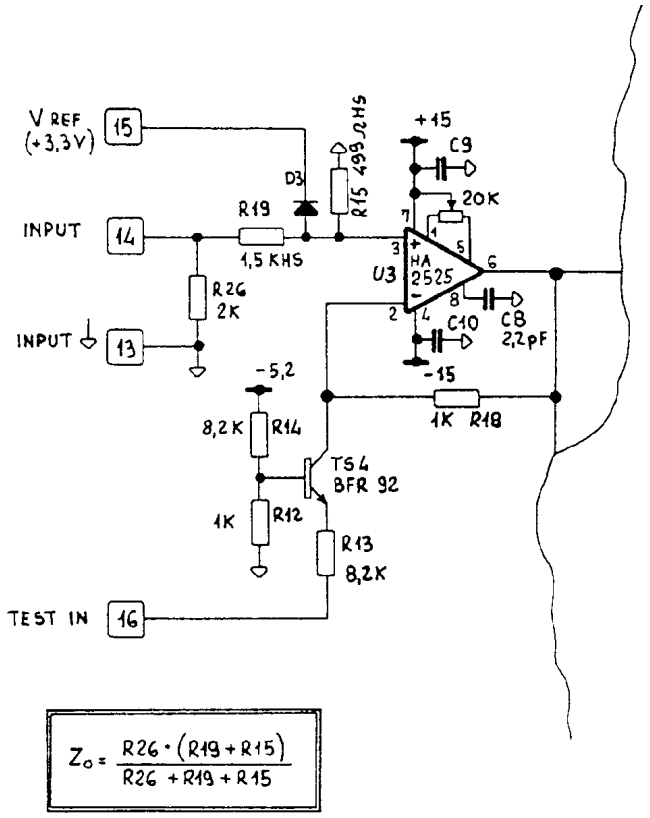


Figure 12: Analog Input Stage

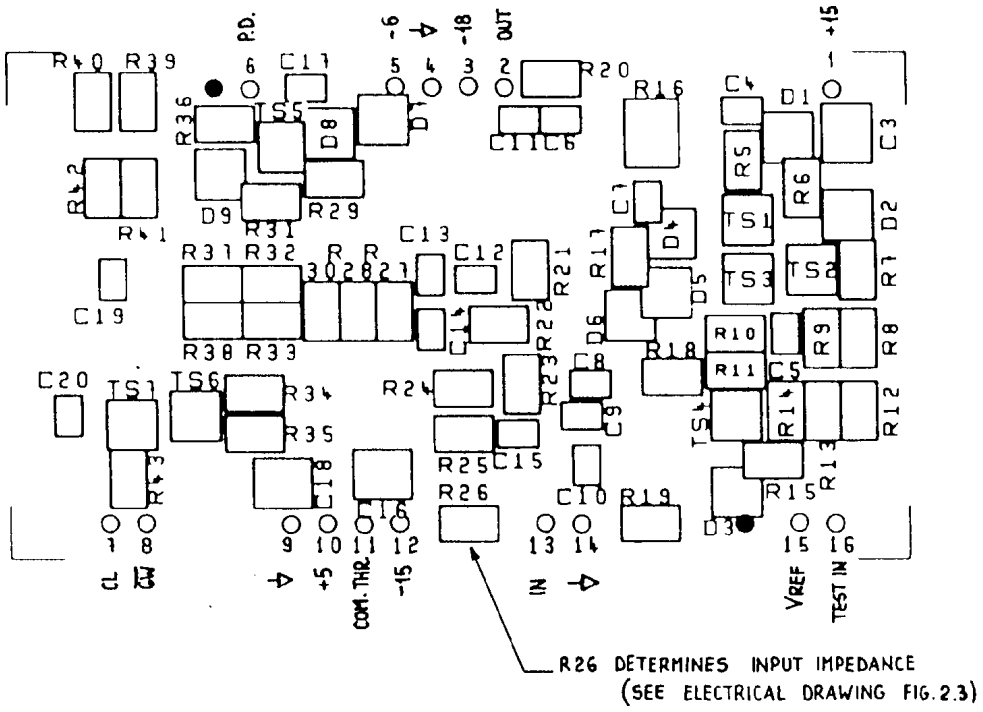


Figure 13: Input Module - Components Layout

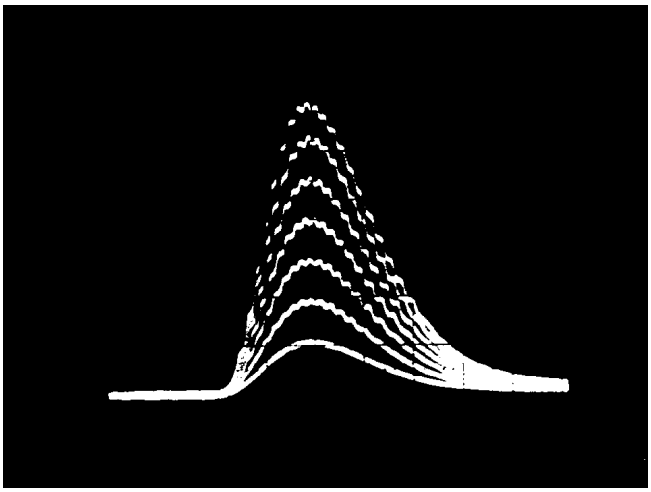


Figure 14: Input Signal

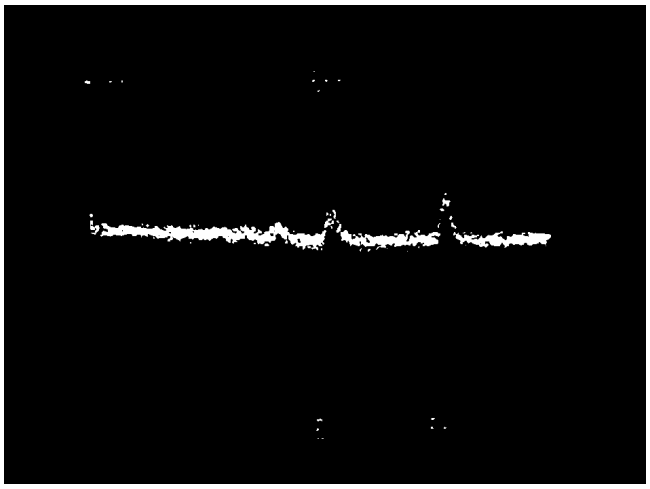


Figure 15: Spectrum with Sliding Pulse Generator