OPERATOR'S MANUAL

MODEL 3420

16-CHANNEL CONSTANT FRACTION DISCRIMINATOR

CE

Revised
September, 1997

(ECO 1003)

LeCroy

Innovators in Instrumentation

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

COOLING	The high power dissipation of the 3420 requires that it be well cooled. Be sure the fans move sufficient air to maintain the exhaust air temperature at less than 50° C.
6 V POWER REQUIREMENT	The 3420 uses significant power from the -6 V and +6 V CAMAC power bus. Be sure that your crate can supply enough current to this and other modules, especially if multiple 3420s are being used.
INSTALLATION	CAMAC crate power should be turned off during insertion or removal of modules to avoid possible damage due to momentary misalignment of contacts.
SPECIFICATIONS	The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

TECHNICAL DATA

LeCroy

3420 CONSTANT FRACTION DISCRIMINATOR

- **Works as a Constant Fraction or Zero Crossing Discriminator**
- **16 Inputs Per Module**
- **Low Time Walk: 200 psec (at 100:1 Dynamic Range)**
- **Individually Programmable Thresholds**
- **Programmable Dead Time and Output Widths**
- **ECLine Compatible**
- **CAMAC Packaging**
- **Built-in Time-to-Charge Converter**

GENERATION OF PRECISE LOGIC PULSES FOR CRITICAL TIMING APPLICATIONS

Discriminators generate precise logic pulses in response to input signals exceeding a given threshold. Constant Fraction Discriminators (CFDs) use a constant fraction of the amplitude of the input pulse as the threshold. This precisely determines the timing of the output pulse relative to the input signal. This technique is not subject to jitter ("time walk") caused by varying amplitudes or rise times of the inputs, as in leading edge discriminators. Output pulses are of standard amplitude and of preset duration. CFDs are the units of choice for use with critical subnanosecond timing or trigger systems.

The Model 3420* is part of the LeCroy family of ECLine programmable logic modules. It has two modes of operation. The first and foremost mode is as a Constant Fraction Discriminator, which results in best timing precision. The other mode is as a zero crossing discriminator. The unit offers many benefits including external control of the output pulse width, the 16 individual thresholds, as well as having built-in test features.

The module features a time-to-charge converter that allows the user to perform precise time measurements in conjunction with a charge sensitive ADC such as the LeCroy 4300B or similar ADC.

*Designed by Michigan State University.

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FUNCTIONAL DESCRIPTION

GENERAL

The LeCroy Model 3420, Constant Fraction Discriminator, is the next step in CAMAC-ECL discriminators. It offers excellent timing accuracy, adjustable analog delay, adjustable fraction, adjustable dead time, adjustable output pulse width, and a wide range of programmable thresholds *for each channel.* It was designed to be a versatile yet flexible module for applications where precise timing is critical.

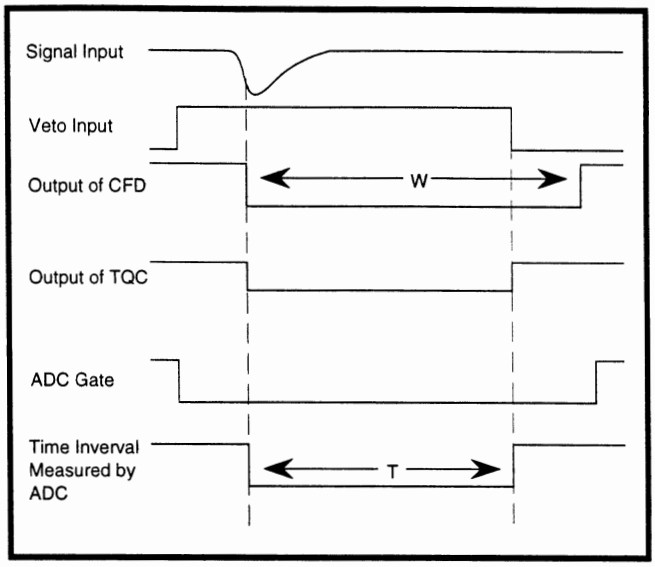
The 3420 offers 2 modes of operation, constant fraction discrimination and zero crossing. In addition, it offers simultaneous time-to-charge conversion.

THRESHOLD AND WIDTH

In the constant fraction mode, the 3420 offers a programmable threshold range from -20 mV to -1.33 V for each of its 16 inputs via CAMAC. All outputs have a width which is programmable from 25 nsec to 250 nsec in 16 nsec steps via CAMAC. Thresholds on each channel and the global dead time and output width values can be read back from CAMAC. Timing jitter on the output is less than 200 psec over a dynamic input signal range of 100:1. This unit has differential ECL logic outputs (which offer noise immunity) and is compatible with LeCroy's ECLine family of CAMAC modules.

DELAY AND FRACTION

The module uses plug-in headers to determine the fraction of the input pulse used for best timing. By changing the headers, the 3420 fraction can be altered

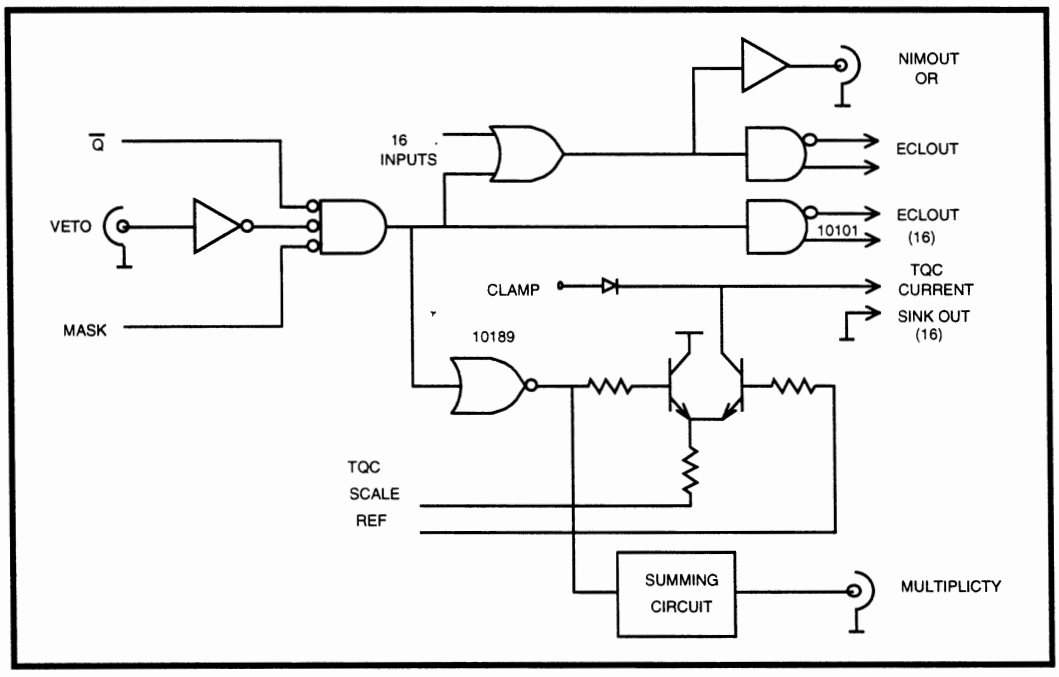


Model 3420 timing diagram when used as a time digitizer together with an ADC. The time digitized by the ADC is "T". For correct operation as a time digitizer, the output pulse width "W" must be set to exceed the duration of the Veto signal; also, the Veto signal must be applied prior to the arrival of the input signal.

or it can be converted into a leading edge or zero-crossing discriminator.

MASKING

For additional system flexibility, input masking is made possible by simultaneously inhibiting any combination of the 16 inputs via CAMAC command. This feature



Constant Fraction Output Section

allows the user to generate or simulate any desired trigger configuration. It also allows complete point-to-point checks of the system electronics without requiring removal of wires or disassembly of the data acquisition system.

TEST FEATURE

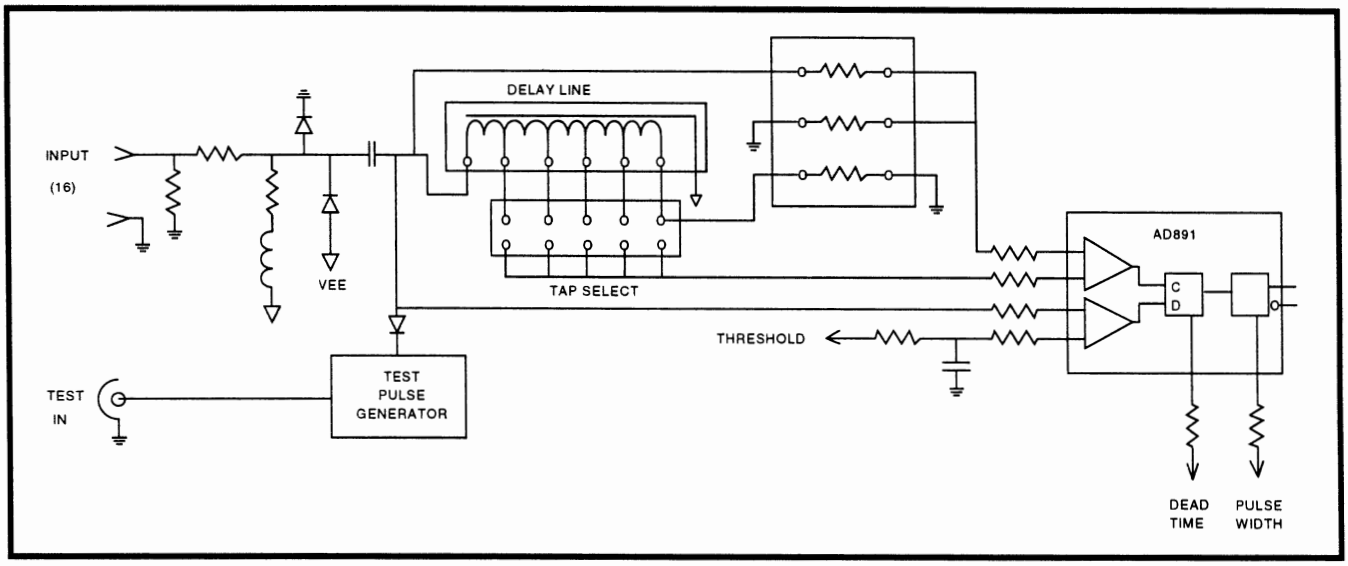
A built-in test feature simulates an input signal for each channel upon receipt of either an F(25) command or a NIM level signal applied to the test input connector. This permits rapid, simultaneous testing of all enabled discriminator channels.

CURRENT SUM

A current sum output is also provided which generates -1 mA per enabled input channel to a front-panel Lemo connector. This output can be used to conveniently monitor discriminator activity or to act as a source for prompt trigger information.

DIGITIZING TIME INTERVALS

The built-in time-to-charge converter (TQC) converts a time interval into a charge. This feature is used with integrating ADCs such as the LeCroy 4300B FERA ADC to provide time measurements with 25 psec resolution with a < 200 psec integral linearity. The time interval measured is the time from the leading edge of the signal input to either the leading edge of the 3420 VETO, acting as a Common Stop (as shown in the timing diagram) or the trailing edge of the 4300B GATE input. Thus, the combination of the TQC with an ADC acts like a Common Stop TDC. By incorporating the TQC into the discriminator module, the Model 3420 can replace both, a discriminator and a separate time-to-charge converter (such as the LeCroy 4303) in most applications, saving cost and CAMAC slots.



Constant Fraction Input Section, One Channel

SPECIFICATIONS

INPUT

Signal Inputs: Sixteen inputs via 2-pin front-panel connectors, 100 Ω, ±2%, 50 Ω optional. Protected to 1 A for 1 μsec; clamping at +1 V and -6 V. Reflections < 5% for input pulses of 5 nsec rise time; input offset voltage typically ±1 mV.
Test Input: One Lemo connector on front panel, 50 Ω; triggers all enabled channels. Requires NIM level signal (-600 mV minimum). Minimum width, 100 nsec. Maximum rate, 1 MHz.
Veto-Input: One Lemo front-panel connector, 50 Ω. Permits simultaneous fast inhibiting of all channels. Requires NIM level signals. Minimum duration, 20 nsec. This input is used to work the module in the time-to-charge mode only. Signal must overlap output pulse.

OUTPUT

Discriminator Outputs: 16 outputs, ECL level (-0.8 V to -1.7 V) into 100 Ω twisted-pair. Duration for all channels, approximately from 25 nsec to 250 nsec ±50% programmable in 16 steps via CAMAC; 0.2%/°C maximum.

Current Sum Output: One, front-panel Lemo connector; 1 mA per fired channel.
OR: One front-panel lemo for NIM level output and one ECL level output on front panel 2-pin header. The output is an OR of 16 input channels which exceed the set threshold.
Time-to-Charge: 16 outputs, 0 -10 μA programmable in 40 μA steps. Suitable for use with LeCroy Model 4300B FERA.

GENERAL

Output Width and Dead Time Adjustments: The unit has an internally generated programmable dead time followed by an output pulse width. Each one of these times must be set via CAMAC. The preset ranges are 20 nsec to 250 nsec. Different choices are possible by user modification (10 nsec to 100 nsec and 50 nsec to 500 nsec).
Operating Modes: Constant fraction discriminator or zero-crossing discriminator, both followed by built-in time-to-charge converter (TQC).
Maximum Rate: 50 MHz at lowest settings for dead time and output pulse width.
Double Pulse Resolution (DPR): 20 nsec, typical.
Input-Output Delay: 15 nsec + constant fraction delay. Delay matching better than 2 nsec.
Test-Output Delay: 30 nsec + constant fraction delay.
Multiple Pulsing: None; one and only one output pulse is produced for each input pulse regardless of input pulse amplitude or duration.

Threshold: -20 mV to -1.33 V ±5% through 8-bit DAC via CAMAC. Stability better than ±100 ppm/°C to 70°C operating temperature. Individually programmable per channel in 5.2 mV steps.
Cross Talk: < 5% with proper cabling & termination.
Walk: < ±200 psec from 100 mV to 5 V (with a pulse of 20 nsec width, rise and fall times of 5 nsec, constant fraction delay of 10 nsec and constant fraction set to 30%).
Built-in Time-to-Charge Converter (TQC): 0 to 10 mA output, programmable in 40 μA steps. Output is a current sink output. It will therefore, drive only properly terminated cable. The output is clamped at -1 V. It can be switched to provide fast NIM signals (-16 mA) by moving an internal jumper. Maximum timing resolution is 25 psec with an internal jitter of approximately 10 psec. When using this mode, the output pulse width must be set to a time greater than the width of the ADC gate pulse. To ensure accurate results a veto pulse should be used to inhibit inputs to the CFD when the ADC is not gated (armed).
TQC Linearity: < 200 psec deviation from a straight line fit.
Constant Fraction and Delay Alteration: Can be altered on a channel-to-channel basis by changing the internal plug-in header and by changing the delay via a 5 tap internal delay line. Factory set fraction = 0.3; delay = 10 nsec, five 2 nsec taps.
Packaging: RF-shielded, CAMAC #1 module.
Power Requirements: 1.00 A at +6 V; 1.75A at -6 V; 0.05 A at +24 V; 0.25 at -24 V.
Weight: 1.6 lbs (0.7 kg).

CAMAC COMMANDS

CAMAC COMMANDS

X:	An X response is generated when a valid N, A, F command is recognized.
Q:	A Q response is generated only if the requested function can be executed.
Z:	Clears mask register at S2 time.

CAMAC FUNCTION CODES

	Data	Description
F(0)•A(0-15):	8 bits	Read THRESHOLD; channel = 0 - 15.
F(1)•A(0):	16 bits	Read MASK Register on R1 - R16; 0 = Mask Off; 1 = Mask On.
F(1)•A(1):	8 bits	Read DEAD TIME (bits 0 - 3) & WIDTH (bits 4 - 7).
F(1)•A(2):	8 bits	Read TIME-TO-CHARGE-SCALE.
F(16)•A(0-15):	8 bits	Write THRESHOLD; channel 0 -15; 0 = 0 V, FF = -1.33 V.
F(17)•A(0):	16 bits	Write MASK Register on W1 - W16; 0 = Mask Off; 1 = Mask On.
F(17)•A(1):	8 bits	Write DEAD TIME (bits 0 - 3) & WIDTH (bits 4 - 7) 16 steps; (0000 = minimum; 1111 = maximum).
F(17)•A(2):	8 bits	Write TIME-TO-CHARGE-SCALE; (0 to - 10 mA).
F(25)•A(0):	n/a	Generate a TEST PULSE.

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model 3420 Fraction Discriminator. In addition, it describes the interface's theory of operation and presents information regarding its function and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier and filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only. In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, ~~(914)~~ 845 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide an extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for details.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department.

PRODUCT DESCRIPTION

OVERVIEW

The LeCroy Model 3420* is a 16-input Constant Fraction Discriminator in a single-width CAMAC module. Constant Fraction Discriminators (CFDs) use a constant fraction (or percentage) of the input pulse to precisely determine the timing of the output pulse leading edge relative to the input signal. This technique is not subject to jitter ("time walk") caused by varying amplitudes of the inputs, such as in leading edge discriminators. This method of discrimination is indispensable in critical sub-nanosecond timing or trigger systems.

This module is part of the LeCroy family of ECLine programmable logic modules. Each channel has its own programmable threshold. Common to all channels is a programmable output width and a dead time control. A programmable mask and test pulse allow computerized system testing and simulation.

The Model 3420 has the unique feature of also providing charge outputs along with the differential ECL logic outputs. The charge outputs become a flexible time-to-digital converter when used with a charge sensitive ADC such as the LeCroy Model 4300B.

SPECIFICATIONS

Input Characteristics

Signal Inputs: 16 inputs via a front-panel 34-pin connector, 100 Ω ±5% (50 Ω optional), AC-coupled (750 nsec time constant). Protected to 1 A for 1 μsec; clamping at +1 V and -6 V.

Threshold: Individually adjustable, -20 mV to -1.4 V set by an 8-bit DAC (5.5 mV steps) programmed via CAMAC. Stability better than ±100 ppm/°C to 70°C operating temperature.

Test Input: One front panel Lemo connector terminated in 50 Ω; drives all channels with a > 800 mV, 20 nsec with a minimum duration of 100 nsec. Requires NIM level signal (-600 mV minimum). Minimum width, 100 nsec. Maximum rate, 1 MHz.

Veto Input: One front panel Lemo connector terminated in 50 Ω. Common to all channels. Allows fast inhibiting of outputs (inhibits only the overlap of the veto and output). Used in the time-to-charge mode.

Output Characteristics

Discriminator Outputs: 16 outputs on one 34-pin, front panel connector; ECL differential level (-0.8, -1.6 V) into 100 Ω twisted pair. Duration: 25 nsec to 250 nsec programmable in 16 nsec steps via CAMAC, common to all channels.

Charge Outputs: 16 outputs on one 34-pin, front panel connector (ground, signal). Negative, current sink outputs suitable for use with charge sensitive ADCs. Duration same as discriminator outputs. Programmable from 1 - 10 mA.

Current Sum Output: One, front panel Lemo connector; 1 mA per triggered channel for duration of discriminator outputs.

**Designed by Michigan State University.*

OR Output: One front panel output provided both as a NIM signal via a Lemo connector and as an ECL differential level (-0.8, -1.6 V) via a 2-pin connector. Duration equal to discriminator output.

Timing Characteristics

Walk: < ±200 psec from 100 mV to 5 V (with a pulse of 20 nsec width, rise and fall times of 5 nsec, constant fraction delay of 10 nsec and constant fraction set to 30%).

GENERAL

Output Width and Dead Time Adjustments: Both the output width and dead time are programmable via CAMAC in the 3420. The preset ranges are 25 nsec to 250 nsec. The output width adjustment determines the width of both the discriminator output and the time-to-charge output. The output width has not been trimmed and can vary ±50%. It must be re-standardized with another logic module if it is to be used as a gate or for overlap coincidence. The dead time adjustment sets a time interval (starting at the same time as the discriminator output) which inhibits the discriminator from triggering again. The dead time MUST always be set as long or longer than the discriminator output. This protects against multiple pulsing.

Maximum Rate: 40 MHz at lowest settings for dead time and output pulse width.

Double Pulse Resolution (DPR): 25 nsec minimum. Depends on dead time setting.

Input to Output Delay: 15 nsec + constant fraction delay. Delay matched to better than 2 nsec.

Test to Output Delay: 30 nsec.

Multiple Pulsing: None; one and only one output pulse is produced regardless of input pulse amplitude so long as the dead time setting is greater than the programmed pulse width.

Cross Talk: <5% with proper cabling and termination.

Built-in Time-to-Charge Converter (TQC): A common 8-bit DAC sets the TQC outputs from 0 to 10 mA. An internal jumper allows switching to a NIM signal (-16 mA). The output is a current sink output, clamped at -1 V, that can only drive a properly terminated cable. It is meant to be used by charge integrating ADCs such as the LeCroy Model 4300B (FERA). Maximum timing resolution is 25 psec with an internal jitter of approximately 10 psec. When used in this mode, the ADC gate must encompass the leading edge of the TQC pulse and terminate before the trailing edge of the TQC pulse. If this is not convenient, the veto input can be used to terminate the TQC pulse before it terminates because of the width setting. The ADC gate can then be set arbitrarily wide to encompass the whole pulse.

TQC Linearity: < 200 psec deviation from a straight line fit.

Constant Fraction and Delay Alteration: Can be altered on a channel-to-channel basis by changing the resistors mounted on an internal DIP adapter and by changing the delay via a 5 tap internal delay line.

Factory set fraction = 30%; delay = 10 nsec max., five 2 nsec taps.

Packaging: RF-shielded, CAMAC #1 module.

Power Requirements: +6 V at 1.00 A; -6 V at 1.75 A; +24 V at .05 A and -24 V at .25 A.

Weight: 1.6 lbs (0.7 kg).

CAMAC COMMANDS

The commands for the 3420 conform to the CAMAC Standard-IEEE Std 583-1975. If the user is unfamiliar with the CAMAC standard, a good reference is *"CAMAC Instrumentation and Interface Standards"*, published by The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017.

Further information is available from LeCroy Research Systems in the form of Application Notes. In particular, AN-33, *"Introduction to CAMAC"*, is very useful.

F(0)•A(0-15):	Reads channel Threshold on CAMAC R1 - R8.
F(1)•A(0):	Reads Mask register on CAMAC R1 - R16.
F(1)•A(1):	Reads Dead Time register on CAMAC R1 - R4 and Width register on CAMAC R5 - R8.
F(1)•A(2):	Reads Time-to-Charge register on CAMAC R1 - R8.
F(16)•A(0-15):	Writes channel Threshold on CAMAC W1 - W8 (-20 mV to -1.4 V, 5.5 mV increments).
F(17)•A(0):	Writes to Mask register on CAMAC W1 - W16.
F(17)•A(1):	Writes to Dead Time register on CAMAC W1 - W4 and Width register on CAMAC W5 - W8 (25 - 250 nsec, 16 nsec increments; 0000=25 nsec, 1111=250 nsec). ~14ns per increment
F(17)•A(2):	Writes to Time-to-Charge register on CAMAC W1 - W8 (0 to 10 mA, 40 μA increments).
F(25)•A(0):	Triggers Test function.

CAMAC Responses

X:	An X response is generated for every valid F, N, A.
Q:	A Q response is generated for every valid F, N, A.
Z:	Clears mask register at S2 time.

INSTALLATION

The 3420 is a CAMAC module and as such must be installed in a CAMAC crate. Care must be taken to ensure the crate power is off before the module is installed. It can be installed in any slot except in the crate controller position (slots 24 and 25).

The 3420 does not draw an excessive amount of power. A 1000 Watt crate such as the LeCroy Model 8025, easily powers a full crate of 3420 modules. However, the user should always check the power capacity of his crate against the power required by the installed modules.

It is best, although not necessary, to adjust the Constant Fraction and Delay setting before installing the module. If the discriminator outputs are not used, jumper J2 must be moved toward the rear of the module to provide a load on the ECL outputs. Unloaded ECL outputs have a subtle effect on the TQC. The TQC output can be changed to a NIM signal by moving jumper J1 toward the top of the module. See Operating Instructions for more details.

The 3420 comes with 50 Ω input impedance and AC coupling. This can be modified to 100 Ω input impedance. See Additional Information for more details.

CAUTION: Once the unit is installed in the crate and powered up, it must be programed because the internal registers can power up loaded with random values. For test purposes, it is best to set all Thresholds to 40 mV, Mask to all zeros, Dead Time and Width to 250 nsec and TQC to 10 mA.

To complete the installation, cables need to be connected to the inputs and outputs. The discriminator outputs are ECL so that standard flat, twisted pair cable can be used. The inputs and TQC outputs are analog and consideration should be given to using miniature shielded cable rather than unshielded cable if maximum performance is desired.

OPERATING INSTRUCTIONS

GENERAL

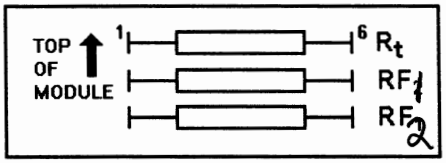
Setup of the Model 3420 can be split into three different categories. The first is to select the hardware configuration for the constant fraction and delay, and position the jumpers for the desired type of operation. This is done with the side cover off. The second is to load the internal registers with the necessary values to obtain the desired performance. The last is to setup up the TQC timing and use the test input.

Selecting the Fraction

The fraction (f) is selected by changing resistors in the Fraction DIP Adapter (see Figure 1). The value can be set from f=0 to f=1 and normally comes from the factory with f=0.3. The fraction selected depends on the application and typically f=0.3 for plastic scintillators and surface barrier silicon detectors while f=0.1 for slower inorganic scintillators such as Na(T).

Implementing the Fraction

Each channel has a 6-pin DIP adapter containing 2 resistors that determine the fraction and one resistor for the delay line termination. Please refer to the accompanying diagram. The relationship of the resistors is as follows:



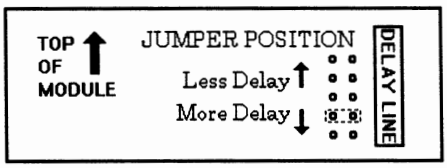
$Rf_1 + Rf_2 = 300\ \Omega$
$Rf_2 = (1 - f) \cdot 300\ \Omega$
$Rf_1 = f \cdot 300\ \Omega$
f = fraction = $Rf_1/(Rf_1 + Rf_2)$
Termination resistor Rt = 100 Ω

see pg 1 of the schematics

Figure 1: Fraction DIP adapter.

Selecting the Delay

A socket mounted tapped delay line is available on each discriminator channel for selecting the appropriate delay to determining the constant fraction. There are 5 equal taps on each delay line with a jumper for selecting the desired tap. The "n" in the model number "3420/n" gives the total delay of the factory supplied delay line. Figure 2 shows the arrangement of the taps on the circuit board along with the formula for selecting the correct delay.



Assuming the following:
t_{rise} = rise time of pulse
f = fraction
t_d = desired delay
Then: $t_d = (1 - f)\ t_{rise}$

Figure 2: Delay Line Tap Layout.

A complete description of how the constant fraction works is discussed in Theory of Operation.

Other Jumper Configurations

There are two other jumpers on the printed circuit board, J1 and J2. J1, located ≈ 2" back from the front panel in the center of the board, determines whether the TQC outputs will be a standard NIM output or an output whose current is controlled by the Time-to-Charge register. Positioning J1 toward the top of the module makes the TQC outputs NIM. J2, located between the two top front panel connectors, creates a load for the discriminator outputs if they are NOT being used. This is necessary for proper operation of the TQC outputs. Position J2 toward the rear

of the module when the discriminator outputs are NOT connected to another module.

Threshold

The internal threshold registers of the 3420 MUST be programmed upon powering up the module. This is accomplished with a CAMAC F(16)•A(i) where i = channel number. The thresholds are programmable from 0 V to -1.4 V in 5.5 mV increments. If the thresholds are set too sensitive, the outputs will oscillate and cause problems. Under ideal conditions, the thresholds can be set to -22 mV and operate satisfactorily. However, input noise, shielding and signal rise time will effect this, so great care should be taken to minimize these effects for best results. The user is encouraged to read the Theory of Operation section of this manual, so that he can fully appreciate the way the threshold works.

Dead Time and Width

The Dead Time & Width register MUST be programmed upon power up. A CAMAC F(17)•A(1) will accomplish this with the bottom 4 bits setting the Dead Time and the upper 4 bits setting the width. All bits = off gives a 25 nsec setting and all bits = on gives a 250 nsec setting with incremental settings of 16 nsec. Satisfactory operation will not occur unless the Dead Time is made ≥ the Width. The Width setting is determined either by the width required by the down stream modules using the discriminator outputs or by the TQC (see following description of Charge Outputs). It is best to re-standardize any outputs (with another logic module) that will be used as a gate or in overlap coincidence because they are not meant for that purpose.

TQC Setup

The TQC (Charge-to-Time Converter) uses the Charge outputs, digitized by a charge ADC such as a FERA, to generate a digital number proportional to the time between when the constant fraction crossing occurred and a reference signal that occurs AFTER the crossing. This reference signal can either be the leading edge of the veto input to the 3420 or the trailing edge of the gate to the charge ADC. The leading edge of the ADC gate MUST encompass the constant fraction crossing under all conditions. It is important that the Width be LARGER than the maximum time that can occur between the constant fraction crossing and the reference signal and if the veto is used, the veto be wide enough to exclude any portion of the Charge output that might be included in the ADC gate, or this approach will not work. Refer to the following timing diagram for more detail:

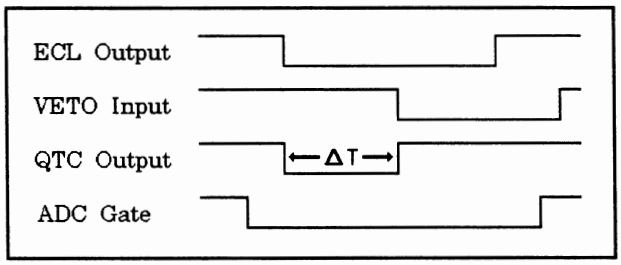


Figure 3: Charge-to-Time Converter Timing Diagram.

Once the correct timing relationships have been established, the current available on the Charge outputs can be adjusted with a CAMAC F(16)•A(2). The output range is 0 to 10 mA in 40 μA increments (8 bit). This allows the user to finely adjust the charge to the ADC as can be seen in the following relationship.

Given: Δt from Figure 3.
I_{TQC} = current at charge outputs
Q_{out} = charge converted by ADC

Then: $Q_{out} = I_{TQC} \cdot \Delta t$

Note: By adding an appropriate amount of delay (20 nsec or more depending on the ADC used) to the QTC output, the OR output and/or the Multiplicity output can be used to gate the ADC.

Test Input

A NIM pulse directed to the Test Input will generate an internal input pulse of > 800 mV amplitude and ≈ 125 nsec duration (equal to the test input width when >125 nsec wide). A CAMAC F(25)•A(0) will also generate the same internal test pulse. This allows the user to test all the channels and by setting the Mask (see following description), send test patterns to down stream modules such as the ECLine family produced by LeCroy.

Mask

The Mask register will be loaded with an arbitrary value on powering up the 3420. This is corrected with a CAMAC F(17)•A(0) which writes a 16 bit word, one bit for each channel (LSB = channel 0), with a "1" masking the channel and a "0" unmasking it. The Mask is retained until changed by user.

Figure 4 shows a simplified block diagram illustrating the input section of one 3420 channel. The incoming signal is split three ways after passing through a limiting circuit and an AC-coupling capacitor. (The test input is ORed into the circuit at this point.) One path is to a comparator that drives the D input of the flip-flop in the AD891 that provides the output of the channel. The other side of this comparator is the Threshold DAC. The other two paths consist of the fraction input which is attenuated by the combination of R1 and R2 and the delayed input that is selected from a tap on the delay line. Both these inputs to the clocking comparator are quiescently at 0 V. The attenuated input goes negative first followed by the delayed input. At their crossing, which comprises the Constant Fraction, the D input (threshold comparison) must be true for an output to occur. It is important that the delay and fraction be matched for proper operation of the circuit, for example:

$$t_{delay} = (1 - \text{fraction}) \bullet t_{rise}$$

Too short a delay will require an excessively high threshold.

Figure 5 illustrates the waveforms presented to and generated by the AD891.

Note that the internally generated Dead Time signal (set by the Dead Time DAC) disables the operation of the flip-flops, thus preventing more than one output occurring during its duration. This is a desirable feature

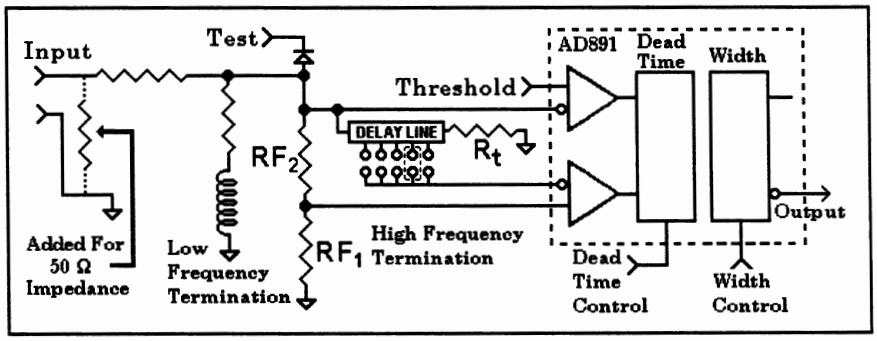


Figure 4: Constant Fraction Input Section, One Channel

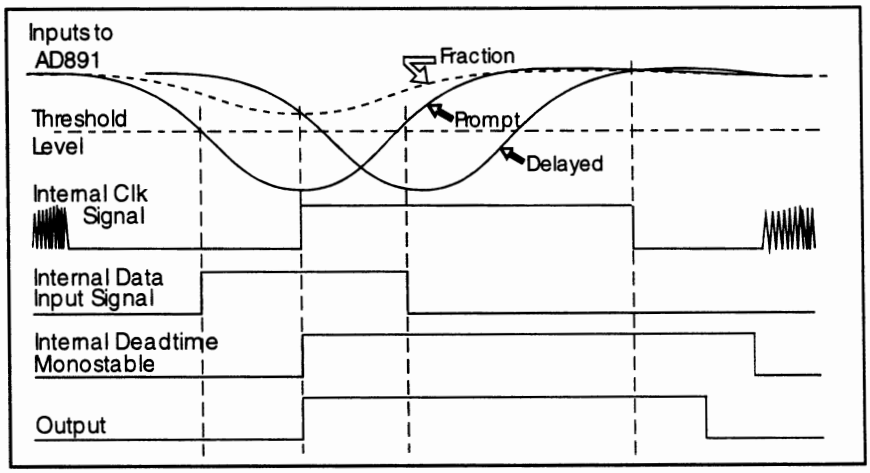


Figure 5: AD 891 Waveforms

when dealing with slow, noisy signals such as encountered from NaI(Tl) scintillators. This also means that the Dead Time MUST be set ≥ the Output Width (set by the Width DAC) or unpredictable outputs can occur.

AD891 Waveforms

Figure 6 shows a simplified block diagram of the output section of one 3420 channel. The output of the AD891, which now determines the width of the output pulse, goes through a three input NAND gate. The other two inputs to this gate, Veto and Mask, are used to control the channel output. The output of the NAND gate drives the module output OR circuit, the ECL output drivers and the TQC circuit. The NOR gate driving the TQC circuit also provides a drive to the summing circuit which generates 1 mA per channel at the Multiplicity summation output. The waveforms in Figure 7 illustrate the operation of this output.

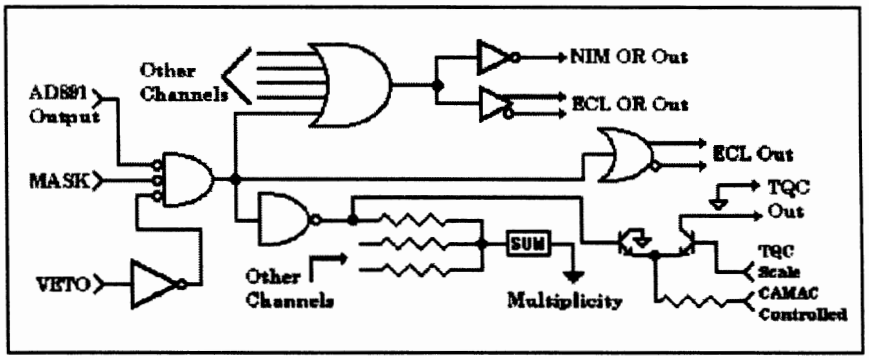


Figure 6: Constant Fraction Output Section One Channel

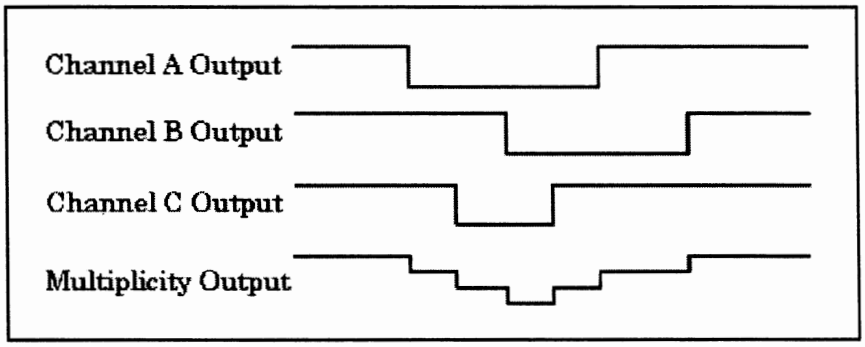


Figure 7: Multiplicity Waveforms

ADDITIONAL INFORMATION

USER MODIFICATIONS

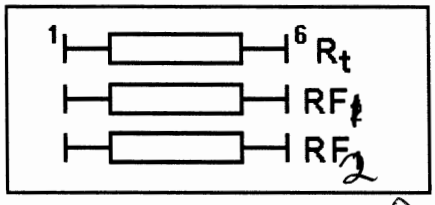
Depending on the application, the user may find it necessary to modify the Model 3420. There are four simple modifications available; changing the input impedance to 100 Ω, replacing the fraction DIP adapters, replacing the delay elements and providing NIM outputs.

INPUT IMPEDANCE

The 3420 comes from the factory with 50 Ω input impedance for the greatest noise immunity. However, the user may elect to use twisted-pair cable which has 100 Ω impedance, is low cost and easily assembled. The user must then remove two 10 pin, SIP, 100 Ω bussed resistor networks at R13 and R21 to change the input impedance to 100 Ω thereby matching the cable. The SIPS are in sockets located in the upper right hand corner of the circuit board when viewed from the component side with the front panel toward the right.

FRACTION

Each channel has its own 6 pin socketed DIP adapter which carries the terminating resistor for the delay element and the two resistors that determine the fraction. Figure 8 shows the relationship of these resistors and a diagram of the adapter.



$Rf_1 + Rf_2 = 300\ \Omega$
$Rf_2 = (1 - f) \cdot 300\ \Omega$
$Rf_1 = f \cdot 300\ \Omega$
f = fraction
Termination resistor Rt = 100 Ω

see pg 1 of the schematics

Figure 8: Resistor Adapter

These adapters are easily located on the PC board because their part identification printed on the board begins with P. When viewed from the component side with the front panel to the right, the resistor arrangement on the adapter corresponds to the diagram above. The standard configuration shipped from the factory is $Rf_2 = 200\ \Omega$, $Rf_1 = 100\ \Omega$ and $Rt = 100\ \Omega$ which makes f = 1/3.

DELAY ELEMENT

The delay element is a socket mounted 7 pin SIP with 5 equally spaced delay taps which is available with a total delay of 5, 10, 20, 30, 40, 50, 60, 75 or 100 nsec. It is available from LeCroy Research Systems or Data Delay Devices, Inc., 3 Mt. Prospect Ave., Clifton, NJ 07013, (201) 773-2299, Fax (201) 773-9672. When ordering from Data Delay Devices, specify their part number 1505-xB where x equals the total delay in nsec as stated previously. The necessary delay is easily calculated by using the following relationship:

$t_{delay} = (1 - \text{fraction}) \cdot t_{rise}$

NIM OUTPUTS

The TQC outputs can be easily configured to provide standard NIM outputs. Jumper J1, which is located ≈ 2" back from the front panel in the center of the board, provides this function. When position toward the top of the module, the outputs are NIM. When positioned toward the bottom of the module, the outputs are TQC. Note: if the ECL outputs are not used, J2, which is located between the two top front panel connectors, must be positioned toward the rear of the module creating a load for the ECL outputs. If the ECL outputs are to connect to another module, then J2 must be positioned toward the front of the module. Unloaded ECL outputs have a subtle effect on the TQC outputs.

INDEX

TECHNICAL INFORMATION

(PARTS LIST, SCHEMATICS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
106433101	CAP CERA MONO 100PF	17
106435102	CAP CERA MONO .001UF	19
106435103	CAP CERA MONO .01UF	24
106438104	CAP CERA MONO .1UF	36
140253106	CAP TANT MOLDED 10UF	1
140413226	CAP TANT MOLDED 22 UF	2
140453105	CAP TANT MOLDED 1 UF	2
140513106	CAP TANT MOLDED 10 UF	3
161225101	RES CARBON FILM 100 OHMS	51
161225102	RES CARBON FILM 1 K	1
161225103	RES CARBON FILM 10 K	2
161225104	RES CARBON FILM 100 K	1
161225122	RES CARBON FILM 1.2 K	2
161225151	RES CARBON FILM 150 OHMS	2
161225153	RES CARBON FILM 15 K	32
161225181	RES CARBON FILM 180 OHMS	1
161225201	RES CARBON FILM 200 OHMS	16
161225221	RES CARBON FILM 220 OHMS	1
161225223	RES CARBON FILM 22 K	2
161225240	RES CARBON FILM 24 OHMS	16
161225330	RES CARBON FILM 33 OHMS	1
161225361	RES CARBON FILM 360 OHMS	1
161225391	RES CARBON FILM 390 OHMS	3
161225392	RES CARBON FILM 3.9 K	1
161225470	RES CARBON FILM 47 OHMS	66
161225510	RES CARBON FILM 51 OHMS	2
161225561	RES CARBON FILM 560 OHMS	2
161225562	RES CARBON FILM 5.6 K	1
161225622	RES CARBON FILM 6.2 K	1
161225681	RES CARBON FILM 680 OHMS	2
161225750	RES CARBON FILM 75 OHMS	16
161225820	RES CARBON FILM 82 OHMS	2
161335121	RES CARBON FILM 120 OHMS	1
161335272	RES CARBON FILM 2.7 K	2
161335680	RES CARBON FILM 68 OHMS	1
161335750	RES CARBON FILM 75 OHMS	1
168531159	RES PREC RN55D 4.01K	1
168531460	RES PREC RN55D 4.99 K	1
168531489	RES PREC RN55D 10.0 K	1
168531499	RES PREC RN55D 12.7K	1
168531510	RES PREC RN55D 16.5 K	2
168531518	RES PREC RN55D 20.0 K	1
168531539	RES PREC RN55D 33.2 K	1
168531577	RES PREC RN55D 82.5 K	1
190042101	RESISTOR NETWORK 100 OHMS	4
190042104	RESISTOR NETWORK 100 K	1
190042151	RESISTOR NETWORK 150 OHMS	4
190042152	RESISTOR NETWORK 1.5 K	2
190042272	RESISTOR NETWORK 2.7 K	2
190042472	RESISTOR NETWORK 4.7 K	2
190042681	RESISTOR NETWORK 680 OHMS	6
190042821	RESISTOR NETWORK 820 OHMS	2

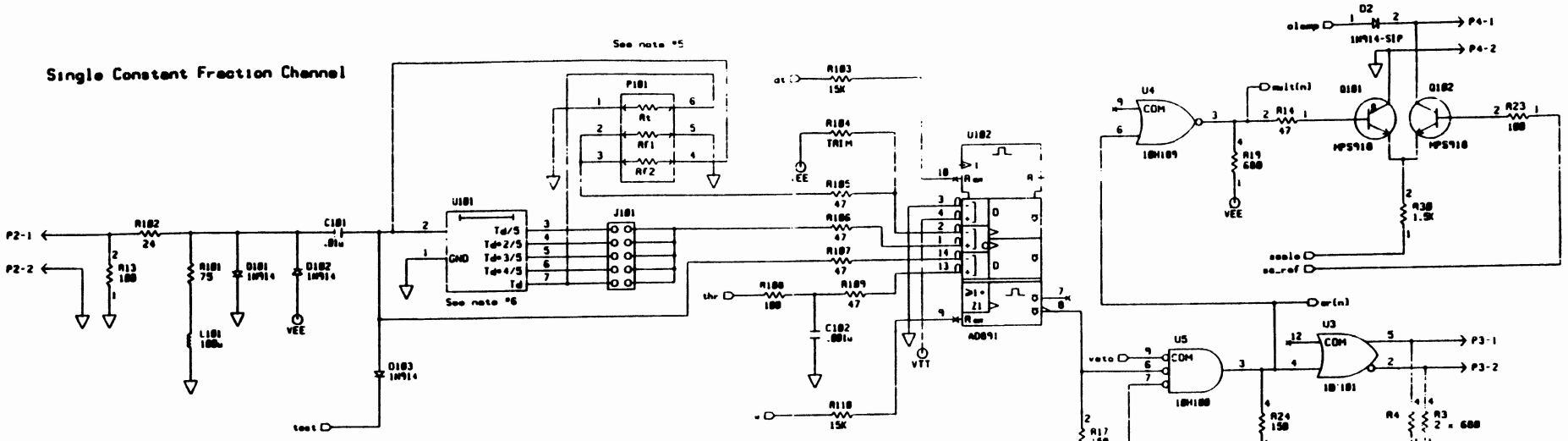
PART NUMBER	DESCRIPTION REMARK	QTY PER
190642102	RESISTOR NETWORK 1 K	1
190662122	RESISTOR NETWORK 1.2 K	2
190662472	RESISTOR NETWORK 4.7 K	2
190832332	RESISTOR NETWORK 3.3K	4
190832470	RES NETWORK 47 OHM	4
200031033	IC 2-INPUT NAND SN7403N	1
200071540	IC OCT INV BUFFER 74HCT540	2
200071642	IC BUS TRANSCVR SN74LS642	2
200167100	IC QUAD 2-IN NOR GATE 10H100	4
200341109	IC 4-5 IN OR/NOR MC10H109	2
200341189	IC HEX INV W/ENABLE 10H189	3
204042016	IC 2-INPUT OR/NOR F10101P	4
205650794	IC 8-BIT REGISTER 74F794PC	3
205751153	IC PROGRAM LOGIC ARRAY 153N DO NOT INCLUDE ON KIT, SEND TO THE PROGRAMMING CENTER FOR PROGRAMMING.	3
207257628	IC QUAD 8-BIT DAC 7628J	4
207271012	IC 12-BIT DAC 8012HP	1
207344316	IC QUAD ANALOG SWITCH HC4316	2
208122337	IC ADJ -VOLT REG LM337T	1
208130400	IC QUAD MONO OP AMP OP-400	5
208130606	IC DEMOS FET ARRAY TP0606N6	2
208213002	IC VOLT REF +5V REF-02	1
208570812	IC VOLT REG +12V LM7812CT	1
208631891	IC BINNED FOR WIDTH AD891	16
208810094	IC PROG POWER SWITCH AMP CA3094E	1
230110005	DIODE SWITCHING 1N4448	59
230111509	DIODE ARRAY 1N914	2
235050001	DIODE RECTIFIER 1N4139	2
270110001	TRANSISTOR NPN PN2369A	3
270110003	TRANSISTOR NPN PN2222A	1
270170103	TRANSISTOR NPN MPS918	33
270170904	TRANSISTOR NPN 2N3904	2
275134918	TRANSISTOR PNP 2N4918	1
275170002	TRANSISTOR PNP 2N5771	1
275170906	TRANSISTOR PNP 2N3906	3
290007010	DELAY LINE 10NS 5 TAP SIP-7	16
300050001	CHOKE FERRITE SINGLE LEAD	4
300500003	CHOKE EPOXY COATED 100 UH	16
400321014	SOCKET IC SOLD TAIL DIP-14	16
400331020	SOCKET IC SOLD TAIL DIP-20	4
400360028	SOCKET IC SOLD TAIL DIP-28	4
400990006	ADAPTER PLUG DIP 6	16
402112001	CONN PC MTG NICKEL LEMO	4
403119234	HDR DBL ROW RT ANGL 34	3
405765003	SOCKET SINGLE WIRE 3	32
405765007	SOCKET SINGLE WIRE 7	16
433220002	FUSE PICO II 125V 3 AMP	2
433221004	FUSE PICO II 125V 1 AMP	2
454310003	HDR SOLD TAIL/MALE 3	2

PART NUMBER	DESCRIPTION REMARK	QTY PER
454318072	HDR SOLD TAIL/MALE 72	3
454321020	HDR SOLD TAIL/FEM 20	1
454370002	SHUNT 2 POS	18
454713004	HDR SOLD TAIL/MALE 4	1
454901205	SHUNT BAR FOR PC FINGERS	1
500860302	INSULATOR FOR TO-220	2
519230001	SNAP RIVET NYLON	3
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209101	REAR PANEL CAMAC SIZE 1	1
555430003	CAPTIVE SCREW ASSEMBLY	2
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
560440004	SCREW PHILIPS 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
593910001	CABLE CO-AXIAL RG178B/U	1
714420001	PC BD PREASS'Y 3420	1
723420001	FRONT PANEL 3420	1
730000002	SIDE COVER RSD GENERIC SHORT	1
MLD92701	IC SINGLE ECL DIFF LINE DRIVER	1

End of report. 127 Details encountered.

NO	REVISION	DATE	BY
A	Chg scale res. & note refs. add char	10/31/91	MCR

Single Constant Fraction Channel



Ch* Reference designators and pin numbers for multi-peak parts for all 16 channels.

1	R13- 2	R1- 2	R2- 3	R5- 1,2	R17- 2	R24- 4	R3- 4	R4- 4	R19- 4	R14- 2,1	R38- 2	R23- 2	D2- 2	U5- 6,7,3	U3- 4,5,2	U4- 6,3
2	R13- 3	R1- 3	R2- 4	R5- 1,2	R22- 9	R24- 7	R3- 5	R4- 5	R19- 3	R16- 1,2	R38- 3	R23- 3	D2- 3	U2- 10,11,14	U3- 7,6,3	U4- 11,14
3	R13- 4	R1- 4	R2- 5	R5- 3,4	R17- 8	R24- 9	R3- 6	R4- 6	R19- 6	R14- 3,4	R38- 4	R23- 4	D2- 4	U11- 10,11,14	U3- 10,11,14	U1- 7,4
4	R13- 5	R1- 5	R2- 6	R5- 3,4	R22- 10	R24- 5	R3- 7	R4- 7	R19- 5	R16- 3,4	R38- 5	R23- 5	D2- 5	U2- 13,12,15	U3- 13,9,15	U4- 7,4
5	R13- 6	R1- 6	R2- 7	R5- 5,6	R17- 6	R24- 3	R3- 8	R4- 8	R19- 8	R14- 6,5	R38- 6	R23- 6	D2- 6	U5- 11,10,14	U6- 4,5,2	U1- 10,13
6	R13- 7	R1- 7	R2- 8	R5- 5,6	R22- 8	R24- 8	R3- 9	R4- 9	R19- 7	R16- 5,6	R38- 7	R23- 7	D2- 7	U2- 7,6,3	U6- 7,6,3	U9- 6,3
7	R13- 8	R1- 8	R2- 9	R5- 7,8	R17- 7	R24- 2	R3- 10	R4- 10	R19- 10	R14- 8,7	R38- 8	R23- 8	D2- 8	U11- 6,7,3	U6- 13,9,15	U1- 6,3
8	R13- 9	R1- 9	R2- 10	R5- 7,8	R22- 7	R24- 6	R8- 2	R7- 2	R19- 9	R16- 7,8	R38- 9	R23- 9	D2- 9	U2- 4,5,2	U6- 10,11,14	U9- 7,4
9	R21- 2	R15- 2	R7- 2	R20- 1,2	R17- 5	R42- 4	R8- 3	R7- 3	R49- 2	R48- 1,2	R45- 2	R44- 2	D1- 2	U11- 12,13,15	U8- 4,5,2	U1- 12,15
10	R21- 3	R15- 3	R7- 4	R18- 1,2	R22- 6	R42- 8	R8- 4	R7- 4	R49- 3	R46- 1,2	R45- 3	R44- 3	D1- 3	U7- 6,7,3	U8- 7,6,3	U4- 10,13
11	R21- 4	R15- 4	R7- 5	R20- 3,4	R17- 4	R42- 9	R8- 5	R7- 5	R49- 4	R48- 3,4	R45- 4	R44- 4	D1- 4	U5- 13,12,15	U8- 10,11,14	U1- 11,14
12	R21- 5	R15- 5	R7- 6	R18- 3,4	R22- 5	R42- 5	R8- 6	R7- 6	R49- 5	R46- 3,4	R45- 5	R44- 5	D1- 5	U7- 10,11,14	U8- 13,9,15	U4- 12,15
13	R21- 6	R15- 6	R7- 7	R20- 5,6	R22- 3	R42- 3	R8- 7	R7- 7	R49- 8	R48- 5,6	R45- 6	R44- 6	D1- 6	U7- 12,13,15	U12- 4,5,2	U9- 5,2
14	R21- 7	R15- 7	R7- 8	R18- 5,6	R22- 2	R42- 7	R8- 8	R7- 8	R49- 7	R46- 5,6	R45- 7	R44- 7	D1- 7	U7- 4,5,2	U12- 7,6,3	U9- 10,13
15	R21- 8	R15- 8	R7- 9	R20- 7,8	R17- 3	R42- 6	R8- 9	R7- 9	R49- 8	R48- 7,8	R45- 8	R44- 8	D1- 8	U11- 4,5,2	U12- 10,11,14	U1- 9,2
16	R21- 9	R15- 9	R7- 10	R18- 7,8	R17- 9	R42- 2	R8- 10	R7- 10	R49- 9	R46- 7,8	R45- 9	R44- 9	D1- 9	U5- 4,5,2	U12- 13,9,15	U4- 9,2

APPROVED

JUL 31 1992

FOR FABRICATION

NOTES:

1. All resistors are 1/8W 5% CC unless specified otherwise.
2. All capacitors are ceramic multilayer unless specified otherwise.
3. Part nos. for channels 2-9 start with 200-900.
   Part nos. for channels 10-16 start with 400-600.
   Except as in chart above.
4. Pin numbers for P2, P3 and P4 can be derived by the formulae 2n-1 for the signal/positive pin and 2n for the ground/negative pin, where 'n' is the channel number.
5. Rt terminates delay line (U101) and should match its characteristic impedance. Rf1 and Rf2 form the fraction and should satisfy the equations:

$$Rf1 = \frac{75 * Rt * fraction}{Rt - 75} \quad \text{(default: 100 Ohms)}$$

$$Rf2 = \frac{75 * Rt * (1 - fraction)}{Rt - 75} \quad \text{(default: 200 Ohms)}$$

6. As a rule of thumb, the selected delay time should be:

Delay = Rise * [illegible]

ITEM	PART NO	MFR	DESCRIPTION	REF DES	QTY

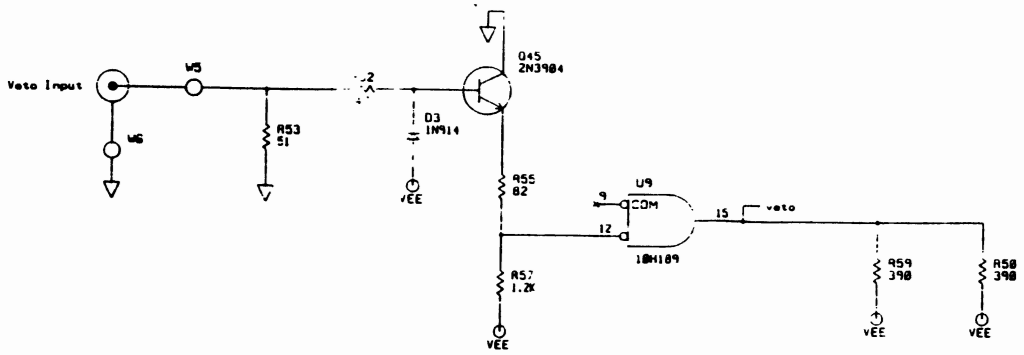
PARTS LIST

NATIONAL SUPERCONDUCTING CYCLOTRON LABORATORY
MICHIGAN STATE UNIVERSITY · EAST LANSING, MICHIGAN

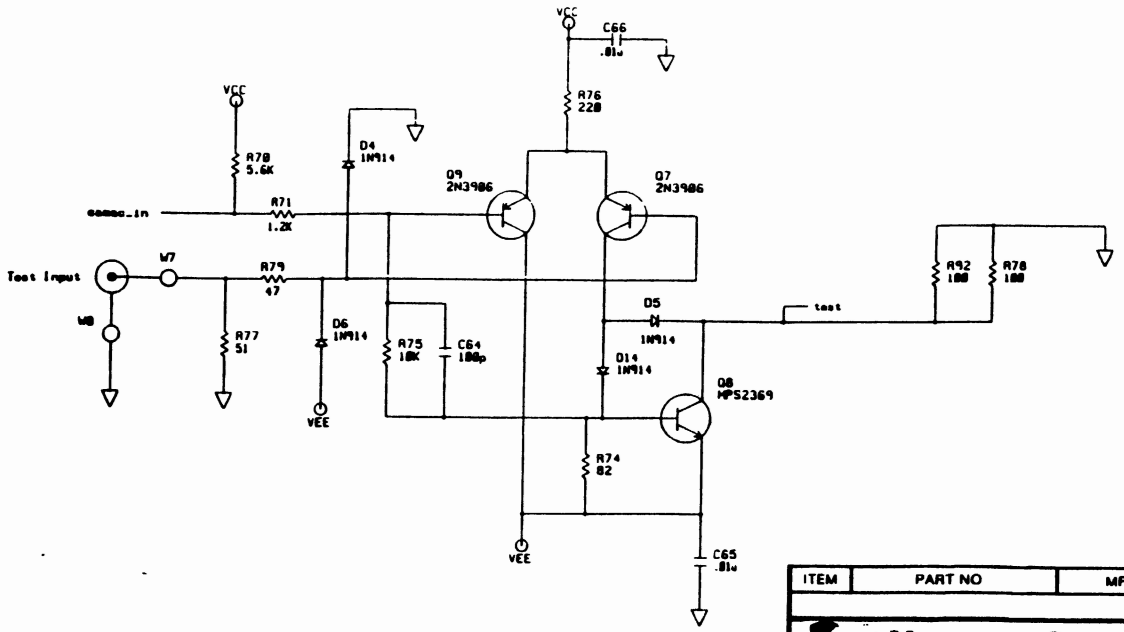
UNLESS OTHERWISE SPECIFIED	DRAWING TYPE Schematic ECO: 1008 01-Jan-95	DATE 6/27/91	DRAWN BY Eric H. Maier
DIMENSIONS ARE IN INCHES			
TOLERANCES	PROJECT TITLE Constant Fraction Discriminator 3420		
MATERIAL	DRAWING NUMBER 01-SCH-IA-21-B	SHEET 1 OF 3	SCALE

PCX FEB 04 1994

NO	REVISION	DATE	BY



Test and Veto Inputs



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JUL 21 1992

FOR FABRICATION

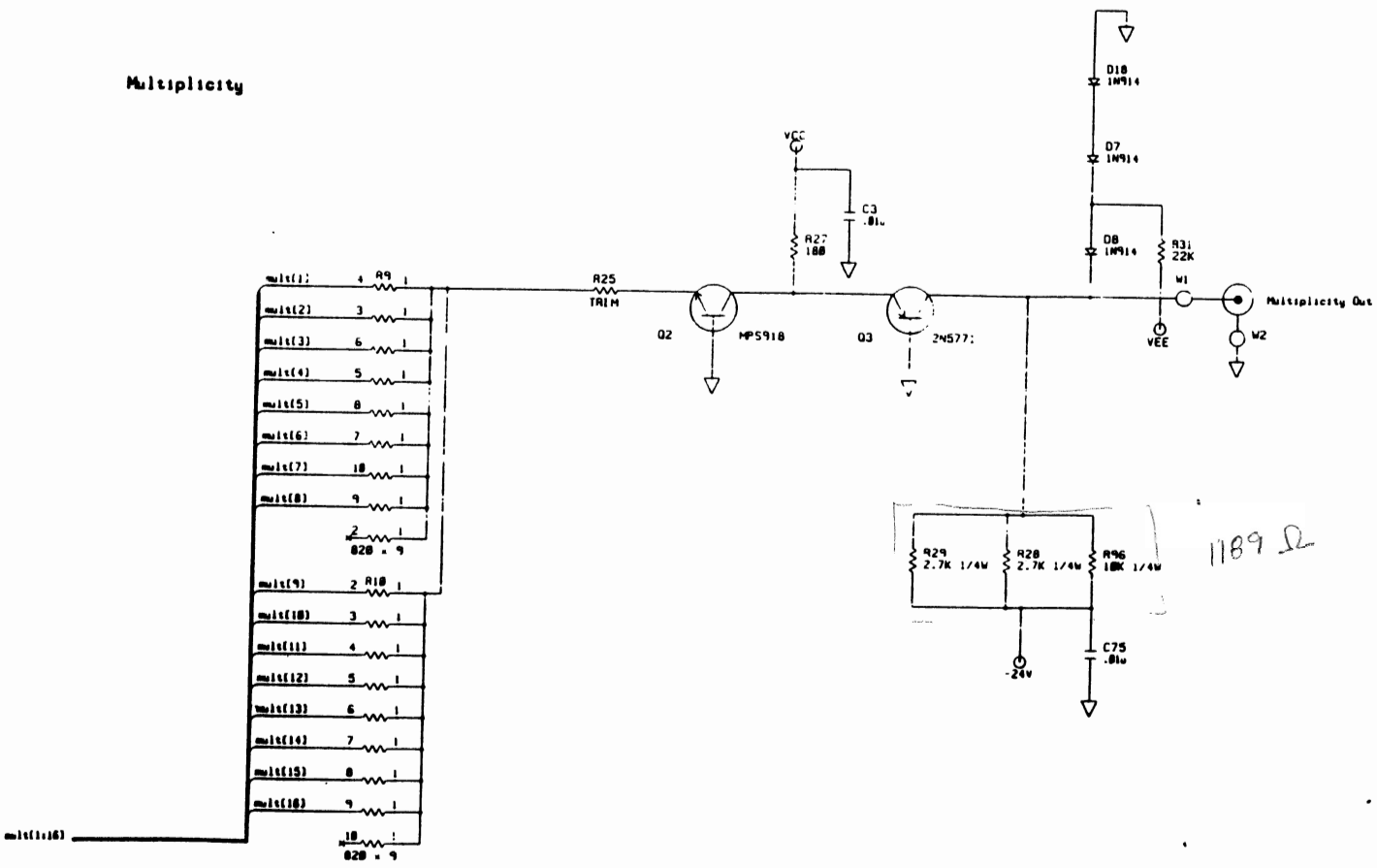
ITEM	PART NO	MFR	DESCRIPTION	REF DES	QTY
PARTS LIST					

NATIONAL SUPERCONDUCTING CYCLOTRON LABORATORY
MICHIGAN STATE UNIVERSITY · EAST LANSING, MICHIGAN

UNLES OTHERWISE SPECIFIED	DRAWING TYPE Schematic ECO: 1003	DATE 6/27/91	DRAWN BY MCH
DIMENSIONS ARE IN INCHES			ENG M. Hellep
TOLERANCES	PROJECT TITLE Constant Fraction Discriminator 3420		
MATERIAL	DRAWING NUMBER 07-EDN-1A-01-B	2 SHEET 13	SCALE / REV

NO	REVISION	DATE	BY

Multiplicity



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NATIONAL SUPERCONDUCTING CYCLOTRON LABORATORY
MICHIGAN STATE UNIVERSITY · EAST LANSING, MICHIGAN

UNLES OTHERWISE SPECIFIED	DRAWING TYPE Schematic ECO: 1005 91-JUN-95	DATE 6/27/91	DRAWN BY HCR
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TOLERANCES	PROJECT TITLE Constant Fraction Discriminator 3420		
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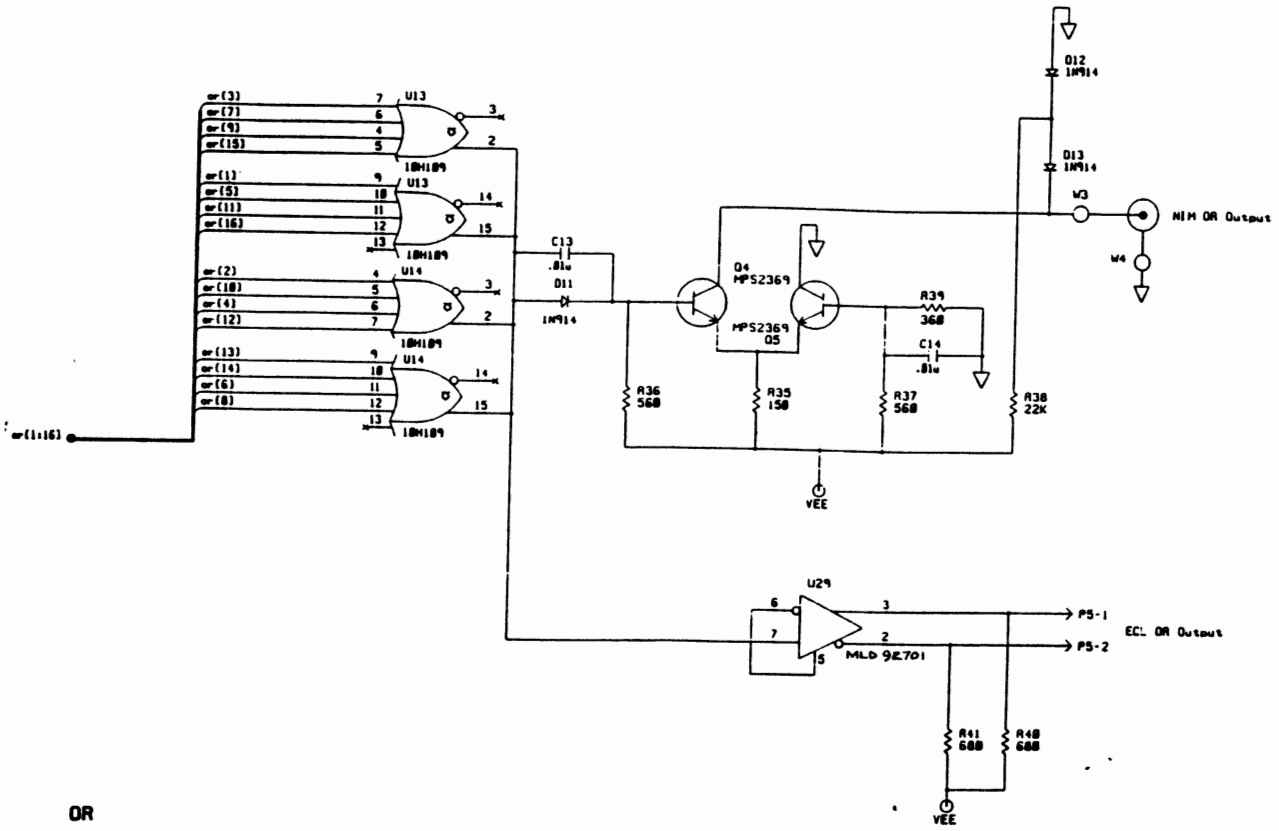
NO	REVISION	DATE	BY



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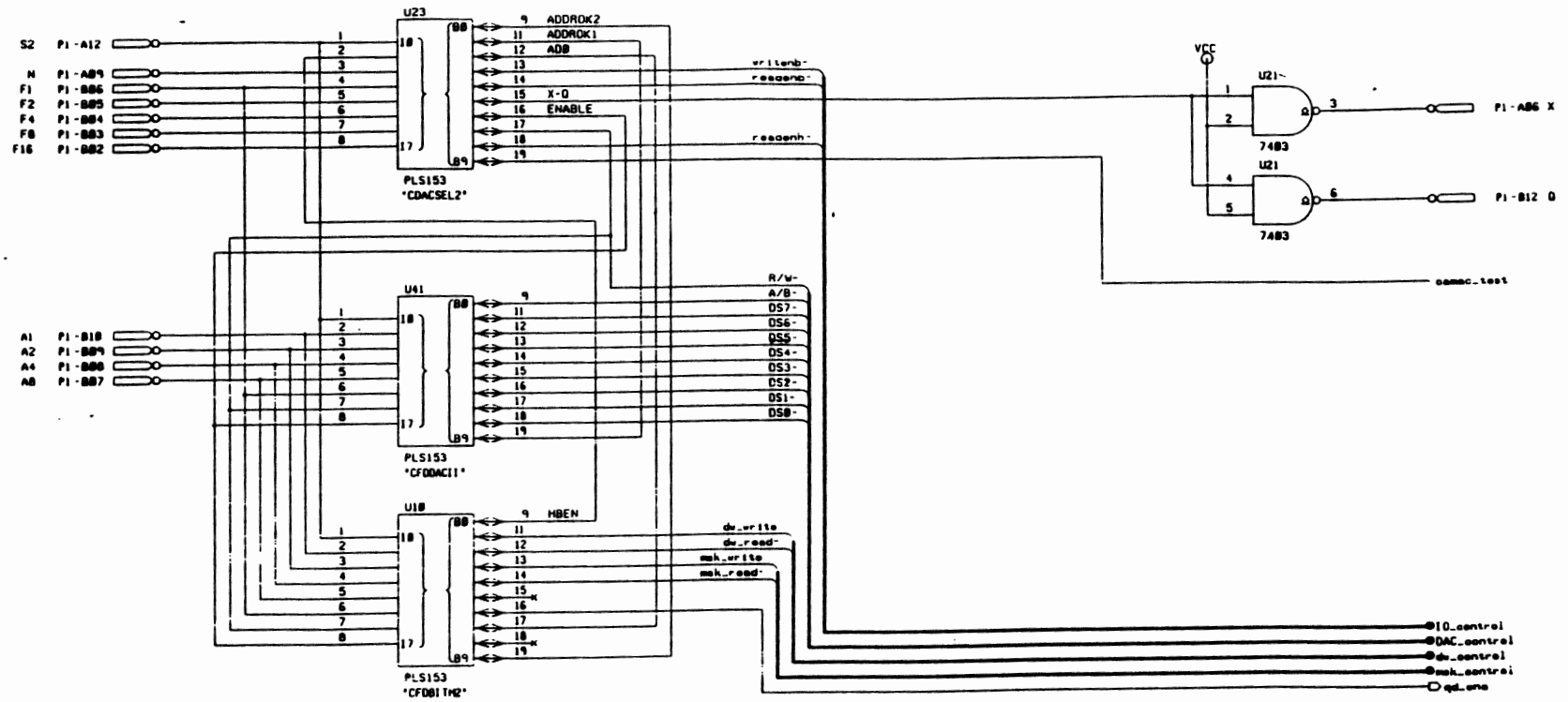

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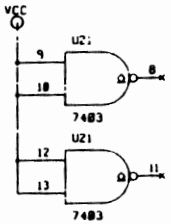

CAMAC Control

ITEM	PART NO	MFR	DESCRIPTION	REF DES	QTY

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NO	REVISION	DATE	BY
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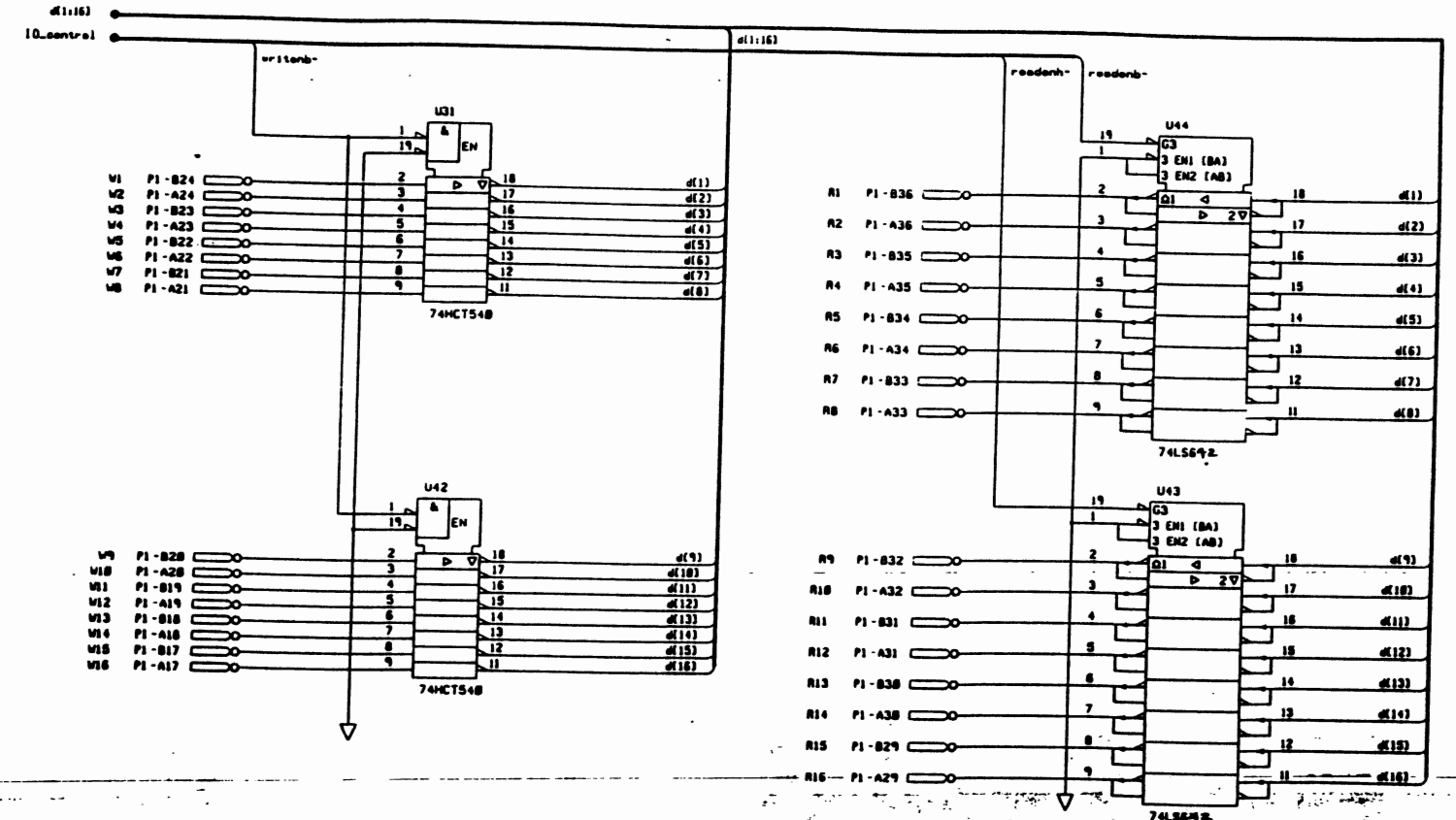

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CAMAC IO

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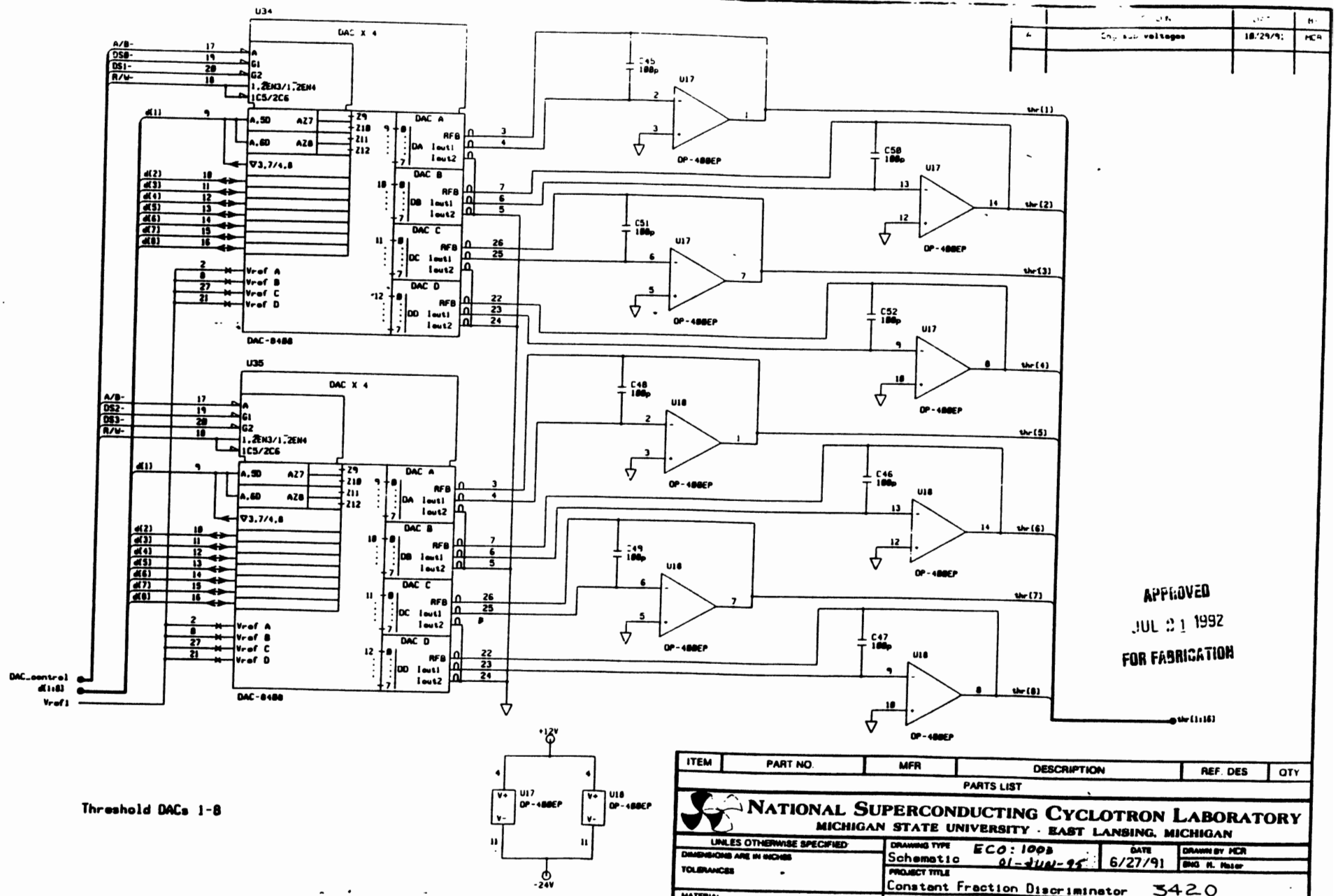

A	Chg sub voltages	10/29/91	MCR

Threshold DACs 1-8

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UNLES OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES
MATERIAL

DRAWING TYPE: Schematic ECO: 1008 01-JUN-95
DATE: 6/27/91
DRAWN BY: MCR
ENG: M. Meier
PROJECT TITLE: Constant Fraction Discriminator 3420
SCALE
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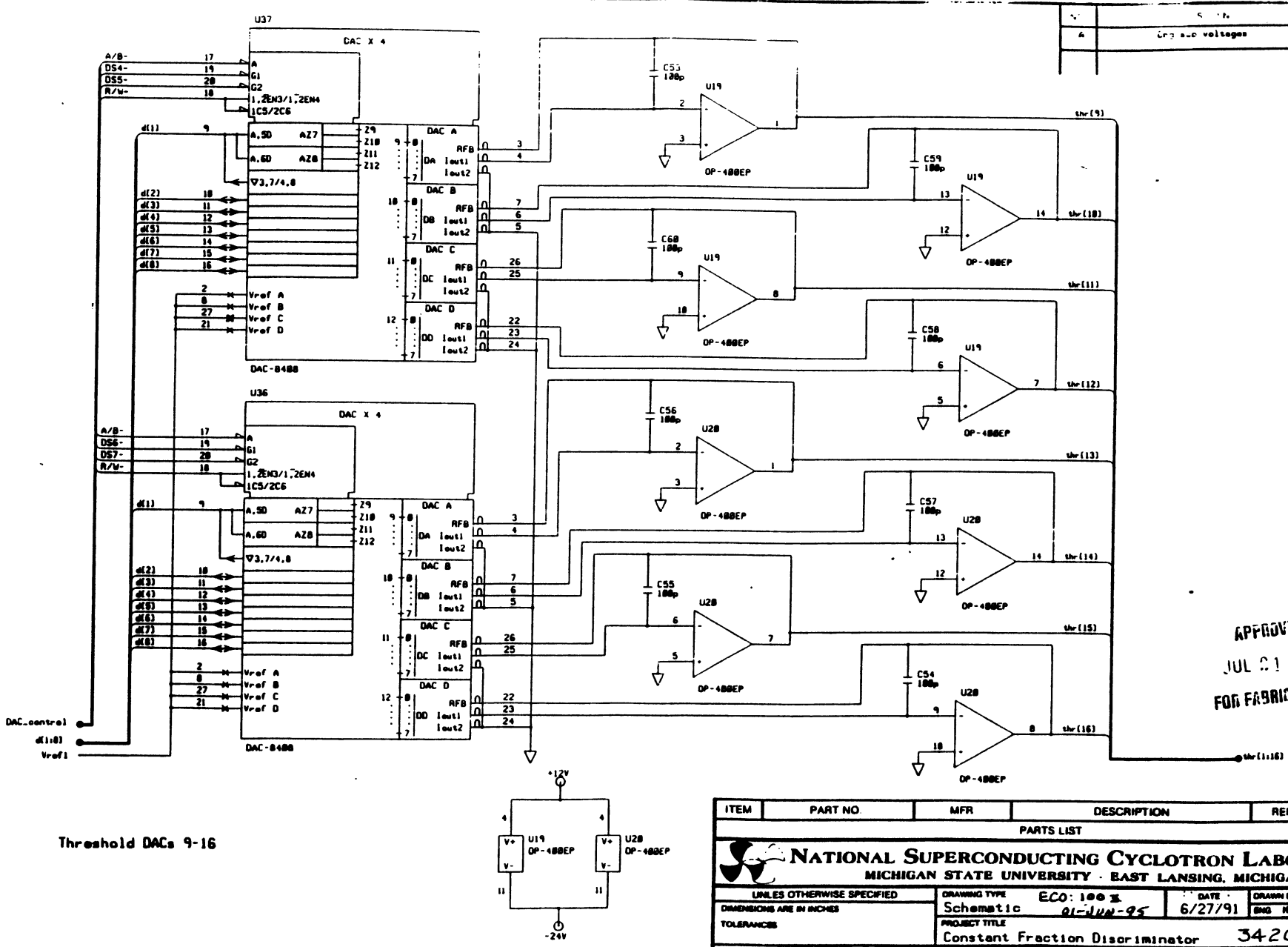

Threshold DACs 9-16

A	Orig. sub voltages	12/24/91	MCR

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817480

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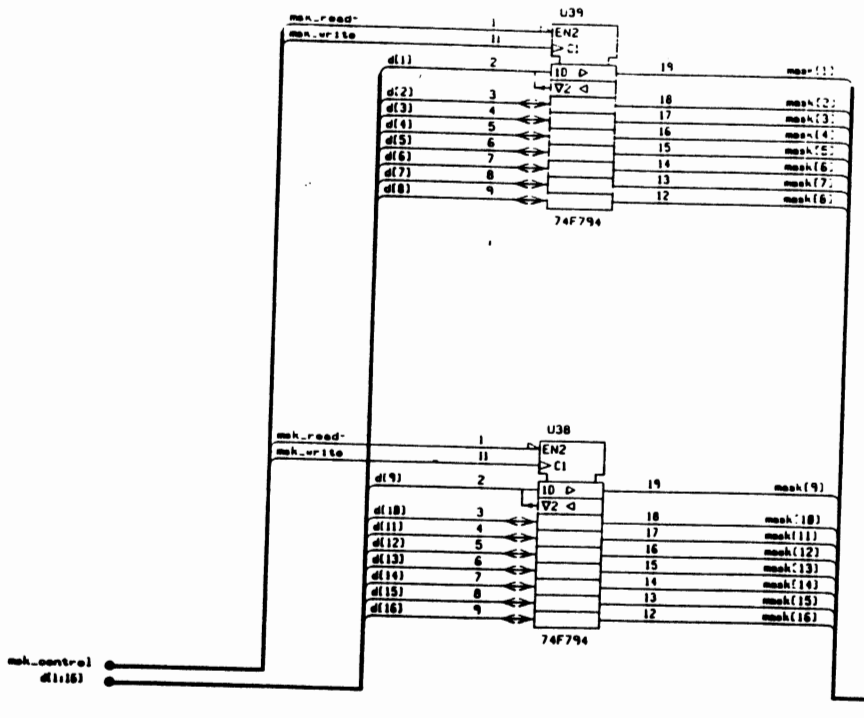

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Mask Register

ITEM	PART NO	MFR	DESCRIPTION	REF DES	QTY
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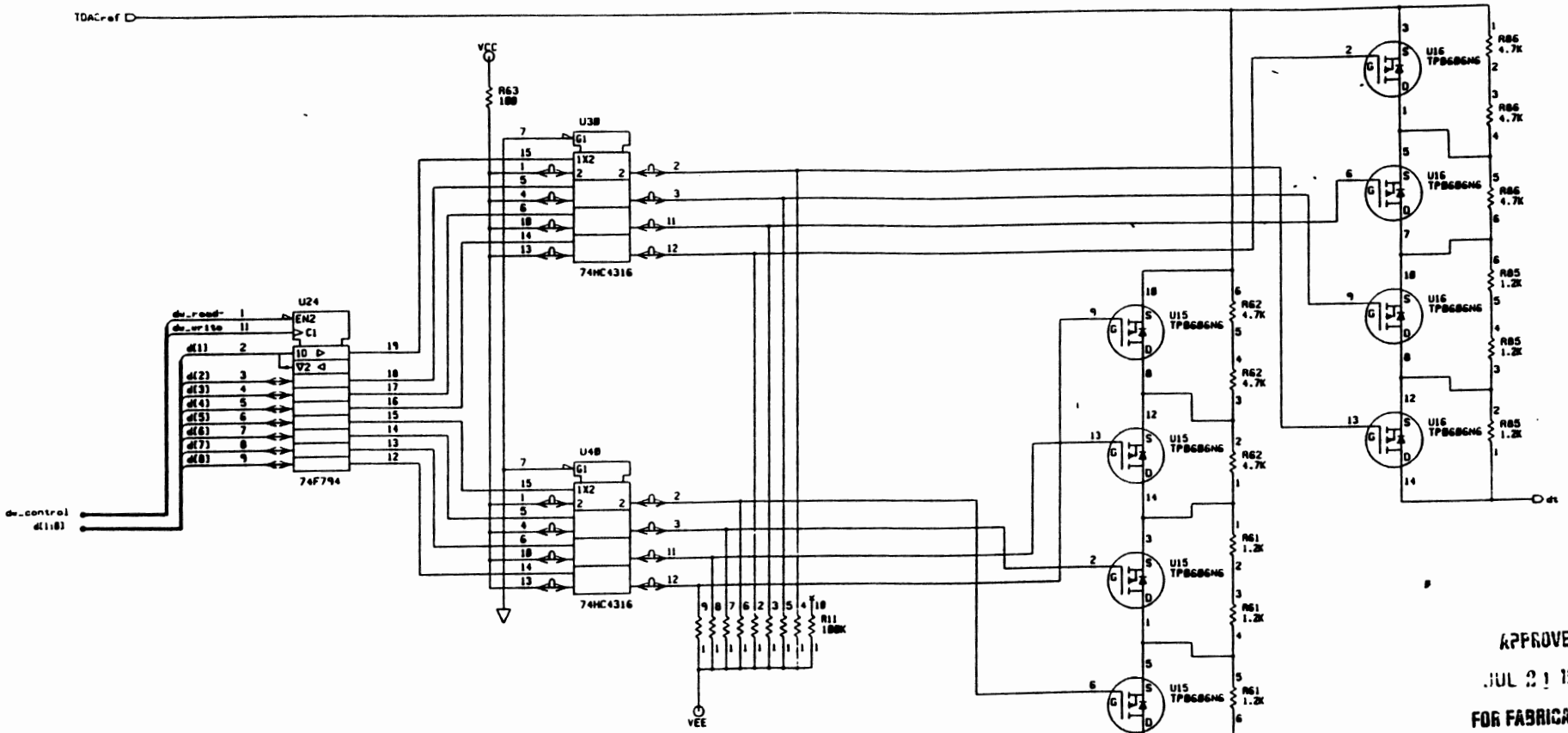
817480

	REVISION	DATE	B



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Dead Time and Width DACs

ITEM	PART NO	MFR	DESCRIPTION	REF DES	QTY
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TOLERANCES	PROJECT TITLE: Constant Fraction Discriminator		ENG: M. Hasler
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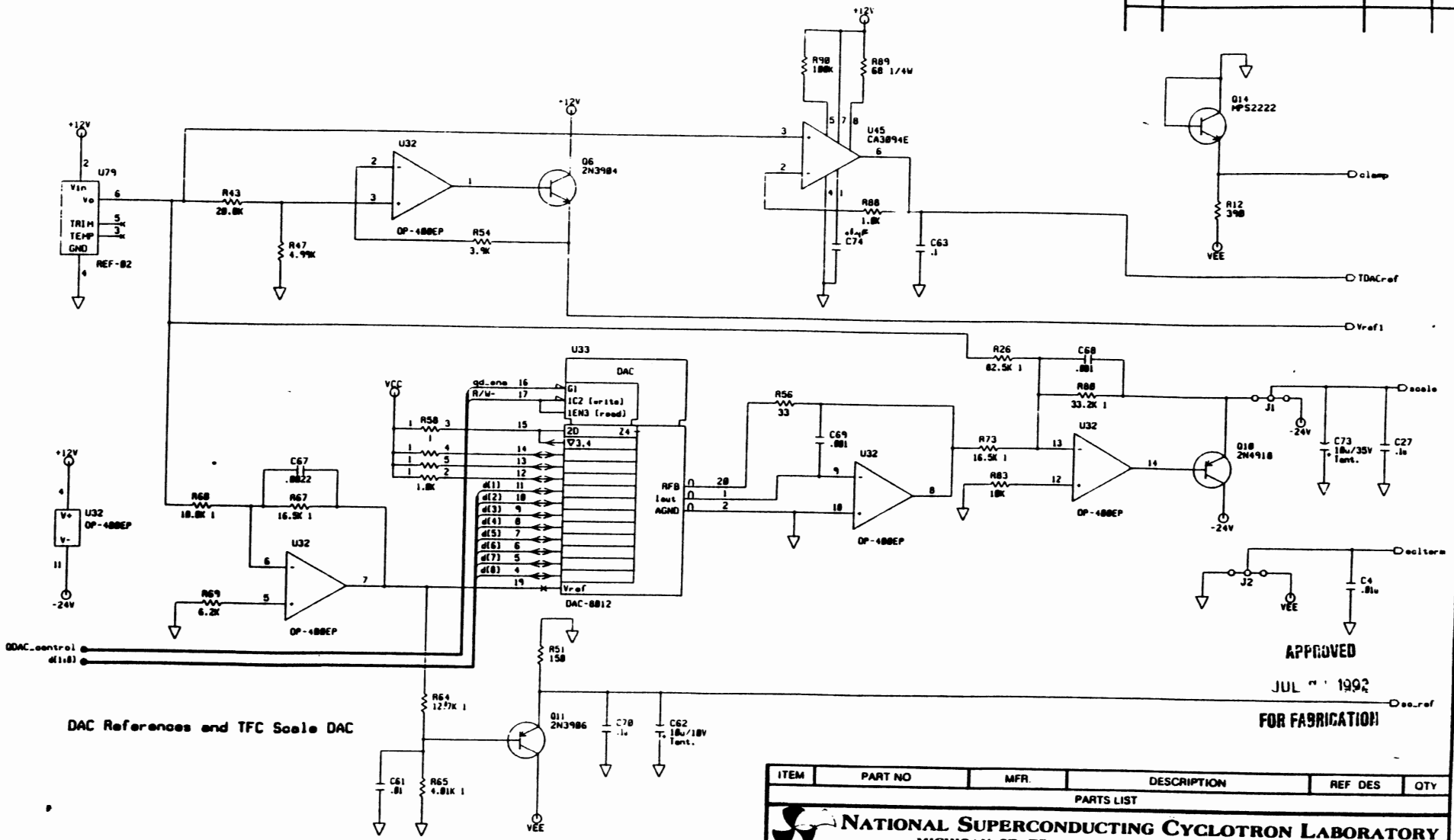

ITEM	PART NO	MFR.	DESCRIPTION	REF DES	QTY

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NATIONAL SUPERCONDUCTING CYCLOTRON LABORATORY
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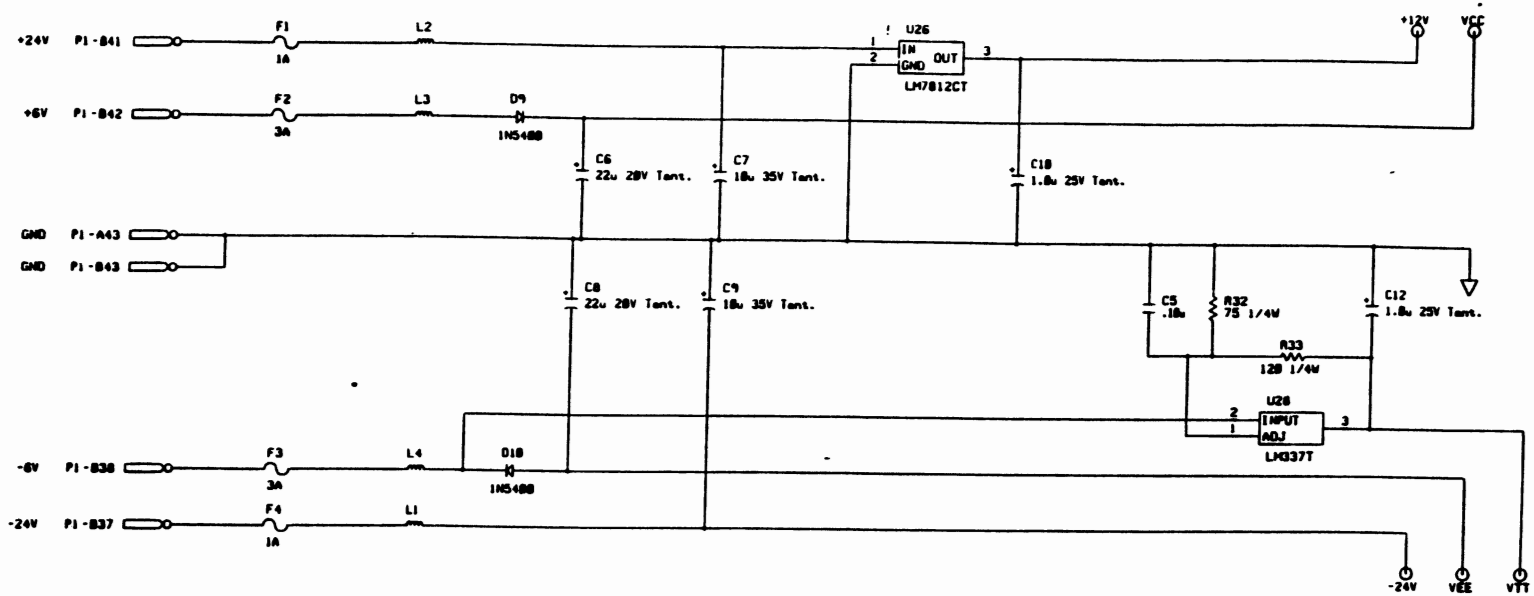
B17408

		DATE	BY
A	Chg diodes - 1N5400 & sup voltages	10/1/91	MCR



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JUL 21 1992

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Power

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UNLESS OTHERWISE SPECIFIED:	DRAWING TYPE: Schematic ECO: 1003 02-JUL-92	DATE: 6/27/91	DRAWN BY: MCR, ENG: H. Nann
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017488

	REVISION	DATE	BY
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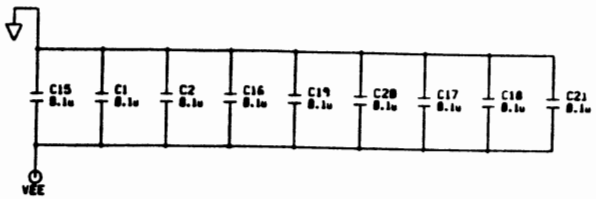
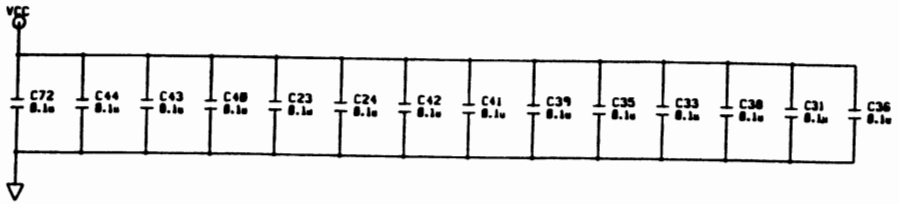
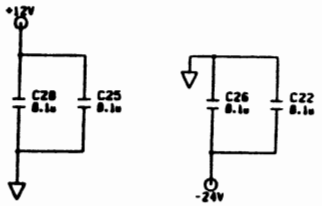
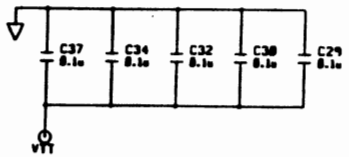






Power - Bypass Capacitors



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ITEM	PART NO.	MFR.	DESCRIPTION	REF. DES	QTY

PARTS LIST

NATIONAL SUPERCONDUCTING CYCLOTRON LABORATORY
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UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES; TOLERANCES; MATERIAL	DRAWING TYPE: Schematic	ECO: 1003 02-JUN-95	DATE: 6/27/91	DRAWN BY: MCR; ENG: N. Hoter
	PROJECT TITLE: Constant Fraction Discriminator			3420
	DRAWING NUMBER: 07-EDN-1A-01-B		SHEET 13 of 13	SCALE — REV A

15 OCT 1993

Addendum to 3420 constant fraction discriminator manual.

As of the above date the input impedance of the 3420 discriminators shipped from the factory is **50 ohms not 100 ohms.** If 100 ohm input impedance is desired then resistor networks R13 and R21 must be removed.

NSRL-398

THE UNIVERSITY OF ROCHESTER

Nuclear Structure Research Laboratory

ROCHESTER, NEW YORK

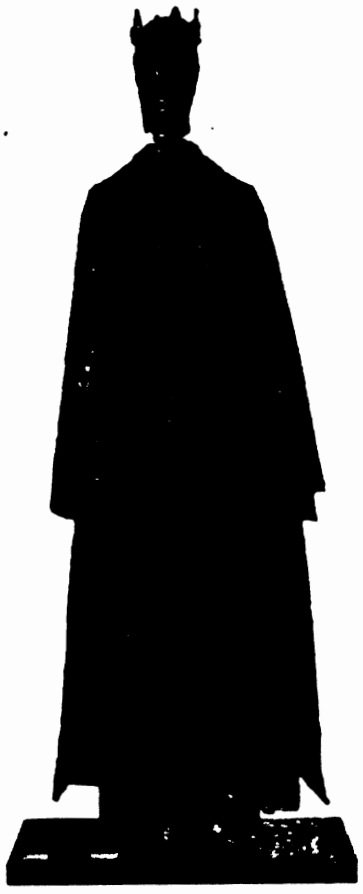
THE SIXTEEN-CHANNEL APEX CONSTANT FRACTION DISCRIMINATOR

M. R. Maier [a, b], P. A. A. Perera [c], M. Robertson [a], and F. L. H. Wolfs [c]

a) National Superconducting Cyclotron Laboratory
Michigan State University

b) Nuclear Science Division
Lawrence Berkeley Laboratory

c) Nuclear Structure Research Laboratory
University of Rochester



Submitted to Nuclear Instruments and Methods
August 1993

THE SIXTEEN-CHANNEL APEX CONSTANT FRACTION DISCRIMINATOR

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ABSTRACT

A sixteen-channel constant fraction discriminator (CFD) has been constructed for the ATLAS Positron EXperiment (APEX). An integrated circuit, recently introduced commercially, contains all the electronic building blocks required to construct a CFD and makes it possible to fit sixteen CFD channels into a single-width CAMAC module. An important new feature is the time-to-charge converter that is part of each CFD channel. Its calibration constant is controlled via CAMAC. The time-to-charge converter allows the use of low-cost charge-sensitive analog-to-digital converters for timing measurements.

I. INTRODUCTION

The sharp lines observed in the energy spectra of positrons emitted in certain heavy-ion collisions are a surprising and unexpected discovery for which there is no consistent explanation, despite more than ten years of work. The peaks have been observed in three distinct experiments [1-3] all carried out at the UNILAC accelerator of the Gesellschaft für Schwerionenforschung (GSI). Subsequent experiments have shown that similar peaks exist in the energy spectra of electrons detected in coincidence with peak positrons [4-7]. The observation that the peaks in the sum energy spectra are narrower than those in the singles spectra and the near equality of the positron and electron energies have been taken as possible evidence for the two-body decay of an isolated, slow-moving, neutral object as the origin of the peaks. The lack of direct information on the angles of emission, however, precludes proof of this hypothesis.

A new series of experiments, aimed at studying in detail the production mechanism of electrons and positrons in heavy-ion collisions, is being carried out at the ATLAS accelerator of Argonne National Laboratory. The ATLAS Positron EXperiment (APEX) is a collaborative effort between scientists from Argonne National Laboratory, Florida State University, Michigan State University, Princeton University, Queen's University, University of Rochester, University of Washington, and Yale University [8-11]. APEX represents a significant improvement in count rate; the APEX data rate will be over an order of magnitude larger than the rates obtained at GSI, partly due to an increase of detection efficiency and partly due to the CW nature of the heavy-ion beams from the ATLAS accelerator. In addition, APEX will directly measure the angles of emission of the electrons and positrons, thus allowing a determination of the invariant mass of the decaying object.

APEX consists of a large solenoidal spectrometer (3.8 m long, 1.7 m diameter), mounted transversely to the beam direction (see Figure 1). Electrons and positrons produced at the target spiral down the solenoid and are detected, on-axis, with two

highly-segmented, 36 cm long, pencil-like arrays of silicon detectors with a total of 432 1-mm-thick PIN diodes [12, 13]. The positrons are identified by detecting the characteristic back-to-back 511 keV γ-radiation associated with positron annihilation in cylindrical, position-sensitive, NaI(Tl) arrays (55 cm long, 42 cm diameter, 6 cm thick) that surround the silicon arrays [14]. The scattered heavy ions are detected in coincidence in an array of heavy-ion detectors that cover the angular range between 20° and 70° with respect to the beam. Two heavymet cones are located next to the target, on the solenoid axis, to shield the NaI and silicon arrays from the large flux of primary γ-rays, and, in addition, to prevent all δ-electrons with energies below 115 keV from reaching the silicon arrays.

Each PIN diode provides energy and time information. Each NaI crystal provides pulse height and time information. The operation of the heavy-ion counters relies solely on time information. For each of these detector systems the timing signals trigger constant fraction discriminators (CFDs). These CFDs were designed specifically for APEX with the following design goals:

1) High-density CAMAC module (at least sixteen CFD channels per module).
2) Low cost (approximately $ 100 per CFD channel).
3) Provide a time-to-charge output which allows the use of low-cost charge-integrating ADCs.

In Section II of this paper the design of the sixteen-channel APEX CFD is described. Its performance is discussed in Section III.

II. CFD DESIGN

The design of the APEX CFD is based on ideas previously published [15] and uses fast comparator integrated circuits (ICs). The space available in a single-width CAMAC module permits only eight CFD channels on one board if standard ICs are used [15].

The company Analog Devices has recently introduced a "rigid disk data qualifier" IC (AD891, see Ref. [16]), whose internal logic contains all the building blocks for a CFD, i.e. comparators, coincidences and two one-shots. The AD891 comes in a 14 pin dual inline plastic (DIP) package. The use of this IC package makes it possible to fit sixteen CFD channels into a single-width CAMAC module.

Figure 2 shows a schematic of the input section of one channel of the APEX CFD. The input network uses plug-in headers to define the trigger fraction and delay. Lumped sum delay lines with five taps (Data Delay Devices 1505-xxB, 2 to 20 ns per tap, xx ns total) are used for the constant fraction delay. The delay-line impedance (100 Ω) is matched to the required input impedance (50 Ω or 100 Ω) by selecting the proper parallel termination. A test pulse, generated on the board, couples via a diode to the input of each individual CFD channel. Sixteen eight-bit digital-to-analog converters (DACs) with memory, controlled via CAMAC, determine the thresholds of the sixteen CFD channels. The dead time and output pulse width are determined by connecting resistors to ground from the corresponding pins. Variations in the internal reference voltage of the different AD891s were found to lead to large channel-to-channel variations in the maximum width of the dead time and output pulse. The variations are significantly reduced when the resistor network that determines the times is connected to a + 5 V reference voltage. This makes the time settings insensitive to the reference voltage of the individual ICs.

Figure 3 shows a schematic of the output section of one channel of the APEX CFD. The output of the AD891 connects to one input of a three-input NAND gate. The other two inputs of the NAND connect to a common VETO and a CAMAC controllable MASK. The output of the NAND connects to an ECL line driver and a time-to-charge converter (TQC). The output of the NAND also connects to circuits that generate the OR output and the MULTIPLICITY output.

The TQCs are CAMAC controllable current sinks with a range from 0 to - 10 mA. They can be switched via a jumper to provide fast NIM level signals (i.e. - 16 mA). The TQCs can be used to generate time spectra with charge-sensitive ADCs (QDCs) by feeding the current source to the linear input of the QDC. If the leading edge of the QDC gate occurs before the leading edge of the TQC output and the trailing edge of the QDC gate occurs before the trailing edge of the TQC output, then the integrated charge will be proportional to the time difference between the leading edge of the TQC and the trailing edge of the QDC gate (see Figure 4a). The advantages of this "overlap" method have been discussed by Braunsfurth, *et al.* [17, 18]. Alternatively, the VETO input can be used to terminate the TQC output (see Figure 4b). The integrated charge of the TQC output is proportional to the time difference between the leading edge of the TQC output and the leading edge of the VETO. In this case the QDC gate must be wide enough to enclose the entire charge pulse.

The CFD circuit itself is built on a four layer board and uses 34 pin 0.1 inch center connectors for the input and output signals, except for the VETO, the OR, the TEST, and the MULTIPLICITY, for which LEMO connectors are used [19].

III. CFD PERFORMANCE

The range of the CFD threshold voltage is - 50 mV to - 1 V with eight bit resolution. The ranges of the dead time and the output pulse width are 25 ns to 250 ns with 4 bit resolution. A sixteen bit mask enables (or disables) each individual channel. The TQC range is 0 to - 10 mA with eight bit resolution. The internal test pulse generator can be triggered from the front panel with a fast NIM signal or via CAMAC. Walk and resolution of the CFD have been measured using a pulse with 5 ns rise and fall times and 20 ns width. The constant fraction delay was 10 ns, and the fraction was 30 %. These

measurements show a walk of less than ± 200 ps for input amplitudes between 100 mV and 5 V and a resolution of less than 50 ps (FWHM).

The crosstalk between adjacent channels is less than 5 % and depends critically on proper input termination and cabling. This cross talk has two effects. First, if the thresholds are set low, a large pulse in one channel can trigger neighboring channels. This effect is easily eliminated from the data since the neighboring channels will have no energy signals associated with the timing signals. Second, the time at which a specific CFD channel generates an output will depend on the presence of signals in neighboring CFD channels. This effect was studied by measuring the time shift of a CFD channel, triggered by a - 0.8 V pulse with 4 ns rise and fall times, as a function of the time difference between the arrival of this signal and the arrival of signals in the neighboring CFD channels. Figure 5 shows the measured shift for channel 2 of an APEX CFD as a function of the time difference between the inputs of channel 2 and channel 3. A positive time difference means that the input of channel 3 arrives before the input of channel 2. The largest shift observed is 200 ps. These variations are not sensitive to the threshold settings but increase with increasing amplitude of the signal sent to channel 3.

The two modes of operation of the TQC (see Section II) provide the same resolution and linearity when the TQC output is connected via a short coaxial cable to the QDC input. However, if the TQC output must be delayed, a significant loss in resolution is observed when the trailing edge of the QDC gate is used as the STOP. This is a result of the distortions of the charge pulse in long cable delays. The loss in resolution does not occur when the VETO is used as the STOP. The results of a measurement of the TQC linearity are shown in Figure 6. The solid line shows the deviation from linearity when the TQC output is connected directly to the QDC. The deviation from linearity is always less than ± 100 ps. The dashed line shows the deviation from linearity when the

TQC output is delayed using 100 feet of twisted pair cable. The maximum deviation from linearity increases but is still less then ± 200 ps.

IV. CONCLUSIONS

Advances in IC technology have enabled the construction of a sixteen-channel CFD which is being used to process the timing signals of several detector types in the APEX experiment. The inclusion of a TQC significantly simplifies the electronics for APEX since a single type of QDC can be used for both the energy and time-of-flight measurements. The measured walk of the APEX CFD is less than ± 200 ps for amplitudes between - 100 mV and - 5 V. The resolution is 50 ps (FWHM). The maximum deviation from linearity of time measurements carried out using the TQC is less than ± 100 ps when the TQC output is fed directly into the QDC, and less than ± 200 ps when the TQC output is delayed using 100 feet of twisted pair cable before being fed into the QDC.

ACKNOWLEDGMENTS

The many contributions from Sam Austin, Russell Betts, Martin Freer, Thomas Happ, Ed Kashy, Phil Wilt and Alan Wuosmaa during the design, construction and evaluation phases of the APEX CFD are gratefully acknowledged. The authors would like to thank Ed Corlett, Stuart Gazes and Phil Wilt for reading the first draft of this paper and providing us with useful comments and suggestions. This work was supported by the United States Department of Energy, Nuclear Physics Division, under Contract No. DE-AC03-765F00098 and W-31-109-ENG-38. Work at the University of Rochester and at Michigan State University was supported by grants from the National Science Foundation.

Reference to a company or product name does not imply approval or recommendation of the product by the Michigan State University, Lawrence Berkeley Laboratory, the University of Rochester, Argonne National Laboratory, or the United States Department of Energy to the exclusion of others that may be suitable.

REFERENCES

† Present address: 4109 Cornell, Okemos, MI 48864, USA

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[19] This unit is now available commercially from LeCroy (Model 3420).

FIGURE CAPTIONS

Fig. 1 Schematic illustration of the APEX apparatus without the heavy-ion detectors.

Fig. 2 Schematic of the input section of one channel of the APEX CFD.

Fig. 3 Schematic of the output section of one channel of the APEX CFD.

Fig. 4 a) Proper timing of the various signals and gates required to operate the TQC in a mode in which the QDC gate supplies the STOP. The shaded region of the TQC OUT indicates the amount of charge integrated by the QDC.

b) Proper timing of the various signals and gates required to operate the TQC in a mode in which the VETO supplies the STOP. The shaded region of the TQC OUT indicates the amount of charge integrated by the QDC.

Fig. 5 Measured time shift of channel 2 of an APEX CFD as a function of the time difference between the inputs of channel 2 and channel 3.

Fig. 6 Deviation from linearity of the TQC output (operated in VETO mode). The solid curve shows the results obtained when the TQC output connects directly to the QDC input. The dashed curve shows the results obtained when the TQC output connects via 100 feet of twisted pair cable to the QDC input.

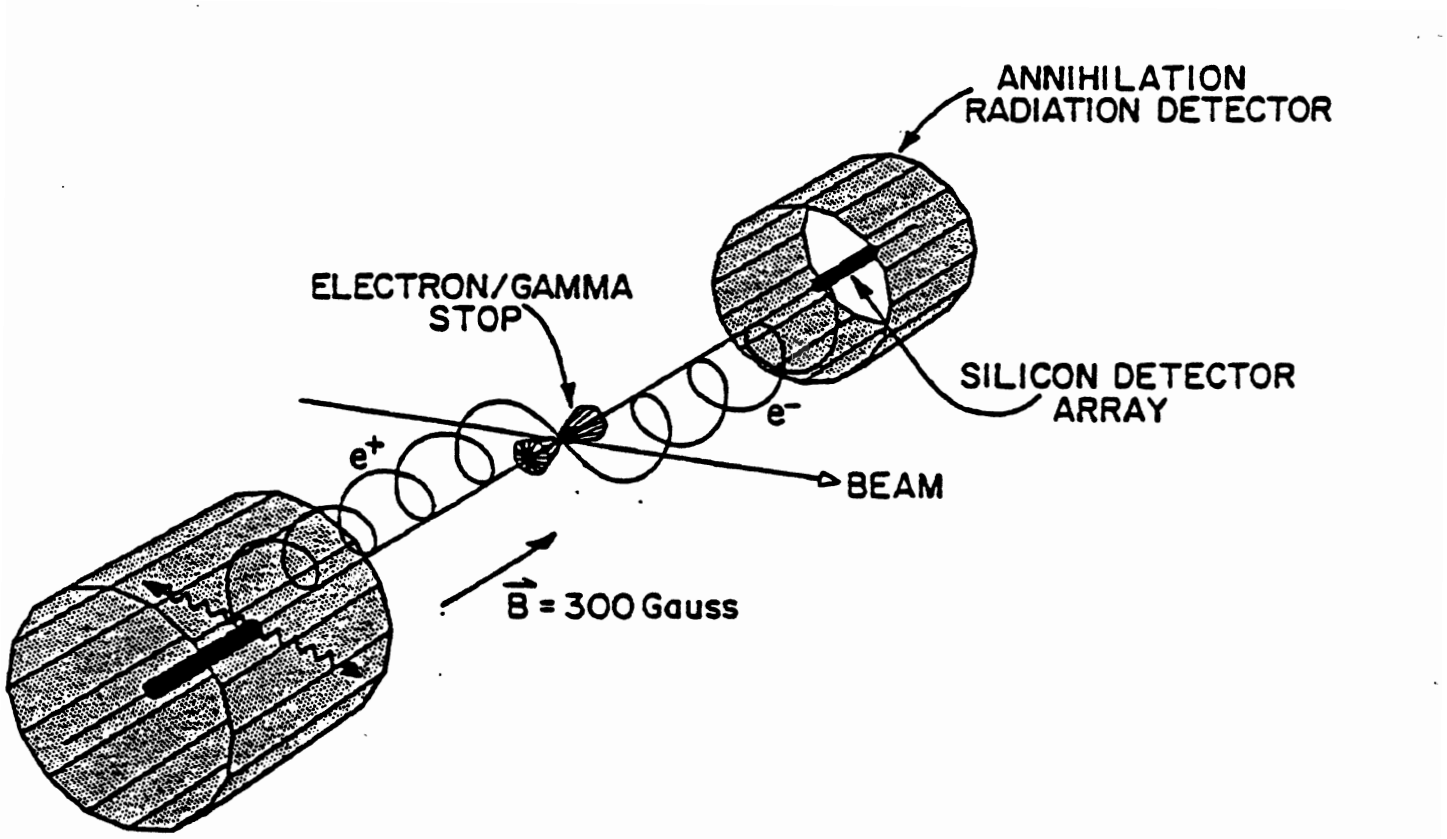
ANNIHILATION
RADIATION DETECTOR
ELECTRON/GAMMA
STOP
SILICON DETECTOR
ARRAY
e⁻
e⁺
BEAM
B = 300 Gauss

Figure 1

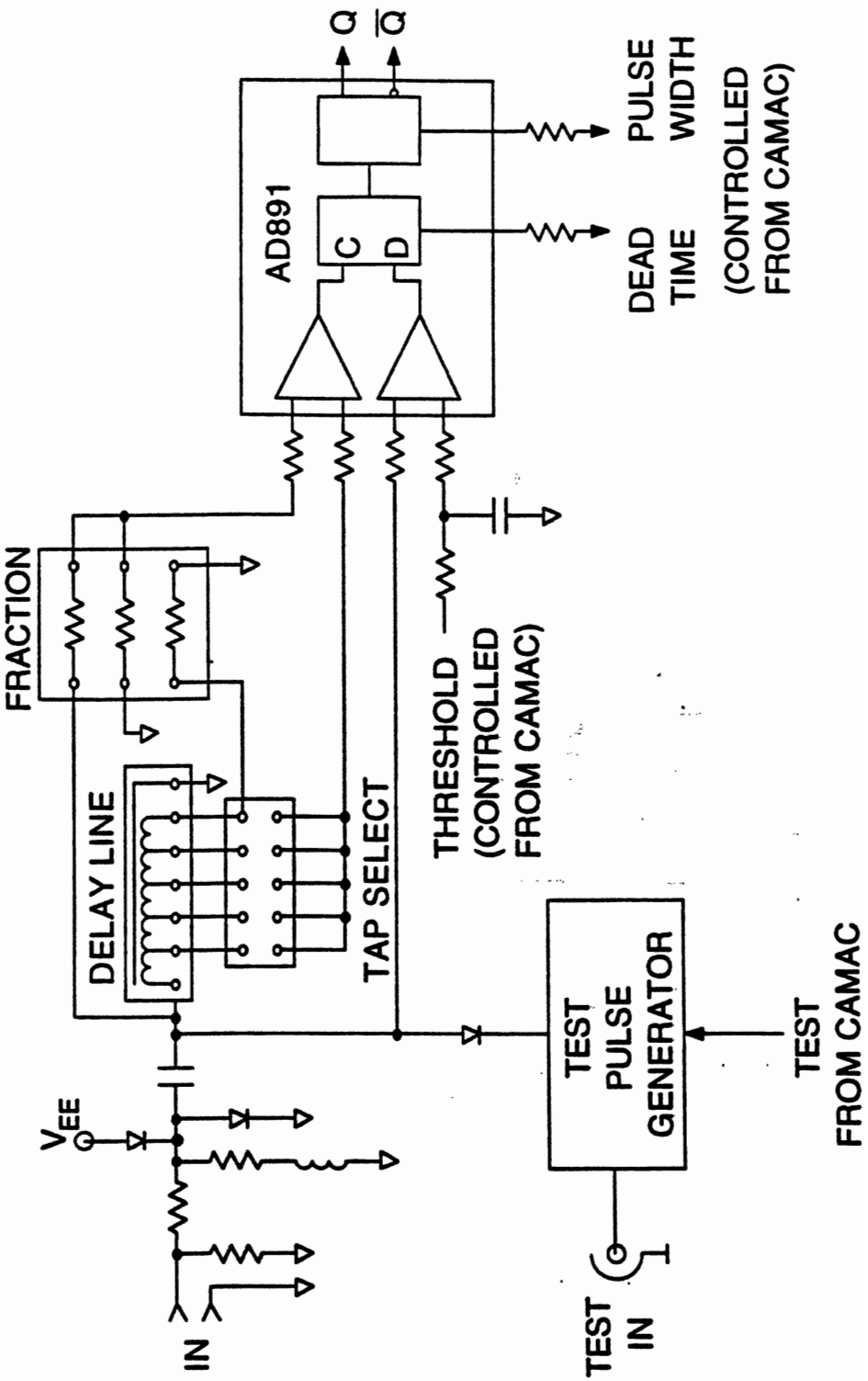
Q
$\overline{Q}$
AD891
C
D
PULSE WIDTH
DEAD TIME
(CONTROLLED FROM CAMAC)
FRACTION
DELAY LINE
TAP SELECT
THRESHOLD (CONTROLLED FROM CAMAC)
V_{EE}
IN
TEST PULSE GENERATOR
TEST IN
TEST FROM CAMAC

Figure 2

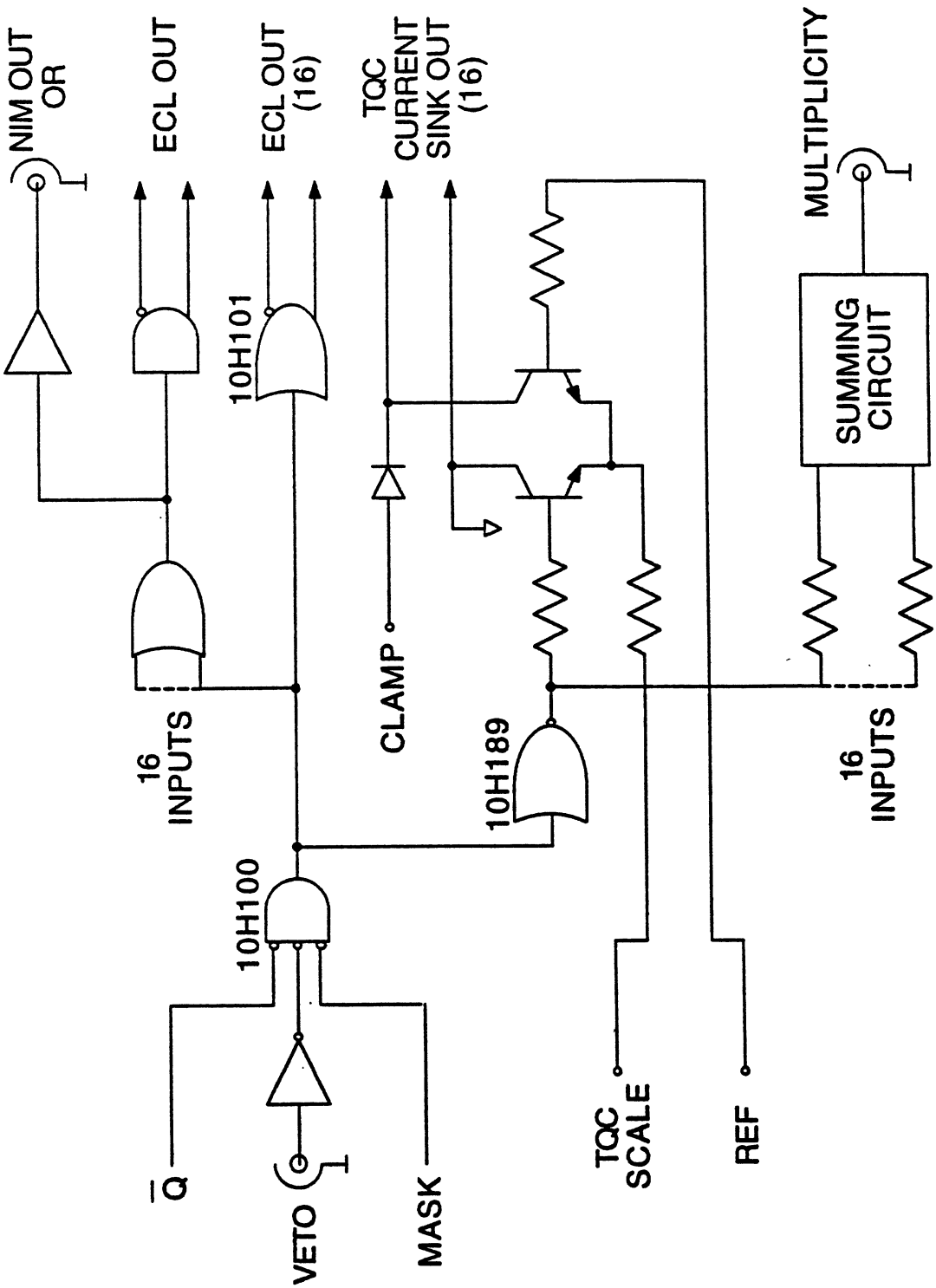
NIM OUT OR
ECL OUT
ECL OUT (16)
TQC CURRENT SINK OUT (16)
MULTIPLICITY
10H101
SUMMING CIRCUIT
16 INPUTS
CLAMP
10H189
16 INPUTS
10H100
Q
VETO
MASK
TQC SCALE
REF

Figure 3

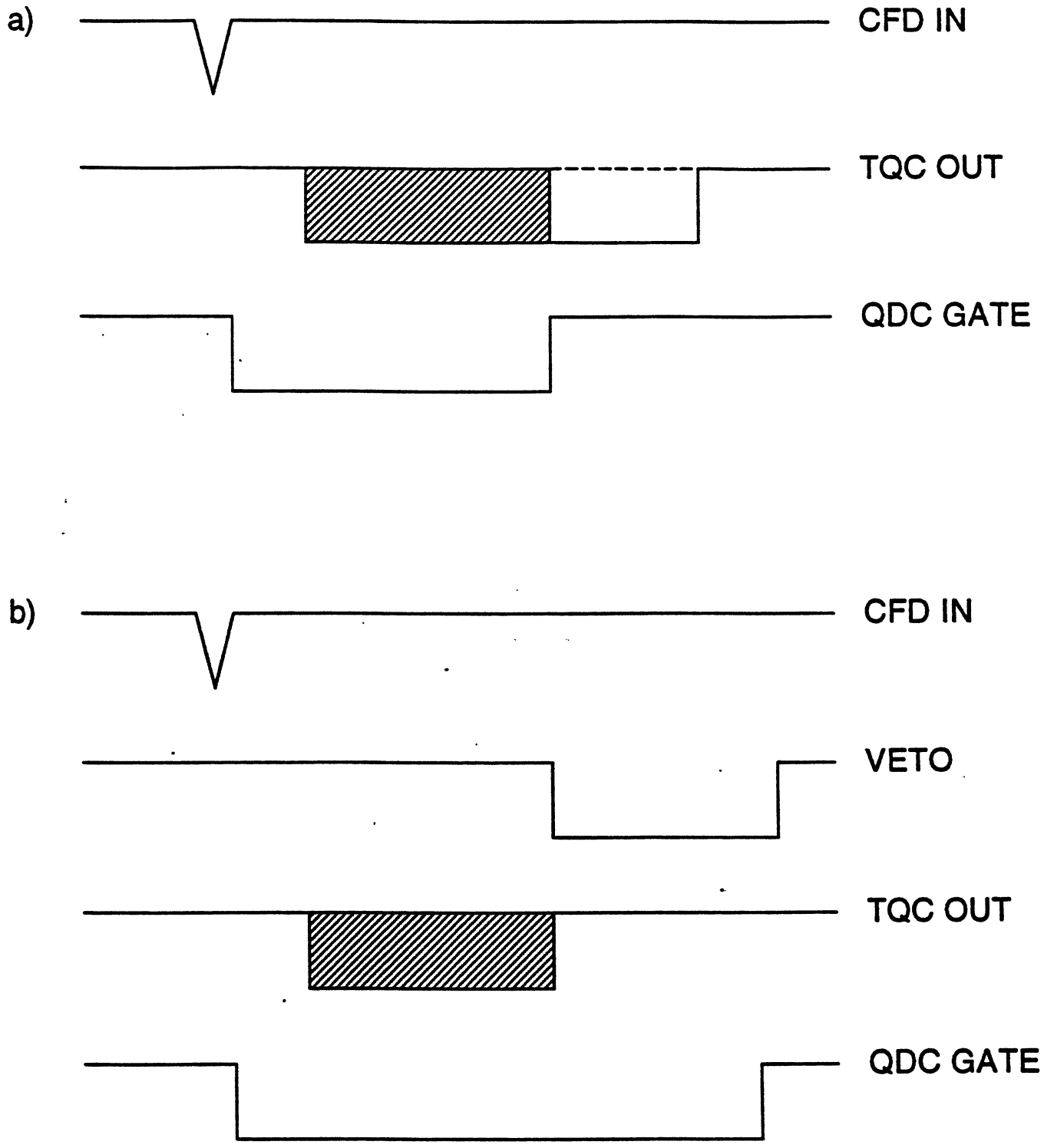

Figure 4

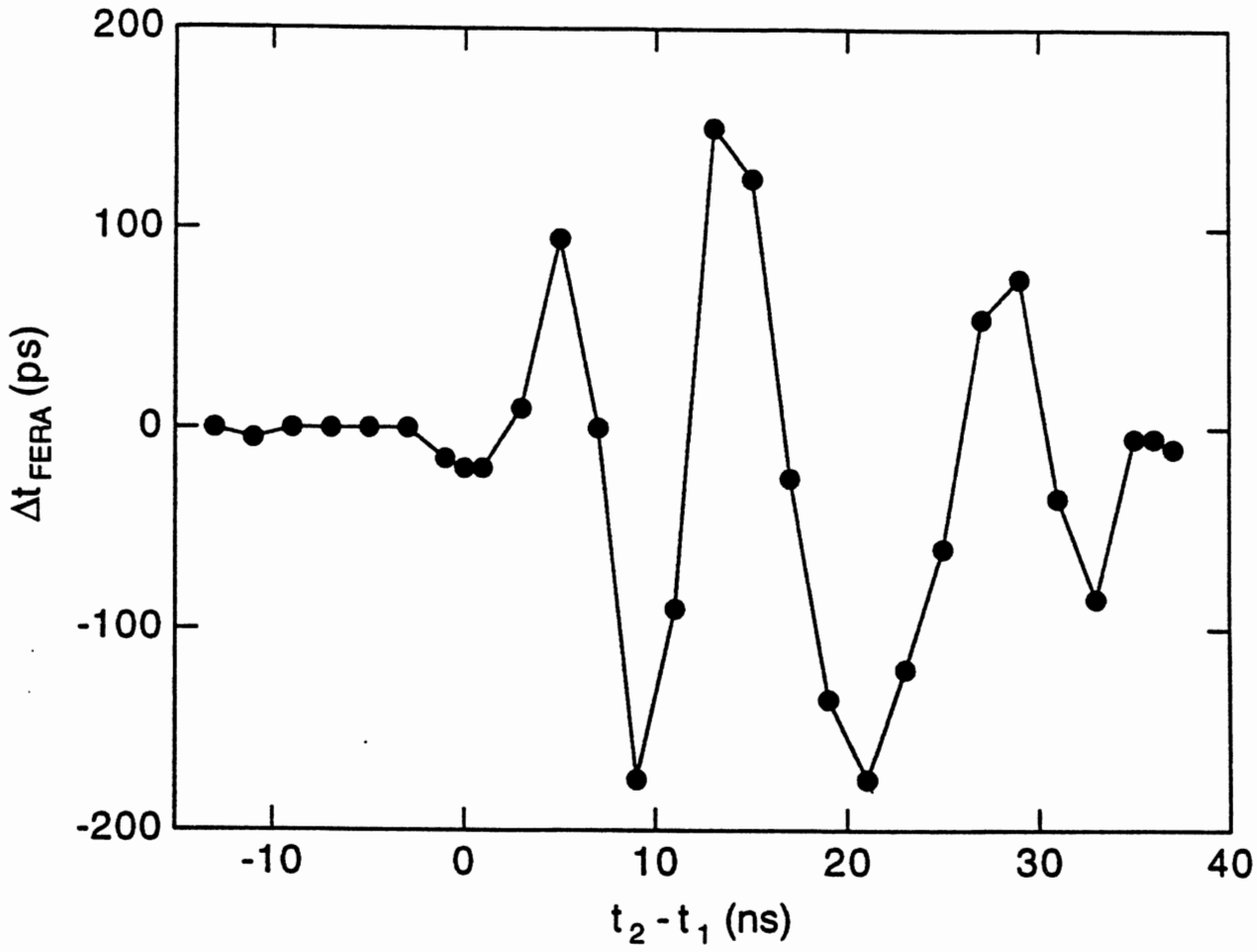

Figure 5

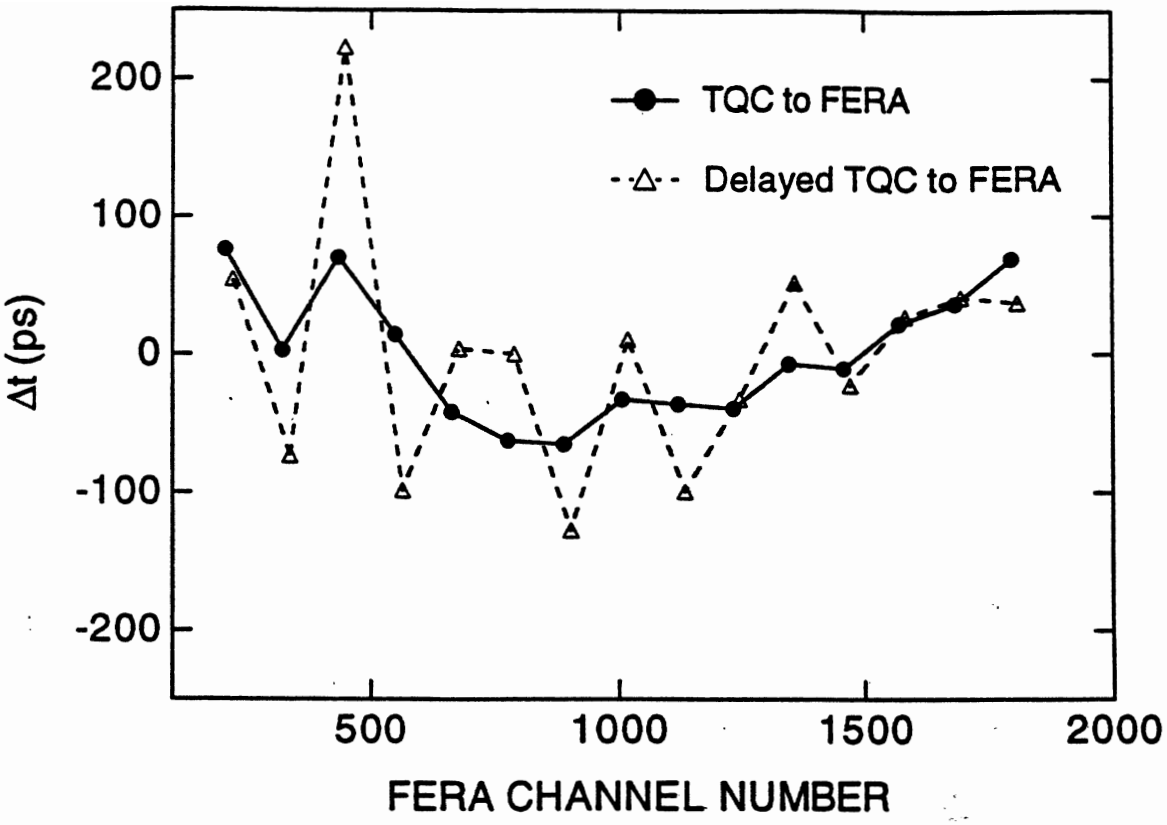
200
100
0
-100
-200
Δt (ps)
500
1000
1500
2000
FERA CHANNEL NUMBER
TQC to FERA
Delayed TQC to FERA

Figure 6