CAMAC ECLine
MODEL 4418
16 CHANNEL, PROGRAMMABLE
LOGIC DELAY/FAN-OUT
USER'S MANUAL

November 1984

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LIST, ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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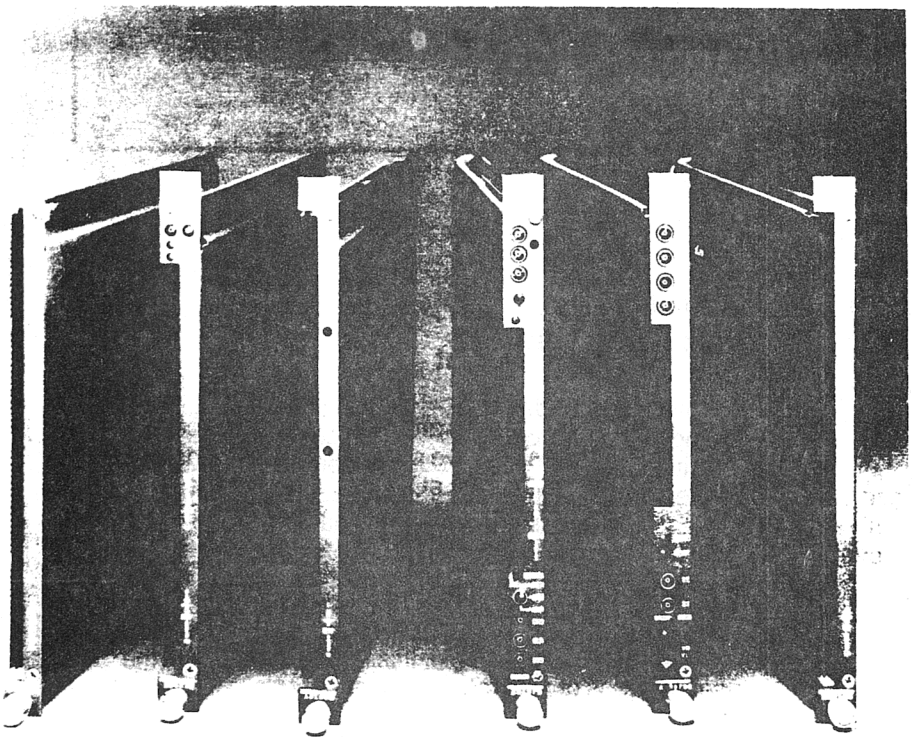
ECLine/CAMAC
Programmable First Level Trigger Modules

4418 PROGRAMMABLE LOGIC DELAY/FAN-OUT
4504 FLASH ADC
4508 PROGRAMMABLE LOOKUP UNIT
4516 PROGRAMMABLE LOGIC UNIT
4532 MAJORITY LOGIC UNIT
4564 OR LOGIC UNIT



- **High Speed First Level Trigger Decisions**
- **Programmable Logic Functions**
- **Compatible with ECLine Data Handler Modules**
- **Compatible with ECLine Discriminators, ADC/TDC, and MWPC Systems**
- **Designed-in Expandability**

FAST, FIRST LEVEL TRIGGER PROCESSING

The LeCroy ECLine family of programmable logic modules include logic delays, Boolean logic and other functions vital for high speed trigger systems. It also includes fast table lookup permitting pre-programmed responses to digital data. Functions are performed in only a few tens of nanoseconds, permitting data to be screened prior to recording and increasing the sensitivity of the experiment.

FEATURES

High Speed - Maximum rates of 65 to 150 MHz , depending on module and programmed features.

Multiple Functions - Relative timing adjustable by programmable logic delay, Majority Logic and simple Boolean Logic (AND/OR) for coincident events, Programmable lookup for complex functions.

Fan-Out Capability - Use of ECL (Emitter Coupled Logic) levels provides outputs suitable for fan-out to several modules (termination resistors may need to be removed on inputs).

Use of Multichannel Differential ECL - Signals for economic, fast, noise immune interconnections.

FUNCTIONAL DESCRIPTION

LeCroy's ECLine family of programmable logic modules are designed to quickly characterize data so that a rough go/no-go decision can be made for further processing. For example, discriminators are employed to ensure that analog signals are of sufficient amplitude to be interesting, and to provide logic outputs of fixed duration. This stage is then followed by a coincidence latch which records the pattern of "interesting signals" that occur within the same time window. The First Level Trigger modules ensure that specific combinations of signals have occurred. (Information on Discriminators and Latches may be found on other ECLine Programmable Logic Data Sheets.)

This first stage of data handling can then either reject the event as uninteresting, or can pass data on for further processing. The more sophisticated line of ECLine Data Handling modules include data conversion, arithmetic operations, fast "do loop" type operations, and specialized pattern recognition/ interpretation. Information on LeCroy Data Handling modules may be found on the Data Handlers technical data sheet. All functions are programmable to provide complete computer control of the triggering and data acquisition systems.

The LeCroy ECLine modules are compatible with the sophisticated FERA (Fast Encoding and Readout ADC) analog and time interval digitizing systems, as well as with the PCOS III Multiwire Proportional Chamber System. For exceptional data rates and on-board event accounting, the ECLine modules are also compatible with the LeCroy FASTBUS Multiple Event Buffer Memory, Model 1892. This compatibility provides a convenient method of storing data from ECLine modules, combining data from ECLine and FASTBUS (IEEE-960) systems, and provides the exceptional speed and data handling capability of the FASTBUS Standard.

Model 4418
Logic Delay/Fan-Out

Fast, passive logic delays are of prime importance for allowing all signals to arrive simultaneously at a data acquisition module. The LeCroy Model 4418 has 16 passive, tapped delay lines, one for each input. Each delay is individually set by computer via CAMAC in 1, 2 or 4 nsec increments (depending on sub-model or "MOD" selected), over a range of fifteen increments. The selection directs an output to "view" a particular tap on the delay line. For example, this feature would give the user a means of accurately aligning signals in time to compensate for differences in cable lengths.

Deadtimeless operation at speeds up to 100 MHz is assured by using passive delay lines and ECL switches. This feature provides the reliability of cable delays together with the speed and fan-out of ECL circuitry. As an added feature, each output is present three places on the front panel to provide additional fan-out capability. The cost of this device rivals cable delays.

Model 4504
Flash ADC

Four independent 4-bit (plus overflow) Flash ADC's are incorporated in the Model 4504. The sampling rate is adjustable from 20 to 100 MHz via front-panel control. Alternatively, a front-panel strobe input can be used to externally control the sampling rate.

The 4-bit ECL outputs are accompanied by a strobe output signal to indicate that the outputs are valid. This feature provides a convenient means to strobe subsequent logic (for example, the Model 4508 Programmable Logic Unit) that uses the Flash ADC results. A front-panel VETO input is provided for disabling the unit during periods when no input data can be processed.

The most common use of the 4504 is as a multiple threshold discriminator . The input may be derived directly from the detectors themselves or the analog outputs of other ECLine modules (Model 4532 for example).

Model 4508
Programmable Lookup Unit

Two independent 8-bit Programmable Lookup Units (PLU's) are included in the Model 4508. Each unit has an 8-bit digital input and an 8-bit digital output. The unit functions as an 8-bit addressable RAM. The contents are pre-programmed via CAMAC by the user. Each 8-bit input is a RAM address, and each 8-bit output is the content of this addressed location.

Output patterns are programmed into the PLU for each of the 256 possible input patterns. This unit can act as a complex logic module , a programmable calibration unit, or it may control the actions of subsequent logic based on the input pattern and programmed lookup table.

Each section of the Model 4508 can operate in one of three modes: Shaped, Overlap or Continuous. In the Shaped Mode, the outputs are a pulse of duration set by a front-panel adjustment. The inputs must be accompanied by a front-panel Strobe input signal . In Overlap Mode, the output pulse width (on all 8 bits) equals the input width if the Strobe input signal arrives before the input. Finally, in Continuous Mode, the output width reflects the time coincidence between Strobe and the inputs pulses.

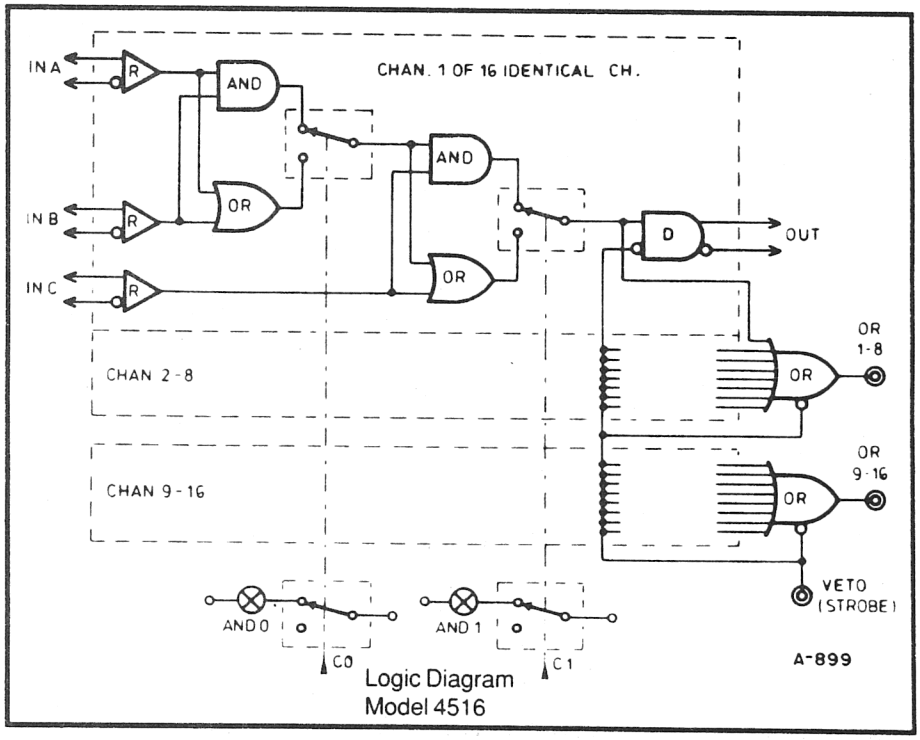
Model 4516
3-Fold AND/OR Logic Unit

Each of the 16 channels of the Model 4516 has three inputs (A, B and C). All channels have a front-panel output that is one of the Boolean combinations: (A•B•C), (A+B)•C, (A•B)+C, or (A+B)+C. The choice of logical function, AND(•) or OR (+), is set for all channels by two switches. These switches are set either by rear-panel manual switch settings or by computer command via CAMAC.

The 150 MHz speed of Model 4516 lends great versatility to this simple module. It can be used as a front-end AND/OR logic module, or an integral component in a higher level trigger processor.

Model 4532
Majority Logic Unit

Experiments that require a minimum number of signals to be present need a Majority Logic Unit. Each of the 32 inputs of the 4532 that is in a logical 1 state gives an incremental increase in a current sum output. An



Logic Diagram
Model 4516

onboard discriminator may then be used to signal when a user set current threshold (multiplicity) is exceeded. The current sum of each 4532 is available on two bridged outputs than permit daisy chaining of several modules. This feature extends the useful number of input sums by 32 inputs per daisy-chained module. For dynamic sampling, the analog output may be connected to an input of the Model 4504 Flash ADC. This unit provides a 4-bit digital output useful for trigger processing circuits.

The status of up to 32 inputs can be monitored and recorded by issuing a strobe. Since the inputs are edge-triggered, the strobe may be a gate of arbitrary duration. Then any inputs which are on during any portion of the gate are recorded and stored in a pattern register. The pattern register can then be read by computer via CAMAC. Alternatively, the 4532 can operate in Overlap Mode where the input pattern is not latched, and the outputs follow the inputs dynamically.

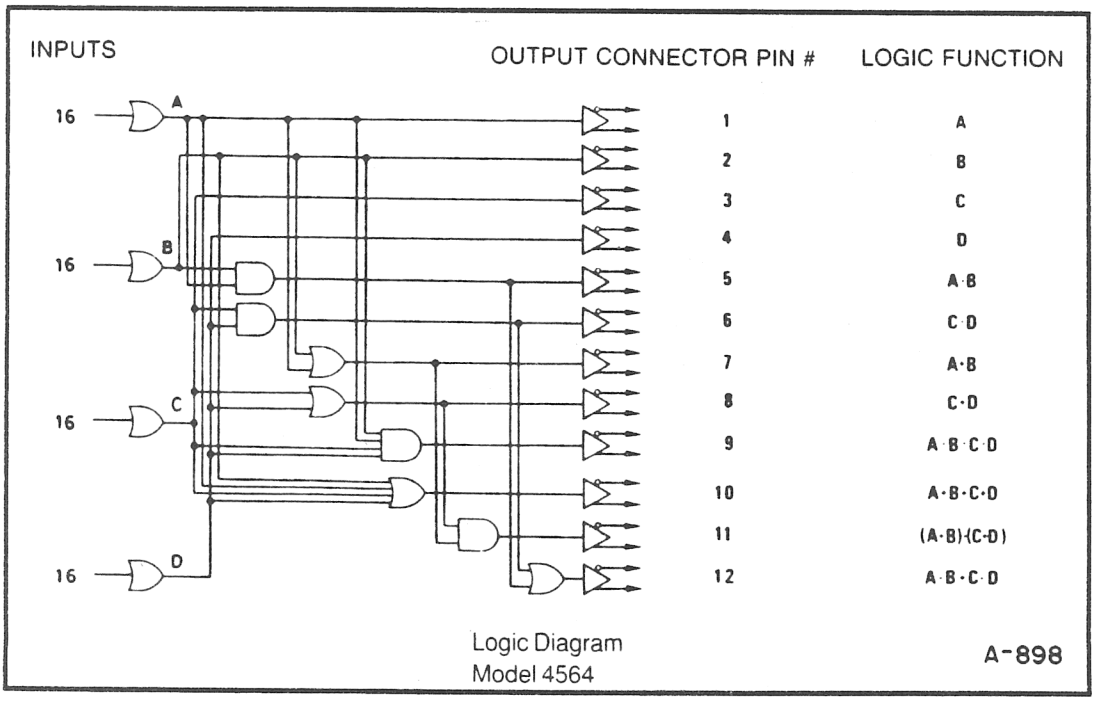
Other features of the Model 4532 are fast OR'ing of adjacent inputs, cluster mode operation, and provisions for cascading several 4532s for use in large detector arrays. Sixteen front-panel outputs give a fast OR output of inputs 1 and 2, 3 and 4, etc. These outputs reduce the number of signals that a second level trigger processor must view, while still maintaining a segmented set of signals. Next, in Cluster Mode, the 4532 will assume that adjacent hits indicate a single event and present only a single increment to the current output. This feature is useful in wire chambers where the close wire spacing often results in two or more adjacent wires giving signals from a single track. Finally, there is a provision for cluster Carry In and Carry Out to permit cascading several modules and permit cluster mode operation across module boundaries.

Model 4564
16 to 64 Fold OR Logic Unit

The Model 4564 is a simple and versatile logic module. It consists of four groups (A,B,C and D) of 16 input OR's followed by a set of additional 2 fold and 4 fold OR and AND functions. These various logic outputs, shown pictorially below, are simultaneously available on a rear - panel connector and the transit time is independent of the function. In addition, the outputs are capable of rates in excess of 100 MHz. Output width is dependent on the input pulse overlap.

For greater flexibility, the 4564 also offers four discriminator/ shaper channels. Internal jumpers allow any of the 12 logic combinations to be input to these channels. The output of discriminators/shapers can be triggered on the leading or tailing edge of the input (jumper selectable) and the width is adjustable from 15 nsec to greater than 500 nsec. Output polarity is also selectable via internal switches. These outputs can be used simply as an adjustable width logic fan-out or can allow for more sophisticated functions.

A typical application of the 4564 is to perform a simple track or pattern recognition for Veto or gate applications.



Logic Diagram
Model 4564

A-898

SPECIFICATIONS

Model 4418
Programmable Logic Delay/Fan-Out

Inputs: 16, DC coupled 100 Ω impedance, on 34-pin header for ECL signals. 100 MHz maximum rate (>35 MHz for Long Range Option), <10 nsec double pulse resolution (<30 nsec for long range option). Minimum width: 5 nsec.

Delay: 15-30 nsec in 1 nsec steps (4418/16), 15-45 nsec in 2 nsec steps (4418/32),15-135 nsec in 8 nsec steps (4418/128): Long Range Option. Delays set by computer for each channel individually.

Outputs: Three for each input, on three 34-pin headers, for compatibility with complementary ECL devices. Width equal to input duration ±1.2 nsec (±4 nsec Long Range Option). Risetime and falltime: 2.5 nsec.

Battery Back-Up: Preserves stored delays for at least 2 hours in the event of power loss.

Crosstalk: Synchronous pulses in adajcent channels can be affected by ±1 nsec typical.

Power: +6 V/50 mA, –6 V/2.5 A (15.3 W total)

Model 4504
Flash ADC

Inputs: Four on coaxial connectors, 50 Ω impedance, 10 nsec minimum width. Analog input range user defined between –2.5 V and +2.5 V. Range, set by computer command by giving low and high voltage reference levels, is divided by 15 to obtain resolution (4 bits).

Strobe: One ECL input for external strobe selected by front-panel switch. Leading edge initiates digitizing of all four inputs simultaneously; falling edge transfers digitized values to outputs and holds until next strobe. Maximum frequency 100 MHz. Alternate switch setting provides internal 20 MHz-100 MHz free-running strobe. Internal strobe frequency set by front-panel adjustment.

Veto: One ECL input inhibits strobe signal.

Outputs: Four, 4-bit ECL outputs on 8-pin headers. Overflow bits provided on 4 two-pin headers.

Strobe Out: Two on two-pin headers (ECL pulses) and two on Lemo connectors (–600 mV pulses) timed with digital outputs for downstream logic. Width is adjustable by front-panel potentiometer in the range of 5 to 25 nsec.

Test Points: Two front-panel test points permit measurement of voltage reference levels.

Input-Output Delay: Strobe trailing edge to digital outputs, typically 15 nsec.

Power: +6 V/1.1 A, –6 V/1.5 A, +24 V/6 mA (15.7 W total)

Model 4508
Memory Lookup Unit

Inputs: Two, 8-bit inputs on 34-pin header, 100 Ω for complementary ECL. Minimum width 10 nsec, maximum rate 65 MHz.

Strobe: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width and must precede input by 2 nsec for exact time coincidence. Latches inputs, except in overlap mode. Maximum frequency >65 MHz. Strobe must be followed by clear except in Overlap Mode.

Clear: Two on Lemo connectors, one per input section, 50 Ω impedance. Requires –600 mV signal, 5 nsec minimum width to clear. Clears pattern register and resets outputs in all modes.

Outputs: Two, 8-bit outputs on 34-pin headers, ECL signals. Width of output in Shaped mode set by front- panel adjustment between <5 nsec to >100 nsec.

Synchro Output: Two on Lemo connectors, one per output section, 50 Ω impedance. Supplies –600 mV pulse out when outputs are ready. Typically used for strobing next unit, or for self-clearing.

Modes: Overlap (OVL) - Output pulse width determined by coincidence between Inputs and Strobe.

Shaped (SHP) - Output pulse width is determined by a front - panel adjustment from <5 to >100 nsec. The unit must be cleared before another input can be latched.

Continuous (CNT) - Output state is latched by the Strobe, until a Clear is applied.

Propagation Delay: (17 ±3) nsec in Overlap Mode. In other modes (21 ±1) nsec independent of logic function and determined by Strobe timing.

Power: +6 V/0.5 A, –6 V/2.6 A (18.6 W total)

Model 4516
Programmable Logic Unit

Inputs: 16 sets of three inputs, 100 Ω (high impedance by removal of socketed terminators), DC coupled, on 34-pin headers, for ECL signals, minimum 2 nsec risetime. Maximum rate 150 MHz.

Veto: One rear-panel Lemo connector, 50 Ω impedance. Requires –600 mV signal. Permits gating of outputs, including OR outputs. Must overlap coincidence for the three front-panel inputs by >5 nsec.

Outputs: 16, one per set of three inputs, complementary ECL logic levels on 34-pin header.

OR Out: Two, one for OR of first 8 outputs, one for second 8 outputs (factory option permits OR'ing of all 16 outputs).

Double Pulse Resolution: 5 nsec at minimum input width.

Coincidence Width: >3.5 nsec determined by input pulse width.

Input-Output Delay: A or B to OUT by 11 nsec typ.; A or B to OR by12 nsec, typ.; C to OUT by 8 nsec, typ.; C to OR by 9 nsec typ.; VETO to OUT by 8 nsec typ.; VETO to OR by 6 nsec typ.

Power: +6 V/50 mA, –6 V/1.25 A (7.8 W total)

Model 4532
Majority Logic Unit

Input : All inputs accept differential ECL level (–0.8 V, –1.7 V) into 110 Ω input impedance (high input impedance is possible by removing socket-mounted terminators).

Data Input (IN): 32 in two 34-pin front-panel connectors; minimum input pulse width 6 nsec.

Reset Input (RTI): Fast reset of the input registers; generates a reset of the analog majority output and of the comparator outputs (MDO, DMO). When the analog output is cascaded with other units, the RTI resets only the contribution from the modules that received the RTI. Minimum input pulse width 6 nsec, maximum width DC. In Memory Disable mode, the RTI is inhibited.

Gate Input (GAI): Normally open when unconnected. Normally closed when connected to a cable providing standard ECLine levels. In Memory Disable Mode, data pulses having an overlap with the GAI will contribute to the outputs. In Memory Enable Mode, data pulses having their leading edge inside the GAI time will be accepted and stored. By deriving the GAI from the DMO, an internally generated time window is possible. Minimum overlap time width with input pulses for majority decisions, 10 nsec. Minimum overlap time width with input pulses for logical OR's, 3 nsec, maximum width DC.

Cluster Carry (CCI): When Cluster Selection is Enabled, receives the carry information on the cluster from the Cluster Cary Output (CCO) of any adjacent majority logic unit.

Analog Majority Inpt/Output (AMIO): High impedance current source; AMIO connectors can be used for daisy chaining of analog majority information within a unit. Transit time between AMIO connectors 2 nsec. Unused output must be terminated with 50 Ω.

Output: All logic outputs provide complementary ECL levels (–0.8 V, –1.7 V) and are capable of driving differential 110 Ω loads.

Data Outputs (OUT): 16 in a 34 pin front-panel connector. In Memory Disable Mode, provides pulses corresponding to an overlap coincidence between the gate pulse and the data inputs. In Memory Enable Mode, provides levels started by the coincidence between the gate pulse and the leading edge of the data pulses.

OR Output (ORO): Provides the logical OR of the 32 channels, otherwise behaves as data outputs.

Strobe Output (STO): Provides a pulse, suitable for strobing of subsequent logic units, at the end of the gate input and delayed by the internal transit time (6 nsec). Width adjustable from 10 to 25 nsec by a trimmer (STROBE WIDTH) accessible from the side of the module.

Majority Discriminated Output (MDO): The AMIO input/output is internally used as input to an adjustable threshold comparator providing the MDO output. Threshold adjustable from 1 to 16 hits by a front-panel potentiometer (MA THR). The output will be a pulse or a level depending on the selected operating mode.

Delayed Majority Output (DMO): Reproduces the output MDO above, after an adjustable delay. A switch on the side of the module (DM RANGE) selects one of two delay ranges; 10-100 nsec or 50-1000 nsec. A front-panel potentiometer (DMO DELAY RANGE) permits continuous adjustment. The DMO is cleared as soon as the MDO is cleared.

Cluster Carry (CCO): When Cluster Selection is Enabled, indicates that Output channel 32 was hit for use in conjunction with channel 1 of a logically adjacent cluster logic in another 4532 module (CCI) input.

Mode Selection: A Memory Enable switch, accessible on the side of the module, selects one of the following modes: Memory Disable - Functions are disabled; the multiplicity calculation is performed on theoverlap of the data inputs. Memory Enable - The data inputs are latched; the multiplicity is determined by the number of leading edges of data input pulses occurring during the gate time. In this mode the unit needs to be cleared either by the reset input (RTI) or by a resetting function.

Cluster Slection: The Cluster Enable switch, accessible on the side of the module, determines one of the two following modes: Cluster Disable - Each data input provides one hit on the Analog Majority Output AMIO; the Cluster Carry Input (CCI) is disabled; Cluster Enable - Any group of adjacent input data pulses will be considered as a single hit. Provision has been made for the clusters to extend beyond the 32 inputs. If an input is present on the logically adjacent channel to input 1 of this unit but is located in another unit, the CCI can be used to indicate its presence. The CCO of this module indicates that channel 32 of this module is present.

Input-Output Delay: Data IN to AMIO - 16 nsec; AMIO to MDO output - 5 nsec; End of gate IN to Strobe OUT by 6 nsec; Data IN to Data OUT by 12 nsec; Data IN to OR OUT by 16 nsec; Reset IN to Data OUT by 20 nsec; Reset IN to OR OUT by 24 nsec; Data IN 32 to Cluster Carry OUT by 11 nsec; Cluster Carry IN to Data IN 1 by 2 nsec. Gate pulse must precede Data pulse by at least 7 nsec.

Power: +6 V/200 mA, –6 V/<3.6 A, +24 V/ 5 mA, –24 V/7 mA (23 W total).

Model 4564
16 to 64 Fold OR Logic Unit

Inputs: 64 in four 2 x 17 front-panel connectors, 110 Ω impedance. Minimum width 6 nsec, maximum frequency >100 MHz.

Overlap Outputs: Rear-panel 2 x 17 pin connector, pins 1 to 12, ECL signals. Width corresponds to overlap (±2 nsec) of inputs of logic function, minimum output 5 nsec, maximum output frequency >100 MHz; transit time 12 nsec ±1 nsec typical, independent of logic function; double pulse resolution 10 nsec typical.

Shaped Outputs: Rear-panel connector pins 13 to 16, any of overlap logic can be converted via jumper option to any of the four discriminator/shapers, output is differential ECL levels and width is internally adjustable from 15 to >500 nsec, can be triggered in leading or trailing edge of inputs (jumper selectable); output polarity internally switch selectable; maximum frequency: 30 MHz, double pulse resolution: 33 nsec.

Power: +6 V/150 mA, –6 V/1.5 A, –24 V/20 mA (10.4 W total)

CAMAC COMMANDS, FUNCTION CODES AND RESPONSES

Model 4418 Programmable Logic Delay/Fan-Out

F16•(A0 to A15):	Load delay time setting on write lines W1 to W4. One subaddress for each channel.
X, Q:	An X and Q response are generated when a valid N, A, F command is recognized.

Model 4504 Flash ADC

F(0)•A(0):	Read digital outputs; R1 to R16, 4 bits per channel.
F(0)•A(1):	Read digital overflow, R1 to R4, 1-bit per channel.
F(16)•A(0):	Write Low Reference Voltage (VL) on 8 bits; range from –2550 mV to +2250 mV in steps of 20 mV.
F(16)•A(1):	Same as above but for the High Reference Voltage (VH).
F(25)•A(0,1):	Equivalent to C.
C:	Generates a strobe during S2 time. This function is not affected by I or VETO input and may be disabled by a side-panel switch. The digital outputs will be set depending on the analog value of the inputs; in particular, if the inputs are disconnected all the digital outputs will correspond to 0 V at the inputs. The output logic state will be determined by the VL and VH reference voltages.
I:	Inhibit strobe.
X, Q:	X=1 and Q=1 responses are generated for any of the above functions.

Model 4508 Programmable Lookup Unit

F(0)•A(0):	Read first section 8-bit input pattern.
F(0)•A(1):	Read second section 8-bit pattern.
F(0)•A(2):	Read first section memory content at the given address; the memory content is displayed on read lines R1-R8, the given address on read lines R9-R16.
F(0)•A(3):	As F(0)•A(2) but for the second section.
F(2)•A(0):	Read first section 8-bit pattern and reset at S2; reset output levels when operating in continuous mode.
F(2)•A(1):	Same as F(2)•A(0), but for the second section.
F(2)•A(2):	Read first section memory content at the given address (as for F(0)•A(2)) and increment address by one at S2.
F(2)•A(3):	Same as F(2)•A(2), but for the second section.
F(9)•A(0):	Clear first section pattern; reset first section output levels when operating in continuous mode.
F(9)•A(1):	As above, but for the second section.
F(9)•A(2) or F(9)•A(3):	Reset memory address in both sections.

F(16)•A(0): Load first section memory content at the given address; data have to be sent on write lines W1-W8;
F(16)•A(1): As above, but for the second section.
F(16)•A(2): Random access to the first section memory (the selected address has to be sent on write lines W9-W16); load memory content with data present on W1-W8, at the selected address.
F(16)•A(3): Same as above, but for the second section.
F(18)•A(0): Load first section memory content, at the given address, with data present on W1-W8; increment address by 1.
F(18)•A(1): As above, but for the second section.
F(18)•A(2) or F(18)•A(3): Load the memory's address register (this address has to be sent on write lines W9-W16).

Z or C: The address register for the memories of both sections is set to 0; pattern registers are cleared.
X: An X=1 response is generated for any valid CAMAC function.
Q: A Q=1 response is generated for any valid CAMAC function, except when the memory addresses overflow. (This latter feature permits one to recognize when the reading or the loading of a memory has been completed).

Model 4516 Programmable Logic Unit

F(26)•A(0): Sets all C0's to AND Mode.
F(24)•A(0): Sets all C0's to OR Mode.
F(26)•A(1): Sets all C1's to AND Mode.
F(24)•A(1): Sets all C1's to OR Mode.
F(27)•A(0): Gives a Q response if C0 switch is in AND Mode.
F(27)•A(1): Gives a Q response if C1 switch in in AND Mode.

X: An X response is generated when a valid N, A, F command is recognized.
Z: Sets all channels to OR Mode.

Model 4532 Majority Logic Unit

F(0)•A(0), A(1): Read input pattern. A(0): channels 1 to 16. A(1): channels 17 to 32. A Q response is generated in Memory Enable Mode only.
F(1)•A(0): Read status register; R1 = 1 if LAM isON; R2 = 1 if LAM Enable switch is ON; R3 = 1 if MEMORY Enable switch is ON; R4 = 1 if CLUSTER Enable switch is ON. Q response is always generated.
F(2)•A(0): Read input pattern, channels 1 to 16. Q response is generated in Memory Enable Mode only.
F(2)•A(1): Read input pattern, channels 17 to 32, and clears the 32-channel memory and LAM at S2. Q response is generated in Memory Enable Mode only.
F(8)•A(0): Test LAM; a Q response is generated if L is ON.
F(9)•A(0): Clears the data memory and LAM.
F(10)•A(0): Test and clear LAM, clears LAM . Q response is generated if L is ON. The clear LAM operation is not executed if Q response is missing.

Z, C: Clears data memory and LAM .
L: A Look-At-Me signal is generated (in Memory Enable Mode only) at the end of the gate input if the OR output is set. The LAM may be enabled or disabled by the LAM enable switch accessible on the side of the module.
X: An X=1 response is generated for any executable function.
Q: A Q=1 response is generated for any executable function in Memory Enable Mode only.

Model 4564 OR Logic Unit - The Model 4564 does not utilize CAMAC Commands or Function Codes.

1. INTRODUCTION

The CAMAC model 4418 is basically a delay for digital signal characterized by programmability, high density, high speed operation and high fan-out.

The unit is conceived as sixteen identical channels, each of them accepting one input and providing three outputs.

Programmability concerns the possibility of selecting the required delay value per channel. Even if the basic module features a time span of 30 nsec and 16 delay steps of 2 nsec, other time spans can be provided on customer request; i.e.,

15 nsec in steps of 1 nsec;

120 nsec in steps of 8 nsec.

The last time span was not included in the original data sheet, it has been introduced indeed only later.

2. CIRCUIT DESCRIPTION

Looking at the detailed circuit diagram, the following should be noted.

The differential ECL input pulses are terminated 2 X 56 resistors. These resistors are mounted on SIL sockets and they can be easily removed then if high input impedance is desired.

The input pulses are then received by a line receiver 10115 the output of which, after an interconnection by twisted-pair cables, goes in parallel to two AND gates 10104. Only one of these two gates at a time is enabled so that the incoming pulse is either sent to the beginning of the following delay line (pin 2) or to its middle point (pin 10).

The choice of the delay is made setting 4 bits, out of which three are used to set one of 8-line multiplexer (10164) and the last one (MSB) to choose the origin of the delay line.

The 4 bits for delay are set via CAMAC and stored in a MOS memory (74C173). Due to the low power consumption of this memory, the memory contents can be kept for a few hours also in case of power failure. In that case indeed and for the time specified, the power is provided by the set of capacitors in parallel to the -M voltage.

3. TIMING CONSIDERATIONS

Besides the programmable time span, a channel presents a constant input to output delay which has to be always added. This constant delay is slightly dependent from the particular channel and from the particular output chosen and it is Tc = (15±1) nsec.

Even if the output timing is guaranteed to be a monotonic function of the programmed step, though the user should be aware of the possible non-linearity.

The following table summarizes the main timing characteristics:

MODEL	FULL RANGE FR (nsec)	STEP (nsec)	STEP PRECISION	OUT WIDTH DISPERSION (±) (nsec)	MAXIMUM FREQUENCY (MHz)
4418	15±1	1	FR/15±300 psec	1	100
4418/100	30±2	2	FR/15±500 psec	1.2	100
4418/200	37.5±2.5	2.5	FR/15±600 psec	1.2	100
4418/300	120±8	8	FR/15±2.5 nsec	4	35

The following remarks apply:

- The quoted non-linearity has two components, the first one reflects a systematic uncertainty due to the precision in manufacturing, the second one expresses the random uncertainty on each step.

- The output width dispersion reflects on the contrary the degradation of rise and fall time of pulses traveling into the delay lines. The width variation will be then more apparent for longer delay.

- Another effect which can influence the fixed delay, is the crosstalk mainly provocated by adjacent channels. This effect is in principle independent from the particular delay range, because it is due to the geometrical properties of the printed board. This effect has been measured to be typically of the order of ±1 nsec.

POSSIBILITY OF CASCADING MODULES

All differential ECL inputs, in ECLine modules, are terminated inside the module by two 56 Ω resistors to VBB, realizing a differential matching impedance of 112 Ω.

The input terminations are included in socket mounted, single in line resistor arrays, which can be removed if more than one unit have to be cascaded on the same driving cable. In this case, only the last unit in the daisy chain must be terminated for proper operation. (For more details see also the ECLine Application Note).

Figures below show the standard input stage of an ECLine module and the lay-out on the board.

WARNING: The resistor arrays are not symmetrical and they must be mounted in the proper way.

ECL CABLES

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twisted-pair cables for one-to-one connection.

Such interconnecting cables can be purchased from LeCroy and in particular, as multiwire cables. Two types are available, one for short connections using just flat cable, the second one for long interconnections using twisted and flat ribbon cable.

The denomination of such cables is as follows:

- STC-DC/34-LL Multiwire cable for short interconnections
- LTC-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twisted-pair cable.

Where LL is the cable length in feet which should be specified by the customer.

TECHNICAL INFORMATION

(SCHEMATICS, PARTS LISTS)

FIS/NCA V4.3A
ZZBPSS.NCA;
ZZIPMS.NCA;

LECROY CORPORATION
4418 PARTS LIST

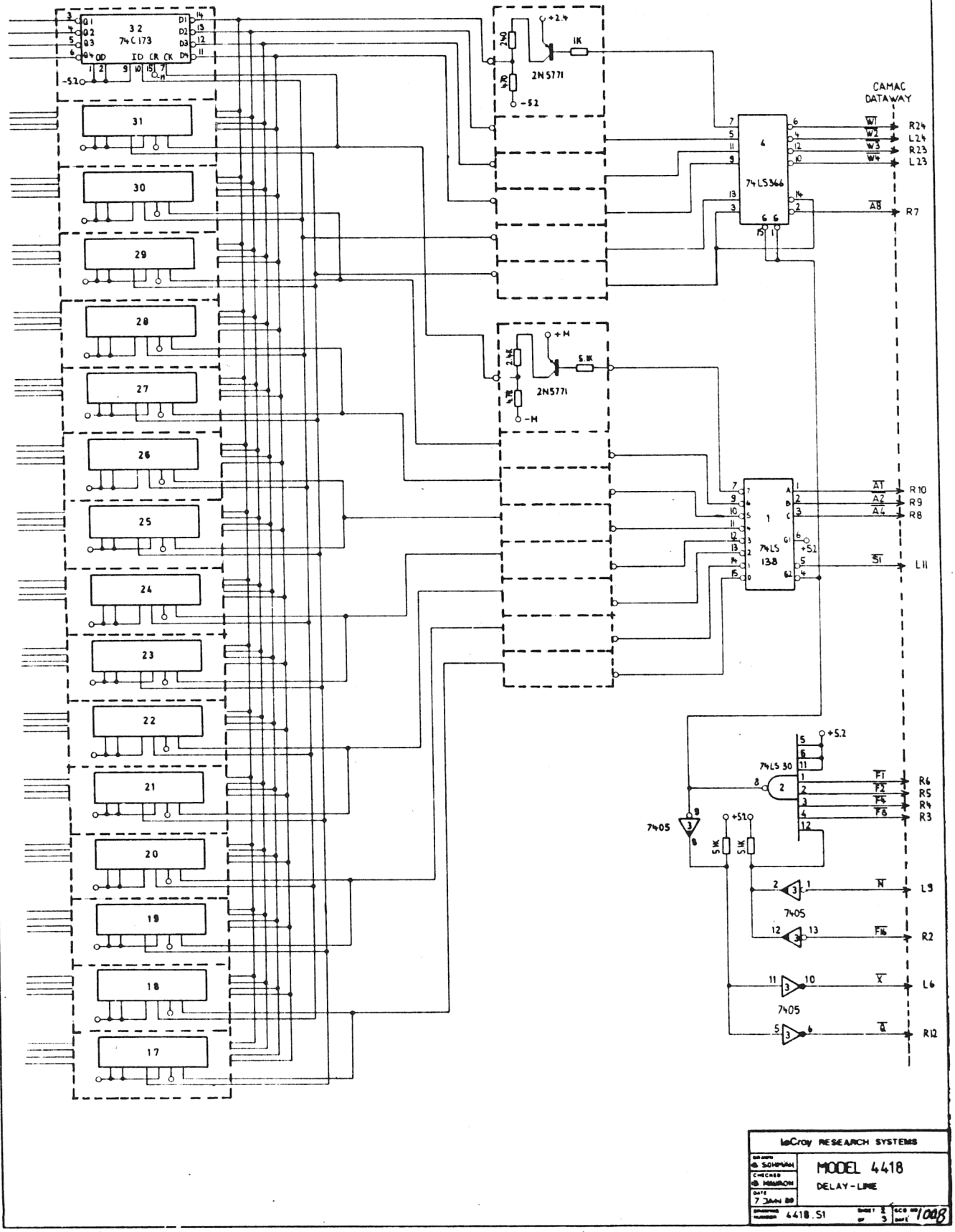
PART NUMBER	DESCRIPTION	QUANTITY PER
102412068	CAP CERA DISC 100V 6.8 PF	48
102412180	CAP CERA DISC 100V 18 PF	16
103327103	CAP CERA MONO 50V .01 UF	74
142124476	CAP TANT DIP CASE 47 UF	5
142824685	CAP TANT DIP CASE 6.8 UF	5
161335102	RES CARBON FILM 1 K	24
161335103	RES CARBON FILM 10 K	18
161335111	RES CARBON FILM 110 OHMS	16
161335123	RES CARBON FILM 12 K	1
161335152	RES CARBON FILM 1.5 K	2
161335220	RES CARBON FILM 22 OHMS	2
161335241	RES CARBON FILM 240 OHMS	6
161335242	RES CARBON FILM 2.4 K	8
161335300	RES CARBON FILM 30 OHMS	1
161335471	RES CARBON FILM 470 OHMS	7
161335472	RES CARBON FILM 4.7 K	8
161335511	RES CARBON FILM 510 OHMS	2
161335512	RES CARBON FILM 5.1 K	10
161335514	RES CARBON FILM 510 K	1
161335750	RES CARBON FILM 75 OHMS	32
181457201	RES VARI CERMET 200 OHMS	1
190042222	RESISTOR NETWORK 2.2 K	1
190042471	RESISTOR NETWORK 470 OHMS	8
190042560	RESISTOR NETWORK 56 OHMS	2
190842222	RESISTOR NETWORK 2.2 K	1
190842471	RESISTOR NETWORK 470 OHMS	6
190842560	RESISTOR NETWORK 56 OHMS	2
200031021	IC HEX INVERTER SN7405N	1
200031052	IC 8-INPUT NAND SN74LS30N	1
200041045	IC BUFFER DM74LS366N	1
200041062	IC DEC/DEMULTP SN74LS138N	1
204042003	IC LINE RECEIVER MC10115P	4
204042012	IC 2-IN AND GATE MC10104P	8
204042016	IC 2-INPUT OR/NOR F10101P	12
204042164	IC 8-LINE MPLX MC10164P	16
206043173	IC D-TYPE FL-FL MM74C173N	16
230110005	DIODE SWITCHING 1N4448	1
235010005	DIODE RECTIFIER 1N4005	1
235050001	DIODE RECTIFIER 1N4139	1
253010835	DIODE HOT CARRIER HP2835	2
270170001	TRANSISTOR NPN 2N5770	18
275170002	TRANSISTOR PNP 2N5771	17
276150194	TRANSISTOR PNP 2N5194	1
290110016	DELAY LINE 16 N-SEC	16
300050001	CHOKE FERRITE SINGLE LEAD	2
400000316	SOCKET IC OPEN FRAME 16	16
403119234	HEADER RT ANGLE 34-PIN	4
405812002	SOCKET STRIP SOLDR 20 POS	3
433220001	FUSE PICO II 125V 10 AMP	1
433221004	FUSE PICO II 125V 1 AMP	1
454310002	HDR DIP SOLD TO PC BD 2	22
454311008	HDR MALE PIN TO WW 8	4
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1

FIS/NCA V4.3A
ZZBPSS.NCA;
ZZIPMS.NCA;

LECROY CORPORATION
4418 PARTS LIST

PART NUMBER	DESCRIPTION	QUANTITY PER
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209001	REAR PANEL CAMAC SIZE #1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
564440004	SCREW ROUND PHIL 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
591023030	WIRE TWIST BLK/RED AWG 30	30
714418003	PC BD PREASS'Y 4418	1
724418003	FRONT PNL PREASS'Y 4418	1
734418003	SIDE ECLINE LEFT 4418	1

End of report. 67 Details encountered.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+M
2.2K
5.1K
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CAMAC
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W4
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A4
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R9
R8
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S1
L11
74LS 30
F1
F2
F4
F6
R6
R5
R4
R3
7405
5.1K
5.1K
+5.2
N
L9
F16
R2
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LeCroy RESEARCH SYSTEMS
G. SOMMAN
MODEL 4418
DELAY-LINE
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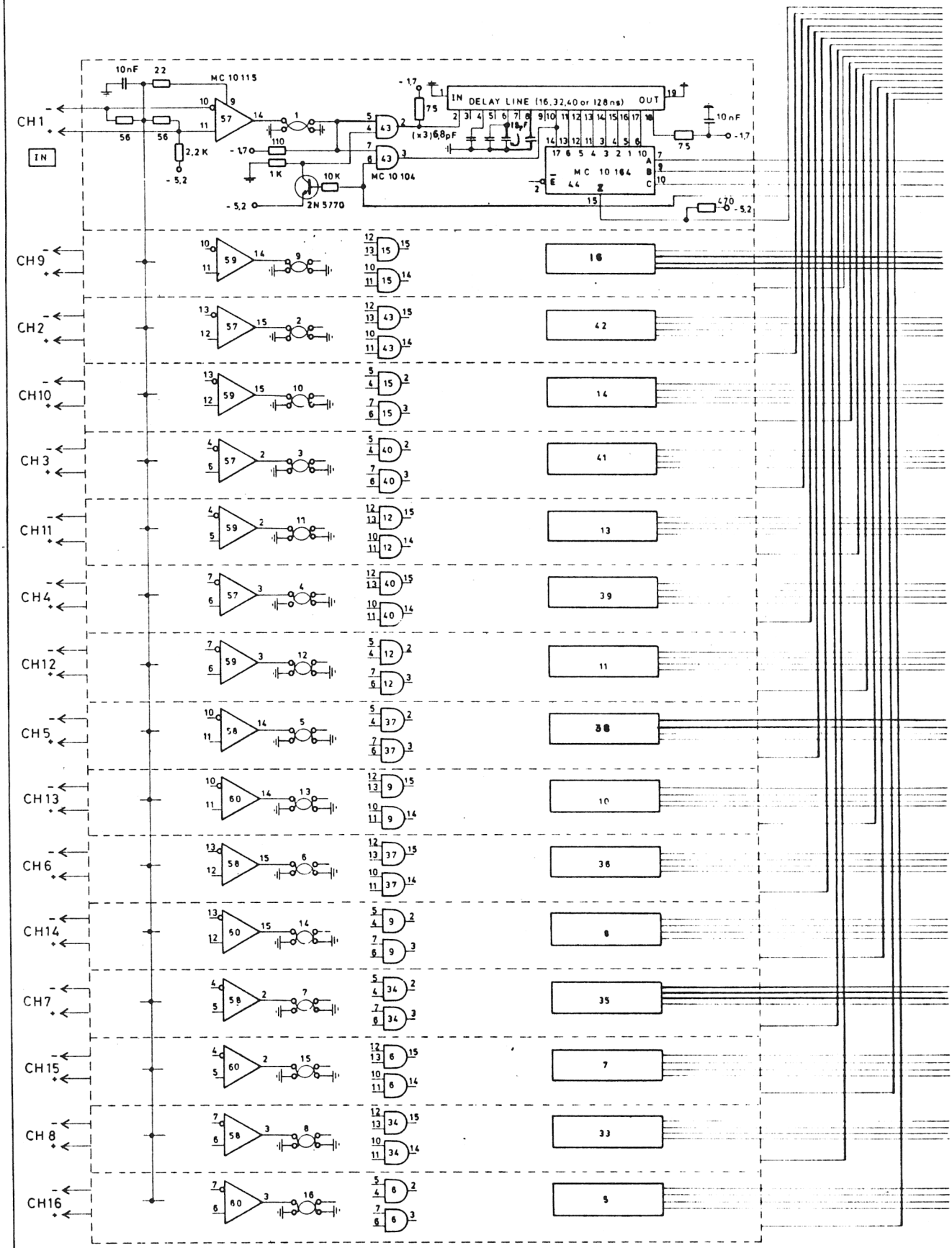

LeCroy RESEARCH SYSTEMS

DRAWN P.DAMIANO	MODEL 4418
CHECKED B.MAURON	DELAY-LINE
DATE 5 MARS 81	
DRAWING NUMBER 4418-SI	SHEET 1 OF 3
ECO # DATE	1003

DEVICE	DESIGNATION	+5.2	GND		-M	-5.2
74 05	3	14	7			
74 LS 30	2	14	7			
74 LS 138	1	16	8			
74 LS 366	4	16	8			
74 C 173	17 32		16		8	
MC 10 101	45 - 56		1, 16			8
MC 10 104	6 9 12 15 34 37 40 43		1, 16			8
MC 10115	57 58 59 60		1, 16			8
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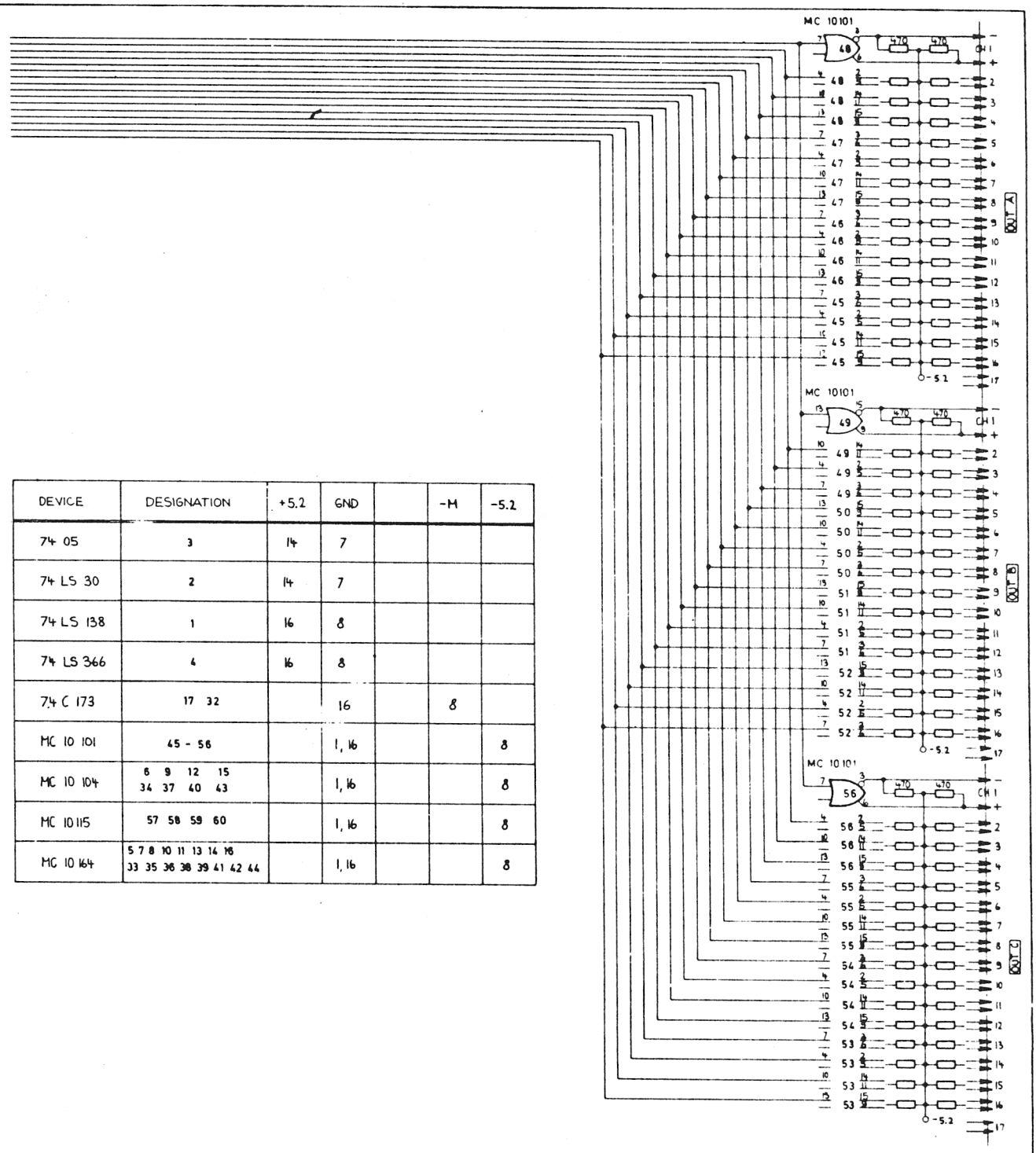

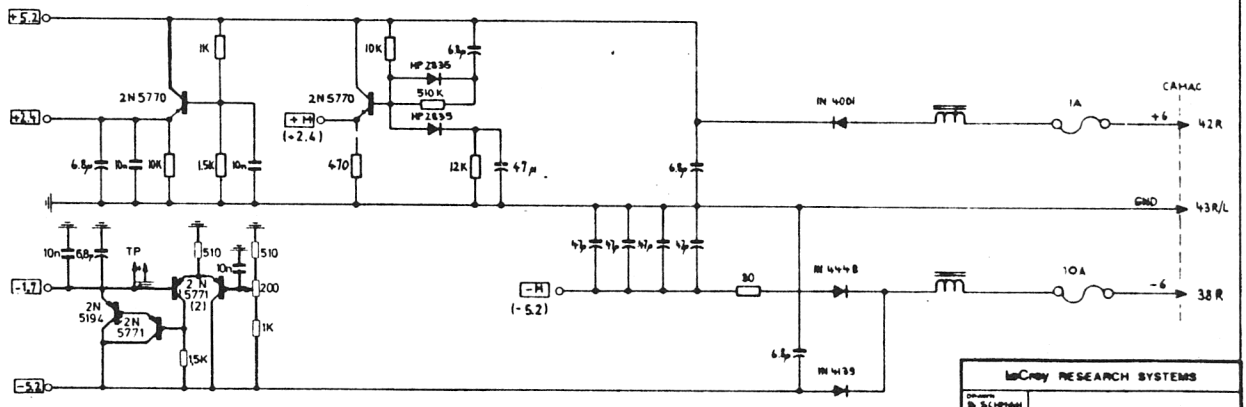

LeCroy RESEARCH SYSTEMS

MODEL 4418
DELAY - LINE

4418 - S1

7008