CAMAC MODEL 4434
32-CHANNEL, 24-BIT SCALER

USER'S MANUAL

November 1982

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF THE UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

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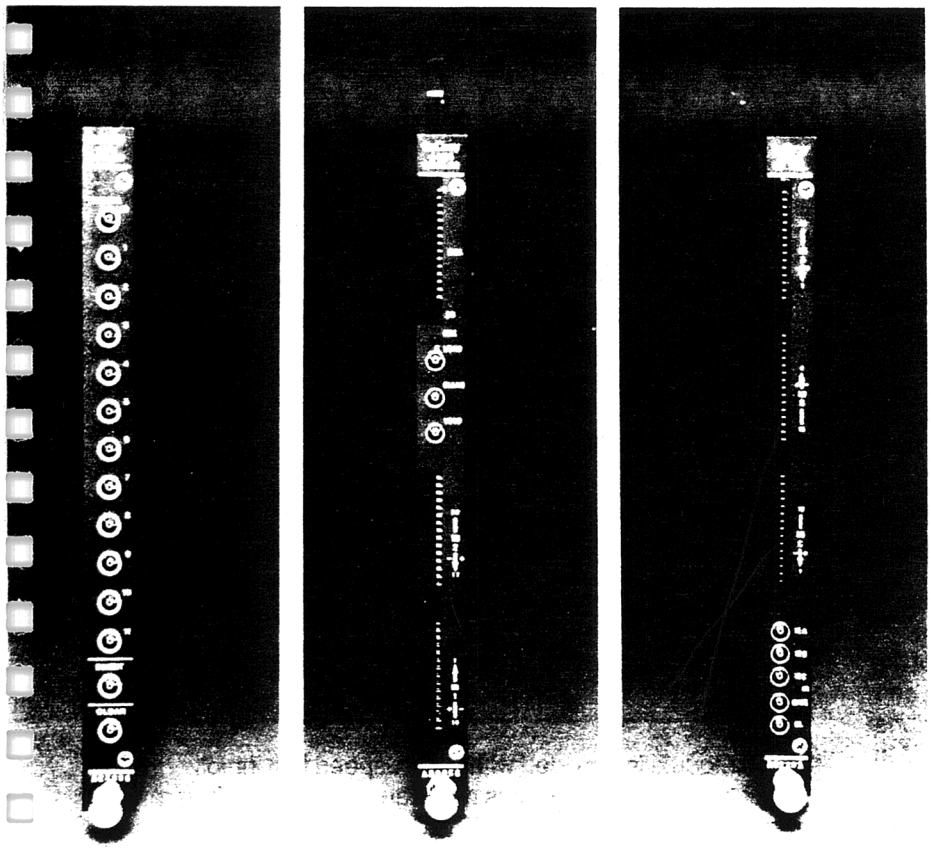


- **CAMAC Packaging**
- **NIM, TTL, and ECL Level Compatibility**
- **High Data Rate for Fast Counting**
- **High Capacity and Density**
- **Control via CAMAC or External Signals**

COUNTING AND REGISTRATION OF LOGIC PULSES

Scalers and latches are data acquistion units that register logic pulses received during a given period. These logic pulses are often generated by discriminators whose function is to output a pulse when an analog signal exceeds a given threshold or level of interest. However, scalers and latches can also be used with other logic modules, including coincidence units, to count or register the number of simultaneous pulses.

Scalers such as the Models 2551 and 4434 count the input signals during an active period. Latches, on the other hand, are data acquisition units that record logic levels ("hit patterns") coincidence with a gate pulse. The Model 4448 Coincidence Register is a latch with 48 inputs and can be used in fast trigger applications.

FEATURES

Conforms to CAMAC Standards - Each of the three units is packaged in single width CAMAC (IEEE-583) modules which offer the highest level of versatility and flexibility in configuring a system while fulfilling the requirements of the specific application.

Accepts Various Inputs - Input to the scalers can be at least one of three common logic pulse formats. This flexibility ensures compatibility with most data collection systems. The Model 2551 accepts NIM level inputs, the 4448 accepts ECL and the 4434 accepts ECL levels or TTL (factory option).

High Counting Rate - The scalers are designed for high counting rate capability to limit data loss. The 2551 exhibits 100 MHz counting rate while the 4434 has >30 MHz instantaneous rate.

High Density - Each unit allows multiple inputs which reduces the physical size and cost of most setups. The Model 2551 has 12 inputs, the 4434 has 32 inputs and the 4448 has 48 separate inputs.

FUNCTIONAL DESCRIPTION

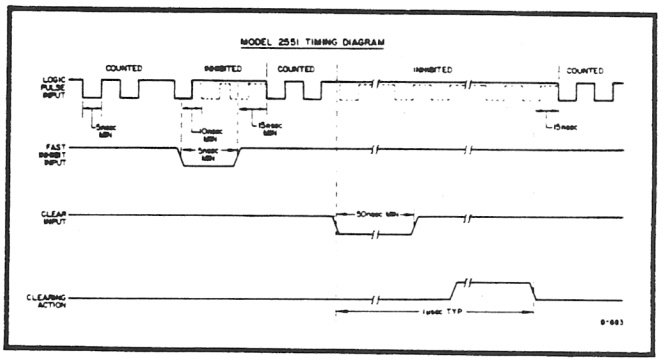
SCALERS AND COUNTERS

Both non-latching (Model 2551) and latching scalers (Model 4434) record the number of input pulses. However, latching scalers can internally store the number of counts for each channel in a buffer. This buffer is independent of the input and can be read out during data collection. In either case, the active duration of the scaler can be a fixed or variable interval depending on the actual application. For example, some applications require data to be collected for a preset time interval. In other cases, the scalers are disabled by Inhibit pulses when certain predetermined conditions are ascertained by associated equipment.

Model 2551 12-Channel Scaler

The LeCroy Model 2551 contains 12 identical 24-bit binary scalers especially designed for use in high speed counting applications. This high performance unit has a capacity of 16,777,215 counts in each of its 12 channels and is packaged as a single width CAMAC module. Added flexibility is provided by allowing cascading of even channels into odd ones by the use of internal jumpers to produce a 48-bit count capacity for up to a total of six channels.

Each scaler is equipped with an extremely wideband input circuit which responds to NIM level logic signals of any duration down to 5 nsec, without multiple-pulsing (in case of wide inputs) and without counting down. The ability to recognize narrow input signals at an equivalent rate of >100 MHz is an important feature, since it assures that the scaler will accurately accumulate any output signal generated by standard discriminator and logic circuits.



Each module is provided with a high-speed fast inhibit which permits simultaneous rejection of input signals at a rate equivalent to 100 MHz. The CAMAC Inhibit (I) provides remote inhibit control from the data acquisition system. The inhibit signal must overlap the input signal, but toggling the inhibit will not cause pulses to be counted.

Fast rejection of unwanted data is provided by the fast clear input. This input allows the entire scaler to be reset by application of a NIM level clear pulse without the need to perform any dataway operations.

The Model 2551 has a built-in test circuit which allows all registers to be checked simultaneously. Application of the CAMAC Increment F(25) Function Code causes each scaler to advance by one count for each S2 timing signal received. The test circuit may be used without disconnecting cables if the CAMAC Inhibit is on. The 24-bit data from any scaler is read in parallel to the common dataway via the rear card edge connector. Individual channel non-destructive readout is accomplished by generating a CAMAC Read F(0) and the appropriate address. Using Read and Clear F(2), the channels will be automatically zeroed after reading the last channel. Clear F(9), CAMAC Clear C, or Initialize Z will zero all channels.

Model 4434
32-Channel Latching Scaler

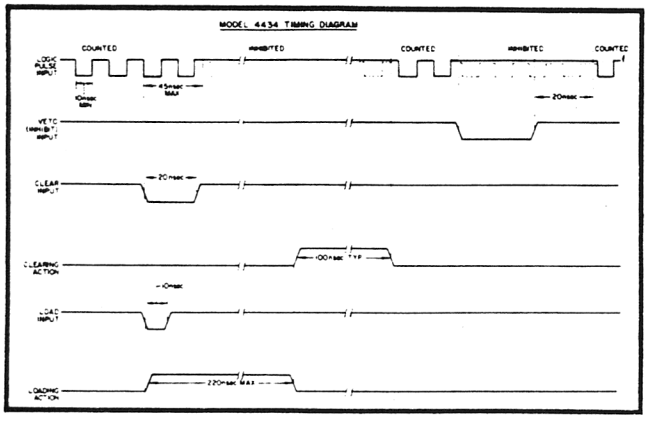
The LeCroy Model 4434 contains 32 channels of 24-bit scalers in a single width CAMAC module. Through the extensive use of LeCroy custom built hybrid circuits, the Model 4434 achieves a dramatic increase in channel density with a very low overall cost per channel.

Signal inputs to the 4434 are complementary ECL levels compatible with ECLine modules. Single ended TTL levels are available as a factory option. Each scaler counts logical signals which have a duration of >10 nsec and a maximum frequency of 20 MHz. The maximum instantaneous rate for the scaler is 30 MHz and a local double pulse resolution of 30 nsec is permitted.

Each channel in the module is followed by an internal buffer or latch which may be used to store and readout accumulated data independent of counting. This readout may take place at any time under standard CAMAC control or under an independent Auxiliary Data Bus control via the front-panel 34-pin connector. In either case, the readout can be performed sequentially or randomly.

LOAD, CLEAR and VETO/INHIBIT input commands can be sent over the CAMAC DATAWAY or via Lemo connectors on the front panel. A common side switch selects NIM or TTL input levels and impedances for the connectors. Test, unit initialize and other commands are available from CAMAC only.

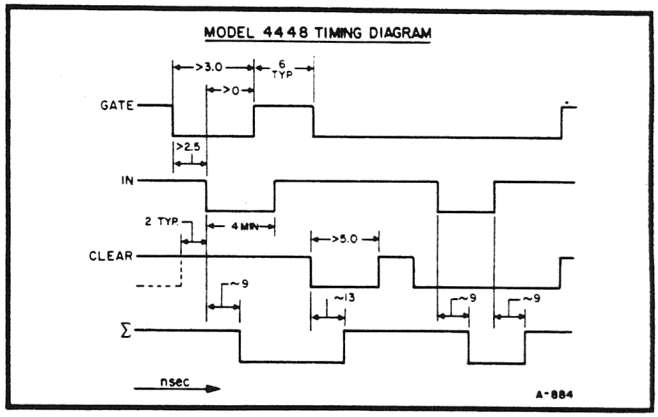
Receipt of a CAMAC or front-panel LOAD command temporarily halts all the scalers for approximately 220 nsec and transfers the contents to the internal buffer memory (see Timing Diagram). The scalers may then be optionally reset before counting is resumed with a CLEAR command. The duration of this action is approximately 100 nsec during which the module's inputs are disabled. During data acquisition, unwanted data is rejected for the duration of a front-panel VETO signal or CAMAC Inhibit command.



LATCHES
Model 4448 Coincidence Register

The LeCroy Model 4448 Coincidence Register is a latch unit offering fast storage capability at an unprecedented high density and low cost. Its complementary ECLine receiver input stage, compatible with inexpensive twisted-pair cable, makes it perfectly suitable for both small and large multi wire proportional chamber and hodoscope systems. The three fast analog outputs providing majority information are extremely useful in fast trigger decision applications.

The logic channels, which seek a coincidence between each input and a common fast gate input, provide coincidence resolving times under 3 nsec. Logical "1" data levels, representing the time coincidence between the common gate and the 48 inputs, are stored in a 48-bit fast buffer register for later readout under CAMAC commands. The facility of performing majority logic is provided by three front-panel summing outputs which are each driven by 16 logic channels. The output current of the summing circuit is proportional, in increments of 100 mV ±10% into 50 Ω per register bit, to the number of coincidences stored in the register.



A front-panel clear input allows NIM levels to clear all three register memories. However, if the clear signal is "True" during the signal input, the outputs of the register memory and analog sum correspond to the coincidence overlap. This feature permits this unit, in conjunction with a discriminator, to be used as a majority logic unit when its clear input is locked in the enabled state. In addition, clear for the three individual 16 input groups is provided via CAMAC.

Pattern information can help speed off-line data sorting and provide a mapping of zero-suppressed recorded data of the detector/sensors. The outputs of three Model 4413 discriminator modules, for example, could be latched into a single 4448. Large detectors arrays such as hodoscope or an MWPC could employ such a system since over 1100 inputs can be housed in a single CAMAC crate.

CAMAC COMMANDS, FUNCTION CODES AND RESPONSES

Model 2551 12-Channel Scaler

F(0): Read registers; requires N and A, A(0) through A(11) are used for channel addresses.

F(2): Read registers and Clear module and LAM; requires N and A (Clears on A(11) only).

F(8): Test Look-At-Me; requires N, and any A from A(0) to A(11) independent of LAM disable: Q response is generated if LAM is set.

F(9): Clear all scaler channels simultaneously; requires N, S2, and A from A(0) to A(11).

F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(11).

F(25): Increment all scalers; requires N, S2, and any A from A(0) to A(11). (Inhibit should be True to prevent input pulses from being counted.)

F(26): Enable Look-At-Me; requires N, S2, and any A from A(0) to A(11). Remains enabled until Z or F(24). Caution: The state of the LAM mark will be arbitrary after power turn-on.

C or Z: All scalers and LAM are cleared by the CAMAC "Clear" or "Initialize" command; requires S2. Z also disables LAM.

I: All Scaler inputs are inhibited during CAMAC "Inhibit" command.

Q: A Q=1 response is generated in recognition of an F(0) or F(2) Read function, or an F(8) if LAM is set for a valid N and A, but there will be no response (Q=0) under any other condition.

X: An X=1 (Command Accepted) response is generated when a valid F, N, and A command is generated.

L: A Look-At-Me signal is generated from the time when first 24th bit is set until a module Clear command. LAM is disabled for the duration of N, can be permanently enabled or disabled by the Enable and Disable function command and can be tested by Test LAM.

Model 4434 32-Channel Latching Scaler

F(0)•A(0): Generates readout of the selected channel; F(0) can be executed and a Q=1 response will be provided under the following conditions:
a) Side switch LAD (Latching Disable) = ON; always if the LED RDE (Readout Enable) is ON.
b) Side switch LAD = OFF; only after a LOAD has been performed and as long as the readout of the given number of channels had not been completed.

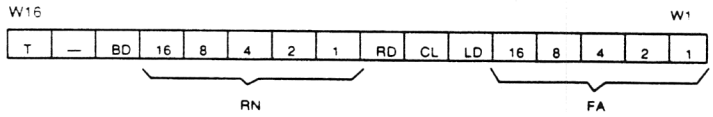
F(2)•A(0): Sequential data readout with auto-increment of the address; F(2) can be executed and a Q=1 response will be provided independent of the Latch Disable switch position if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been completed. Note: if the number of scalers to be read is RN+1>32-FA then the readout, after address 31, will continue with addresses 0, 1, 2, etc., until RN+1 channels have been read.

F(8)•(0): Test LAM: Q=1 response is generated when LAM is ON.

F(10)•A(0): Test and Clear LAM; a Q=1 response is generated when LAM is ON. LAM is cleared at S2.
Note: LAM goes on again after F(10) in the following cases:
a) Switch LOF (LAM at Overflow) = ON and scaler not cleared.
b) Switch LDR (LAM Data Ready) = ON and data readout not finished.

F(16)•A(0): Load register CR (Command Register); F(16) can always be executed and a Q=1 response is generated.

The Command Register is a 16-bit word with the following format and explanation:



FA: First Address to be read.

RN: Readout Number; defines how many channels (minus one) have to be read starting from the address FA; after a Z command, RN is set to 31 and FA to 0.

T: Test; when T=1 permanently inhibits signal inputs; increments at S2 all scalers by one count; after a Z command T=0.

LD: Load; LD=1 performs a load if switch LAD (Latching Disable) = OFF; after 0.8 µsec the module will be ready for readout; enables functions F(0) and F(2).

CL: Clear; CL=1 clears all the 32 scalers.

RD: Readout Enable; RD=1 prepares the module for readout, does not require a LOAD; readout can be started after 0.8 µsec.

Z: Initialize the unit at S2, i.e., all scalers, buffer and LAM are cleared as well as register CR.

C: Clear all scalers at S2.

I: All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front-panel VETO input.

X: A X=1 response is generated in recognition of any valid function.

Q: A Q=1 response is generated in recognition of any executable function.

L : Look-At-Me signal can be generated according to several possible options described in the specification section.

Model 4448 48-Input Coincidence Register/Latch

F(0)•A(0): Reads register A (Inputs 1-16).

F(0)•A(1): Reads register B (Inputs 17-32).

F(0)•A(2): Reads register C (Inputs 33-48).

F(2)•A(0): Reads and clears register A.

F(2)•A(1): Reads and clears register B.

F(2)•A(2): Reads and clears register C.

F(8)•(A0+A1+A2): Clears all registers

F(9)•A(0): Clears register A.

F(9)•A(1): Clears register B.

F(9)•A(2): Clears register C.

Z or C: Clears registers during S2 (Used for special test feature option.)

I: Inhibit gate input.

L: LAM: logic OR of all registers (switchable on or off for each register A, B, or C).

SPECIFICATIONS

MODEL	2551	4434	4448
General			
Function:	Counter	Latching Counter[2]	Latch
No. of Inputs:	12	32	48
Rate (MHz):	100	20 typical 30 instantaneous	150 MHz typical
Capacity:	24 bits or 48 bits by cascading channels[1]	24 bits (16,777,215 counts)	—
Double Pulse Resolution	10 nsec	<30 nsec	8 nsec max., 6 nsec typ.
Inputs			
Signal:	– 600 mV NIM into 50 Ω direct coupled. Reflections <10% with 1 nsec risetime. Min. width 7 nsec FWHM	Differential ECL (TTL factory option). 110 Ω pin-to-pin with Differential ECL, 560 Ω to ±5 V for TTL. Min. width 15 nsec	Differential ECL, 100 Ω direct coupled. <10% at 2 nsec risetime. Minimum width 4 nsec. Input sensitivity ±20 mV
Clear:	– 500 mV NIM, ≥50 nsec clears all channels within 1 μsec or via CAMAC command	>20 nsec, NIM (TTL) will disable inputs for 100 nsec and clear scalers or via CAMAC command	– 600 mV, >5 nsec, 2 nsec settling time after clear or CAMAC F(9) command
Inhibit/Veto/Gate:	– 500 mV, >5 nsec must precede input by 10 nsec or via CAMAC inhibit	NIM (TTL) pulse or via CAMAC inhibit	– 600 mV NIM, >3 nsec or via CAMAC inhibit[3]
Load:	n/a	>10 nsec NIM or TTL pulse or CAMAC F(16)	n/a
Outputs			
Data Output:	Via CAMAC command	Via CAMAC command or via auxiliary bus	Via CAMAC command
Miscellaneous Output:	n/a	Total of 16 4434s may be integrated to auxiliary bus. This bus must end in an independent controller, permits addressed readout of content independent of CAMAC. Front-panel 24-pin connector	3 summing outputs from each 16 inputs groups. – 100 mV ±10% presented for each register latched. Max. output – 0.7 V (50 Ω) corresponds to 7 set registers. Risetime 3 nsec, delay of 9 nsec
Power Consumption:			
+6 V	1.2 A	3.1 A (ECL version) 2.8 A (TTL version)	400 mA
– 6 V	100 mA	400 mA (ECL version) 40 mA (TTL version)	1.9 A

Notes:

1. By internal wire jumper option, even numbered channels may be cascaded with subsequent odd numbered channels to provide 48 bit channels. Any scaler generates LAM when 24th bit is set.
2. A set of side accessible switches allows the user to select different options as follows: LAD; Latching Disable; when ON the module works as a normal non-latching scaler. OVF; Overflow decides whether an overflow condition occurs when bit 16 of any scaler is ON or when bit 24 is ON, LCO: Load and Clear at Overflow when ON, LOF: LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value. LRE: LAM at Readout Enable; a LAM is generated after a readout request. LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there are date to be read. BAD: 4 bit Bus Address; defines module address in the auxiliary bus. VBR: Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus ouput registers (<200 nsec). NIM/TTL: Decides pulse standard accepted by inputs LOAD, CLEAR, and VETO.
3. Gate input delay: 2.5 nsec. Coincidence with 2.5 nsec and greater determined by input and gate pulse duration.

SECTION 1

OPERATING INSTRUCTIONS

1.2 General

Packaging: Single Width CAMAC standard module.

Power Consumption

	TTL Version	ECL Version
+6 V	2.8 A	3.1 A
-6 V	40 mA	400 mA

1.3 Input Characteristics

Signal Inputs: 32, in two 2 X 17-pin front-panel connectors, BERG 7578D-101-34.

Input Levels: Differential ECL (factory option is available to accept TTL single-ended inputs with the scaler incrementing on the negative going transition).

Input Impedance: 100 Ω pin-to-pin with differential ECL, 560 Ω to +5 V for TTL single-ended inputs.

Input Pulse Width: 15 nsec minimum.

Double Pulse Resolution: <30 nsec

Maximum Frequency: >20 MHz.

Maximum Instantaneous Rate: >30 MHz.

1.4 Command Inputs

General: The LOAD, CLEAR and VETO inputs each have a single front-panel Lemo-type connector; a common side switch selects either negative going NIM or TTL levels, input impedance 50 Ω for NIM pulses; 50 Ω AC and 100 Ω DC to +5 V for TTL pulses.

Load Input: A LOAD pulse with >10 nsec width will disable inputs for 220 nsec and shift the scaler contents into a 32-word X 24-bit buffer; the LOAD command can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC **F(16)** or **Z**; a front-panel LED (RDE, Readout Enabled) is lit in recognition of a Load command.

Clear Input: A CLEAR pulse with >20 nsec width will disable inputs for a duration of approximately 100 nsec and clear the 32 scalers.

Veto Input: Disables inputs for the duration of the VETO; see Figure 1.1 (action identical to CAMAC INHIBIT).

1.5 CAMAC Commands and Functions

NOTE: The following notation is used in this section:

CR: Command Register; loaded by **F(16)**.
FA: First Address to be read.
RN: Readout Number; defines how many channels (minus one) have to be read in the module.

Z: Initialize the unit at S2, i.e., all scalers, buffer and LAM are cleared as well as register CR; FA is set to 0 and RN is set to 31.

C: Clear all scalers at S2.

I: All scaler inputs are inhibited during CAMAC INHIBIT command; the action is identical to that of the front panel VETO input.

X: An X=1 response is generated in recognition of any valid function.

Q: A Q=1 response is generated in recognition of any executable function.

L: A Look-at-Me signal can be generated according to several possible options described in the "Option Switches" section below.

F(0)·A(0): Generates readout of the selected channel; **F(0)** can be executed and a Q=1 response will be provided under the following conditions:

a. Side switch LAD (Latching Disable) = ON: always if RDE (Readout Enabled) is ON.

b. Side switch LAD = OFF: only after a LOAD has been performed and as long as the readout of the given number of channels has not been completed.

F(2)·A(0): Sequential data readout with auto-increment of the address; F(2) can be executed and a Q=1 response will be provided independent of the Latching Disable switch position, if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been

completed.

NOTE: if the number of scalers to be read is RN + 1 >32-FA then the readout, after address 31, will continue with the addresses 0, 1, 2, etc. until RN + 1 channels have been read.

F(8)·A(0): Test LAM; Q=1 response is generated when LAM is ON.

F(10)·A(0): Test and clear LAM; a Q=1 response is generated when LAM is ON. LAM is cleared at S2.

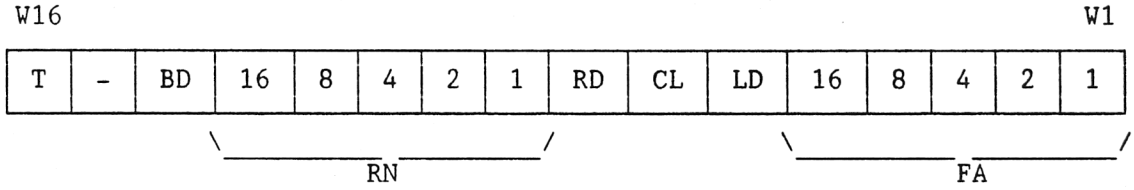
NOTE: LAM goes on again after F(10) in the following cases:

a. Switch LOF (LAM at Overflow) = ON and scaler is not cleared.

b. Switch LDR (LAM Data Ready) = ON and data readout not finished.

F(16)·A(0): Load register CR (Command Register); **F(16)** can always be executed and a Q=1 response is generated.

The Command Register is a 16-bit word with the following format and explanation:



All these data, except for the bits LD, CL, RD, are stored in an internal memory at S1 where they will be kept until a new **F(16)** or a **Z** command is received.

FA = First Address; gives the address of first channel to be read and can assume values from 0 to 31; the FA value is loaded in an internal Address Counter (AC) automatically incremented by one every time a new channel has been read and therefore defines which channel will be read next; after 31, the AC will continue counting 0, 1, 2, etc. until the given number of channels. RN + 1, has been read; after a Z command, FA is set to 0.

RN = Readout Number, defines how many channels have to be starting from the first address FA; RN may assume values ranging from 0 to 31, the

number of channels read will be RN + 1; this value is automatically loaded in a decrementing counter Read Counter (RC) at the start of a readout sequence; after a Z command RN is set to 31.

LD = Load; LD=1 performs a Load if switch LAD=OFF; also loads counters AC and RC; after 0.8 µsec, the module will be ready for readout; enables functions **F(0)** and **F(2)**.

CL = Clear; CL=1 clears all the 32 scalers.

RD = Readout enable; RD=1 prepares the module for readout and does not require a LOAD; readout can be started after 0.8 µsec; this bit can be used to read data again.

BD = Bus Disable; BD=1 disables the Auxiliary Bus readout; after a **Z** command BD=0.

T = Test; T=1 inhibits signal inputs; performs increment test on all the 32 channels. For this test the 24 bits of each scaler are considered as three words of 8 bits. The three words are all incremented by one (this permits the complete test of the module in only 256 cycles in total).

The bit T is memorized and it will keep a permanent inhibit on the 32 scaler inputs until T is overwritten or a **Z** command applied; after a **Z** command T=0.

To summarize, **F(16)** can generate the following operation sequences (X=no care):

T	RD	CL	LD	Sequence Generated:
0	0	0	0	Load Command Register (CR) only.
0	X	0	1	Load scaler contents into the internal buffer and start readout.
0	0	1	0	Clears all the 32 scalers.
0	X	1	1	Load scalers into buffer; clear scalers; start a readout.
0	1	0	0	Start a readout without pre-loading.
0	1	1	0	Clears all scalers and start a readout.
1	0	0	0	Inhibit all signal inputs, clear all scalers, and

				increment all channels.
1	X	0	1	Inhibit all signal inputs, increment all channels by one, load scalers into buffer and start a readout.
1	1	0	0	Inhibit all signal inputs, increment all channels by one and start a readout.
1	X	1	1	Inhibit all signal inputs, increment all channels by one, load buffer, clear scalers and start readout.

1.6 Side Switch Options

A set of switches, accessible on the side of the module, permits the user to select different options as follows:

LAD: Latching Disable; when LAD=ON the internal buffer becomes transparent so that the Load function is no longer effective and can be used only to start a readout.

OVF: Overflow; in position 16 (24) and overflow condition occurs when bit 16 (24) scaler in ON (16 or 24-bit half full scale).

LCO: Load and Clear at Overflow; a Load is automatically generated, followed by a Clear and a start readout, when an overflow occurs.

LOF: LAM at Overflow; a LAM is generated as soon as at least one of the scalers arrives at half full scale; a LAM can be cleared by a **Z** command or, if the scalers are cleared, by an **F(10)**.

LRE: LAM at Readout Enable; a LAM is generated after a readout request. A LAM can be cleared by a **Z** command or an **F(10)**.

LDR: LAM Data Ready; a LAM is generated after a readout request and as long as there is data to be read.

BAD: Bus Address; 4 bit, defines the module address on the Auxiliary BUS.

VBR: Veto by Bus Readout; enable a VETO of all scaler inputs during the loading of the BUS output register (<200 nsec).

NIM/TTL: Sets the standard for pulses accepted by inputs LOAD, CLEAR and VETO.

NIM: 0 = 0 mA; 1 = -12 mA.

TTL: 0 = 2.5 V; 1 = 0.5 V.

1.7 Auxiliary Bus Specifications

General: All BUS lines are in TTL low power Shottky technology, negative logic.

Level 0: >2 V
Level 1: <0.8 V

DA 1 to 24: Data and Address lines:

DA 1 to 9
(Address Inputs) Level 0: < 100 µA at 5 V
Level 1: <-400 µA at 0.4 V

DA 1 to 24
(Data Output), Tri-state Output

Level 0: >3.1 V at -1 mA
Level 1: <0.4 V at 12 mA

ARY: Address Ready Input: Impedance 6.8 KΩ
(Integration 80 nsec)

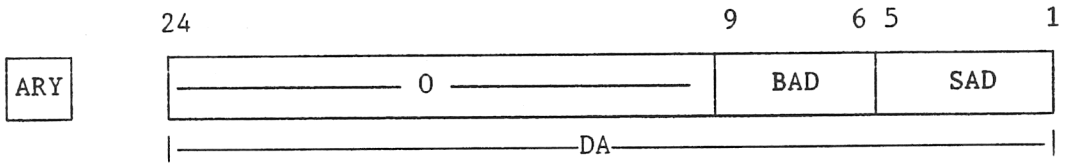
DRY: Data Ready Output: Open Collector

Level 0: <50 µA at 5 V
Level 1: <0.4 V at 16 mA

EGD: Enable Ground: Impedance 10 KΩ at +5 V.

This line must be grounded by the BUS controller.

1.8 Address Transfer Structure



1.9 Data Transfer Structure

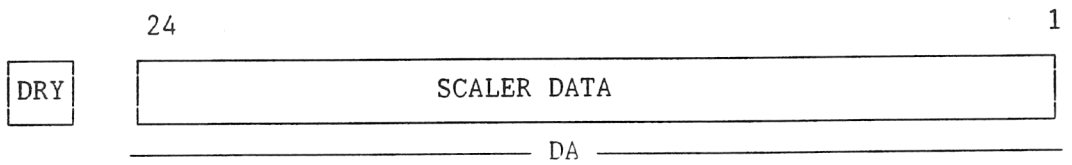


Figure 1.1

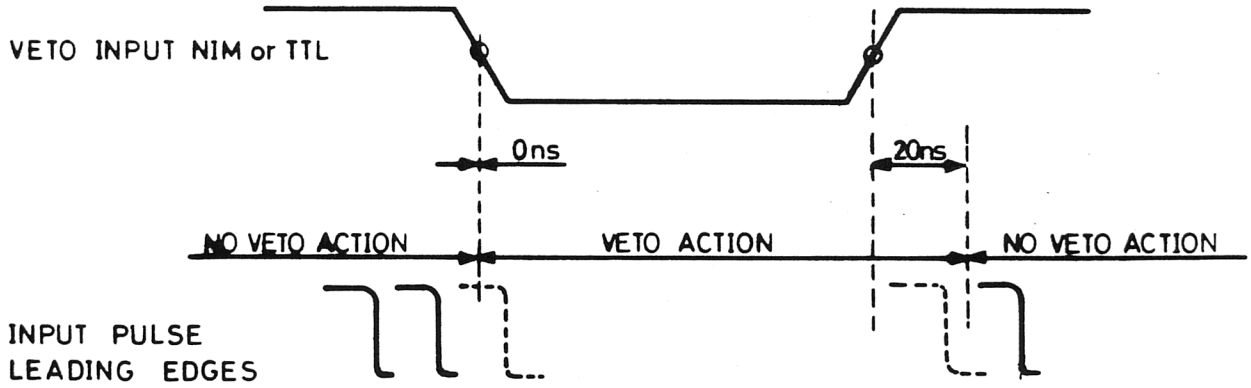


Figure 1.2

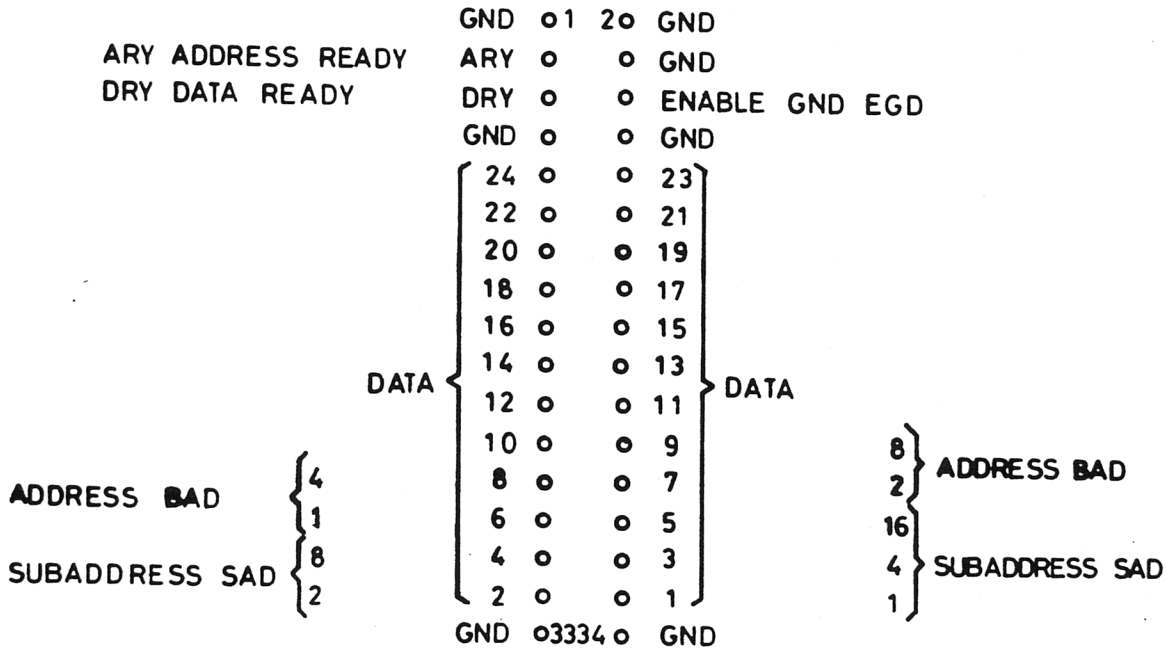
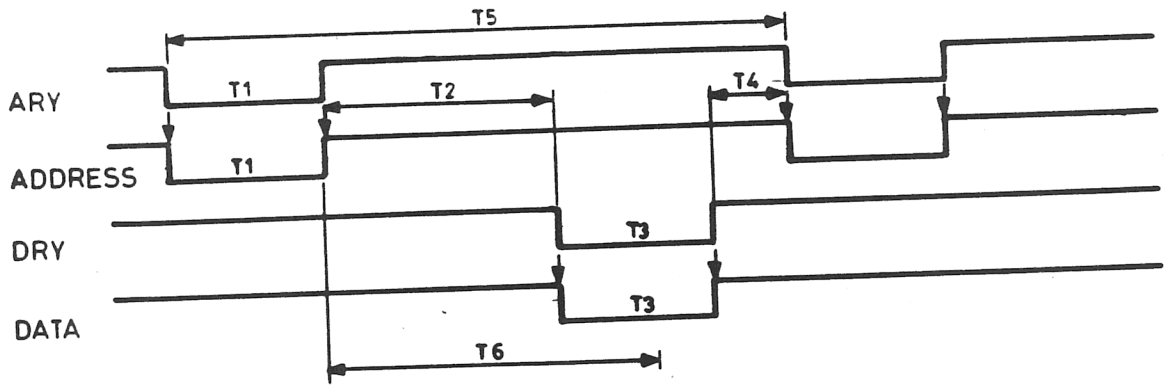


Figure 1.3



SECTION 2

TECHNICAL DESCRIPTION

In this chapter, information concerning the Model 4434 scaler and simple data acquisition program concepts are presented.

Figure 2.1 shows a functional block diagram for the 4434 user that will be referred to in the following paragraphs (2.1 to 2.4).

2.1 LOAD Scaler Function

This function is performed either by sending an external LOAD signal (NIM or TTL, width greater than 10 nsec) **or** by **F(16)·A(0)** with bit W6=1.

At the time this function is executed, the following actions occur:

a. All scaler inputs are inhibited for less than 220 nsec; the inhibit action, with respect to inputs on front-panel connectors, starts 30 nsec (typical) to 45 nsec (maximum) after leading edge of input LOAD pulse.

b. All scaler contents are loaded into a temporary register with 32 words of 24 bits each.

c. If CAMAC load is given **(F(16)·A(0))**, the 10 bits W1/W5 and W9/W13 are loaded into the first address and readout number registers at S1, thus defining the first address to be read and the number of channels to be read.

d. The address and readout counters are set to the value of the address and readout registers; readout is initialized.

e. The content of the first scaler to be read is loaded into the output register; this operation occurs (maximum) 500 nsec after LOAD time (or <900 nsec if the BUS readout is simultaneously initialized).

2.2 CLEAR Scaler Function

This function is performed either by sending an external CLEAR signal NIM or TTL, width greater than 20 nsec) or by F(16)·A(0) with bit W7=1: CAMAC Z or C also perform this function.

Following this operation, all scaler contents are set to zero. Figure 2.2 shows the CLEAR timing diagram.

2.3 VETO Action

For all 32 scalers, counting can be inhibited by setting the CAMAC INHIBIT line on or by input VETO action; counting is inhibited either when input veto level is below -0.4 V (NIM veto) or +2 V (TTL veto).

If VBR switch (Veto by BUS Readout) is ON, a Veto is applied for each

readout demand from the BUS (duration <200 nsec).

Please note that inhibit (or VETO) pulses are not counted, whatever the state of the scaler inputs.

2.4 READ Scaler Sequences (Read Out)

Preliminary remark: any READ sequence will permit the user to read the scaler states (counts) at the time the last LOAD function has been performed, except when the Model 4434 scaler is set to "latching disable mode" (see: Side Switch Options - Section 1.6).

There are basically two ways of reading the scaler contents by CAMAC:

a. Sequential read out: F(2)·A(0)
   When using F(2)·A(0), consecutive channels are read sequentially, starting from the channel addressed by the address register content.

   The Q=1 response is generated for each F(2)·A(0) function, until the last channel has been read (Q=0 is given when the readout number is = RN+1).

b. Random read out: F(0)·A(0)

   If the user wants to read one specific channel, he has to first write that channel address by sending F(16)·A(0) with W8 set to 1 and W1 to W5 containing the specific channel address and then to read the scaler contents by using F(0)·A(0). Please note that F(0) does not increment the address counter and thus and F(2) sequence may always follow a single F(0) read out. The first F(2) would then give the same result as the preceding F(0) read out.

Final remarks: (see also Figure 2.4)

1. Any read out sequence must be preceded by a LOAD function or by an F(16)·A(0) with W8 set to one; in the latter case, the read out will enable the user to re-read the scaler register contents (which remain unchanged until the next LOAD function execution).

2. Q=1 for F(0) is given if read out has been correctly initialized (see above).

3. Q=1 for F(2) is given if read out has been correctly initialized and if last channel has not been read.

2.5 TEST Function

Figure 2.3 shows a 24-bit scaler block diagram that represents the scaler operation for the TEST function.

When F(16)·A(0) with W16=1 is performed, each byte (8 bits/byte) of each scaler is incremented by one, and if the content of the preceding (left side) byte counter was 255 decimals, the counter is incremented by two; this operation needs 12 µsec to be performed; the VETO is set.

The user can choose between the two following sequences to control the Model 4434 operations with the TEST function:

a. Test and verify each step

CLEAR SCALERS

S TEST + LOAD (F(16)·A(0) WITH BIT W6 = W16 = 1)
READ OUT and VERIFY (32 X F(2)·A(0))

repeat S n times

b. Test and verify the final value

CLEAR SCALERS

S TEST (F(16)·A(0) WITH BIT W16 = 1)

Repeat S n-1 TIMES (CYCLE TIME >12 μsec)

TEST + LOAD (F(16)·A(0) with bit W6 = W16 =1)

READ OUT and verify results (n TESTS)

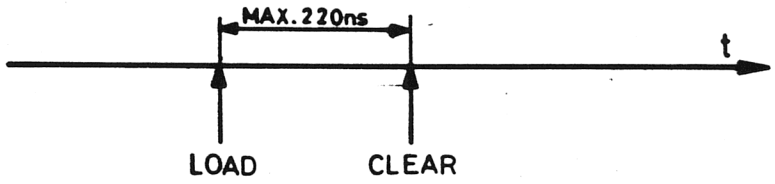
WHEN COMPLETE TEST HAS BEEN PERFORMED, F(16)·A(0) WITH BIT W16=0 OR Z MUST BE SENT TO REMOVE VETO!

2.6 Multiple Functions

As can be seen from Section 2.5, some functions can be executed "simultaneously" by the Model 4434 scaler. The purpose of this section is to define all multiple functions that can be executed and the order in which they are performed.

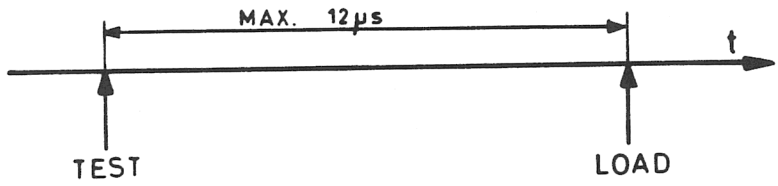
a. LOAD + CLEAR

When simultaneously initialized, these functions are executed according to the following timing diagram:



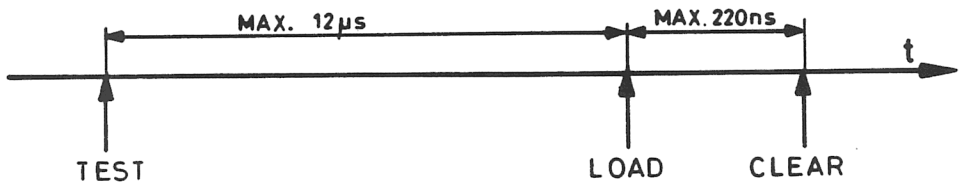
b. TEST + LOAD

When simultaneously initialized, these functions are executed according to the following diagram:



c. TEST + LOAD + CLEAR

When simultaneously initialized, these functions are executed according to the following timing diagram:



2.7 LAM and Switch Settings

a. Switch LAD (Latching Disable)

When set, the Model 4434 is set to latching disable mode, all data acquired during read out process are now relative to the time and read out is in progress. Therefore, if the scalers are counting, the data read may be "erroneous".

Note: it is still necessary to initialize the read out process by using F(16)·A(0) with W8=1.

b. Switch OVF (Overflow)

By default (switch overflow on 16) on "overflow" condition occurs when bit 16 of any scaler is ON (set to 1); when setting switch overflow to 24 an "overflow" condition occurs when bit 24 of any scaler is ON.

c. Switch LCO (Load and Clear at Overflow)

When ON, switch LCO will enable the automatic load and clear function (see Section 2.6) as soon as an "overflow" condition occurs.

This switch must be set to OFF if the user wants to test the scaler operation (see Section 2.5).

d. Switch LOF (LAM Request at Overflow)

When ON, switch LOF will enable automatic LAM generation as soon as an "overflow" condition occurs and is maintained as long as overflow condition is present.

e. Switch LDR (LAM Request when Data Ready)

When ON, switch LDR will enable automatic LAM generation as soon as the 24-bit output register (see Figure 2.1) contains the data to be read.

In this case, LAM is set each time the read out has been initialized.

L is cleared by F(0)·S(2) or F(2)·S(2) and is set approximately 500 nsec late until the last channel has been read.

f. Switch LRE (LAM Request at Readout Enable)

When ON, switch LRE will enable automatic LAM generation after a readout request.

Final Remark:

LAM and Q response to F(8) and F(10) operations conform to the EUR 4100 e (1972) CAMAC specifications.

2.8 Addressable Read Only Auxiliary BUS

This BUS allows, at any time, the readout of any of the 32 scalers independent of the CAMAC dataway.

The BUS requires and independent controller which is the BUS Master.

A data transfer on the auxiliary BUS is initiated by the BUS Master by sending a 9 parallel bit word, defining the address of the desired scaler, together with a synchronization pulse ARY (Address Ready).

The 9-bit address word includes 4 bits for the address BAD of the modules connected to the BUS (BAD = Bus ADdress). The BAD may range from 0 to 15. Up to 16 4434 modules can be connected to the same Auxiliary BUS. The address BAD is set for each module by a binary switch, accessible on the side of the module. The other 5 bits in the address word define the subaddress SAD inside the given moduel (SAD ranges from 0 to 31).

Responding to a readout request, the addressed 4434 will send on the Auxiliary BUS, after the end of the ARY signal, the content of the addressed scaler, as a 24 parallel bit word, together with a synchronization signal DRY (Data Ready). Readouts by CAMAC and by Auxiliary BUS, when acting together, proceed by time sharing, CAMAC having priority. The response time on the Auxiliary BUS will be affected. (Response time from 500 nsec to 900 nsec.)

In addition, when a 4434 is in test mode, the readout by Auxiliary BUS will be halted during a complete test cycle (12.8 µsec).

The Bit BD (BUS Disable) of the Command Register CR, allows the suspension of the readout by the Auxiliary BUS. The bit BD is reset to zero by a Z command.

Depending on the type of CAMAC readout chosen for a particular 4434, two types of readout by Auxiliary BUS are possible:

a. Spying Readout

   In this case, a CAMAC readout has not been initialized (LED RDE OFF) or the switch LAD (Latching Disable) is on.

   The content of a scaler is loaded on the Auxiliary BUS output register even when the scaler is counting. The data can eventually be wrong. The possibility of wrong data can be avoided by setting the switch VBR (Veto by BUS Readout). The switch has the effect of halting counting over all the 32 channels during 200 nsec, that is, by the time needed to load the output register.

b. Latched Readout

   In this case, a CAMAC readout has been initialized (LED RDE ON).

   The data loaded in the Auxiliary BUS output register will be taken out of the latches associated with each scaler. The above is valid as long as readout via CAMAC is not finished. This readout mode allows the readout of the same data both by CAMAC and by Auxiliary BUS.

2.9 Input Options

Scaler Counting Inputs

The 32 scaler inputs can be set to operate either in ECL differential input mode or in TTL single ended input mode.

This is done by inserting the appropriate set of termination resistor networks into the input termination single-in-line sockets and eight jumpers.

a. Differential (ECL) Input Model

   Figures 2.5 and 2.7 show the input termination arrangement.

b. Single Ended TTL Input Mode (MOD 100)

   Figures 2.6 and 2.8 show the input termination arrangement.

2.10 Cables

Interconnections between different ECLine modules, for transmission of different ECL pulse pairs, can be made either by multiwire cables or by single twister-pair cables for one to one connections.

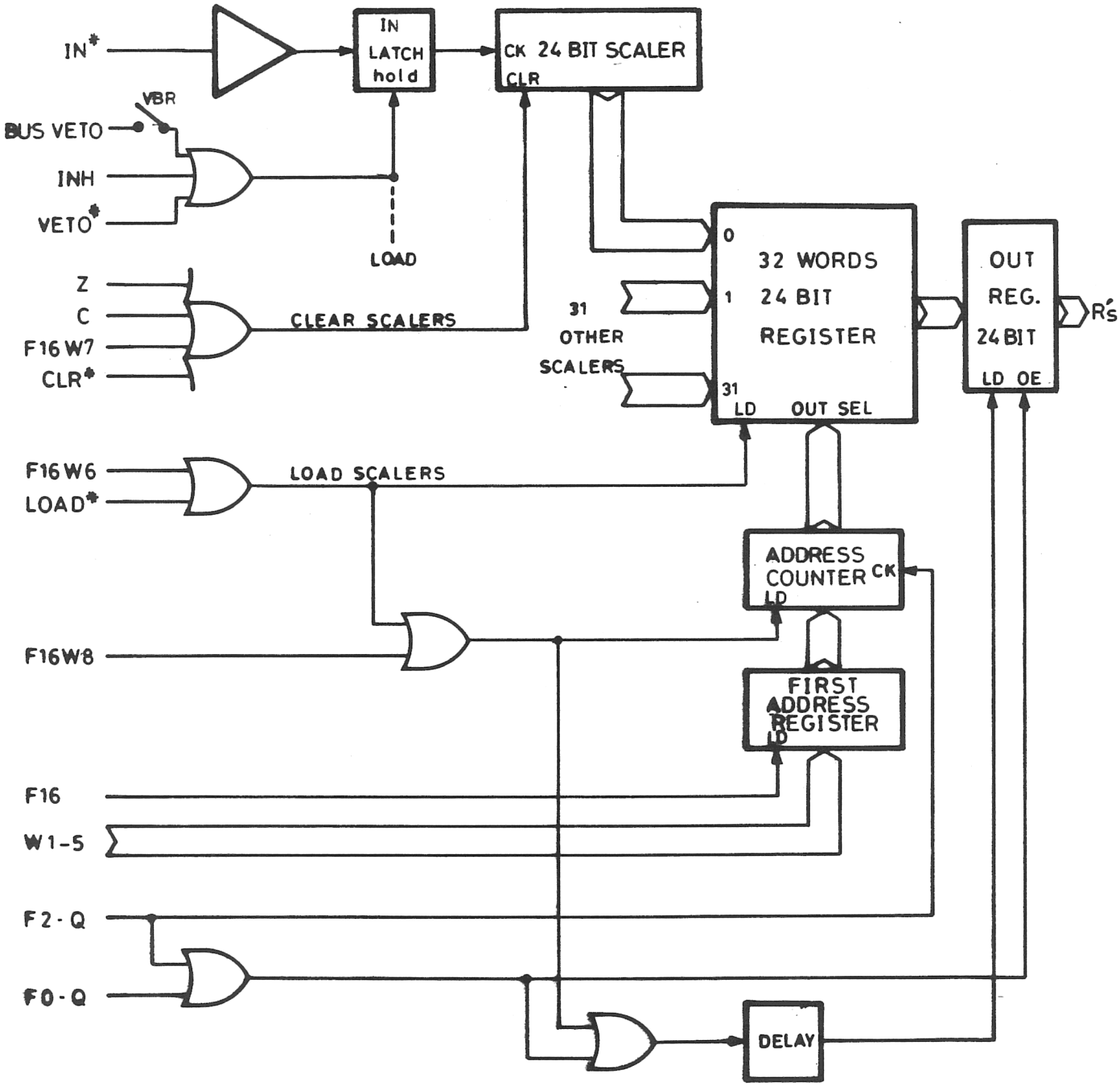
Such interconnecting cables may be purchased from LeCroy and in particular, as multiwire cables, two types are available; one for short interconnections using just flat cable, the second for long interconnections using twisted and flat ribbon cable.

The notation used in ordering these cables is as follows:

- STC-DC/34-LL Multiwire cable for short interconnections
- LTD-DC/34-LL Multiwire cable for long interconnections
- STP-DC/02-LL Single twister-pair cable.

Where LL is the cable length in feet which should be specified by the customer.

FUNCTIONAL BLOCK DIAGRAM



Remarks :

a) SYMBOL * means front panel input SIGNAL.

b) The following functional block diagram should not be used for timing calculations.

Figure 2.1

CLEAR TIMING DIAGRAM

ALL TIMES REFERED TO FRONT PANEL INPUT CONNECTORS

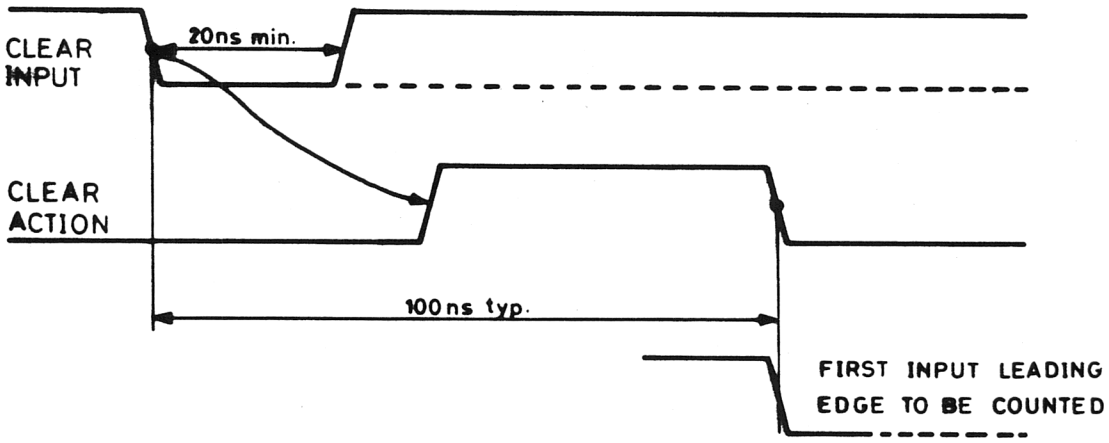


Figure 2.2

TEST INCREMENTATION BLOCK DIAGRAM

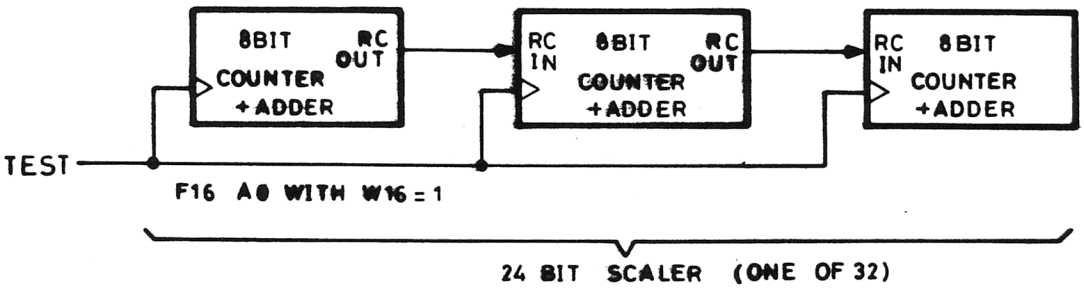


Figure 2.3

FUNCTIONAL BLOCK DIAGRAM LAM & ANSWER LOGIC

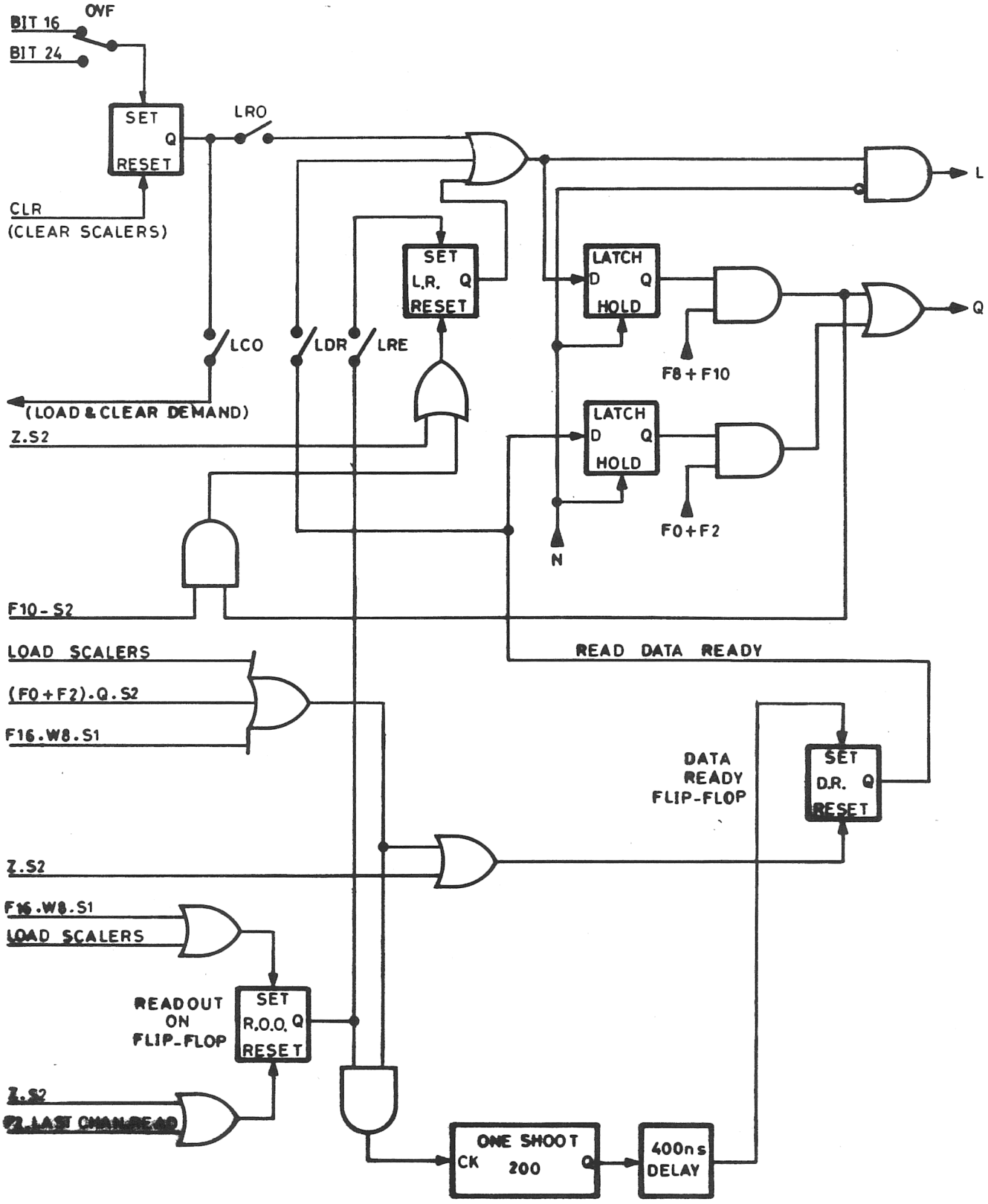
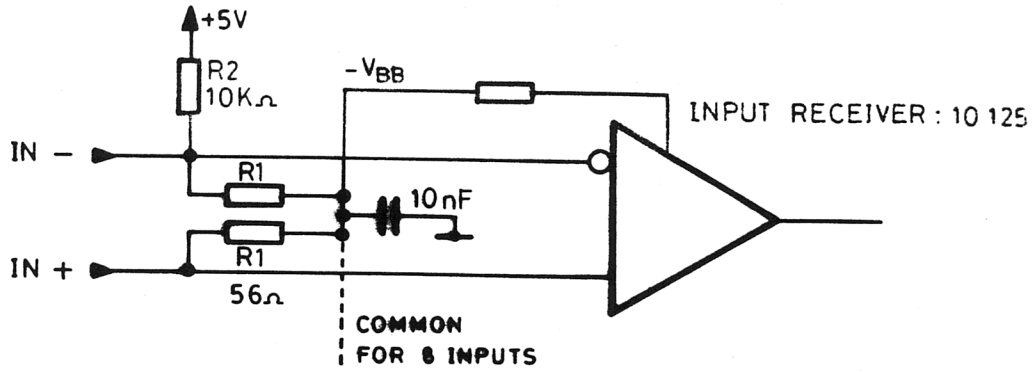


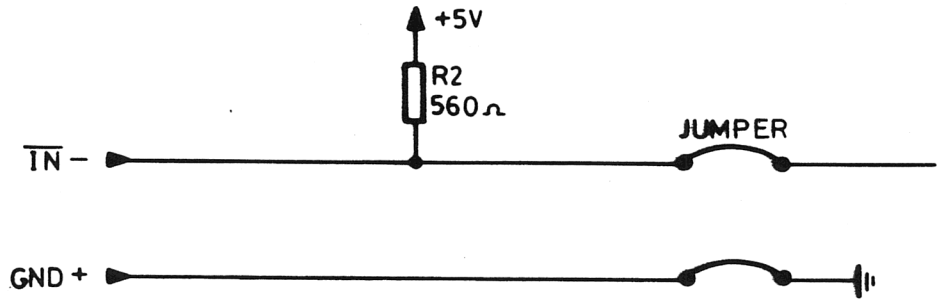
Figure 2.4



ECL DIFFERENTIAL INPUT MODE

Common mode input range: $-1.3\ V \pm 0.2\ V$
Differential mode input range: $\pm 0.6\ V$

Figure 2.5



TTL SINGLE ENDED MODE

Note: + inputs are connected to ground in this mode; negative TTL input pulses enter the scaler via the - input; the last pair of each 34-pin input connector is connected to ground to give a return path for the input currents (last pair of each input cable).

Figure 2.6

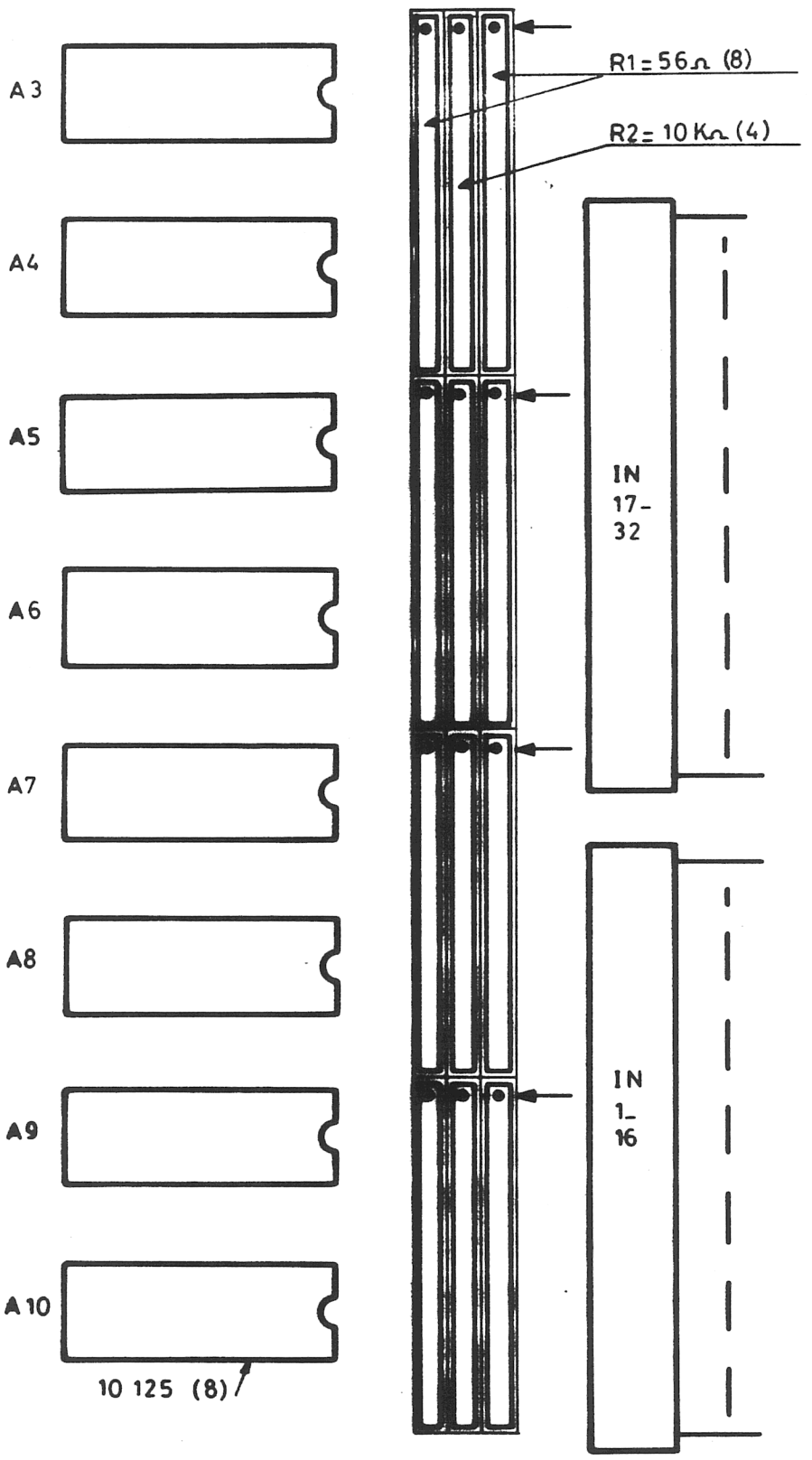

ECL DIFFERENTIAL MODE
A3
A4
A5
A6
A7
A8
A9
A10
10 125 (8)
R1=56Ω (8)
R2=10KΩ (4)
IN 17-32
IN 1-16

Figure 2.7

TTL SINGLE ENDED MODE

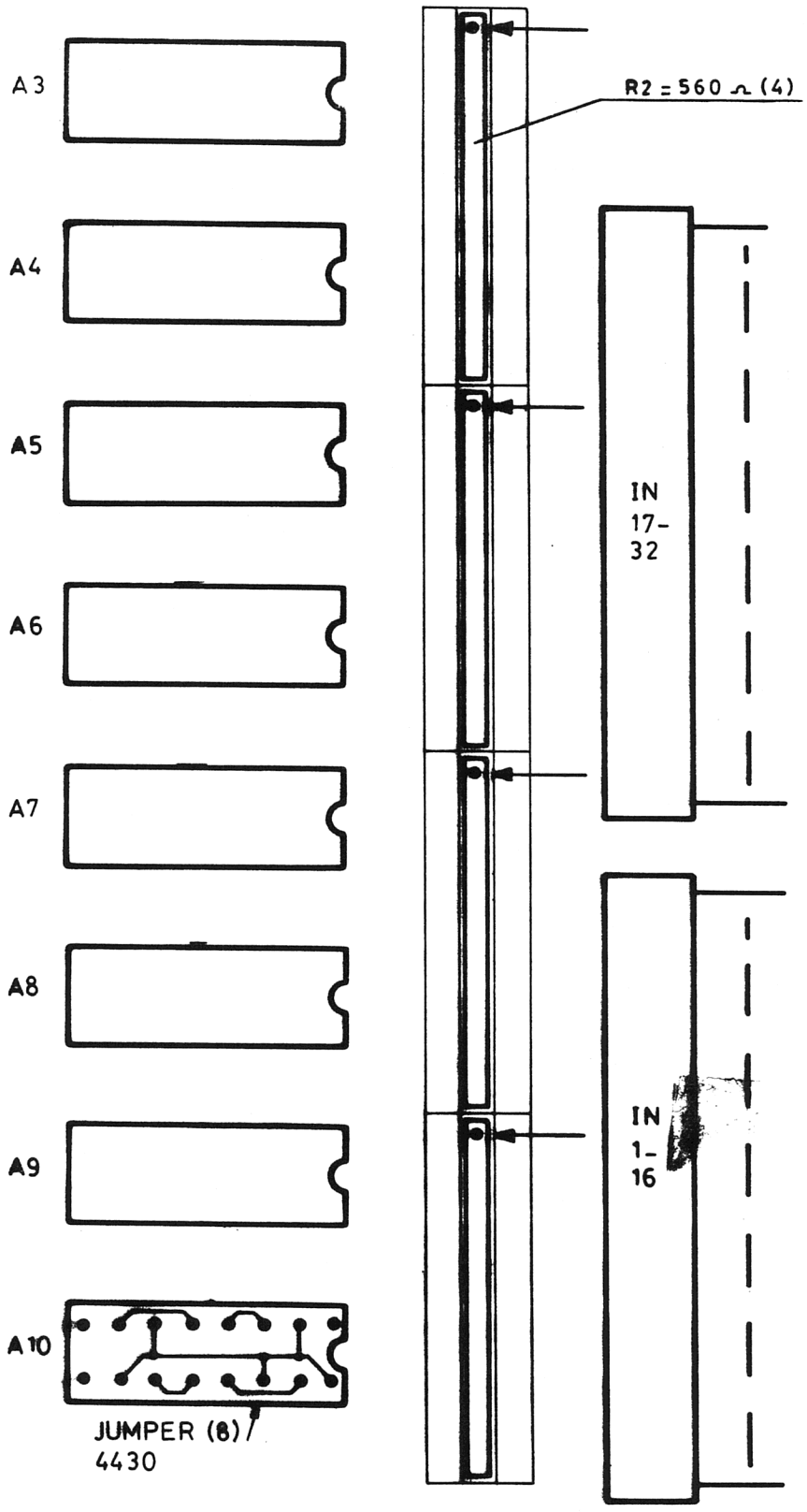


Figure 2.8

TECHNICAL INFORMATION

(SCHEMATICS, PARTS LISTS)

LECROY CORPORATION
4434 PARTS LIST

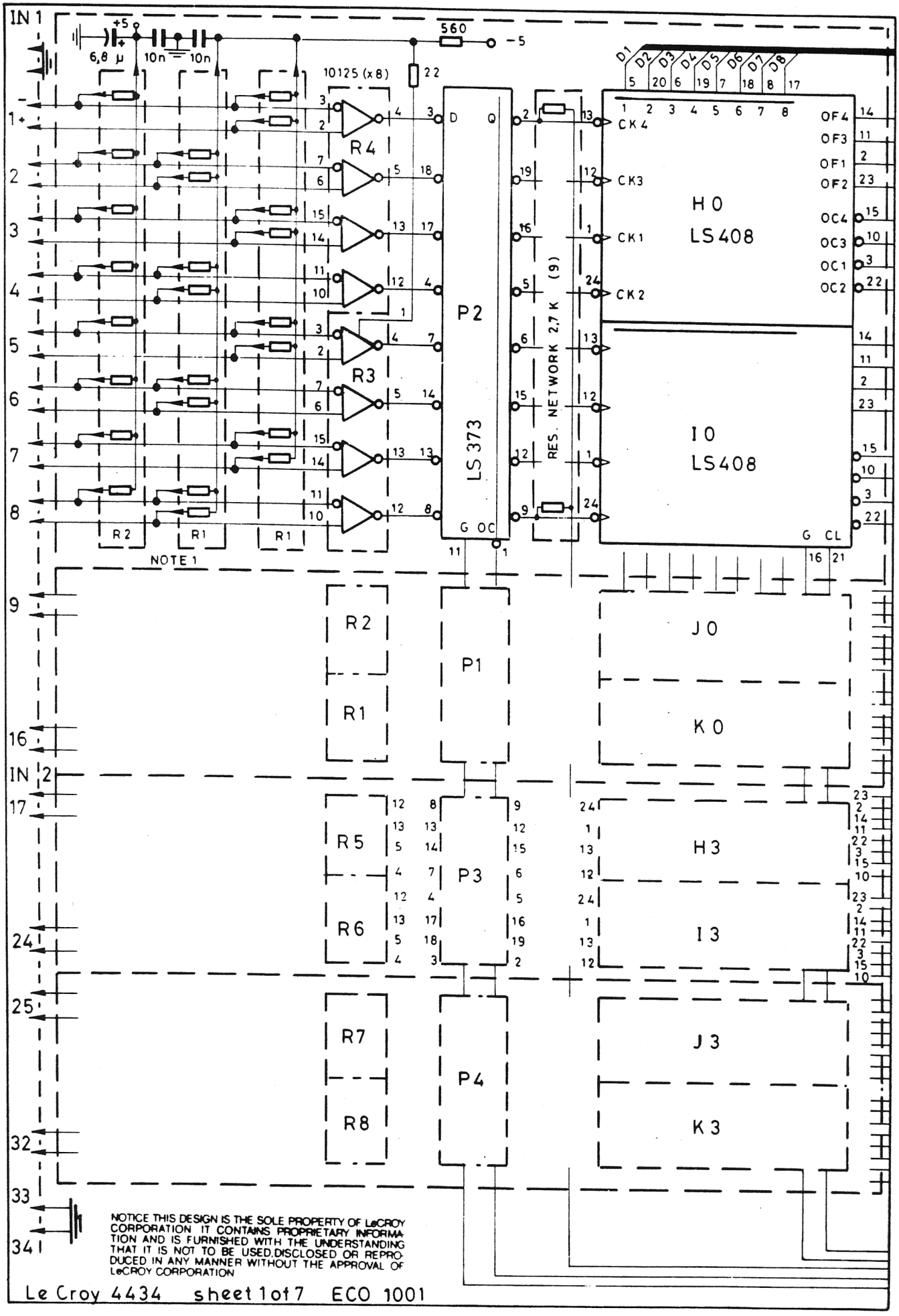
PART NUMBER	DESCRIPTION	QUANTITY PER
102412100	CAP CERA DISC 100V 10 PF	4
102412101	CAP CERA DISC 100V 100PF	2
102412221	CAP CERA DISC 100V 220 PF	1
102412330	CAP CERA DISC 100V 33PF	3
102484471	CAP CERA DISC 100V 470 PF	2
103327103	CAP CERA MONO 50V .01 UF	46
142824685	CAP TANT DIP CASE 6.8 UF	5
161335101	RES CARBON FILM 100 OHMS	6
161335102	RES CARBON FILM 1 K	2
161335103	RES CARBON FILM 10 K	2
161335123	RES CARBON FILM 12 K	2
161335220	RES CARBON FILM 22 OHMS	4
161335222	RES CARBON FILM 2.2 K	4
161335271	RES CARBON FILM 270 OHMS	1
161335332	RES CARBON FILM 3.3 K	2
161335390	RES CARBON FILM 39 OHMS	2
161335391	RES CARBON FILM 390 OHMS	1
161335472	RES CARBON FILM 4.7 K	2
161335561	RES CARBON FILM 560 OHMS	5
161335681	RES CARBON FILM 680 OHMS	2
161335682	RES CARBON FILM 6.8 K	1
161335750	RES CARBON FILM 75 OHMS	1
181457202	RES VARI CERMET 2 K	1
190042103	RESISTOR NETWORK 10 K	4
190042272	RESISTOR NETWORK 2.7 K	6
190042560	RESISTOR NETWORK 56 OHMS	8
190642103	RESISTOR NETWORK 10 K	2
200031028	IC 2-INPUT NAND SN74LS00N	1
200031029	IC D-TYP FLOP SN74S74N	1
200031033	IC 2-INPUT NAND SN7403N	7
200031047	IC 3-INPUT NAND SN74LS10N	2
200031049	IC D-TYP FLOP SN74LS74N	3
200031051	IC 2-INPUT NOR SN74LS02N	2
200031073	IC 2-IN POS OR SN74LS32N	3
200031076	IC 2-INPUT NAND SN74S37N	2
200031077	IC 3-INPUT AND SN74LS11N	1
200031097	IC COUNTER SN74LS197N	1
200031101	IC BIN COUNTER SN74LS393N	2
200031380	IC BUS RECEIVER DS8836N	1
200041008	IC J-K FLOP SN74S112N	1
200041017	IC J-K FLOP SN74LS112N	1
200041027	IC QUAD SEL/MP SN74LS157N	3
200041033	IC D-TYP FLOP SN74LS174N	3
200041042	IC UP/DN COUNT SN74LS191N	3
200041043	IC 4-BIT MAGNIT SN74LS85N	1
200041062	IC DEC/DEMULTP SN74LS138N	5
200041071	IC FULL ADDER SN74LS283N	4
200041139	IC DEC/MULTIPL SN74LS139N	1
200041251	IC 8-IN MULTIPLX 74LS251	4
200041375	IC 4-BIT LATCH SN74LS375N	1
200062009	IC 576-BIT RAM N82S09N	2
200071373	IC D-TYP LATCH 74LS373N	7
200071533	IC D-TYP LATCH 74LS533	5
200330054	IC AND-OR-INV SN74LS54N	1

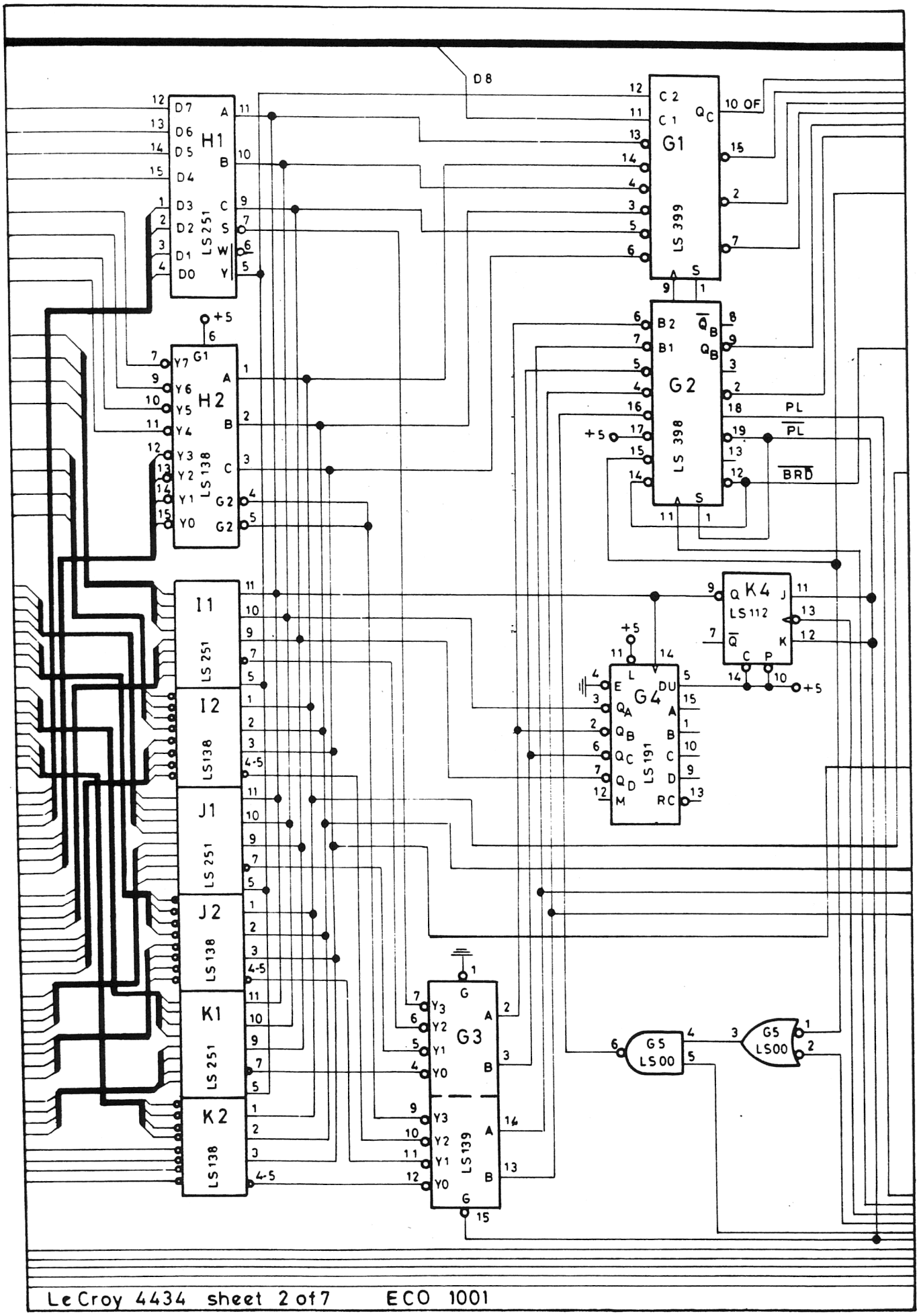
XENTIS V3.1A
ZZBPSS
ZZIPMS

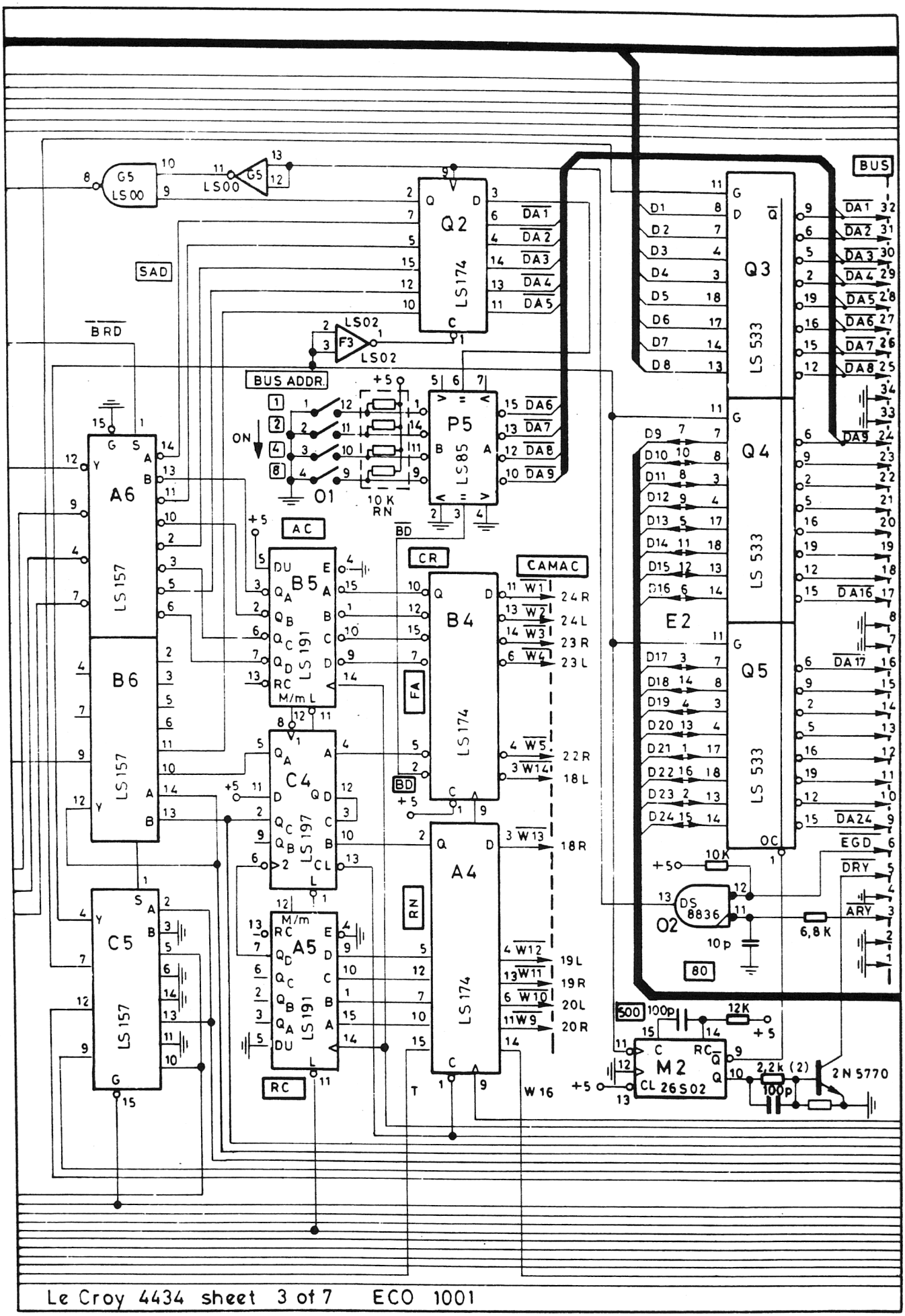
LECROY CORPORATION
4434 PARTS LIST

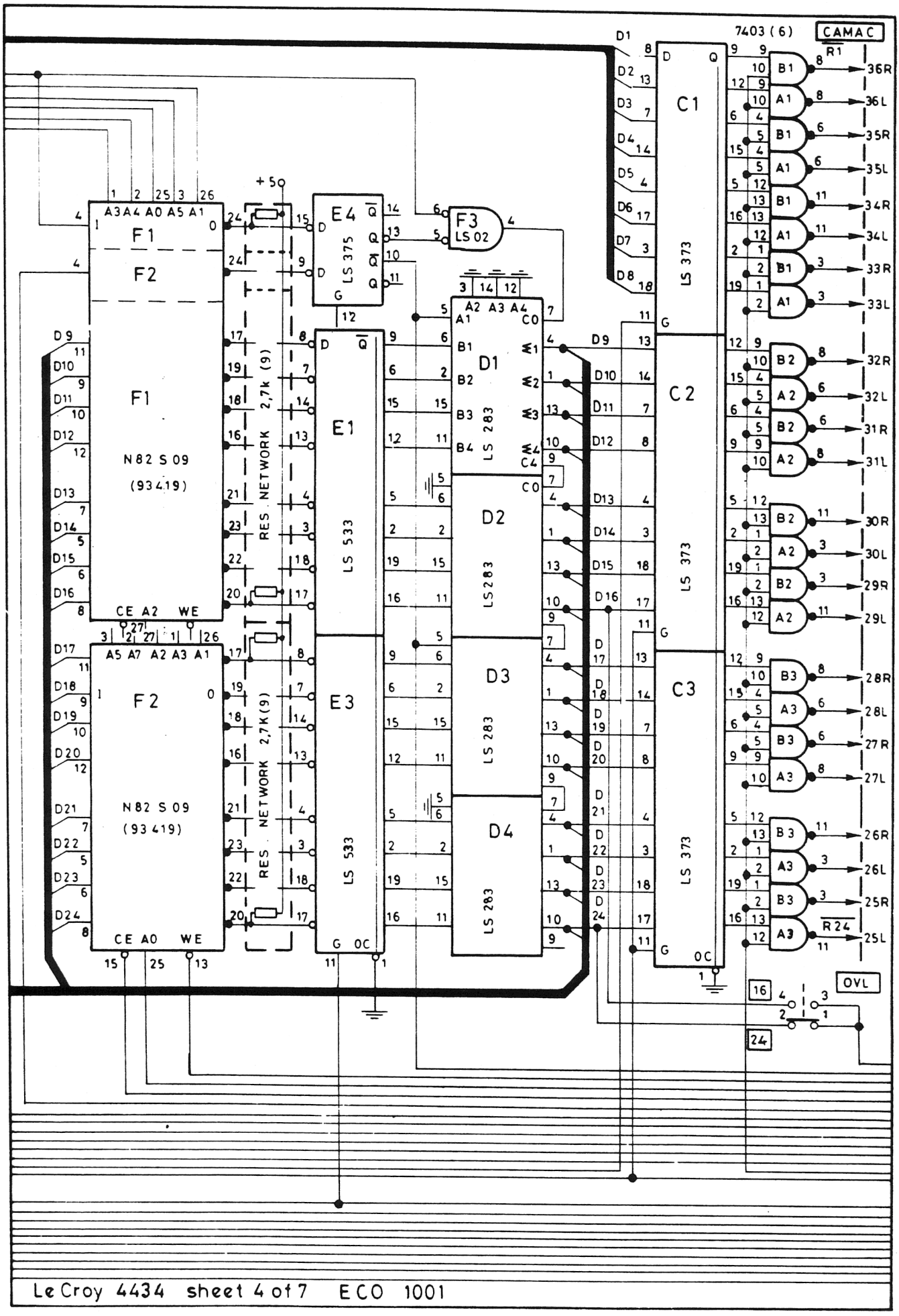
PART NUMBER	DESCRIPTION	QUANTITY PER
200331011	IC 3-IN AND GATE SN74S11	1
200441002	IC MULTIVIBRATOR AM26S02	1
204042008	IC QUAD TRANSL MC10125P	8
207340399	IC 2-IN MPLX SN74LS399N	1
207370398	IC 4-IN MPLX SN74LS398N	1
208031003	IC VOLT COMPARATOR NE521A	2
230110005	DIODE SWITCHING 1N4448	7
235010005	DIODE RECTIFIER 1N4005	1
235050001	DIODE RECTIFIER 1N4139	1
256233209	DIODE LED RED MV5075C	1
270110001	TRANSISTOR NPN PN2369A	1
270170001	TRANSISTOR NPN 2N5770	2
300050001	CHOKE FERRITE SINGLE LEAD	2
400030016	SOCKET IC ST DIP-16	8
400341024	SOCKET IC ST DIP-24	8
402130001	CONN LEMO RT ANGLE PC MTG	3
403119234	HDR DBL ROW RT ANGL 34	3
403180008	HEADER WIREWRAP 8-PIN	4
405812002	SOCKET STRIP SOLDR 20 POS	6
411451002	SWITCH ROCKER PC MTG 4PST	1
411651001	SWITCH ROCKER PC MTG 6PST	1
419211001	SWITCH SLIDE DIP-MTG DPST	2
433220001	FUSE PICO II 125V 10 AMP	1
433221004	FUSE PICO II 125V 1 AMP	1
454310002	HDR DIP SOLD TO PC BD 2	2
521000004	SPACER HEX 2-56X.417	4
540203001	SIDE COVER CAMAC STD(LIP)	1
540206078	RAIL CAMAC STD TOP W/LIP	1
540206178	RAIL CAMAC STD BOT W/LIP	1
540209001	REAR PANEL CAMAC SIZE #1	1
555430003	CAPTIVE SCREW ASSEMBLY	1
560256005	SCREW PHILIPS 2-56X5/16	4
560440003	SCREW PHILIPS 4-40X3/16	4
564440004	SCREW ROUND PHIL 4-40X1/4	2
567440006	SCREW FLAT PHIL 4-40X3/8	2
568256002	SCREW FLAT PHIL 2-56X1/8	4
591663030	WIRE KYNAR BLU LSF AWG 30	20
714434003	PC BD PREASS'Y 4434	1
724434003	FRONT PNL PREASSY 4434	1
734434003	SIDE ECLINE LEFT 4434	1
LS408	LATCHING SCALER	8

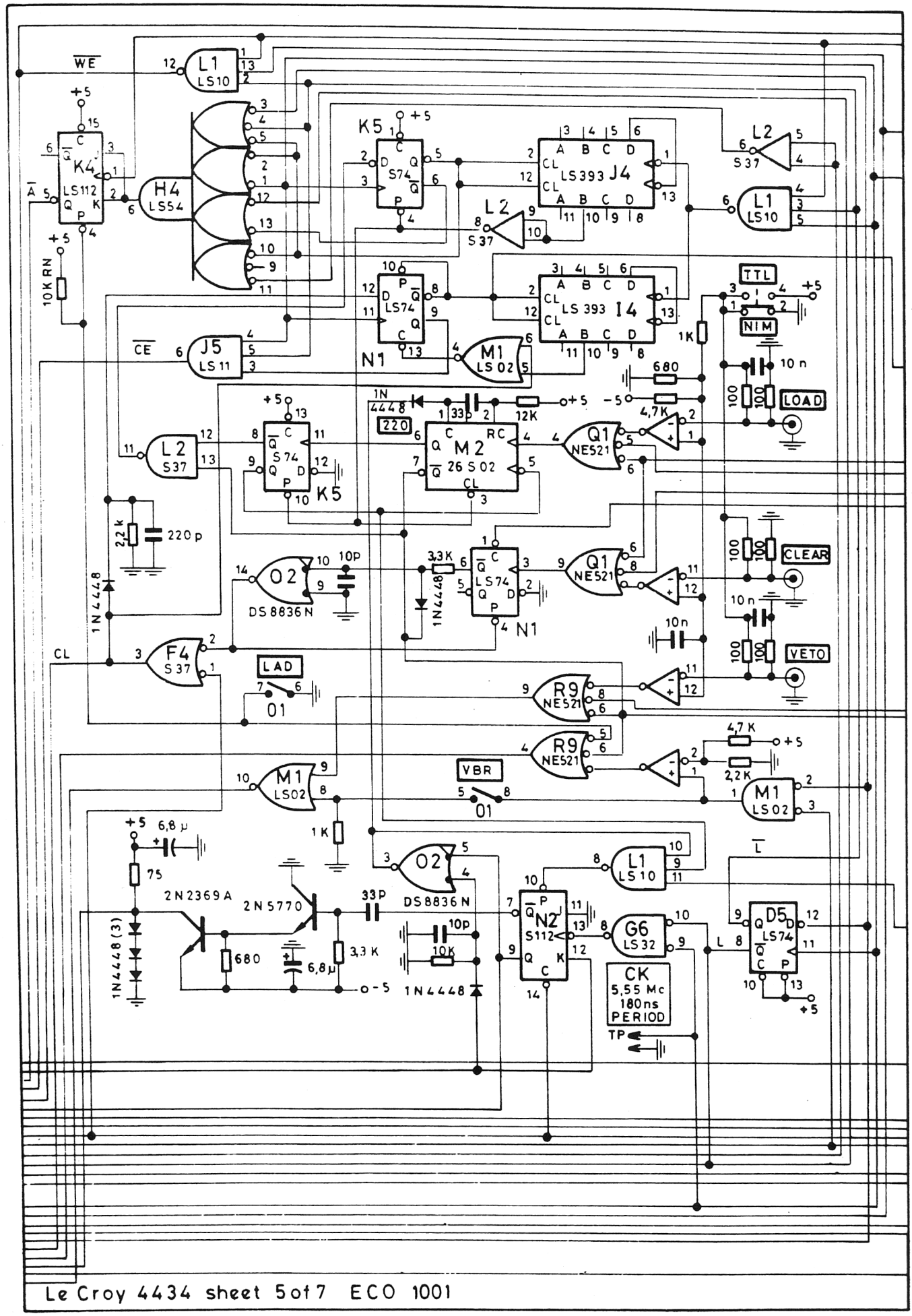
End of report. 95 Details encountered.


IN 1
+5
6,8 µ
10n
10n
560
-5
10125 (x8)
22
D1
D2
D3
D4
D5
D6
D7
D8
5
20
6
19
7
18
8
17
R4
R3
P2
LS 373
D
Q
G
OC
RES. NETWORK 2,7 K (9)
CK4
CK3
CK1
CK2
H0
LS408
I0
LS408
OF4
OF3
OF1
OF2
OC4
OC3
OC1
OC2
G
CL
R2
R1
R1
NOTE 1
R2
R1
P1
J0
K0
IN 2
R5
R6
P3
H3
I3
R7
R8
P4
J3
K3
NOTICE THIS DESIGN IS THE SOLE PROPERTY OF LeCROY CORPORATION IT CONTAINS PROPRIETARY INFORMATION AND IS FURNISHED WITH THE UNDERSTANDING THAT IT IS NOT TO BE USED,DISCLOSED OR REPRODUCED IN ANY MANNER WITHOUT THE APPROVAL OF LeCROY CORPORATION
Le Croy 4434 sheet 1 of 7 ECO 1001

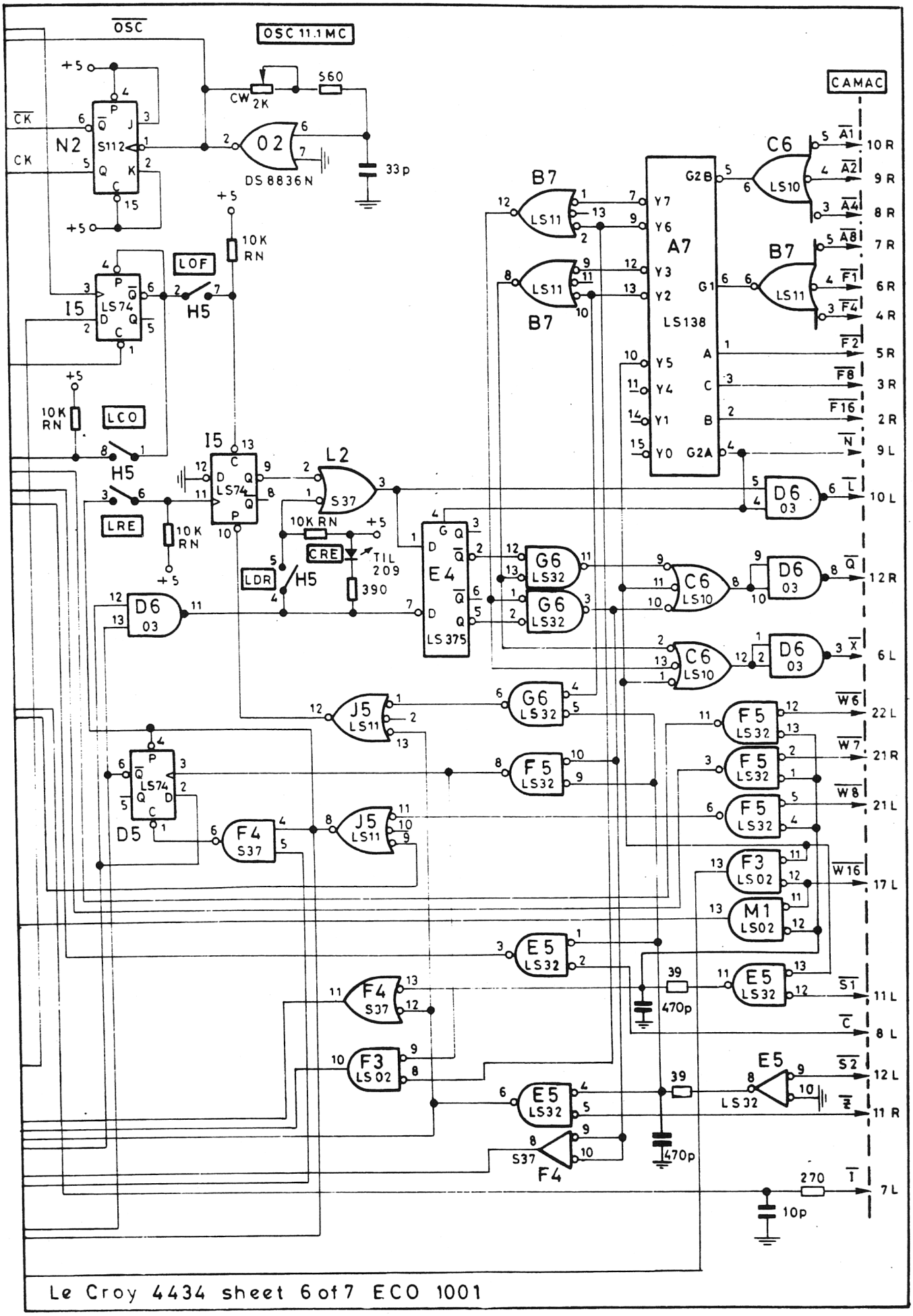

D8
H1
LS 251
D7
D6
D5
D4
D3
D2
D1
D0
H2
LS 138
Y7 G1
Y6
Y5
Y4
Y3
Y2
Y1
Y0
+5
G1
LS 399
C 2
C 1
10 OF
G2
LS 398
PL
BRD
K4
LS 112
G4
LS 191
I1
LS 251
I2
LS 138
J1
LS 251
J2
LS 138
K1
LS 251
K2
LS 138
G3
LS 139
G5
LS 00


BUS
SAD
BRD
BUS ADDR.
ON
AC
CR
CAMAC
FA
BD
RN
RC
80
500
Q2
LS174
Q3
LS 533
Q4
LS 533
Q5
LS 533
E2
P5
LS85
A6
LS 157
B6
LS 157
C5
LS 157
B5
LS 191
C4
LS 197
A5
LS 191
B4
LS174
A4
LS174
M2
26S02
O1
O2
10 K RN
DS 8836
2N 5770
6,8 K
10p
100p
12K
2,2k (2)
W 16
Le Croy 4434 sheet 3 of 7 ECO 1001

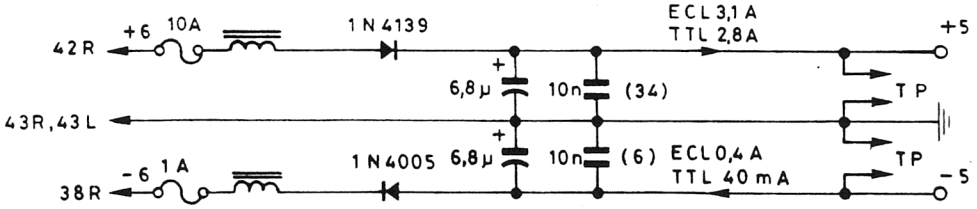

7403 (6)
CAMAC
F1
F2
N82 S09
(93419)
RES. NETWORK 2,7k (9)
E1
E3
E4
LS 375
LS 533
F3
LS 02
D1
D2
D3
D4
LS 283
C1
C2
C3
LS 373
CE A2 WE
CE A0 WE
OVL
Le Croy 4434 sheet 4 of 7 ECO 1001



Le Croy 4434 sheet 5 of 7 ECO 1001


OSC
OSC 11.1 MC
CAMAC
+5
CW 2K
S60
33p
CK
N2
S112
02
DS 8836N
10K RN
LOF
H5
I5
LS74
LCO
LRE
LDR
CRE
TIL 209
390
L2
S37
E4
LS 375
B7
LS11
A7
LS138
C6
LS10
D6
03
G6
LS32
F5
J5
F4
F3
LS02
M1
E5
D5
470p
39
270
10p
W6
W7
W8
W16
S1
S2
C
T
Le Croy 4434 sheet 6 of 7 ECO 1001

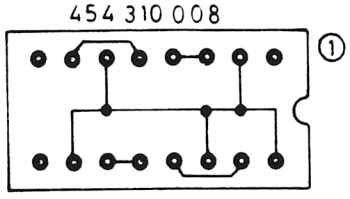
LeCROY	IC	DESIGNATION	- 5	GND	+ 5
200 031 028	74LS00	G5		7	14
200 031 051	74LS02	F3, M1		7	14
200 031 033	7403	A1, A2, A3, B1, B2, B3, D6		7	14
200 031 047	74LS10	C6, L1		7	14
200 031 077	74LS11	B7, J5		7	14
200 031 073	74LS32	G6, F5, E5		7	14
200 031 076	74S37	F4, L2		7	14
200 330 054	74LS54	H4		7	14
200 031 029	74S74	K5		7	14
200 031 049	74LS74	D5, I5, N1		7	14
200 041 043	74LS85	P5		8	16
200 041 008	74S112	N2		8	16
200 041 017	74LS112	K4		8	16
200 041 062	74LS138	A7, H2, I2, J2, K2		8	16
200 041 139	74LS139	G3		8	16
200 041 027	74LS157	A6, B6, C5		8	16
200 041 033	74LS174	A4, B4, Q2		8	16
200 041 042	74LS191	A5, B5, G4		8	16
200 031 097	74LS197	C4		7	14
200 041 251	74LS251	K1, J1, I1, H1		8	16
200 041 071	74LS283	D1, D2, D3, D4		8	16
200 071 373	74LS373	C1, C2, C3, P1, P2, P3, P4		10	20
200 041 375	74LS375	E4		8	16
200 031 101	74LS393	I4, J4		7	14
207 370 398	74LS398	G2		10	20
207 340 399	74LS399	G1		8	16
200 071 533	74LS533	E1, E3, Q3, Q4, Q5		10	20
200 042 005	96S02	M2		8	16
200 031 380	DS8836N	O2		1	8
200 062 009	N82S09N	F1, F2		14	28
208 031 003	NE521	Q1, R9	13	7	14
204 042 008	10125	R1, R2, R3, R4, R5, R6, R7, R8	8	16	9
210 080 408	LS408	H0, H3, I0, I3, J0, J3, K0, K3		4	9



NOTE :

- ECL COMPLEMENTARY INPUTS R1 = 56 Ohm (8), R2 = 10 KOhm (4)
- TTL NEGATIVE SINGLE ENDED INPUTS (OPTION MOD 100)
  R1 NOT USED, R2 = 560 Ohm (4)
  10125 (8) REPLACED BY JUMPER (8)

JUMPER : (8)



LeCroy RESEARCH SYSTEMS

DRAWN P.DAMIANO	MODEL 4434 LATCHING SCALER 32 CHANNEL
CHECKED JP.VITTET	
DATE 12.2.82	
DRAWING NUMBER 4434-S1	SHEET 7 OF 7
ECO NO 1001 DATE 27-01-84	