OPERATOR'S MANUAL

MODEL 4564
16 to 64 FOLD OR
LOGIC UNIT

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LeCroy

Innovators in Instrumentation

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1 GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the Model 4564. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

The Service Documentation, packaged separately, should be consulted for the schematics, parts lists and other materials that apply to the specific version of the instrument as identified by its ECO number.

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2 PRODUCT DESCRIPTION

OVERVIEW

The Model 4564 is a simple and versatile logic module which the front panel layout is shown in Figure 1. It consists of four groups (A,B, C and D) of 16 input OR's followed by a set of additional two fold and four fold OR and AND functions. These various logic outputs are simultaneously available on a rear-panel connector and the transit time is independent of the function. In addition, the outputs are capable of rates in excess of 100 MHz. Output width is dependent on the input pulse overlap. Figure 1 shows the front panel layout.

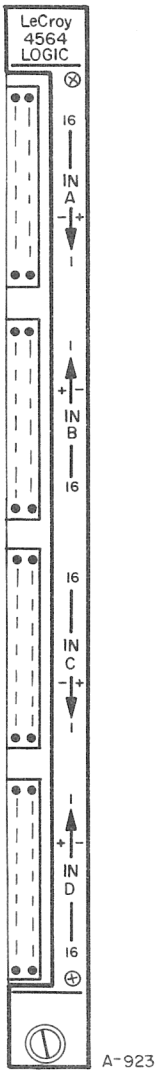


Figure 1
Front Panel Layout

For greater flexibility, the 4564 also offers four Discriminator/ Shaper channels which utilize LeCroy HVL100 hybrids. The thresholds of these hybrids are internally set for use with ECL levels. Internal jumpers allow any of the 12 logic combinations to be input to these channels. The output of Discriminators/ Shapers can be triggered on the leading or trailing edge of the input (jumper selectable) and the width is adjustable from 15 nsec to greater than 500 nsec. Output polarity is also selectable via internal switches. These outputs can be used simply as an adjustable width logic fan-out or can allow for more sophisticated functions.

Even more complex logic can be performed using additional 4564 modules or by feeding of the outputs of a module into a different input group of the same module. Of course in this case, the original inputs must be delayed for correct timing.

A typical application of the 4564 is to perform a simple track or pattern recognition for veto or gate applications of which examples are shown in Chapter 4.

SPECIFICATIONS

Input Characteristics

Signal Input: 64 in four 2 × 17 front-panel connectors, 110 Ω impedance. Minimum width 6 nsec, maximum frequency >100 MHz.

Output Characteristics

Overlap Outputs: Rear-panel 2 × 17 pin connector, pins 1 to 12. Output is differential ECL levels and width corresponds to overlap (±2 nsec) of inputs of logic function; minimum output width 5 nsec; maximum output frequency >100 MHz; transit time 12 nsec ±1 nsec typical, independent of logic function; double pulse resolution 10 nsec typical.

Shaped Outputs: Rear-panel connector pins 13 to 16. Any of overlap logic can be converted via jumper option to any of the four Discriminator/Shapers. Output is differential ECL levels and width is internally adjustable from 15 to >500 nsec. Output can be triggered in leading or trailing edge of inputs (jumper selectable); output polarity is internally switch selectable; maximum frequency: 30 MHz, double pulse resolution: 30 nsec.

Power: +6 V/150 mA, -6 V/1.5 A, -24 V/20 mA (10.4 W total).

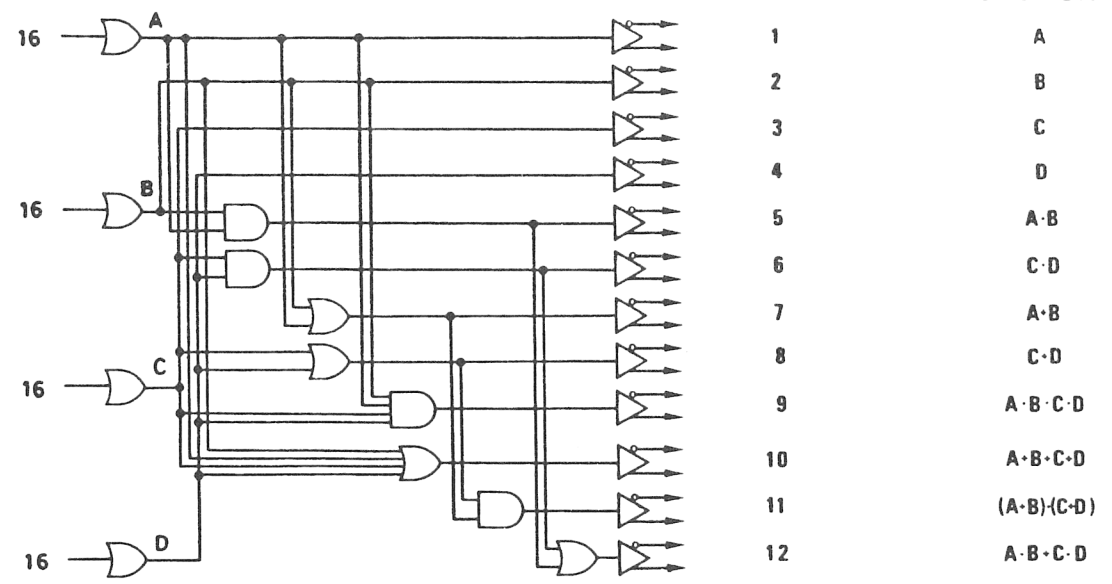
CONTROLS AND CONNECTORS

Signal Inputs

Signal inputs to the 64 channels of the module are made via front-panel 2-pin connectors in one of the four 16 input OR groups, A,B,C or D. All inputs require differential ECL levels of 6 nsec minimum width.

Outputs

Outputs of the module are available on the rear-panel 2 × 17 pin connector and are differential ECL levels. Pins 1 through 12 are for straight-through logic functions shown pictorially in Figure 2. The pulse width is equal to the overlap of the inputs to the logic function. Pins 13–16 are the outputs of the Discriminator/Shaper channels in which the output width is internally adjustable via internal potentiometers (see below). These output logic pulse can be triggered on leading or trailing edge (jumper selectable) of the selected inputs (logic functions). Pin 17 is not used.



Output Logic Diagram

Figure 2

The shaped outputs can be used for several different functions. Since the output width is adjustable, these outputs can be used to supply a standard logic output pulse of fixed duration for selected logic functions. This feature is important when using the 4564 with other units which require minimum input widths of standard ECL pulses and thus where the overlapped output may not be suitable. By using more than one Discriminator/Shaper channel, the unit can be used as an adjustable-width, normal or complementary logic fan-out.

For further flexibility the output pulse may be triggered on the leading edge of input to the Discriminator/Shaper channel or the trailing edge. This setup allows for more sophisticated logic functions.

Since the Discriminator/Shaper channels are used with the Overlap logic outputs of the 4564, the threshold of these internal discriminators are set to trigger at a level suitable with standard differential ECL signal levels. Therefore, all threshold parameters and uncertainties (i.e., hysteresis, minimum input charge input, etc.) usually associated with discriminators are minimized

due to the threshold setting and use of these levels. The exception is the double pulse resolution which is specified as 30 nsec typical.

Discriminator/ Shaper Controls

Output Width Adjust: four internal potentiometers allow the output width of the four shaped outputs to be adjusted from 15 nsec to greater than 500 nsec.

Polarity Switches: internal switches allow output polarity selection of the four shaped channels.

Function Selection: internal socket allows for jumper selection of logic function for each of the four Discriminator/Shaper channels and/or triggering on leading or trailing edge. See Chapter 3 for more details.

CAMAC COMMANDS

The 4564 is a high speed logic module and therefore does not have remote programmability.

3 INSTALLATION

GENERAL

The 4564 requires significant power from the -6 V line. It should be determined prior to installation whether the crate can support one or more 4564's with other modules which are to be used in the crate.

Prior to installation in the crate, the Discriminator/Shaper channels must be configured if they are to be used. Details on the location of the internal jumpers and potentiometers and instructions for setup can be found later in this chapter.

Once the unit is in the crate, input signals must be applied to the front-panel connectors. Since all 16 inputs of each of the four input groups are OR'd together, care should be taken to connect the inputs in such a manner to allow for the correct logic function to be performed. For example, two signals which are to be AND'd can not be connected to the same input group.

The desired outputs must then be connected to the appropriate pins on the rear panel. All Overlap logic functions are available at all times so that required connections are simply made. However, the four Discriminator/Shaper channels must be configured using internal jumpers and controls before an output is available. All outputs are differential ECL signal levels.

CABLES

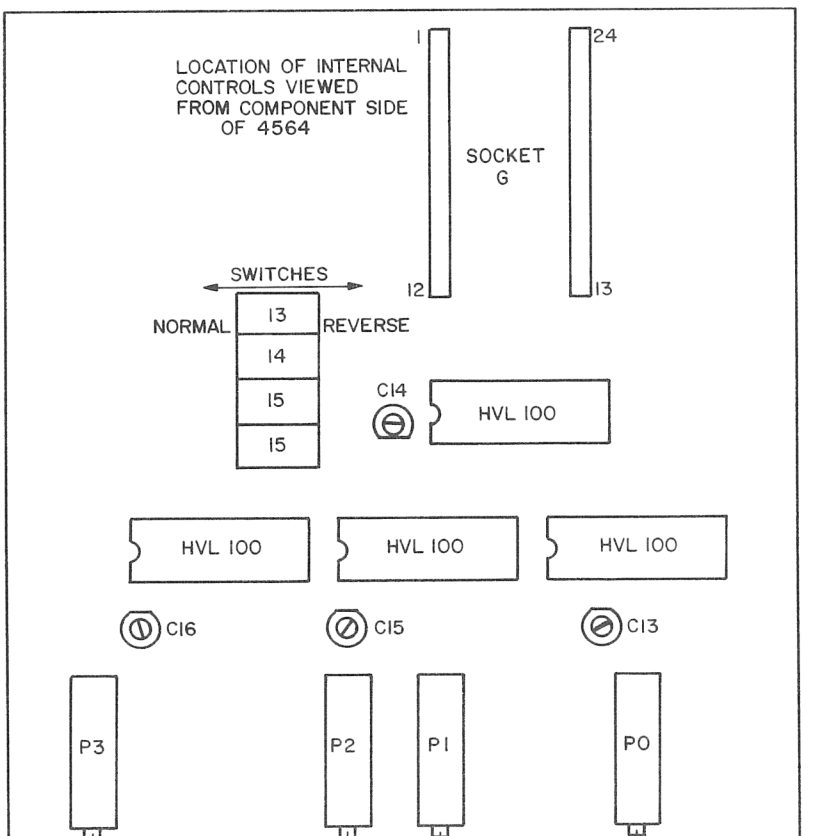
Interconnections between the Model 4564 and various other ECLine modules can be made either by multiwire cables or by single twisted-pair cables for one-to-one connections. Both of these types of cables muts be suitable for the transmission of differential ECL pulse pairs and, if desired, can be purchased from LeCroy. In particular, there are two types of multiwire cables available; one for short connections using flat cable and the second for long interconnections using twisted-pair and flat ribbon cable. The model numbers of these cables are as follows:

STC-DC/34-L Flat multiwire cable for short interconnections
LTC-DC/34-L Twisted-pair multiwire cable for
or DC/34-L for long interconnections
STP-DC/02-L Single twisted-pair cable, 3 foot maximum length.

Note that -L is the cable length in feet which should be specified by the user when ordering.

SETUP OF DISCRIMINATOR/ SHAPER CHANNELS

As mentioned previously, the Discriminator/Shaper channels must be configured by using internal controls and jumpers before use. These internal components include a jumper socket, four polarity switches and four potentiometers. Figure 3 shows the location of these components as viewed from the component side of the pc board. The Discriminator/Shaper channels can be used for several different functions and a more detailed explanation may be found in Chapter 2.



Location of Internal Controls Viewed from Component Side of the 4564

Figure 3

The first step in setting up the Discriminator/Shaper channels is to determine the logic function required and whether the output

of the channel should be triggered on the leading or trailing edge of the logic input signal. Table 1 lists the pin number and function available on Socket G. Table 2 lists the pin number, the channel and the edge triggering for the Discriminator/Shaper inputs.

Table 1

4564 Logic Function Outputs	Internal Socket G Pin #
A	24
B	23
C	22
D	21
A AND B	20
C AND D	19
A OR B	18
C OR D	17
A AND B AND C AND D	16
A OR B OR C OR D	15
(A OR B) AND (C OR D)	14
(A AND B) OR (C AND D)	13

Table 2

4564 Discriminator/Shaper Inputs	Internal Socket G Pin #
Channel 1 Leading Edge Trigger	2
Channel 1 Trailing Edge Trigger	3
Channel 2 Leading Edge Trigger	5
Channel 2 Trailing Edge Trigger	6
Channel 3 Leading Edge Trigger	8
Channel 3 Trailing Edge Trigger	9
Channel 4 Leading Edge Trigger	11
Channel 4 Trailing Edge Trigger	12

Once the required function has been determined, a jumper wire is connected from the appropriate pin on Socket G in Table 1 to the appropriate pin on the same socket listed in Table 2. The jumper wires can either be soldered into Socket G or can be made removable by using a wire with connection pins compatible with the socket. Up to four wires can be connected representing the inputs to the four Discriminator/Shaper channels. *Note that the wires should be as short as possible. Care should*

be taken so that the jumper wire, if not insulated, does not contact the module side cover.

Lastly, the output polarity is then selected and the output width is adjusted. Table 3 lists the potentiometers and switchs which correspond to each of the shaped output pins. The normal polarity is selected by moving the switch toward the rear of the module. Conversely, the reversed polarity position is toward the front of the module. The output widths are adjusted using four potentiometers P0–P3. The width is increased by monitoring the appropriate output channel with an oscillioscope with a probe suitable for differential ECL levels (such as the LeCroy Model 4001) and turning the potentiometer clockwise until the desired width is observed.

Table 3

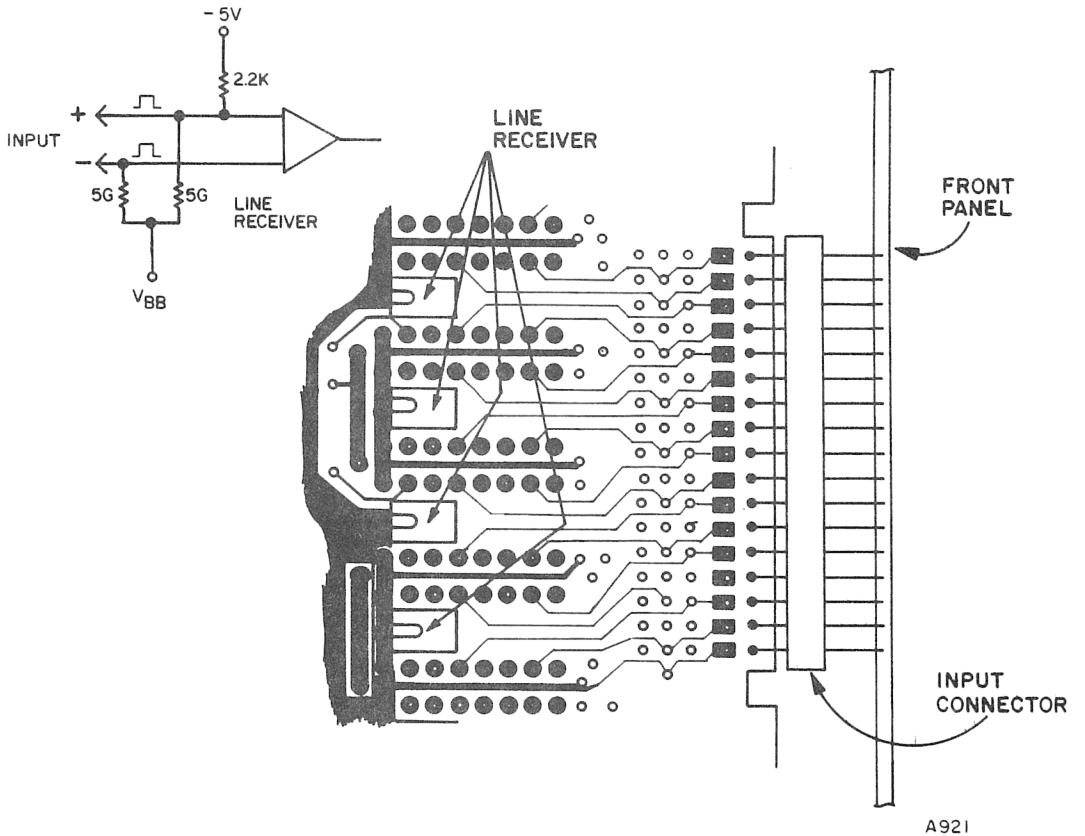
Shaped Output Pin #	Discriminator/ Shaper Channel	Corresponding Output Width Potentiometer	Corresponding Polarity Switch
13	1	P0	13
14	2	P1	14
15	3	P2	15
16	4	P3	16

CASCADING MODULES

All differential ECL inputs in the LeCroy ECLine modules are terminated inside the module by two 56 Ω resistors. These resistors are referenced to VBB, thus realizing a differential matching impedance of 112 Ω.

The input terminations are included in socket mounted, single in–line resistor arrays (sip packs). These arrays can be removed to make a high input impedance, thus allowing several modules to be driven by the same source in a bus configuration. The last module in this bus or daisy chain must be terminated for proper operation. Figure 4 shows the standard input stage of the ECLine module, the layout of the board and the location of the resistor arrays.

Please note that the arrays are not symmetrical and they must be mounted in the proper orientation.



Location of ECL Input Terminators

Figure 4

4 OPERATING INSTRUCTIONS

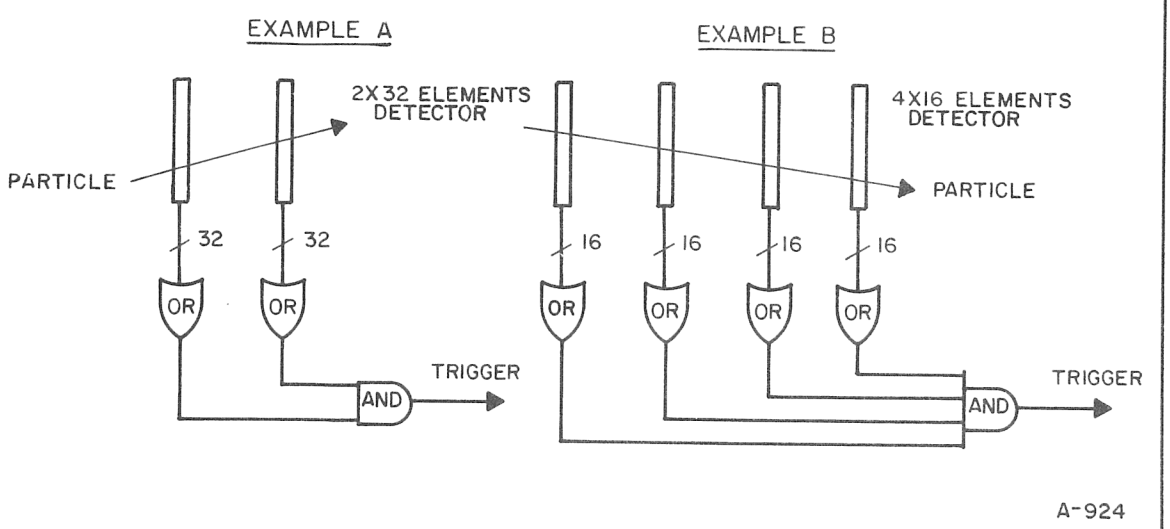
GENERAL

Since the Model 4564 does not have remote programmability nor any front-panel controls, there are no operational demands of the user other than setup and installation covered in the previous chapter. If additional outputs are required, the connections are made directly to the rear panel for the Overlap outputs. For Discriminator/Shaper channels, the side cover must be removed and internally reconfigured.

APPLICATION EXAMPLES

The 4564 is a simple and flexible multifunction logic module which can be used to solve Trigger/Veto logic problems. A few application examples shown in a simplified form follow.

A typical example of the use of the 4564 is shown in Figure 5. A "telescope" of beam chambers or plastic scintillator hodoscope planes is shown below where the 4564 can perform a simple track or pattern recognition. In this case, the data acquisition system is triggered only when a particle passes through any of the 32 detector elements in both of the two detector planes in example A or through all four planes in example B.

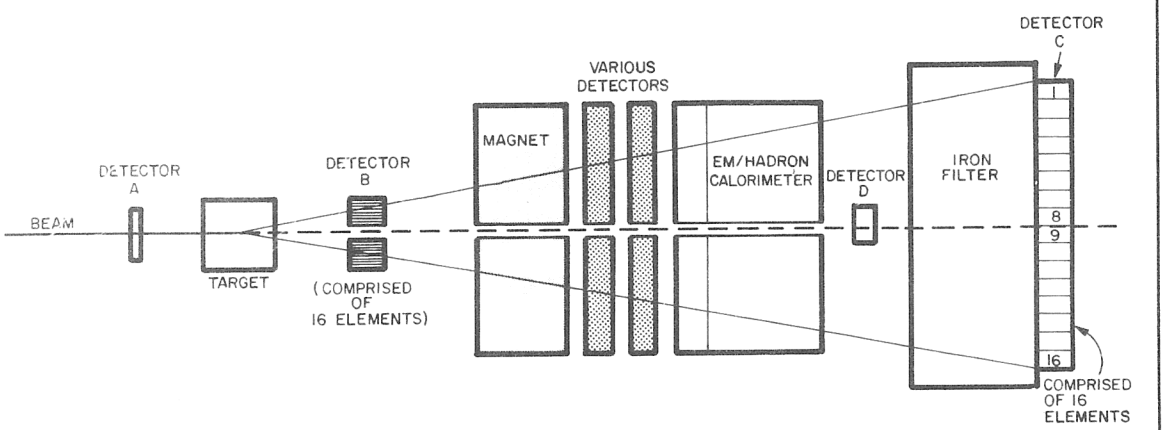


Block Diagram of a Hodoscope Trigger
Figure 5

The logic functions in these examples are (A OR B) AND (C OR D) which the Overlap output is available on pin 11 on the

rear panel and A AND B AND C AND D available on pin 9 respectively.

The final two examples are shown below in Figure 6 for a system veto and general trigger. In this simplistic example, events to be studied such as muons emerge out of the target off–axis. Therefore, a veto should be generated when all detectors in the beam line see an event. Conversely, a trigger should only be generated when the detectors A, B, C are hit, since the central elements of detector C are used to detect any event which is non–interacting in the system. The logic for the veto in this example is A AND (C8 OR C9) AND D while the logic for the general trigger is (A AND B AND C) NOT D.



Cross Section of a Fixed Target Experiment
Demonstrating an Example of a Veto and/or Trigger

Figure 6

The AND functions are straightforward. The outputs of the detectors are converted into ECL levels by a unit such as a discriminator and which are connected to the appropriate inputs of the 4564. The NOT function, seemingly more complex, is easily created by using a complementary input to Group D of the 4564. With ECL levels, this complementary signal is available by simply giving the ECL cable a half twist. More specifically, complementary signals are created by connecting the plus output pin of the discriminator to the minus input pin of the 4564 and vice versa. With the above setup the output for the system Veto or general trigger is available on pin 9 of the rear–panel connector.

5 THEORY OF OPERATION

The Model 4564 is a very useful unit which has a straight-forward and simple design. The module accepts differential ECL inputs which are connected to four separate input groups (IN A - IN D) comprised of 16 inputs per group. Each group uses four 10115 Quadruple Line Receivers for a total of 16 (A1 - A16) to convert the inputs to single-ended ECL. The change to single-ended logic allows for wire-OR'ing of the group inputs and allows more simple logic processing.

After conversion, the 16 fold OR signals are routed to four IC's which perform various logic functions. These ICs are NOR line drivers (C+D) an AND gate (F), and a OR/NOR gate (E). The outputs of these IC's are fed to quadruple OR/NOR gates (M-O) and 560 Ω pull down resistors which produce the resulting logic function outputs in true differential ECL. Note that two 10014 (B+H) which are used before and after the four logic IC's (C-F) to terminate the transmission lines between the gates and drivers.

Four Discriminator/Shaper circuits are included in the module to allow the user to set a preselected output width instead of being restricted to the overlap time of the inputs which satisfy the logic. In addition, the user can select (via jumpers) whether the outputs of the Discriminator/Shaper channels is triggered on the leading or trailing edge of the chosen logic function. The logic function to be used is selected by placing a jumper across the appropriate positions on socket G (see Chapter 3 for more details). Discrimination is performed by four HVL100 comparator hybrids labeled J-L. Output width can be set from 15 nsec to 500 nsec by adjusting the 1K trim pots P0-P3 and the polarity of the outputs is selected by four switches on the board (13-15). After discrimination/shaping, the signals go to an ECL driver P for conversion to differential ECL.

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