

MODEL 622
NIM LOGIC UNIT

CE

Revised
July, 1996

(ECO 1007)



Corporate Headquarters

700 Chestnut Ridge Road

Chestnut Ridge, NY 10977-6499

Tel: (914) 578-6013 Fax: (914) 578-5984

E-mail: lrs_sales@lecroy.com

lrs_support@lecroy.com

A T T E N T I O N

CRATE POWER SHOULD BE TURNED OFF DURING INSERTION AND REMOVAL OF UNIT TO AVOID POSSIBLE DAMAGE CAUSED BY MOMENTARY MISALIGNMENT OF CONTACTS.

THIS INSTRUMENT CONTAINS SEMICONDUCTORS THAT CAN BE DAMAGED BY ELECTROSTATIC DISCHARGE. SEE APPENDIX BEFORE REPAIRING OR HANDLING ANY COMPONENTS.

SEE POCKET IN BACK OF MANUAL FOR SCHEMATICS, PARTS LISTS, AND ADDITIONAL ADDENDA WITH ANY CHANGES TO MANUAL.

A T T E N T I O N

CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

WARRANTY

LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

In exercising this warranty, LeCroy will repair or, at its option, replace any product returned to the Customer Service Department or an authorized service facility within the warranty period, provided that the warrantor's examination discloses that the product is defective due to workmanship or materials and has not been caused by misuse, neglect, accident or abnormal conditions or operations.

The purchaser is responsible for the transportation and insurance charges arising from the return of products to the servicing facility. LeCroy will return all in-warranty products with transportation prepaid.

This warranty is in lieu of all other warranties, express or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. LeCroy shall not be liable for any special, incidental, or consequential damages, whether in contract, or otherwise.

PRODUCT ASSISTANCE

Answers to questions concerning installation, calibration, and use of LeCroy equipment are available from the Customer Service Department, 700 Chestnut Ridge Road, Chestnut Ridge, New York, 10977-6499, (914) 578-6030.

MAINTENANCE AGREEMENTS

LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

- Copy the software for backup or modification purposes in support of your use of the software on a single machine.
- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

SERVICE PROCEDURE

Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

TABLE OF CONTENTS

Page

SECTION 1 - SPECIFICATIONS

1.1	Technical Data Sheet	
1.2	Logic Inputs	1-1
1.3	Common Inhibit Input	1-1
1.4	Bridged Outputs	1-1
1.5	Fast Negative Timing Output	1-2
1.6	Complementary Output	1-2
1.7	Output Width	1-2
1.8	Output Width Uncertainty	1-2
1.9	Coincidence Characteristics	1-3
1.10	Coincidence Curve Method of Measuring Resolving Time	1-3
1.11	Timing Characteristics	1-4
1.12	Packaging	1-5
1.13	Power Requirements	1-5
1.14	Recommended Use of the NIM Power Bins	1-5

Figures for Section 1

FUNCTION 2 - FUNCTIONAL DESCRIPTION

2.1	General	2-1
2.2	Input Logic-Level-to-Analog Converter	2-1
2.3	Discriminator and Pulse Standardizer Stage	2-1
2.4	Timing Stage	2-2
2.5	Output Stage	2-3
2.6	Internal Power Supplies	2-4

Figures for Section 2

SECTION 3 - APPENDIX

Handling of Static Sensitive Semiconductors

Technical Data Sheet and
Module Photograph and Front Panel Features

365AL DUAL 4-FOLD MAJORITY LOGIC UNIT
465 TRIPLE 4-FOLD LOGIC UNIT
622 QUAD 2 INPUT LOGIC UNIT

- NIM Packaging
- High Speed
- Multiple Input
- Multiple Output
- Selectable Number of Coincident Inputs

FOR HIGH SPEED OPERATIONS

A logic unit generates a precise standard pulse when the inputs correspond to preset logical conditions. The inputs to the logic modules are standard NIM logic levels typically generated by a discriminator or another logic module. The inputs are restandardized and then compared to the setting of the module.

The logical conditions which can be selected are 4-fold, 3-fold (Model 365AL and Model 465), AND (all units) and an OR (Model 365AL and Model 622). If only one input is selected, then the units will act as a logic fan-out. The output of the logic module has a duration that is either the same period as the coincidence of the inputs (465) or is adjustable via a front-panel potentiometer for maximum flexibility. The output of a logic module is typically part of a trigger system which triggers, gates or disables a data acquisition system.

LeCroy's family of NIM logic modules are flexible and versatile. They offer a number of features and can be easily configured.

Corporate Headquarters: 700 Chestnut Ridge Road, Chestnut Ridge,
NY 10977-6499, USA. Tel: (914) 578-6013 Fax: (914) 578-5984
E-mail: lrs_sales@lecroy.com ■ lrs_support@lecroy.com
WWW: <http://www.lecroy.com>

European Headquarters: 2, rue du Pre-de-la-Fontaine, CH-1217 Meyrin 1
Geneva, Switzerland, Tel: (022) 719 2228 Fax: (022) 719 2230

FEATURES

Multiple Channels - Each module has up to 3 channels and has 2 or 4 inputs per channel. A minimum of 5 outputs are available.

High Speed - All modules have greater than 110 MHz operation. In addition, all channels have adjustable output pulse widths.

Selectable Logic Function - Each unit has a switch selectable logic function from 4-fold coincidence (365AL and 465), to majority logic (365AL) to AND/OR (622).

High Performance - All three modules experience no multiple pulsing, have good output width stability and as low as 5 nsec double pulse resolution.

FUNCTIONAL DESCRIPTION

LeCroy's NIM logic units offer flexibility, versatility, high speed and performance packaged in a single width NIM module. All together they provide the functions of majority logic, up to 4-fold coincidence, fan-in and fan-out and AND/OR Logic along with > 110 MHz operation. Each of the channels accept up to 2, Model 622, or 4, Model 365AL and Model 465, standard NIM logic signals.

Both the 365AL and the 465 have inputs which may be individually enabled or disabled without altering cabling or termination by means of front-panel switches. In the 465, with all inputs enabled, four inputs are required. Disabling the logic inputs is equivalent to reducing the number of simultaneous negative input signals required for an output. Thus, each channel may be programmed for 4-fold, 3-fold or 2-fold logic decisions. With only one input enabled, each channel operates as a logic fan-out.

The 365AL, however, has a selectable number of coincidence values to allow programming of one to

four simultaneous input signals required for an output. Thus, it can operate similar to the 465 or can be used for the majority logic as well as a logic fan-in. Alternatively, the 622 features 4 channels with switch selectable AND or an OR output condition of the two inputs.

All three units offer at least 2 sets of bridged outputs and at least one complementary output as well as continuously adjustable output pulse duration. The output pulse width is set via a front-panel screwdriver control pot from 5 nsec to 600 nsec for the 622. The outputs are highly stable and independent of input amplitude, duration and rate. All units are updating and can be retrigged before the end of an output pulse. The 465 also has bridged overlap outputs (-32 mA) whose output pulse width is equal in duration to the coincidence overlap.

Note that each unit can be used in a CAMAC crate with the Model 4501A NIM-to-CAMAC adapter.

SPECIFICATIONS

Model 365AL

INPUT

Logic Inputs: 4 Lemo-type connectors; 50 Ω impedance; negative NIM level input requirements; each input can be separately enabled or disabled.

Veto Input: Lemo-type connector; 50 Ω impedance; negative NIM level input requirements. Requires 3 nsec minimum width delayed 3 nsec from leading edge of input.

Bin Gate: Via rear connector; clamp to ground from +4 V inhibit; rise times and fall times < 50 nsec.

OUTPUT

Outputs: 3 pairs; 2 negative (quiescently 0 mA, -32 mA during output), one complementary (quiescently -32 mA, 0 mA during output).

Fan-out: 6-fold, if each output drives two 50 Ω loads. (Any used output pair should drive 25 Ω for proper amplitude and shape.)

Duration: Continuously adjustable from less than 4 nsec to greater than 50 nsec by means of front-panel screwdriver-adjustable potentiometer. Updating.

Output Rise and Fall Times: 1.2 nsec typical. Fall time is 2.2 nsec maximum at 10 nsec pulse width and longer.

GENERAL

Functions: AND; OR; Majority Logic; Leading Edge Inhibit; Complement; Pulse standardization without multiple pulsing; coincidence level determined by front-panel selector.

Coincidence Width: 1 nsec and up, determined by input pulse durations.

Rate: 150 MHz minimum.

Input-Output Delay: Approximately 10 nsec.

Double Pulse Resolution: Typical 5 nsec; (6.5 nsec for triple pulses).

Packaging: NIM single-width module; Lemo-type connectors used for all inputs and outputs.

Power Requirements: 55 mA at +12 V (increases to 120 mA if both channels in 4-fold coincidence), 165 mA at -12 V, 22 mA at -24 V.

Model 465

INPUT

Logic Inputs: 4; Lemo connectors; 50 Ω impedance; negative NIM-level input requirements; each input can be separately enabled or disabled by front-panel push-buttons.

Veto Input: Standard negative NIM-level signal, 3.5 nsec minimum width. Requires complete overlap of input coincidence for linear outputs and prompt overlap of the leading edge of the input signal that would otherwise create the coincidence condition for the preset outputs. (Veto should precede this leading edge by approximately 5 nsec in this case.)

Bin Gate: Via rear connector; clamp to ground from +4 V inhibits; rise times and fall times < 50 nsec.

OUTPUT

Preset: 3; one bridged negative (quiescently 0 mA, -32 mA during output) one complementary (quiescently -16 mA, 0 mA during output). Updating.

Overlap: One bridged negative; quiescently 0 V, -32 mA during output; duration equal to coincidence overlap. Non-updating.

Fan-Out: 5 fold, if each output drives a 50 Ω load.

Duration: Continuously adjustable from less than 5 nsec to greater than 500 nsec by means of front-panel screwdriver-adjustable potentiometer. Width stability better than $\pm 0.2\%/^{\circ}\text{C}$.

Output Rise Times: OUT: 2.0 nsec typical (maximum 2.5 nsec). $\overline{\text{OUT}}$: 2.2 nsec typical (maximum 2.5 nsec; 3.0 nsec with negative output unterminated).

Output Fall Times: OUT: 2.0 nsec typical (maximum 2.5 nsec). $\overline{\text{OUT}}$: 2.2 nsec typical (maximum 2.5 nsec). Both are slightly longer on wide output durations.

GENERAL

Functions: 2-fold, 3-fold, or 4-fold coincidences plus fan-out determined by selectively disabling logic input.

Coincidence Width: ≥ 1 nsec, determined by input pulse durations.

Rate: 0 to > 120 MHz.

Input-Output Delay: 13 nsec for preset outputs; 8.5 nsec for overlap output.

Double Pulse Resolution: 8 nsec.

Multiple Pulsing: None; one and only one output pulse of preset duration is produced each time the input conditions are satisfied regardless of the duration of the input pulses or their overlap.

Packaging: Single-width AEC/NIM module; in conformance with AEC standard; Lemo connectors used for all inputs and outputs.

Power Requirements: 65 mA at +12 V, 135 mA at -12 V, 125 mA at +6 V, 640 mA at -6 V, 5 mA at -24 V.

Model 622

INPUT

No. of Channels: 4, all identical.

Logic Inputs: 2, 50 Ω direct-coupled; reflections < 7% for standard negative NIM of 2 nsec rise time.

Veto Input: Front-panel connector permits simultaneous inhibiting of all channels; 50 Ω ; requires negative NIM-level signal; direct-coupled; must overlap leading edge of input signal that would otherwise cause the coincidence condition; must precede input by approximately 5 nsec.

Bin Gate: Via rear connector, with rear-panel ON/OFF switch; quiescently +4 V, clamping to ground inhibits logic unit; direct-coupled; rise times and fall times approximately 50 nsec.

OUTPUT

Bridged Negative: 2 pairs; NIM (quiescently 0 mA, -32 mA during output), duration, 5 nsec to 1 μsec , continuously variable up to 600 nsec via front-panel screwdriver control (narrower widths possible at slight expense of amplitude); rise times and fall times (all outputs terminated in 50 Ω) typically 2.0 nsec (maximum 2.5 nsec). Output fall times slightly longer on wide output durations. Width stability better than $\pm 0.2\%/^{\circ}\text{C}$ maximum. Updating.

Fast Negative Timing: One NIM (quiescently 0 mA, -16 mA during output). Other characteristics same as above, except rise times are typically 1.5 nsec (maximum 2.0 nsec) and minimum width is ≤ 6 nsec.

Complementary: One NIM (quiescently, -16 mA, 0 mA during output). Other characteristics same as for Fast Negative Timing Output.

GENERAL

Functions: Fan-in (2-fold); coincidence; inhibit.

Coincidence Width: Determined by input pulse durations; total widths approximately 1.0 nsec and up.

Rate: 110 MHz typical, input and output.

Input-Output Delay: 9.5 nsec typical.

Double Pulse Resolution: < 9 nsec at minimum output width setting.

Multiple Pulsing: None; one and only one output pulse of preset duration is produced for each input pulse, regardless of input pulse amplitude or duration.

Packaging: In RF-shielded, AEC/NIM #1 module (AEC Report #TID-20893); Lemo-type connectors.

Power Requirements: 450 mA at -6 V, 215 mA at +6 V, 165 mA at -12 V, 20 mA at +12 V, 85 mA at -24 V.

NIM LOGIC UNIT SELECTION CHART

Model	365AL	465	622
INPUT			
No. of Channels	2	3	4
No. of Inputs	4	4	2
FUNCTION			
Logic	Majority 4-fold selectable coincidence level	Up to 4-fold	AND/OR
GENERAL			
Packaging	Single-width NIM	Single-width NIM	Single-width NIM
Maximum Rate	150 MHz	120 MHz	110 MHz
D.P.R.	5 nsec (6.5 nsec for triple pulses)	8 nsec	< 9 nsec
OUTPUT			
No. of Outputs	4 NIM, 2 $\overline{\text{NIM}}$	Preset: 2 NIM, 1 $\overline{\text{NIM}}$ Overlap: 2 NIM	4 NIM, 1 Fast NIM Timing, 1 $\overline{\text{NIM}}$
Width	4 nsec to 50 nsec	5 nsec to 500 nsec (preset only)	5 nsec to 1 μsec
POWER			
-24 V	22 mA	5 mA	85 mA
-12 V	165 mA	135 mA	165 mA
-6 V	600 mA	640 mA	450 mA
+6 V	425 mA	125 mA	215 mA
+12 V	55 mA (120 mA if both in 4 fold coincidence)	65 mA	20 mA

SECTION 1

SPECIFICATIONS

1.2 Logic Inputs

The Model 622 has direct-coupled, 50 Ω impedance inputs which accept fast NIM logic signals. These inputs, typically driven from a discriminator or other logic unit, are protected both for transient and DC signals up to ± 5 V. Since the input reflections are less than 7% for signals of as little as 2 nsec risetime, even the maximum level signal in the NIM-specified range for a logic input (i.e., -1.8 V) will reflect only approximately 125 mV, eliminating the probability of accepting multiple pulses corresponding to only one original input pulse.

1.3 Common Inhibit Input

The common inhibit input of the 622 requires NIM logical one input signals. In order to inhibit (veto) a coincidence, the applied veto pulse must overlap the entire input signal that would otherwise cause the coincidence condition. Due to internal delays, the leading edge of the veto signal should precede the coincidence by at least ≤ 5 nsec (see Figure 1.1).

To veto signals when the 622 is set in the "OR" condition, the inhibit signal must merely overlap the pulse it is to inhibit, subject to the $\{5$ nsec delay mentioned above.

1.4 Bridged Output

The Model 622 has two pairs of current source 50 Ω outputs, delivering -32 mA of current during the output and 0 mA quiescently. These outputs are of the switched current source type, requiring no quiescent current and permitting extremely low power dissipation in the total circuit. The standard switched current outputs maintain a risetime of 2.5 nsec and a reasonably clean shape, as long as care is taken to terminate at least one-half of the other bridged output in that channel.

The shape of typical outputs from a 622 are shown in Figure 1.2.

Using the typical output pulse shape in Figure 1.2 as a visual reference, LRS output shapes for current switched outputs (such as on Models 622, 621L, 621AL, 621BL,

621BLP) are set up to adhere to the restrictions in Figure 1.3, with adjacent output pair terminated into 50 ohm.

In applications where it is necessary to drive very long cable lengths from a logic unit output it is common to use only one half of the bridged 32 mA output and to leave the other half unterminated. This effectively sends all 32 mA into the one cable, giving nearly a double amplitude output. It is important to know that the 622 has clamp diodes that limit the output amplitude so as not to saturate the output transistors. This limit is approximately -1.4 V. It cannot be assumed, therefore, that the 32 mA into one 50 ohm cable will give a 1.6 volt output signal.

1.5 Fast Negative Timing Output

The fast negative timing output on the 622 is a full differential type current source output. Its name originates from the shorter risetime (1.3 nsec vs. 2.5 nsec) compared with the other 4 negative outputs on the 622. Because the risetime is much faster, there is less timing inaccuracy created by differing "threshold" levels of subsequent circuits.

1.6 Complementary Output

The single complementary output is actually the output from the collector of the other half of the differential pair supplying current to the fast negative timing output. It is a 50 ohm output with quiescent level at -16 mA, and logical 1 at 0 mA. Risetime and other characteristics are similar to that of the fast negative timing output.

1.7 Output Width

The output range of the Model 622 is 5.0 nsec to 1 μ sec, continuously adjustable via front-panel potentiometer. Because the potentiometer is very sensitive beyond 600 nsec, it is actually almost impossible to set the width between 600 nsec and 1 μ sec. As a result, the specifications indicate continuous adjustment up to 600 nsec, with a = 1 μ sec setting at the far end of the pot.

1.8 Output Width Uncertainty

External conditions are the main contributions to output uncertainty in the Model 622. Variations in both temperature and NIM bin voltage can cause slight changes

in output width with consequences that may be adverse to subsequent coincidence measurements. If the output pulses are to be simply counted, then the leading edge is the important factor and width variations are unimportant.

Figure 1.4 indicates the uncertainty in output width of the 622 as a function of reasonable variations in temperature and supply voltage. Since the 622 has power supply regulation in it and is very well temperature compensated, the width variations are small.

1.9 Coincidence Characteristics

Minimum Coincidence Overlap (Coincidence Resolving Time): The required coincidence overlap time of two input signals with the 622 set in the "AND" mode is approximately 1.1 nsec. Although this measurement should be made with two pulses of zero risetime for an absolute result, functionally, no discriminator or other logic unit driving the 622 could output such fast pulses. The measurements on the 622 were therefore made with an LRS Model 161 Dual Discriminator of 1.5 nsec risetime and falltime.

One method used at LRS is to measure the overlap time is as follows. Two 10 nsec FWHM pulses from a single source are initially separated in time and fed into the inputs of the Model 622. The output of the 622 is displayed on an oscilloscope which is being externally triggered by the source (see Figure 1.5). One pulse is then moved in time until it begins to overlap the other pulse. Initially, no output will appear from the 622 (see Figure 1.6). At some duration of overlap, output pulses will always appear. The minimum coincidence overlap is defined in LRS terminology as that amount of overlap which produces one output on the average for every two sets of inputs (i.e., 50% point). From the waveforms below this is equal to $T_2 - T_0$. The 50% point can be quite accurately estimated on the oscilloscope (externally triggered) by adjusting the second pulse delay for equal intensity of trace (of the output states) for the duration of the output pulse. The minimum resolving time for the Model 622 is 1.1 nsec. The resolving time jitter can also be measured by taking the difference between the 0% limit and the 100% limit ($T_3 - T_1$). The resolving time jitter for the Model 622 is ± 20 psec.

1.10 Coincidence Curve Method of Measuring Resolving Time

An alternate method used at LRS to measure the resolving

time and time jitter involves making a coincidence curve and then measuring its "risetime" and "falltime". Two pulses from a single source are initially separated in time and fed into the inputs of the 622, at the same time being collectively counted in a scaler (see Figure 1.7). The 622 output is also counted into another scaler channel.

As the variable delay is adjusted, the two pulses become more coincident. By comparing the counts in the two scaler channels at different delay amounts, a curve can be made representing Rate Out/Rate In vs. Time Delay where the time delay is measured from the trailing edge of Pulse A to the leading edge of Pulse B. (The previous waveform diagram is valid for this measurement also, except Pulse A delay should be continued until its leading edge is past the trailing edge of Pulse B).

The resultant coincidence curve for this measurement appears in Figure 1.8.

The minimum coincidence overlap or minimum resolving time of the logic unit is defined as one-half the difference between the sum of the input pulse widths and the coincidence width measured above. Alternately (but with more difficulty), if t_0 represents the time at which pulse A trailing edge and Pulse B leading edge are exactly coincident in time, then the minimum resolving time is equal to $t_2 - t_0$.

If input pulses A and B are identical in shape, and if the inputs to the coincidence unit are identical, the trailing edge side of the coincidence curve should be symmetrical to the leading edge. If they differ, the larger one (either 0% to 100% or 100% to 0%) is specified as the resolving time jitter.

It is important to note that the major contribution toward resolving time jitter in typical logic units is the instability of the "threshold" level of the differential amplifier following the input "AND" stage, particularly for inputs with slow inherent risetimes (i.e., ≥ 2 nsec). In the 622, a true high sensitivity discriminator is used which has a very stable and jitter-free threshold (the LD601C hybrid used in all LRS multichannel NIM discriminators). For this reason, the resolving time jitter of the 622 is quite small.

1.11 Timing Characteristics

Maximum continuous pulse train (CW from RF terminology)

rate capability of the 622 is guaranteed at 100 MHz. Typically, the maximum rate is 110 MHz, with some units being capable of operation up to 120 MHz for small bursts of input pulses. The measurement for maximum rate is made by applying pulses to one of the two inputs, with the mode switch set in the "OR" position.

The double pulse resolution (DPR), as opposed to CW rate capability, defines the speed of a logic unit in high energy physics applications, since the double pulse or the pulse burst is apt to occur, whereas a CW input pulse train would be unlikely. For a logic unit in the "AND" mode, the coincidence width of the input pulses would limit the double pulse resolution of the unit. Each input itself is capable of operation at a 110 MHz CW rate and a DPR of 9 nsec. This measurement is made by setting the 622 in the "OR" mode, putting in two 4 nsec FWHM pulses spaced approximately 10 nsec apart at the half maximum points (i.e., -375 mV for a -750 mV input signal) and finding how far this 10 nsec time difference can be lowered before the 622 output pulse achieves only a 50% firing rate (i.e., Rate Out/Rate In = 0.5). Alternately, with the 622 set in the "OR" position, two pulses can be fed from different cables into the two inputs. By varying the time from leading edge of one (half max. point) to the leading edge of the other, the DPR can be measured. Care should be taken to use pulses of as narrow a width as possible when measuring minimum double pulse resolution.

1.12 Packaging

The 622 Quad Coincidence Unit is packaged in a #1 NIM module with Lemo-type connectors. Due to front-panel space limitations, the 622 is not offered with BNC's.

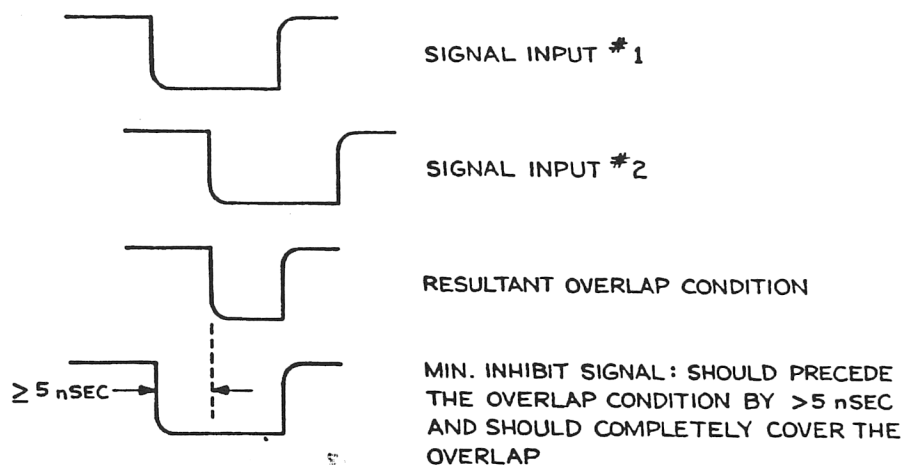
1.13 Power Requirements

The current usage of the 622 is low enough to permit the use of the 12 modules per standard 96-watt NIM bin offering 5 A of +6 V, 2 A of ± 12 V, and 1 A of ± 24 V. The maximum power used is 7.8 watts, which does not exceed the 8 watts recommended by the NIM standard for the maximum power dissipation for a single NIM slot.

1.14 Recommended Use of the NIM Power Bins

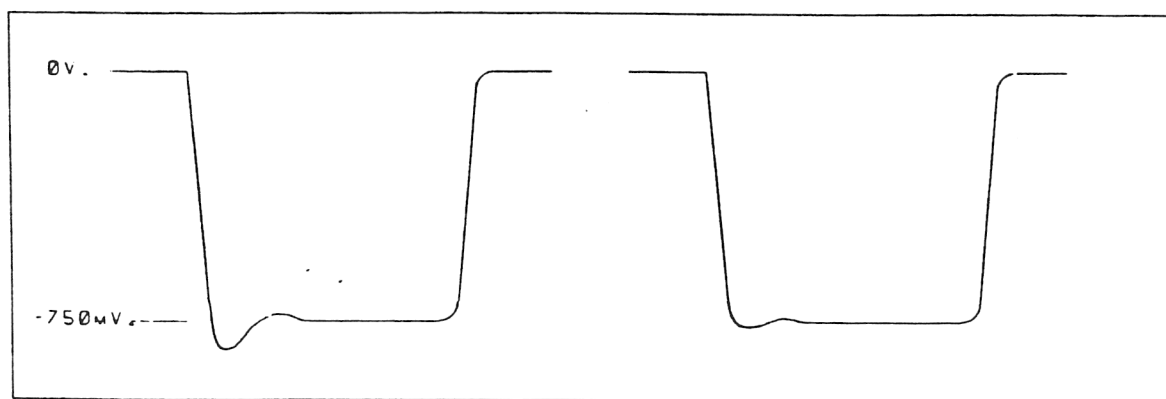
It is highly recommended to keep any NIM bin at as constant a temperature as possible, using air conditioning in the trailer or experimental station and definitely using fans to assure an air flow through all

modules in every bin. Elimination of large temperature variations removes the worry of temperature drift effects upon modules of any manufacturer, and the forced air flow is good insurance against the potential failure of components in the modules due to excessive heating for extended periods of time. Despite the fact that all components are pre-aged and burned-in before insertion into LRS modules, and the modules themselves are temperature cycled for days under power between initial test and final test, it is recommended to avoid subjecting any modules to adverse operating conditions if it could be avoided.



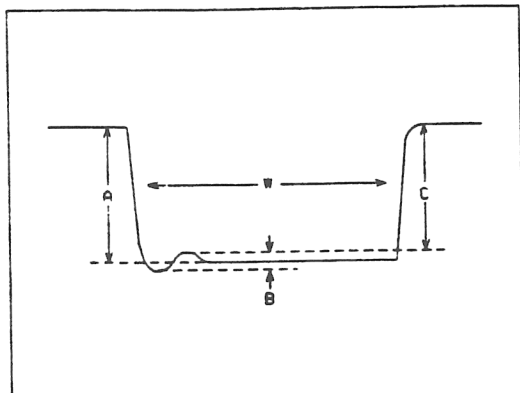
INHIBIT INPUT - SIGNAL INPUT OVERLAP REQUIREMENT

Figure 1.1



MODEL 622 OUTPUT WAVEFORMS

Figure 1.2



AMPLITUDE: $-700\text{mV} < A < -850\text{mV}$.

OVERSHOOT: $B < 10\%$ OF A; C DOES NOT REACH -600mV

RISETIME: $< 2.5 \text{ NSEC.}$

FALLTIME: $< 2.5 \text{ NSEC. AT MINIMUM WIDTH.}$

MINIMUM WIDTH: $W_{\text{MIN}} \text{ (FWHM)} < 5.0 \text{ NSEC.}$

MAXIMUM WIDTH: $W_{\text{MAX}} \text{ (FWHM)} = 1 \text{ USEC.}$

Figure 1.3

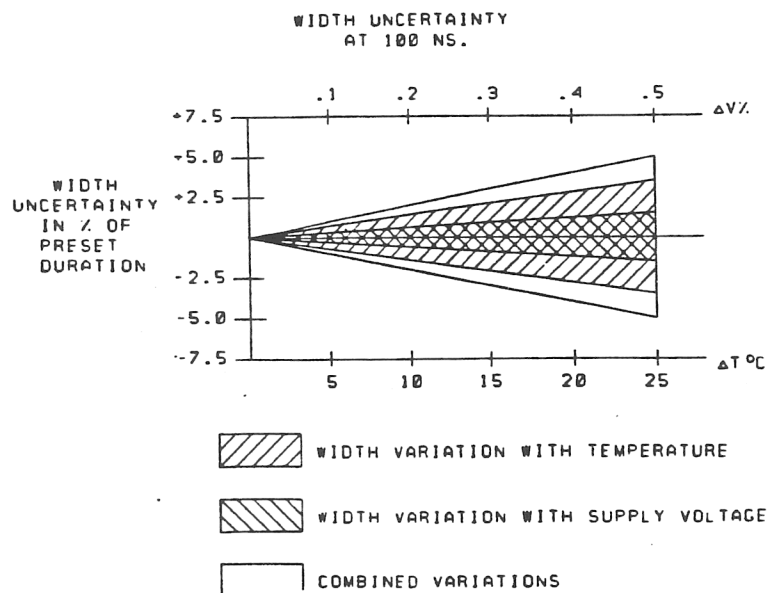


Figure 1.4

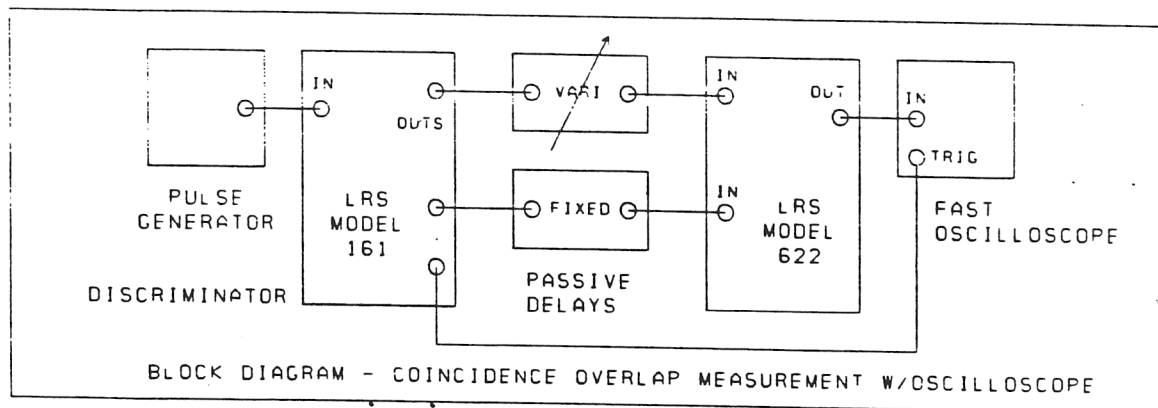


Figure 1.5

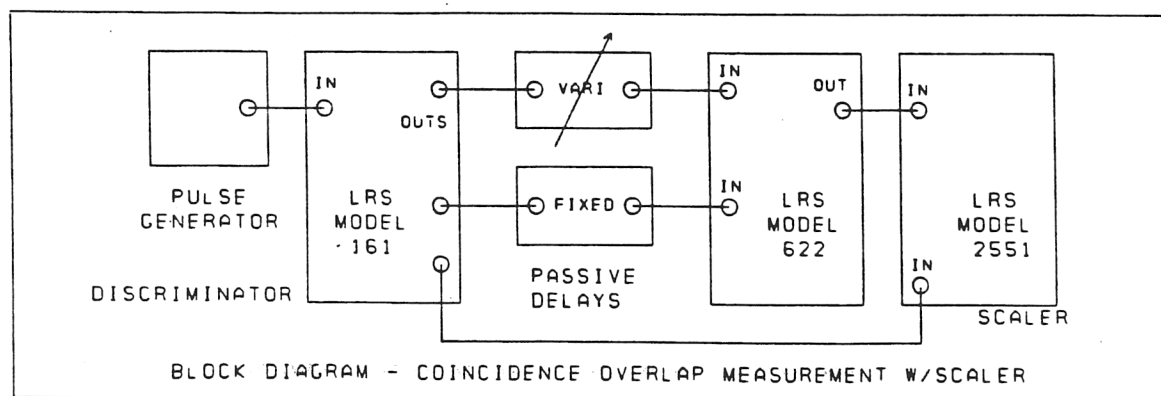


Figure 1.6

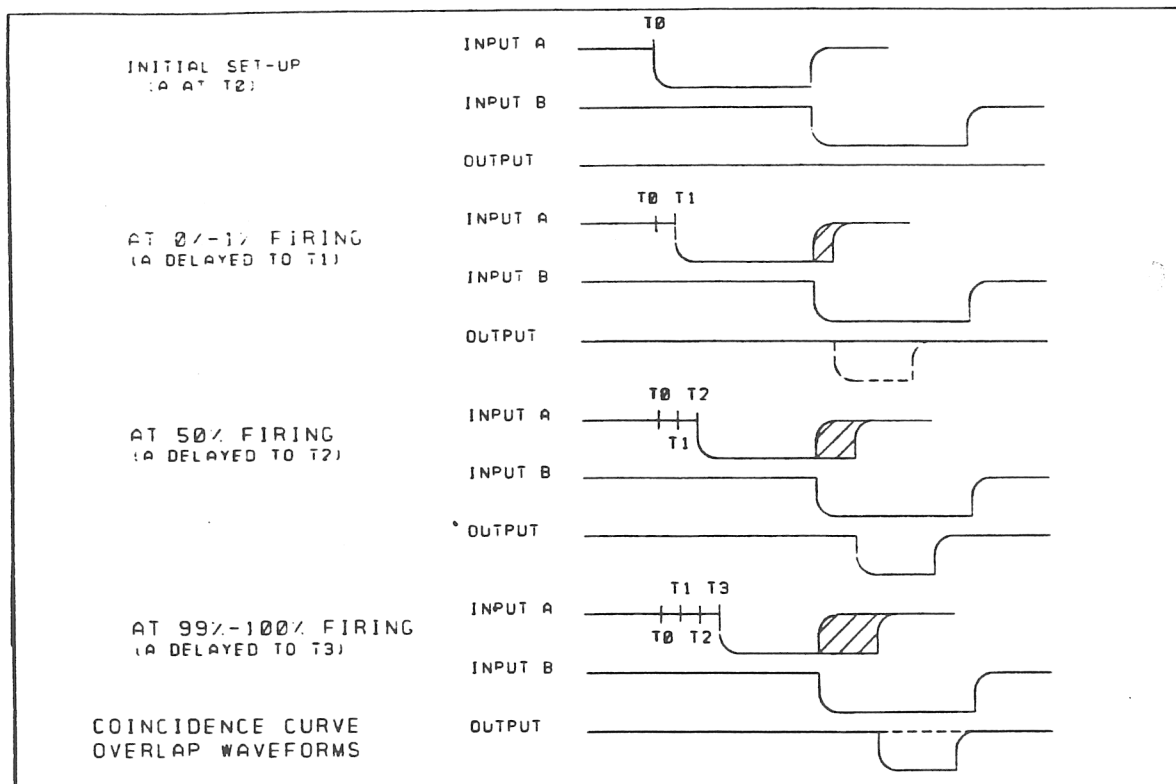


Figure 1.7

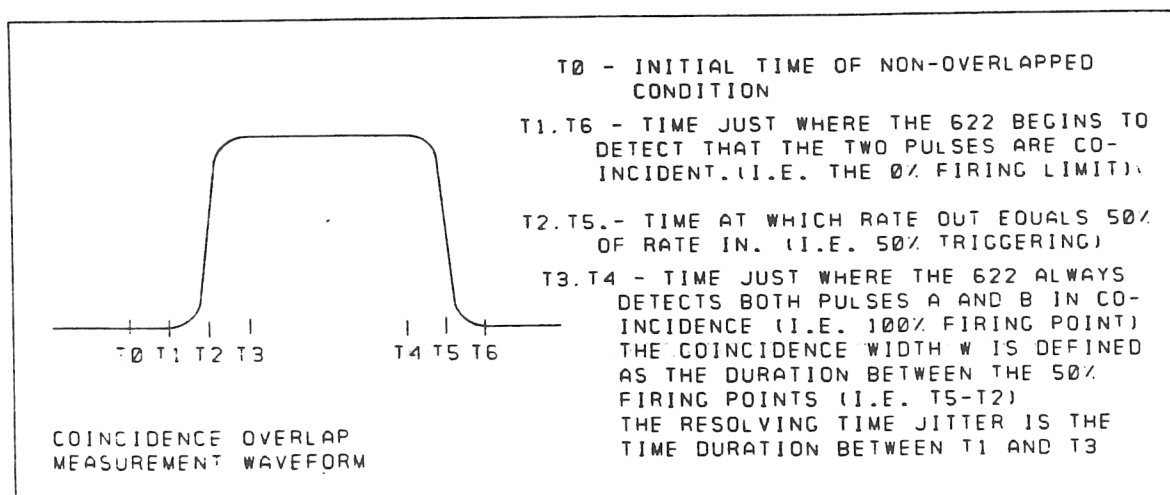


Figure 1.8

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 General

Each of the four channels of the Model 622 is composed of four basic sections. The Input Logic-Level-to-Analog Converter, the Discriminator Stage, the Timing or Pulse-Former Stage, and the Output Stage. A block diagram of the Model 622 can be in Figure 2.1 and a complete schematic can be found at the end of this manual.

2.2 Input Logic-Level-to-Analog Converter

The input stage accepts two inputs, and (via a two diode current switch) removes one unit of current per input from the resistor diodes connected to the -IN of the LD601C. The result is that with no inputs, the voltage at -IN is near zero V, with one NIM-level input the -IN voltage will go to about -250 mV, with two inputs it goes to about -450 mV to detect the existence of two time coincident inputs (AND mode).

2.3 Discriminator and Pulse Standardizer Stage

The discriminator and pulse former stage is based on the LRS Model LD601C hybrid. This unit contains all of the circuitry of the discriminator as is functionally presented below. The threshold level is set by changing the voltage bias on a fast differential amplifier which has a small amount of internal positive feedback to provide regeneration at threshold. In actual operation the V_T is grounded, and the threshold level is determined by the 2.5:1 (AND) or 4:1 (OR) voltage divider (composed of the switch selected external 150 Ω or 300 Ω resistor and the internal 100 Ω resistor) operating from -0.8 V (Figure 2.2).

When an input signal applied to -IN is equal to the threshold voltage at +IN the amplifier output will begin to go positive. This will force +IN closer to 0 V, which increases the differential input voltage in such a direction that the output locks and then the cycle reverses. The amplifier output thus provides a time-over-threshold pulse with fixed amplitude. This pulse can be monitored at the AMPL. OUT point (Pin 6). The quiescent level should be nominally -2.4 V going to -1.6 V during the pulse. The leading edge of this output

sets the latch circuit which is used as a pulse width standardizer. Before the amplifier and the latch can be set, the inhibit inputs (used for the bin gate and veto) must be off. The required level at Pins 7 and 16 of the LD601 must be 0 to -1.6 V to enable, and -2.5 to -6.0 to disable. The purpose of the first inhibit is to avoid generating a low level transient at the output associated with the leading edge of an amplified input pulse inhibited at the dV/dt stage only. (The common inhibit driver provides a level shift so that 0 V at the bin gate or -600 mV at the veto input will inhibit, greater than +3 V at the bin gate input or 0 V at the veto input will enable). Once the latch is set, a latch OUTPUT is available to start the 622 timing stage. The OUTPUT amplitude and leading edge should be similar in appearance to the AMPL. OUT above, but the width of the output will be fixed independent of the input width. Internally, the latch output is fed back to reset the latch after a short time delay, thus generating a short output pulse whose actual width can be set by the proper external section of RC time constant and voltage levels at Pin 3. It is set at approximately 3 nsec in the Model 622.

Older 622's used LD601B hybrids, while more recent units use LD601C's. These two hybrids are identical and interchangeable.

2.4 Timing Stage

The timing or pulse-forming stage of the 622 utilizes three stages of MC1692 MECL receiver for amplifying and shaping. The timing is done by first charging a 33 pf capacitor with the pulse from the LD601C (via one MC1692 stage) and the differential stage (composed of two A430 transistors) until it is clamped by the FD777 diode to a voltage set indirectly by the front-panel width potentiometer (via two stages of 747). The discharge rate is set by the current source stage composed of the width potentiometer, one stage of 747, the current source transistor, and its associated 604 Ω emitter resistor. The actual current is varied from near zero (for the 1 μ sec maximum width) to about 10 mA (for the 5 nsec minimum width). Thus, simultaneously, as the width is increased, the clamp voltage is increased (allowing more initial charge to be stored on the timing capacitor) and the current is decreased (reducing the rate of discharge), thus multiplying the effect of the width control. An internal trim resistor, T, sets the minimum width to 5 nsec. The effect of the 2N5962 and the diodes associated with it are to provide fast recovery of the

timing capacitor. The 1692 ECL amplifiers are interconnected in a manner to provide stable leading edge timing and fast risetimes and falltimes of the output pulse. The first amplifier (output pin 3) provides final shaping and standardization of the pulse from the LD601C to the timing stage, as well as driving the output stage directly via a second 1692 amplifier (output pin 14). This provides a prompt output pulse for the duration of the 601C output, independent of the delay encountered in initializing the timing stage. Before the 601C output is over, the timing capacitor is charged, causing the third 1692 amplifier (output pin 15) to now maintain the pulse level to the output stage (using emitter ORing until the timing capacitor is subsequently discharged to a sufficiently low level (approximately -2.0 V)). At this point (because of regeneration) the third amplifier promptly switches back to its quiescent off condition, terminating the output pulse.

2.5 Output Stage

The output stages of the 622 utilize two different types of circuits. The single normal and complementary outputs use a conventional differential stage. This stage requires a continuous 16 mA of current which is quiescently available at the complementary output connector. During an output pulse, the MC 1692 receiver will switch from the quiescent level of -2.4 V to a higher level of -1.6 V, causing the differential stage to switch the 16 mA current from the complementary to the normal output connector for the duration of the pulse. The other two pairs of outputs each supply 32 mA of current during the pulse, because at this time the bases of the two A430 transistors are at -1.6 V. The emitters are therefore at about -2.4 V. This places about 600 mV across each 16 Ω emitter resistor, and the resulting 32 mA will be available at each output connector pair for the duration of the pulse. Quiescently, the bases of these transistors are at -2.4 V; therefore, there is only a -600 mV drop available for V_{BE} so the transistors are off, resulting in a substantial power saving.

All outputs are diode clamped so they will provide proper operation even without output loads. Without the diode path for the current during the pulse, even on a single output stage, the current would have to be supplied via the transistor base, which would severely load the driver and not allow proper drive to the remaining stages.

The amplitudes of the Model 622's can be trimmed, if necessary, with resistors (labeled T) in parallel with

the 10 Ω emitter resistors.

2.6 Internal Power Supplies

Four internal power supplies are used to generate the -0.8, -2.35, -3.0, and -11.5 V which are special bias voltages used by the four channels. These stages provide voltage regulation and tracking and provide proper temperature compensation for the other sections, particularly the width and threshold circuits. They depend to some degree on uniform heating of the entire circuit board. Heating local areas of the board may cause drifting, but during use in a normal bin environment, these supplies compensate to stabilize operation. In all cases, the power supply uses a LM301 operational amplifier to maintain the output voltage of a series-pass transistor equal to an input reference voltage. The reference voltages are adjusted via individual potentiometers or trimmed resistors.

If the -6 voltage is sequenced on before the +6 voltage, the LD601C may be forced into a DC latched condition. To prevent this, a relay contact does not supply the -6 VDC until the relay coil, operating from the +6 VDC, is energized. This insures that the +6 is up before the -6 in any power-on sequence.

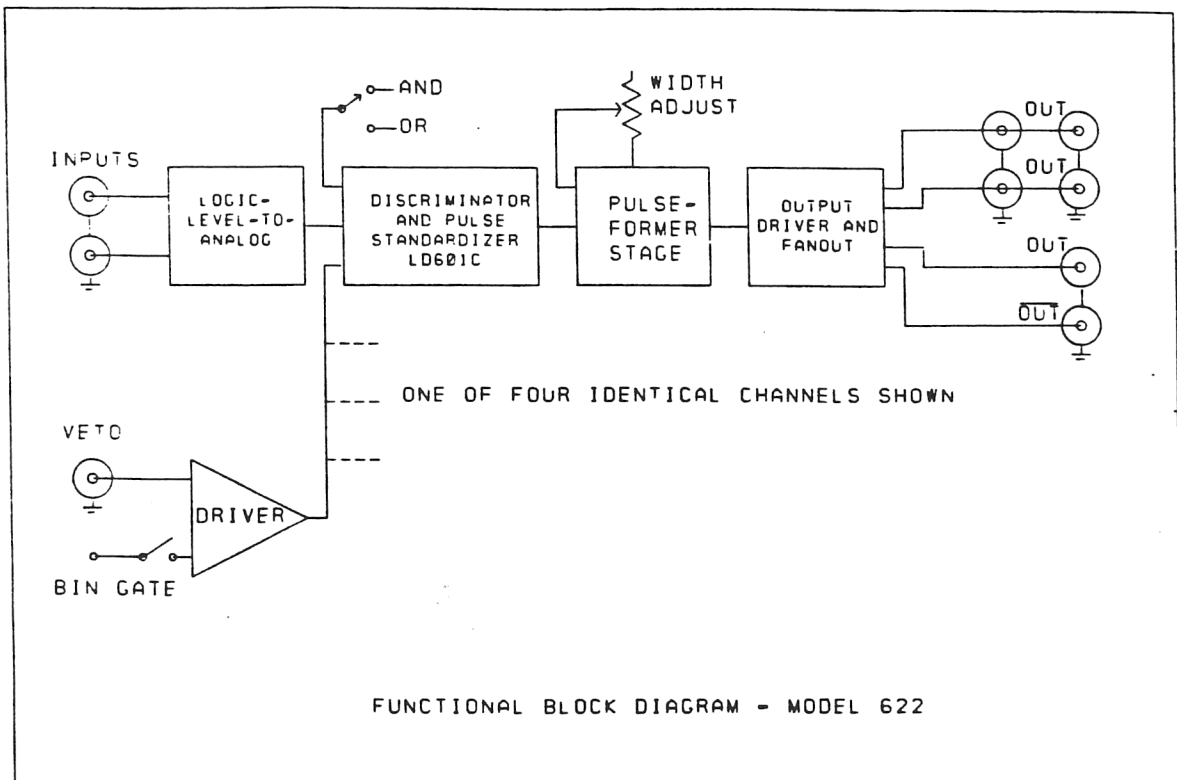


Figure 2.1

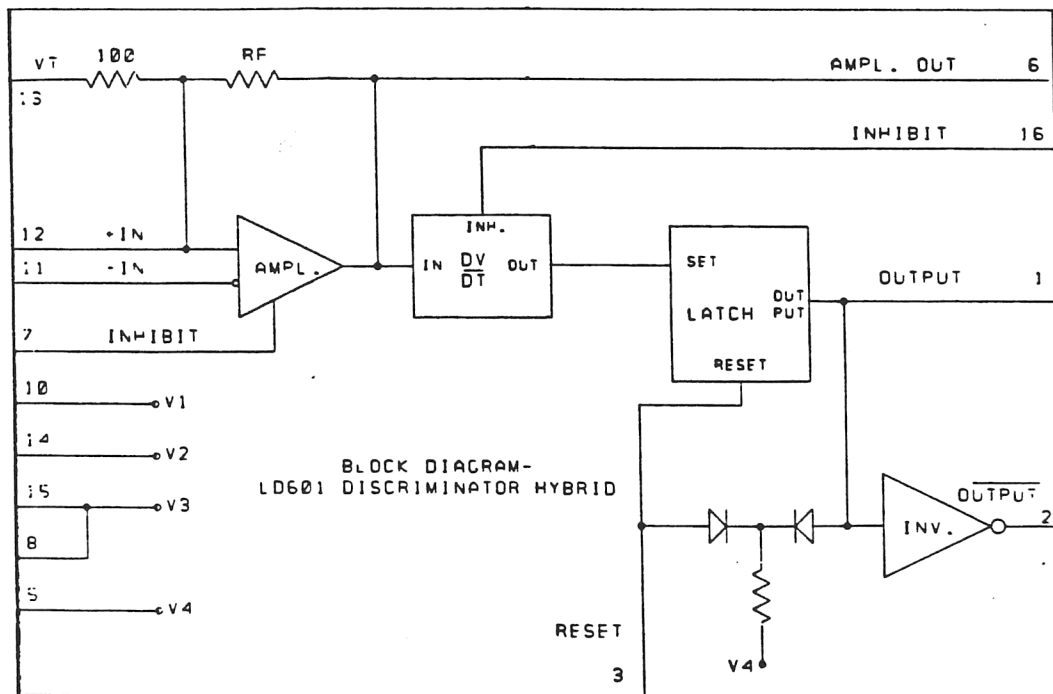


Figure 2.2

SECTION 3

APPENDIX

Handling Of Static Sensitive Semiconductors

Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. You can minimize the chances of destroying such devices by:

- A. Knowing that there is a problem.
- B. Learning the guidelines for handling them and using the procedures, and packaging and bench techniques that are recommended.

Key to all guidelines is to MINIMIZE HANDLING. However, when repairing an instrument with static sensitive devices:

1. Discharge personal static before handling devices. (Use of a grounded, conductive armband is ideal).
2. Handle devices by the body, not the pins.
3. Be sure work station, soldering irons, etc., are grounded. Work station should have anti-static work surface.
4. Do not slide devices over any surface. In particular, avoid use of plastic, vinyl or Styrofoam unless it is treated to be conductive.
5. Keep sensitive devices in original containers until ready for use.
6. Do not insert or remove parts under power.

TECHNICAL INFORMATION
(PARTS LIST, SCHEMATICS)

PART NUMBER	DESCRIPTION REMARK	QTY PER
102245103	CAP CERA DISC 25V .01 UF	51
102444220	CAP CERA DISC 100V 22 PF	8
106435103	CAP CERA MONO .01UF	12
116515330	CAP DIP MICA DM10 33 PF	4
141854685	CAP TANT DIP 6.8 UF	22
142124476	CAP TANT DIP CASE 47 UF	12
147147090	CAP ALUM METAL CAN 90 UF	2
158879007	CAP VARIABLE 6-35 PF	4
161335100	RES CARBON FILM 10 OHMS	1
161335101	RES CARBON FILM 100 OHMS	9
161335102	RES CARBON FILM 1 K	17
161335103	RES CARBON FILM 10 K	4
161335104	RES CARBON FILM 100 K	4
161335121	RES CARBON FILM 120 OHMS	4
161335123	RES CARBON FILM 12 K	4
161335132	RES CARBON FILM 1.3 K	1
161335151	RES CARBON FILM 150 OHMS	12
161335152	RES CARBON FILM 1.5 K	1
161335160	RES CARBON FILM 16 OHMS	8
161335182	RES COMP 1/4W 5% 1.8 K	9
161335200	RES CARBON FILM 20 OHMS	4
161335201	RES CARBON FILM 200 OHMS	8
161335205	RES CARBON FILM 2 MEG	4
161335222	RES CARBON FILM 2.2 K	5
161335242	RES CARBON FILM 2.4 K	1
161335271	RES CARBON FILM 270 OHMS	1
161335301	RES CARBON FILM 300 OHMS	1
161335331	RES CARBON FILM 330 OHMS	1
161335361	RES CARBON FILM 360 OHMS	4
161335391	RES CARBON FILM 390 OHMS	8
161335431	RES CARBON FILM 430 OHMS	1
161335510	RES CARBON FILM 51 OHMS	1
161335511	RES CARBON FILM 510 OHMS	2
161335512	RES CARBON FILM 5.1 K	1
161335561	RES CARBON FILM 560 OHMS	5
161335620	RES CARBON FILM 62 OHMS	8
161335622	RES CARBON FILM 6.2 K	1
161335682	RES CARBON FILM 6.8 K	1
161335751	RES CARBON FILM 750 OHMS	1
161335752	RES CARBON FILM 7.5 K	1
161335822	RES CARBON FILM 8.2 K	4
161335910	RES CARBON FILM 91 OHMS	4
161445056	RES CARBON FILM 5.6 OHMS	2
161665221	RES COMP 2W 5% 220 OHMS	1
168531373	RES PREC RN55D 619 OHMS	4
168531381	RES PREC RN55D 750 OHMS	1
168531389	RES PREC RN55D 909 OHMS	1
168531437	RES PREC RN55D 2.87 K	1
168531497	RES PREC RN55D 12.1 K	1
168531609	RES PREC RN55D 178 K	4
168531621	RES PREC RN55D 237 K	4
181457102	RES VARI CERMET 1 K	1

PART NUMBER	DESCRIPTION REMARK	QTY PER
181457502	RES VARI CERMET 5 K	1
182537103	RES VARI CERMET 10 K	4
204021004	IC LINE RECEIVER MC1692L	4
208011003	IC SINGLE OP AMP LM301AN	4
208034001	IC DUAL OP AMP UA747	4
230110005	DIODE SWITCHING 1N4448	3
230110700	DIODE SWITCHING FD700	4
240225703	DIODE ZENER 3.6V 1N5989A	1
240225705	DIODE ZENER 4.7V 1N5992A	5
	SEND 4 PIECES FOR EACH UNIT TO RSD PRODUCTION FOR MATCHING.	
253010811	DIODE SCHOTTKY HP2811	8
253010835	DIODE SCHOTTKY HP2835	49
270130401	TRANSISTOR NPN A401	16
	SEND TO RSD PROD. FOR MATCHING.	
270170001	TRANSISTOR NPN 2N5770	9
270170002	TRANSISTOR NPN 2N5962	4
270190001	TRANSISTOR NPN PWR 2N3054	1
275150003	TRANSISTOR PNP 40319	1
275170002	TRANSISTOR PNP 2N5771	8
275190001	TRANSISTOR PNP PWR 2N3740	2
300010001	BEAD SHIELDING FERRITE	24
300020001	BEAD SHIELDING "1/2" SIZE	28
300050001	CHOKE FERRITE SINGLE LEAD	5
400010008	SOCKET IC SOLD TAIL DIP-8	4
400020014	SOCKET IC SOLD TAIL DIP-14	4
400030016	SOCKET IC SOLD TAIL DIP-16	8
402030000	CONN CO-AX LEMO	33
402030001	HOOD FOR BULKHD LEMO CONN	9
402030002	SPANNER NUT SMALL OD LEMO	33
402030003	GROUND LUG NONLOCK LEMO	4
405112001	CONNECTOR BLOCK (PIN)	1
405212002	GUIDE PIN (MALE)	1
405213001	GUIDE PIN (MALE)	1
405312001	GUIDE PIN (FEMALE)	2
405410016	CONNECTOR PIN (MALE)	7
405613001	CONNECTOR HOOD	1
410112102	SWITCH TOGGLE SPDT	4
420212001	SWITCH SLIDE DPDT	1
500120002	TRANSIPAD "LARGE"	1
520000510	STANDOFF GLASS 8MM	102
521400020	SPACER ROUND #4 5/8	2
523400022	ROLL PIN SIZE #4 11/16 LG	4
540103102	SIDE COVER NIM LEFT	1
540103103	SIDE COVER NIM RIGHT	1
540105001	BRACKET NIM WRAP SIZE #1	2
555611001	CAPTIVE SCREW 6-32	2
555621002	CAPTIVE SCREW RETAINER	2
560440005	SCREW PHILIPS 4-40X5/16	4

XENTIS V4.2C
MPSS
INPMS
MRES

LeCroy-Company Confidential Data
622 PARTS LIST
LeCroy-Company Confidential Data

PAGE 3
1-AUG-1997
MANUALBOM.XCF;13

PART NUMBER	DESCRIPTION REMARK	QTY PER
560440013	SCREW PHILIPS 4-40X13/16	2
567256004	SCREW FLAT PHIL 2-56X1/4	4
568440003	SCREW FLAT PHIL 4-40X3/16	10
577400001	WASHER SHAKEPROOF SIZE 4	12
580440001	NUT HEX STANDARD 4-40	6
585141237	RIVET "POP" ALU 1/8X.237	2
590001022	WIRE TEFLON 7/30 BLK 22	1
590111022	WIRE TEFLON 7/30 BRN 22	1
590331022	WIRE TEFLON 7/30 ORA 22	1
590441022	WIRE TEFLON 7/30 YEL 22	1
590551022	WIRE TEFLON 7/30 GRN 22	1
590661022	WIRE TEFLON 7/30 BLU 22	1
590881022	WIRE TEFLON 7/30 GRAY 22	1
591101022	WIRE BUS TIN-COPP AWG 22	1
593910001	CABLE CO-AXIAL RG178B/U	6
595901022	SLEEVING TEFLON AWG 22	1
710622013	PC BD PREASS'Y 622	1
720622013	FRONT PNL PREASS'Y 622	1
740000002	WRAPAROUND NIM 1 BIN GATE	1
LD601C	HYBRID DISC	4

nd of report. 124 Details encountered.

