PCOS 4 SYSTEM MANUAL

CE

PRELIMINARY

LeCroy

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

COOLING It is imperative that the modules be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50° C.

INSTALLATION Crate power should be turned off during insertion or removal of modules in accordance with the CAMAC specification.

SPECIFICATIONS The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

TABLE OF CONTENTS

GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the covered instruments. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

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PCOS PRODUCT DESCRIPTION

INTRODUCTION

Proportional chambers are one of the workhorses of particle physics experiments. The readout electronics has evolved over more than 2 decades of experience. PCOS 4 is the latest and most highly integrated commercially available readout system.

This system contains just 2 basic components, a preamplifier integrated circuit (MQS104) and a delay and coincidence integrated circuit (MDL108). All required functionality for test and operation are provided by these two chips. This high degree of integration provides a low cost and reliable system unmatched by any previous proportional chamber readout system.

The MQS104 is a high gain transimpedance amplifier, combined with a four stage shaping amplifier. The output pulse shape is optimized for fast proportional chambers. The width is about 30 nsec, and the double pulse resolution is better than 50 nsec. The effective noise level is less than 4000 electrons.

The MDL108 integrated circuit combines the discriminator, delay element, coincidence gate and all readout logic in one 8 channel BiCMOS chip. The delay element is adjustable from 400 nsec to more than 800 nsec. The delay of any channel can be adjusted to within 1 nsec of the nominal value. A phase locked loop and voltage controlled delay elements maintain this accuracy from chip to chip and over time and temperature. The readout of the latched data is via a shift register, clocked at 20 MHz. A parity bit is added to the 8 bits of wire data to provide error detection. This chip contains all logic required to set up, control, test and readout eight wires. Three eight input OR outputs, a prompt OR, a delayed OR and a latched OR are provided for testing and trigger purposes.

SYSTEM COMPONENTS

The complete PCOS4 system includes the 2741 Chamber Mounted Cards, a backplane which matches the chamber connector spacing, and two controller modules, the 2748 Quad Stream Readout Controller module and the 2749 PCOS 4 System Driver module. The special backplane must match the chamber dimensions and therefore must be provided by the user.

The two controller modules are available either as single width CAMAC modules (2748CAM and 2749CAM) or as single width VME modules (2748VME and 2749VME). These are described in detail in separate manuals. Although very similar, there are small differences between the CAMAC and VME versions.

The chamber mounted cards are available in three versions, the 2741-16Y and 2741M-16Y are large cards designed for ease of mounting on the chamber. The 2741-16H is a much smaller card, designed for mounting in a restricted space.

The 2741-16Y chamber mounted card contains a complete proportional chamber readout system for 16 wires. This card contains four MQS104 preamplifier chips, two MDL108 delay chips, the discrete components required for wire protection at the preamplifier inputs, NIM-to-TTL converters for the GATE and FAST CLEAR inputs, a test pulser and local power regulation.

There are two edge connectors on the 2741-16Y cards, a chamber connector and a readout/control/power connector. These are on the same edge of the card, allowing easy removal and replacement of a card. The chamber connector connects directly to the chamber wires. The readout connector plugs into a special backplane which supplies power, common signals and the daisy chain wiring to form the shift register. The coincidence GATE is distributed to the cards on this backplane. Up to 16 cards can be combined to make a readout and control stream of up to 256 wires.

One 2741-16Y card in each stream is configured as a Master (2741M-16Y), and contains in addition to the components on a normal (slave) card (2741-16Y), the drivers, receivers and a third connector for readout and control. One 16 wire cable (8 twisted pairs) from the master card in each readout string connects to the 2748 stream controller module in a nearby rack. The Master and Slave versions of the 2741-16Y use the same printed circuit card. The slave card contains the wiring and all passive components for the master function. A slave card can easily be converted to a master (in the field if necessary) by simply installing two integrated circuits and one connector.

There are also two edge connectors on the 2741-16H cards, a chamber connector and a readout/control/power connector. However, these are on opposite edges of the card. This complicates installation and service, but does provide for a very compact system. Both connectors are 36 contacts and 0.100" pitch. The 2 connectors are keyed, so the card can only be installed in the correct orientation (provided that the chamber and backplane connectors are appropriately keyed). The special backplane which supplies power, common signals and the daisy chain wiring to form the shift register also provides the master function. All 2741-16H cards are slaves, there is no 2741M-16H card. The cable from the master section of the backplane leads to the 2748 stream controller module.

Each 2748 controller can handle four readout streams, or up to 1024 wires. The time to read the data from the chamber mounted boards to the controller is less than 16 microseconds for streams of 256 wires. The formatted data is available for readout over CAMAC (or VME) at that time. The 16 bit data word consists of an eight bit block of adjacent wires (one bit for each wire), and the location of that wire block (7 bits for 1024 wires). Only blocks of wires containing at least one wire struck are read out. The total readout time depends of course on the system speed. A fast clear is provided to clear an event before readout, and a slow clear to abort a readout in progress. The 2749 System Driver module provides precisely timed pulse pairs for the delay stabilization, and the interface to the experiment’s trigger system.

SYSTEM INTERCONNECTIONS

The Chamber cards are mounted on a special backplane which is mechanically part of the chamber. This backplane supplies the power, GATE and FAST CLEAR signals, and the control and readout daisy chain. The Y cards require that one card in each backplane be a Master and that it is inserted in the special Master slot. The daisy chain wiring on the backplane determines which position is the Master and which are Slaves. The H cards are all slaves, the Master functions are part of the backplane.

The readout and control cable is an 8 twisted pair twist & flat cable, up to 20 meters in length. All 4 cables from a given 2748 controller must be the same length, within 0.25 meters.

Within a crate all 2748 stream controllers are connected by a front panel control bus to a single 2749 system driver in the crate. One 2749 is required for each crate. The crate is completely standard, and uses a standard (CAMAC) crate controller or VME master module.

The 2749 communicates with the experiment's trigger system, and coordinates the 2748 stream controllers.

There are 3 inputs to the 2749, READ, ABORT and CAL. READ and ABORT are fast NIM pulses which command the system to readout the 2741 cards, or to abort a readout in progress. CAL is a fast NIM level which enables calibration mode.

There are also 3 outputs, all fast NIM signals. BUSY is a level which is the OR of the BUSY outputs of all the 2748 cards. BUSY indicates readout in progress and should be used in the trigger to block further GATEs. TGATE is used to send the calibration pulse pair to the MDL108 chips and for internal test modes. TGATE MUST be OR'ed with the experiment's trigger GATE and distributed to all 2741 cards. Similarly, TCLEAR should be OR'ed with the experiment's FAST CLEAR signal and distributed to all 2741 cards.

SYSTEM CONFIGURATION

Each MDL108 chip in the system requires 16 unique bytes of configuration data. The data acquisition system must maintain a data base of the required threshold settings and trim settings for each wire in the system. As part of the initialization procedure after power up, this data must be downloaded to the 2741 cards.

The 2748 controller modules must be loaded with the 2741 card count for each of the 4 streams connected to the module. Only as many streams as required need be connected, but stream 0 must be connected to at least one 2741M card or backplane master section (to return the clock). The stream and mode register is set to the desired mode (0 for normal data operation). All 4 stream cables connected to a particular 2748 must be the same type and length, within 0.25 meters. The returning clock from stream 0 is used as the system clock during readout, so all 4 streams must have the same cable delay (and stream 0 must be present).

The 2749 System controller must have the width and separation register set for the desired delay time. The 2-bit calibrate and clock mode register must be set as required.

An example of the configuration procedure for one 2741 card, with comments, is shown in the reference section.

NORMAL DATA MODE

In this mode the GATE and FAST CLEAR come from the experiment's trigger system. After each GATE the data is safely latched in the MDL108 chips. The GATE is followed by either a FAST CLEAR to the 2741 cards, or a READ pulse to the 2749 System controller. The read pulse begins the transfer of the data from the 2741 cards to the 2748 controller memories. The data transfer takes place at 20 MHz. For the maximum of 16 cards per stream, this takes less than 16 microseconds. All streams perform this data transfer at the same time, so this is the system dead time. During this period an ABORT pulse at the 2749 will clear the data and abort processing, returning to data mode. At the end of the dead time, all data is stored in the 2748 modules, awaiting readout by the host system.

TEST MODES

The PCOS4 system has several built in test modes to ensure the integrity of the system.

All registers in the 2748, 2749 and 2741 cards are read and write. The data paths are easily checked by simple random number writes and reads. Most registers are actually less than 8 bits, so the read results should be appropriately masked to eliminate non-existent bits (the shift register has 8 bits in every byte of course).

The TEST mode uses the GATE signal to capacitively couple a small charge (about 100k electrons) to each wire at the input to the MQS104. If the GATE is long enough (longer than the delay setting), the signal exiting the delay line will be in coincidence with the GATE and be latched. This can be read out as if in normal data mode.

Using the channel enables, one can easily test the complete amplifier-shaper-comparator-delay-latch chain of each channel in the system. The test enable bit for each channel allows the one-shot to be triggered by the leading edge of the GATE rather than the comparator output. There are 3 OR outputs on each 2741 card, which are the OR of all 16 channels on the card. They are the prompt OR, which is the one-shot output, the delayed OR, which is the output of the delay line, and the latched OR, which is the OR of the latched data bits. These ORs are open drain outputs and can be configured (on the backplane) with pull-ups to produce a 50 to 100 mV pulse in a properly terminated 50 ohm line. These outputs are intended for test and diagnostic purposes, and are extensively used for production testing of the 2741 cards. They are intended to be disabled during normal operation, to prevent feedback to the chamber wires. The latched OR outputs can be used in a second level trigger without fear of feedback, since they are the result of the GATE signal.

DELAY LINE ADJUSTMENT AND CALIBRATION

The MDL108s contain nine identical voltage controlled delay lines, one for each channel and a reference delay line which is part of a phase locked loop. There is also a trim delay section in each line which allows precise matching of the nine delay lines. These nine delay lines share a common control voltage, which is produced by an internal DAC. The DAC can be written or read, and is automatically adjusted when the system is in Calibrate mode. In Calibrate mode, a pulse pair with spacing equal to the desired delay is received on the GATE line. The internal control voltage DAC is incremented if the delay is not long enough or decremented if the delay is too long. The pulse pairs are repeated until the delay of the reference delay line is equal to the pulse spacing.

During operation, the PCOS4 system will require occasional recalibration to maintain the delay at the desired value. The interval between calibrations will depend on the environment. The primary cause of changes in the delay is temperature variation. Voltage variations are eliminated by the use of local regulators on each 2741 card.

For normal changes in room temperature recalibration once every few seconds is adequate. Each recalibration requires a few Phase Lock Loop cycles. Starting from a fully configured normal data mode, simply send a NIM level to the CAL input of the 2749. Calibration cycles will occur automatically, at a rate of one every 10 microseconds. The required mode changes, control pulses and timed pulse pairs are controlled by the 2749 module. The system will return to normal mode within 10 microseconds after removing the NIM signal.

The suggested initial operating sequence:

INITIAL START UP: At least 10,000 calibration cycles, or at least 100 milliseconds.

WHILE WARMING UP: 10 calibrations per second, at least 100 cycles each. This takes only 10 milliseconds every second, for 1% dead time.

STABLE RUNNING: 1 calibration every second, with at least 100 cycles. This takes about 1 millisecond, for 0.1% dead time.

Depending on the local environment, calibration may be required either more or less often than this suggested sequence. This is readily determined by reading the delay DAC from each MDL108 chip.

TRIMMING THE SYSTEM FOR MAXIMUM TIMING PERFORMANCE

The delay of all channels can be adjusted to be the same over the entire system by using the trim delay section (16 steps of 1 ns) on each channel. This requires however that the experimenter measure a delay curve for each wire in the system!

Two items are required that are not built in to the PCOS4 system. First, a controlled test pulse must be provided on the chamber, independent of the GATE distribution. Second, the Gate delay must be swept over a large interval with small time steps. A precision gate generator, such as the LeCroy Model 4222 is ideal for this task. After a delay curve is

measured for each channel, the appropriate trim value can be determined. This may need to be iterated, since the trim section is not precisely 1 ns per step. Note that the trim section of the reference channel can be used to shift all channels on the chip simultaneously, effectively shifting the range of the trim sections for the chip.

If carefully done, this technique can compensate for any variation in the GATE distribution, in particular the skew on the backplanes. The end result can be a system with the coincidence gates matched to within 1 ns over all channels.

REFERENCE DATA

MQS104 Preamplifer and Shaper

The MQS104 is a high gain transimpedance amplifier, combined with a four stage shaping amplifier. The output pulse shape is optimized for fast proportional chambers. The width is about 30 nsec, and the double pulse resolution is better than 50 nsec. The measured impulse response is shown. This integrated circuit is implemented as a 4 channel device, in a medium speed bipolar process. The chip to chip variation in shaping time is expected to be less than 10%. The effective noise level is less than 4000 electrons, with protection elements and wire capacitance added to the input circuit. The transimpedance gain is approximately 500K ohms, with differential output. Please refer to the MQS104 data sheet for the current specifications.

MDL108 Discriminator, Delay and Latch

The MDL108 integrated circuit combines the discriminator, delay element, coincidence gate and all readout logic in one 8 channel BiCMOS chip. The discriminator threshold is adjustable down to 1000 electrons, well into the noise. The delay element is adjustable from less than 400 nsec to more than 800 nsec. The delay of any channel can be adjusted to within 1 nsec of the nominal value. A phase locked loop and voltage controlled delay elements maintain this accuracy from chip to chip and over time and temperature. This phase locked loop is enabled only as required, and does not run continuously. The coincidence gate can be as short as 30 nsec. The leading edge of the input pulse must be within the gate to produce a latched bit.

The readout of the latched data is via a shift register, clocked at 20 MHz. The chip contains all logic required to set up, control, test and readout eight wires. The discriminator thresholds are adjusted in groups of four. There is an enable and a delay trim for each of the eight channels. All communication to and from the chip is via digital shift registers. A parity bit is added to each group of eight wires during readout, to identify transmission errors. Three eight input OR outputs, A prompt OR, a delayed OR and a latched OR are provided for test and trigger purposes.

Each of the 8 inputs is a differential comparator, with adjustable thresholds. The inputs must be AC coupled to use the built-in threshold adjustment. There is a set of DACs (one for the plus inputs and one for the minus inputs) for channels 1-4 and a separate set for channels 5-8. The four threshold DACs can be set from 3 volts to 4.3 volts, with 6 mV resolution (using a nonlinear 6 bit DAC).

The comparator is followed by selection logic, a monostable, a delay trim section, a controllable delay line, a coincidence gate and latch, and a readout shift register.

The selection logic enables or disables the comparator output of each channel, and enables or disables a test pulse input to each channel. The monostable is a simple delay line controlled one shot, with a range of 20 to 40 nsec in 4 steps. The recovery dead time (after the output pulse) is equal to the output width (or the sum of output width plus the input width if the input width is greater than the output width). The 2 bit control register which controls the monostable is common to all channels on the chip.

The delay trim section consists of 15 delay elements, approximately 1 nsec each. The 4 trim bits select the delay from 0 to 15 nsec. There are 4 separate trim control bits for each channel.

The delay line consists of 150 current limited inverter stages, each with a minimum delay of 2 nsec, and a maximum of at least 6 nsec. The control voltage is provided by the delay line DAC.

The coincidence latch is a D flip flop with the delayed input signal as the clock and a common Gate signal as the D input. This is followed by a set reset flip flop to store the latched signal (later input signals outside the Gate will reset the D flip flop).

The Readout begins with a pulse to transfer the data from the set reset Flip flop to the shift register. The data is then clocked out at 20 MHz. A ninth shift register bit contains the ODD parity of the 8 latched signal channels.

The delay lines are controlled by a phase locked loop and a ninth delay line, the reference delay, which is identical to the 8 signal delay lines. In PLL mode, a pair of Gate pulses with separation equal to the desired delay is input the delay line. Detection circuitry determines whether the delay is greater or less than the desired delay, and sets a direction bit accordingly. A count pulse then increments or decrements the up down counter which in turn drives the delay DAC, a 10 bit nonlinear DAC (the resulting delay transfer curve is approximately linear). An initial calibration period is required, with several thousand pulse pairs, to set the DAC to the proper value. Then only occasional pulse pairs are required to track changes in temperature and power supply voltage. To determine if the calibration rate is sufficient, read out the delay DAC value, apply 100 pulse pairs, and read the delay DAC again. If the value has changed more than 1 count, the interval between calibrations should be reduced. The counter logic implements some hidden bits in the up down counter to suppress noise. Three successive counts in the same direction are required to change the counter by one count. The PLL bit (a read only bit in ine of the control registers) indicates whether the loop is locked, or still changing.

INPUT SIGNALS

shift data
shift clock
mode 0
mode 1

PULSE1
PULSE2
GATE
FAST CLEAR

OUTPUT SIGNALS

shift data
shift clock (just a copy of the input shift clock)
Test pulse (just a copy of GATE during MODE 1 only)

OPERATING MODES

Mode 0 Normal Mode

Normal data mode, GATE is the coincidence gate
pulse1 transfers data to the data Shift Register
pulse2 OR the fast clear resets the data register
shift clock clocks the data shift register
format: 8 bits of data AND 1 odd parity bit

Mode 1 Test Mode

GATE is the test pulse output and the coincidence gate
pulse1 transfers data to data Shift Register
pulse2 OR the fast clear resets the data register
shift clock clocks the data shift register
format: 8 bits of data AND 1 odd parity bit

Mode 2 Control Mode

UPLOAD, Pulse1 transfers control register data to the control Shift Register, then shift clock is used to upload to the controller.

DOWNLOAD, shift clock is used to download data to the control shift register on the chamber card, then pulse2 transfers the data to the control registers. NO parity.

Mode 3 Phase Locked Loop Mode

GATE is the Pulse Pair source
the pulse separation determines the delay time
pulse1 clocks the up/down counter
pulse2 resets the PLL flip flops (and the direction!)

REGISTERS

Data Register

8 bits, plus odd parity, 9 bits total

During MODE 0 or MODE 1 the data shift register is connected to data in/out
pulse1 transfers the 9 bits to the DATA shift register,
shift clock shifts the data shift register
MS bit is parity, next is channel 8
MS bit comes out first

Control Register

16 bytes, no parity

byte 1	threshold dac for channels 1-4, +
byte 2	threshold dac for channels 1-4, -
byte 3	threshold dac for channels 5-8, +
byte 4	threshold dac for channels 5-8, -
byte 5	control register for channel 1
byte 6	control register for channel 2
byte 7	control register for channel 3
byte 8	control register for channel 4

byte 9	control register for channel 5
byte 10	control register for channel 6
byte 11	control register for channel 7
byte 12	control register for channel 8
byte 13	control register for reference channel
byte 14	miscellaneous control
byte 15,16	value for/from 10 bit up-down counter, + state bits for counter control state machines

(byte count must be even)

During MODE 2 ONLY:
The control shift register is connected to data in/out
pulse1 transfers data from the actual registers to the control shift register
shift clock shifts the control shift register
pulse2 transfers data from the control shift register to the actual registers

Control Register Bit Definitions

Threshold voltage DACs are 6 bits, 0-5. bits 6,7 are unused

Channel control, 1 byte per channel (8 channels)

0	enable
1	test enable
2	_trim 3 (complement)
3	_trim 3 (complement)
4	_trim 1 (complement)
5	_trim 0 (complement)
6	
7	

Channel control, 1 byte for reference channel

0	oneshot width bit 0
1	oneshot width bit 1
2	_trim 3 (complement)
3	_trim 2 (complement)
4	_trim 1 (complement)
5	_trim 0 (complement)
6	
7	

Miscellaneous control, 1 byte

0	bypass all delay elements
1	enable prompt OR
2	enable delayed OR
3	enable latched OR
4	select test output polarity 0=negative pulse
5	PLL lock flag (read only)
6	
7	

Delay DAC (driven from the up-down counter, bytes 15,16)

byte 15 0-7	ls bits of 10 bit up-down counter
byte 16 0-1	ms bits of 10 bit up-down counter
byte 16 2-4	count enable state machine, 3 bits
byte 16 5-7	lock detection state machine, 3 bits

SAMPLE CONFIGURATION SEQUENCE

This sequence of CAMAC operations will correctly load the configuration data for a stream consisting of one 2741 cards, or 16 wires. This assumes a 2748CAM stream controller module. The instructions for the 2748VME are similar, please refer to the 2748VME manual for details.

Set the MODE to 2, select the stream to be downloaded.

mode =2, stream =0
CAMAC write to the 2748, F17, A4, data= 2 hex

First send the data for the MDL108 which controls wires 0-7 on the first 2741 card.

The first 2 bytes are the delay DAC setting (ls 10 bits) and control bits for the up/down counter (ms 6 bits), set the DAC to 512 and clear the control bits. The control bits are intended for production testing and should be set to zero.

CAMAC write to the 2748, F16, A1, data= 0200 hex

The F16, A1 command to the 2748 writes 2 bytes to the controller register. The controller then shifts the 16 bits to the 2741 card, taking about 17 microseconds to do so. During this period the BUSY test, F27, A0 will return Q = 1. A system with a fast CAMAC controller should test that busy is off before the next F16, A1.

Next, the miscellaneous control register (ms byte) and the reference channel control register (ls byte).

misc bit 0:	bypass
1:	enable prompt OR
2:	enable delayed OR
3:	enable latched OR
4:	select test output polarity
5:	PLL lock flag (read only)

Reference channel

bit 0-1:	oneshot width
bit 2-5:	trim delay value

set bypass off, all ORs ON, select test polarity=0 (leading edge of the GATE)
set oneshot width = 3 (maximum, about 40 ns), reference trim delay = 8 (midscale).

CAMAC write to the 2748, F16, A1, data= 0E03 hex

Next, the control registers for channels 8 (ms byte) and 7 (ls byte) (wires 0,1)

bit 0:	enable comparator output
bit 1:	enable test input (GATE)
bit 2-5:	trim delay value

set channel 8, comparator ON, test OFF, trim= 4
set channel 7, comparator ON, test OFF, trim= 3

CAMAC write to the 2748, F16, A1, data= 110D hex

set channels 6, 5 in the same way (wires 2,3)

CAMAC write to the 2748, F16, A1, data= 110D hex

set channels 4, 3 in the same way (wires 4,5)

CAMAC write to the 2748, F16, A1, data= 110D hex

set channels 2, 1 in the same way (wires 6,7)

CAMAC write to the 2748, F16, A1, data= 110D hex

Set the comparator thresholds for channels 1-4 (wires 5-7) to 50 mV. Set the negative input to full scale = 63. Set the positive input to full scale - 50 mV. The DAC is not linear, the first 58 steps are 20 mV each, the last 5 steps are 6 mV each. The actual voltages produced by the DACs can be measured on pins 30-33 of the MDL108 chip on the 2741 board.

DAC Voltage = 2.55 Volts + value * 20 mV (value < 59)
= 3.71 Volts + (value-58) * 6 mV (value > 58)

The comparator threshold is the voltage difference between the 2 inputs. By appropriately choosing the 2 voltages, the threshold can be set between -1.2 Volts and + 1.2 Volts with 6 mV resolution.

For normal operation with the MQS104 preamplifier, the negative input should be set more POSITIVE than the positive input. For a 50 mV threshold, set the negative input to 63 (about 3.74 volts) and the positive input to 57 (about 3.69 volts).

CAMAC write to the 2748, F16, A1, data= 3F39 hex

Set the threshold for channels 5-8 (wires 0-3) to 64 mv.

CAMAC write to the 2748, F16, A1, data= 3E38 hex

The data for wires 0-7 is now in the shift register inside the MDL108 for wires 8-15. Proceed to send the data for wires 8-15. This requires 8 more CAMAC writes, F16, A1. Now the data for all 16 wires are in the correct position in the shift registers in both MDL108 chips.

Load the data into the MDL108s by providing a Pulse2.

CAMAC write to the 2748, F25, A1.

The data is now completely loaded for a stream consisting of only one 2741 card, or 16 wires. For larger streams with multiple cards, do not send the Pulse2 yet, but continue to load data for wires 16 and up (up to 255). The data for ALL wires must be loaded into the shift register before the Pulse2 to the MDL108s. Then send Pulse2 with the F25, A1 CAMAC operation.

This sequence must be repeated for every stream in the system (up to 4 times for each 2748 controller card).

2741-16Y PRODUCT DESCRIPTION

THE 2741-16Y CHAMBER MOUNTED CARD SPECIFICATIONS

The 2741-16Y chamber mounted card contains a complete proportional chamber readout system for 16 wires. This card contains four MQS104 preamplifier chips, two MDL108 delay chips, the discrete components required for wire protection at the preamplifier inputs, NIM-to-TTL converters for the GATE and FAST CLEAR inputs, a test pulser and local power regulation.

There are two edge connectors on the 2741-16Y cards, a chamber connector and a readout/control/power connector. These are on the same edge of the card, allowing easy removal and replacement of a card. The chamber connector (double sided, 36 contacts, 0.156" pitch) connects directly to the chamber wires. The readout connector (double sided, 36 contacts, 0.100" pitch) plugs into a the backplane which supplies power, common signals and the daisy chain wiring (to form the shift register) for up to 16 cards, or 256 wires.

One 2741-16Y card in each stream is configured as a Master (2741M-16Y), and contains in addition to the components on a normal (slave) card (2741-16Y), the drivers, receivers and a third connector to communicate to the 2748 controller modules. The Master and Slave versions of the 2741-16Y use the same printed circuit card. The slave card contains the wiring and all passive components for the master function. A slave card can easily be converted to a master (in the field if necessary) by simply installing 2 integrated circuits and one connector.

PCOS4 2741-16Y CONNECTOR PIN ASSIGNMENTS

The 36 pin input connector on the chamber mounted board

1	GROUND			A	GROUND
2	wire #	15	(last read)	B	“
3		14		C	“
4		13		D	“
5		12		E	“
6		11		F	“
7		10		G	“
8		9		H	“
9		8		J	“
10		7		K	“
11		6		L	“
12		5		M	“
13		4		N	“
14		3		O	“
15		2		P	“
16		1		R	“
17	wire #	0	(first read)	S	“
18	GROUND			V	GROUND

The 36 pin readout connector on the chamber mounted board

1	Gate (NIM, bussed)	2	GROUND
3	GROUND	4	GROUND
5	fast reset (NIM, bussed)	6	GROUND
7	latched OR (bus)	8	GROUND
9	delayed OR (bus)	10	GROUND
11	prompt OR (bus)	12	GROUND
13	clock in (daisy chain)	14	clock out (daisy chain)
15	data out (daisy chain)	16	data in (daisy chain)
17	data from master to slave	18	data from slave to master
19	clock from master to slave	20	GROUND
21	mode bit 0 from Master	22	mode bit 0 to slave (bus)
23	mode bit 1 from Master	24	mode bit 1 to slave (bus)
25	pulse1 from Master	26	pulse1 to slave (bus)
27	pulse2 from Master	28	pulse2 to slave (bus)
29	GROUND	30	GROUND
31	minus voltage (-5 V)	32	minus voltage (-5 V)
33	plus voltage (+7 V)	34	plus voltage (+7 V)
35	plus voltage (+12 V)	36	plus voltage (+12 V)

The 16 pin Master connector (IDC header) (connects the master chamber mounted board to the controller) all signals are differential

1,2	clock in (from controller)
13,14	clock out (to controller)
11,12	data in
15,16	data out
3,4	mode bit 0
5,6	mode bit 1
7,8	pulse1
9,10	pulse2

THE CUSTOM BACKPLANE FOR THE 2741-16Y CARDS

A simple backplane schematic is shown. The functions are to supply power, GATE and FAST CLEAR signals, the daisy chain readout connections, and the pullups for the OR outputs. This is a passive backplane, no active devices are required.

The simple pullups on the OR lines are suitable only for test purposes. The OR signals are clamped on the 2741 card at +2 volts, and ground. Many alternate pullup schemes are possible, which can terminate the line impedance and match a 50 ohm output cable. It is also possible to level shift the signals to negative levels.

The GATE distribution must be a controlled impedance line for best coincidence resolution. Each 2741-16Y card loads the GATE line with approximately 2.5 pF of capacitance. This must be considered in the impedance calculations. The Fast Clear and the OR outputs should also be controlled impedance lines. If possible, the OR output lines should be completely shielded (between 2 grounded layers on the circuit board). The GATE and FAST CLEAR lines must be terminated with an appropriate resistor to ground. If the FAST CLEAR is not used, the termination will pull the line to logic zero. The FAST CLEAR line MUST not be allowed to float.

The pins assigned to the Master do not conflict with the Slave. A Master card can be inserted in a Slave position and function properly as a Slave. The Data OUT from the Master is connected to DATA IN on the furthest (last in the shift register chain) Slave. The Clock Out from the Master is connected to Clock In on the nearest Slave (the Slave on the Master board!). Note that the clock and the data propagate in opposite directions on the backplane.

2741-16H PRODUCT DESCRIPTION

2741-16H PCOS4 CHAMBER MOUNTED CARD

The 2741-16H card was designed to fit in a small space. The card is compatible with the 2741-16Y, with 2 exceptions, which allow the card to be made as small as possible. There is no master version of this card. All cards are slaves, and the master functions are supplied by the back-plane. There are no NIM-to-TTL converters on the card, these are also on the backplane. The GATE and FAST CLEAR signals must arrive at the card as TTL (or CMOS) signals.

The H chamber cards (2741-16H) have a 0.100 inch pitch, 36 contact (2 x 18) edge connector for the chamber connection, with pin assign-ments as on the LeCroy 2735 preamplifier and discriminator card.

The backplane connector is also a 0.100 inch, 36 contact (2 x 18) edge connector, on the opposite edge of the chamber board. The cards are first plugged into the chamber, then the backplane is installed onto the cards. Obviously, the connector spacing on the backplane must exactly match the connector spacing on the chamber.

Note that the two connectors are arranged so that the odd ins are on side one and the even pins are on side two. The drawings show which wire is read out first, and the arrangement of the backplane and the wire chamber connectors which results in a monotonic ordering of the wires during readout. The two edge connectors are keyed differently, to avoid incorrect installation.

2741-16H PCOS4 CHAMBER MOUNTED CARD SPECIFICATIONS

Size: 4.5" x 2.125" x 0.5".
Number of Channels: 16.
Power Required at the Connector: +12 V, ±0.5 V, .2 A +7 V, ±0.5 V, 0.05 A -5.2 V, ±0.2 V, 0.04 A.
Negative Input Signal, Diode Clamped: -0.7 V, + 2 V.
Input Impedance: 250 ohms.
Input Connector: 36 contact (2 x 18) PC card edge connector, 0.100" contact spacing.
Readout and Control Connector: 36 contact (2 x 18) PC card edge connector, 0.100" contact spacing.
External Signals Required: GATE, TTL, 30 ns minimum width; FAST CLEAR, TTL, 100 ns minimum width.

PCOS4 2741-16H CONNECTOR PIN ASSIGNMENTS

The 36 pin input connector on the chamber mounted board 2 x 18 edge connector, 0.100" pitch.

1	GROUND	2	GROUND		
3	“	4	wire #	0	(last wire to be read out)
5	“	6		1	
- - - polarizing key slot					
7	“	8		2	
9	“	10		3	
11	“	12		4	
13	“	14		5	
15	“	16		6	
17	“	18		7	
19	“	20		8	
21	“	22		9	
23	“	24		10	
25	“	26		11	
27	“	28		12	
29	“	30		13	
31	“	32		14	
33	“	34	wire #	15	(first wire to be read out)
35	GROUND	36	GROUND		

The 36 pin readout connector on the chamber mounted board 2 x 18 edge connector, 0.100" pitch

1	Gate (TTL, bussed)	2	GROUND
3	GROUND	4	GROUND
5	fast reset (TTL, bussed)	6	GROUND
7	GROUND	8	GROUND
9	latched OR (bus)	10	GROUND
11	GROUND	12	GROUND
13	delayed OR (bus)	14	GROUND
15	GROUND	16	GROUND
17	prompt OR (bus)	18	GROUND
19	GROUND	20	GROUND
20	clock in (daisy chain)	22	clock out (daisy chain)
21	data out (daisy chain)	24	data in (daisy chain)
- - -polarizing key slot			
23	mode bit 0	26	mode bit 1
27	pulse1	28	pulse2
29	GROUND	30	GROUND
31	minus voltage (-5 V)	32	minus voltage (-5 V)
33	plus voltage (+7 V)	34	plus voltage (+7 V)
35	plus voltage (+12 V)	36	plus voltage (+12 V)

THE CUSTOM BACKPLANE FOR THE 2741-16H CARDS

The backplane for the H version of PCOS4 contains the active circuitry for the interface to the 2748 controller and the trigger, as well as the passive components and daisy chain wiring that are on the Y version.

As noted above, the chamber connector and the backplane connector are on opposite edges of the chamber board. The cards are first plugged into the chamber, then the backplane is installed onto the cards. The

chamber cards should be aligned with card guides so that all connectors can be inserted simultaneously. Obviously, the connector spacing on the backplane must exactly match the connector spacing on the chamber. The backplane contains controlled impedance lines, and daisy chain wiring. For good results, the backplane must be a PC board, it cannot be a ribbon cable. It can be a flexible PC board, which will make installation easier by allowing connectors to be inserted one at a time.

The 2 fast NIM inputs, the GATE and the FAST CLEAR are converted to TTL on the backplane before being distributed to each chamber card, instead of being distributed as fast NIM, which requires the level converters on each chamber card. The circuit shown uses a LeCroy MVL407, a 10H125 and a 74F3037 to convert the NIM level to TTL with low timing skew. These two signals are distributed on 100 ohm controlled impedance microstrip lines on the backplane board, and are terminated to +2.5 volts to balance the load on the 74F3037. The GATE line starts as 50 ohms, then splits into 2 100 ohm lines to maintain low gate timing skew over the backplane. Timing skew is not important for the FAST CLEAR, but the pulse shape must be clean with no ringing.

The 3 open drain OR outputs are pulled up to +250 mV and matched to a 50 ohm output on the backplane. These outputs are used primarily for diagnostics and testing, and may be left off the backplane if not required. Other impedance matching circuits can be used, and the outputs can be level shifted (using the -5.2 volt supply) to produce negative pulses if required.

The interface to the controller uses RS485 drivers and receivers, which are adequate for use at 10 MHz readout rate. The 20 MHz readout rate used by PCOS4 requires a low timing skew clock receiver, with better skew than the standard RS-485 receivers. This is accomplished with a LeCroy MVL407 and 10H125.

THE 16 PIN MASTER CONNECTOR (IDC HEADER, 2 X 8)

This connects the readout backplane to the controller. All signals are differential RS-485.

1,2	clock in (from controller)
13,14	clock out (to controller)
11,12	data in
15,16	data out
3,4	mode bit 0
5,6	mode bit 1
7,8	pulse1
9,10	pulse2

Other backplane signals.

These are converted to TTL on the backplane and distributed to the chamber cards as TTL. They most conveniently arrive at the backplane as NIM signals on 50 ohm coaxial cable.

GATE, FAST CLEAR

The FAST CLEAR signal must not be left floating. If not driven by the backplane, the FAST CLEAR MUST be pulled to ground (logic 0) with a resistor to ground.

VME STREAM & SYSTEM CONTROLLER

INTRODUCTION

2748VME & 2749VME

The LeCroy 2748VME is a VME readout module for PCOS4 chamber cards. It provides the ability to configure and readout each chamber card. In conjunction with the 2749VME PCOS4 driver unit it is used to calibrate the chamber card delays. The 2749VME provides the interface between the readout system and the experimenter's trigger electronics.

GENERAL DESCRIPTION

Each 2748VME is capable of reading out up to 256 wires from each of four streams giving a total of 1024 wires per unit. In a 22 slot crate a maximum of twenty 2748VMEs and one 2749VME can be accommodated, allowing a maximum of in excess of 20K wires per VME crate. It should be noted that the stream readout time can be improved by reducing the number of chamber cards per 2748VME.

The modules are used with a standard VME controller and crate. A front panel bus connector is provided that can connect a full crate of 2748VME units to one 2749VME. The calibration and trigger interface is performed by the 2749VME which communicates with the 2748VMEs via the front panel command bus.

The modules physical dimensions, power requirements, control and readout protocol are in compliance with ANSI/IEEE standard 1014 rev. C.

The 2748VME, controlled by a VME master, is used to serially download the configuration information for the chamber cards. It also supports readback to verify the contents. The four streams are configured separately, to allow the thresholds (and other parameters) to be changed on a board by board basis. The data is transferred in 16 bit words. During configuration upload or download data is shifted out at a 1.25 MHz. This allows the initial configuration of each 2748VME with 64 chamber cards in less than 10 ms.

During delay calibration mode, the 2748VME generates the necessary signals to arm and enable the increment /decrement of the PLL circuits on each chamber card. The programmable gates (with the desired delay) are created by the 2749VME and distributed by the user through his main gate fan out. The synchronization of the 2748VME and 2749VME signals is achieved using the front panel flat cable command bus.

In order to readout the chamber cards the 2748VME is triggered into stream readout mode (either directly over the VME bus, or from the 2749VME.). The 2748VME then automatically handles the readout of all the streams under its control. The data is zero suppressed and then encoded before being written into a page of buffer memory. At the end of readout the encoded data can be accessed over VME. The data from all four streams is merged into one set of data. The number of chamber cards connected to each stream is programmable. This allows less than the maximum number of wires to be connected to each 2748VME. Using this feature the chamber cards may be grouped with one 2748VME connected to each logical chamber plane, greatly simplifying cabling. The data is readout from the stream serially at 20 MHz. The stream readout time for the 2748VME is:

the maximum number of wires on any single stream x (9/8) x 50 ns + 1 μs

It is important to realize that the stream readout time is independent of the number of wires hit and is determined by the stream with the most wires; hence, to reduce readout time the streams should be evenly populated. The 2748VME unit has a 16 event dual ported buffer with negligible performance reduction with coincident stream readout and VME access.

The crystal controlled timebase within the 2749VME is derived from a 100 ppm crystal. Including all other instabilities within the system this allows the calibration pulse pair spacing to be set with a stability of < 0.5 ns. This is more than adequate to set up the delays on the chamber cards. The 2749VME is capable under VME control of providing a variety of test signals which can be used to verify system operation with the minimum of external circuitry. The 2749VME includes a simple (non-latching) 8 bit scaler, that can be used for monitoring the hit output of a 2748VME in a simple evaluation system. Note that for a system with multiple 2748VMEs if this feature is required for a second level trigger, a separate scaler would be required.

SPECIFICATIONS

Please refer to the Model 2748VME and 2749VME technical data sheets for a complete summary of all relevant specifications.

2748VME FRONT PANEL

The LeCroy Module 2748VME front panel provides the user with connectors for system integration and LEDs to assist system debugging. See section 3 for more information regarding cabling. Note the streams are in reverse order relative to the 2748CAM. This is because the VME standard requires connectors to be mounted on the opposite side of the card to CAMAC. In order to preserve the polarization on the connectors the simplest solution was to reverse the order of the streams.

Displays

Stream activity LED: A four element activity LED is provided; each segment will flash when its corresponding stream contains at least one hit during stream readout. Stream 3 is the top light and stream 0 the bottom. This is again in the reverse order of LEDs on the 2748CAM.

Connections

The 2748VME connects to the chamber cards via 4 stream cables. Each of these cables consists of 8 differential pairs. In order to conserve panel space the cables are paired into two 34 pin headers. This leaves 1 pair in the center of the 34 wire cable that is not used; to reduce noise pickup, this pair is grounded at the 2748VME. It is not intended that this be used a ground connection between the chamber and the readout crate and hence it should be left disconnected at the far end.

In addition, a front panel lemo NIM output is provided which gives a short pulse during stream readout for each MDL108 that has at least one coincidence. Pulses from this output are intended to be counted using a scaler for trigger decisions or simply used as a diagnostic aid with an oscilloscope. A 16-pin connector is provided for connection of the flat cable front panel command bus connecting the 2748VMEs to the 2749VME.

Address

At the top of the front panel are two hexadecimal rotary switches. These are used to set the module's unique VME address. The 2748VME is only addressable in A24 mode and occupies 64K of address space. The switches select one of 256 base addresses for the unit.

2749VME FRONT PANEL

The LeCroy Model 2749VME front panel provides the user with connectors for system integration and LEDs to assist system debugging. See section 3 for more information regarding cabling.

Displays

Status LED: A four element LED display is used to monitor the following signals. These signals are all pulse stretched to give a visible flash. The LEDs are not marked but are in order from top to bottom:

1. Readout: VME or front panel READOUT
2. Abort: VME or front panel ABORT
3. CAL: VME or front panel CAL
4. BUSY: BUSY signal (this is the wire-OR of BUSY from all the 2748VME's wire-OR occurs over command bus)

Connections

The 2749VME connects to the trigger system via a series of NIM signal level lemo cables.

NIM Inputs: The following NIM inputs are terminated in 50 ohms to ground on the 2749VME.

READ - This edge sensitive NIM signal will cause the 2749VME to trigger the 2748VMEs into stream readout (assuming they are correctly set up). Minimum pulse width is 100 ns.

ABORT - This level sensitive NIM signal will cause the 2749VME to signal the 2748VMEs to abort any stream readout in progress. If an event is awaiting VME readout, it will be cleared. In addition, the 2748VMEs will assert P2. P2 is a signal distributed over the stream cables to all chamber cards which will clear any event held in the 2741 cards. Minimum pulse width is 100 ns.

CAL - This is a level sensitive NIM input. While active a series of pulse pairs with a programmable spacing will be generated on TGATE. In addition, the 2748VMEs will be signaled to send the necessary pulses to the chamber cards before and after the gate pulses. The repetition rate of the pulse pairs is approximately 100 kHz.

SCLR (early units are marked "1") - This is an edge sensitive input connected to an 8 bit scaler that can be readout under VME control.

FCW (early units are marked "2") - This is a level sensitive input fanned out to all the 2748VMEs and allows the use of an externally generated fast clear window (FCW). If this signal is asserted before the start of stream readout the unit will pause after the stream readout before irrevocably advancing the pointers. This allows an ABORT to be asserted at any time from 500 ns after the readout pulse up to the end of the fast clear window pulse. Note the front end will be held in a cleared state from the end of stream readout until the end of the FCW pulse. Note this feature is not available in the 2749CAM.

NIM Outputs: The following NIM outputs can sink 16 mA into a single terminated 50 ohm load. They are not designed for use with double terminations.

TGATE - This signal will under program control generate programmable width gate pulses for test purposes or when CAL is active generates calibration pulse pairs. For test use a VME operation triggers a single gate pulse. In normal circumstances this should be included the OR for the chamber card GATE. Note the TGATE can be configured to act as a trigger for an external calibration standard. In this case the external double pulse rather than the TGATE should be OR'ed into the chamber gate.

TCLR - This output goes active when either the Abort input active or an internal abort is generated using F25•A1. It should be OR'ed into the chamber card fast clear.

TBUSY - This output is the OR of the 2748VME busy lines. It may be monitored to determine when the system is ready for another gate.

TPLS (early units are marked "3") - This output provides a programmable width pulse immediately upon VME trigger.

Address

At the top of the front panel are two hexadecimal rotary switches. These are used to set the module's unique VME address.

BUFFERING SCHEME

The 2748VME implements a sixteen event 16 page multiple event buffer. Each page is segmented into four 32 word (16 bit) segments, one for each stream. The buffering system is straightforward to use. A RDOUT pulse from the trigger system (or software) is distributed by the 2749VME. All the 2748VME units perform a stream readout which transfers the data from the stream cards into a free page of the multievent buffer. The BUSY signal from the 2749VME can be used to determine when this stream readout is complete. BUSY should be folded into the total experiment BUSY to inhibit further RDOUT pulses. The buffer is transparently dual ported. The 2749VME can be interrogated over VME to determine that an event is available for VME transfer. The VME master may then read the number of words in the event (from a memory mapped register) and initiate a block transfer (or programmed IO) from a single IO location to read an event. Coincident with VME readout a subsequent stream readout may occur. There is no speed penalty for either activity. A header word containing the buffer page number (useful to verify system synchronization), a word count and a user programmable ID field is inserted as the first word of the data stream. A number of test modes are provided to both aid in board diagnostics and experimental system testing.

When a RDOUT pulse is applied to the unit either over the command bus from the 2749VME, or by VME access, a stream readout occurs. During stream readout sparsified event data is written into the appropriate segment of the page. At this stage data is ordered in a round robin sequence from the streams. When the stream readout is complete and the FCW input is not asserted, the number of words in each segment is written into a separate housekeeping memory. The write pointer is advanced and the 2748VME is ready for a new RDOUT command (indicated by BUSY being deasserted). If the write pointer cannot be advanced because the 16 buffers are full then BUSY will remain on until an event is transferred over VME.

If the FCW window is asserted (level sensitive) prior to the end of stream readout, the writing of the housekeeping memory and pointer advance will be delayed and BUSY will remain asserted until FCW is deasserted. This allows an ABORT to be applied at any time from 500 ns after the RDOUT pulse up to the end of the FCW.

Once an event is present in the buffer (assuming there is no event already awaiting VME transfer) all the streams will be automatically sequentially transferred into the output FIFO for VME transfer. The housekeeping memory is used to determine the correct number of words to be copied from each stream segment. The four stream counts are added together plus one (for the header word) to give the total event word count. The buffering process reorders the data in channel order (stream 0,1,2,3) rather than the original interleaved stream order. The word count in the header always indicates the number of 16 bit words (including the header itself). If transferring data in 32 bit words it is necessary to divide this number by 2 (and round up) to determine the number of 32 bit words to be transferred.

The event becomes available to VME after the first few words are written into the output FIFO from the event buffer memory. This is signaled by the NCD (No Complete Data) bit of the 2748VME (the wire-OR of all 2748VME NCD) clearing. If a second RDOUT pulse is received while an older event is being transferred into the output FIFO no penalty will result in stream readout time, since the memory is transparently dual ported. It is guaranteed that the FIFO can never be run dry by a fast master once the 2748VME has indicated it has an event ready even with a coincident 100% occupancy event being written to the memory. Hence the DTACK response time never increases significantly due to contention with stream readout.

The presence of data in the 2748VME is best determined by polling the 2749VME. The 2749VME NCD bit is reset when all units have a new event ready to be transferred over VME. It is important to note that as soon as the first word is read from (base + 0x20) (the header word), the NCD bit will be reasserted. This bit is the OR of the NCD bits in each of the 2748VMEs. This bit is always set except when a fresh event (i.e. not partially transferred) is waiting to be transferred over VME. In normal operation after a non-empty poll the 2749VME would not be accessed until all the 2748VME units have transferred their data over VME. At this point the next poll would indicate whether at least the first few words of a fresh event had been transferred to the output FIFO of all the 2748VME units. Typically 500 ns after reading the last 2748VME, the 2749VME would indicate that a fresh event is available (assuming the buffer wasn't empty).

In normal operation when reading out the 2748VME, it is necessary to know the word count. This may be determined from the header word. The header word is accessible either as the first word of the data stream (base+0x20) or non destructively from (base + 0x34). Reading the header from (base + 0x34) will not affect the empty bit and the header word will still be the first word read from (base+0x20). Once the header is read from (base + 0x20) it is no longer available from either memory address. If it is desired to leave the header word in the data stream, getting the word count from (base + 0x34) is the best solution. Note that

if a block transfer is attempted that exceeds the number of words in the event, the last words will all be undefined. If a fresh transfer is attempted before the unit has data, the lower 16 bits (in 32 or 16 bit transfers) will be 0xFFFF and the upper 32 bits will be undefined. Under no circumstances will two events be concatenated without AS rising in between the accesses to (base+0x20). It is recommended that the word count register is used to determine the length of a transfer.

For compatibility with STRUCK VME modules an additional readout option is provided. Coincident with the last valid word of a VME block transfer an interrupt bit may be asserted. This is not a standard VME operation as it is asserted with the same timing as a data bit. If this mode is used no other master on the bus should use the selected interrupt level. With this mode, the Struck master performs source terminated transfers and can automatically skip to the next 2748VME at the end of the current 2748VME event readout.

If AFTER reading the header word and possibly additional data words of a event it is desired to discard the data, a VME access to any register other than (base + 0x20) in the 2748VME will cause the current event to be discarded. Note access to other VME addresses BEFORE reading the header word of the event will not cause the discarding of data.

A number of test features are built into the 2748VME that allow test patterns to be transferred over VME with no external connections. The buffer memory may be written by manipulating the page register (base + 0x14), the address register (base+0x18) and performing memory writes (base + 0x3C). The unit should always be in mode 2 when loading test events. Note that the address register permits access to all 4 streams of a single event with bits 5 and 6 indicating the specific stream. After the buffer has been written it is necessary to load the housekeeping RAM with the word count of each stream. This is achieved by writing to the HDR01 (base+0x2C) and HDR23 (base + 0x30) registers. The page register should be programmed with the write pointer set to the page beyond the last event and the read pointer set to the first event to be read out. The maximum number of events that can be loaded for a test event is 15. When the mode register is returned to mode 0 the first event will be automatically transferred to the output FIFO. Once a series of test events are loaded they are indistinguishable from normal events written into the memory by stream readout. There are no constraints on the value of the data words. The header word is always calculated from the particular buffer page housekeeping contents which are totaled from all 4 streams plus 1 (for the initial event header word) to give the word count.

It is important not to issue RDOUT pulses without an active stream cable connected to stream 0. The result would be CLOCKFAIL. This may be detected in either the failing 2748VME or globally with the 2749VME. The unit cannot be used in test mode until a master reset and abort are issued.

For example to setup a test transfer with one event in the first page:

1,2 from stream 0
5,6 from stream 1
8 from stream 2
nothing from stream 3

1. (base+0x28) = 1 // reset the unit
2. (base+0x28) = 16 // abort the unit to reset any clock failures
3. (base+0x10) = 2 // set the mode to 2
4. (base+0x14) = 0 // set the page register to the first page
5. (base+0x18) = 0 // select stream 0 address 0 and write 1 to it
6. (base+0x3c) = 1
7. (base+0x18) = 1 // select stream 0 address 1 and write 2 to it
8. (base+0x3c) = 2
9. (base+0x18) = 0x20 // select stream 1 address 0 and write 5 to it
10. (base+0x3c) = 5
11. (base+0x18) = 0x21 // select stream 1 address 1 and write 6 to it
12. (base+0x3c) = 6
13. (base+0x18) = 0x40 // select stream 2 address 0 and write 8 to it
14. (base+0x3c) = 8
15. (base+0x2c) = 0x202 // 2 words in each of stream 0 and 1
16. (base+0x30) = 0x1 // 1 word in stream 2 and none in stream3
17. (base+0x14) = 0x10 // write pointer 1 beyond read pointer pointing at event
18. (base+0x10) = 0 // automatically copy event into FIFO
19. READ DATA NORMALLY

2748VME INTERFACE

VME Address Map

The 2748VME is essentially a D16 unit with no block transfer capability. However, to improve performance on data readout, accesses from (base+0x20) are more flexible. D32 and or block transfers are permitted. To improve performance 8 bit transfers from (base+0x20) are NOT permitted.

The following lists show the byte addressing to which the 2748VME responds.

Offset from base address	bits	function
0x00	4-0	Stream 0 Board Count
0x04	4-0	Stream 1 Board Count
0x08	4-0	Stream 2 Board Count
0x0C	4-0	Stream 3 Board Count
0x10		Mode register
	1-0	Mode
	3-2	Stream Number
	4	RUN
	7	CLOCKFAIL (read only)
	11-8	Header Word Tag
	12	NCD (read only)
	13	FULL (read only)
	14	reserved
	15	BUSY (read only)
0x14		Page Register
	3-0	Read pointer
	7-4	Write pointer
0x18		TEST Write address register

	6-5	stream
	4-0	data word address
0x20		Data Register
	31-0	SEE NOTE BELOW
	15-0	
0x24	15-0	Configuration Upload/Download
0x28		Pulse Bits (write only)
	0	VME Clear
	1	VME P 1
	2	VME P 2
	3	VME Readout
	4	VME Abort
	5	TEST Calibrate
0x2C		TEST HD01 (write only)
	5-0	Stream 0 word count
	13-8	Stream 1 word count
0x30		TEST HD23 (write only)
	5-0	Stream 2 word count
	13-8	Stream 3 word count
0x3C	0-15	TEST write to memory (write only)

Pulse bits + Status bits (base+0x28)

RESET: (write 0x01) This will reset all events in the unit and clear the command register. It will also reset the CLOCKFAIL bit. The unit should be reconfigured after a RESET. If a clock failure occurs this causes the internal clock within the unit to stop. It is recommended that TWO resets are applied (the first restarts the clock) to reliably reset the unit.

P1: (write 0x02) Trigger P1 to all cards. See Operating Instructions. This should only be attempted in mode 2. Note that P1 pulses necessary during stream readout are generated automatically by readout.

P2: (write 0x04) Trigger P2 to all cards. See operating Instructions. Note that P2 pulses necessary during stream readout are generated automatically by readout. To issue a P2 clear pulse to broadcast a fast clear to the front end cards use ABORT (which can be broadcast from a 2749VME).

Readout: (write 0x08) Trigger Readout on 2748VME. Note that normally readout would be broadcast to all 2748VMEs in a crate by triggering 2749VME. In this case this command does need to be used.

Abort: (write 0x10) If there is no stream readout in progress P2 is pulsed to all the chamber cards which causes any event registered in the chamber cards to be reset (equivalent to P2 pulse). If a stream readout is in progress or awaiting the end of FCW the readout is aborted and the complete event will be erased. Normally this would be broadcast by triggering an abort to the 2749VME.

Mode + Status Register (base+0x10)

The mode register is broken into four fields. The two least significant bits (0 and 1) are the mode (0-3). The modes are as follows.

Mode	Function
0	Normal data readout mode
1	Test readout mode: This mode is identical to Mode 0 as far as the 2748VME is concerned, the mode is echoed to all chamber cards on the four streams which causes them to generate test data. For further information see chamber card manual.
2	Configuration mode: This is used to download and verify setup information in the chamber cards.
3	Calibration mode (note not set directly, see below).

In normal circumstances calibrations are achieved under the control of a 2749VME. In this case the mode on the 2748VME mode should be 0 or 1. When the 2749VME is switched into calibration mode it will automatically pulse the 2748VME streams to mode 3 during a CAL cycle. However, the mode read back from the mode register on the 2748VME would always be that written (that is 0 or 1).

Bits 2 and 3 of the mode register select the stream for configuration. This information is ONLY used in mode 2. When configuration data is written and readback from the chamber cards only one of the streams is placed in mode 2, The 2748VME forces the other streams into mode 0 which prevents the P1 and P2 pulses corrupting the non-selected chamber cards configuration data. Though it should be noted that switching to configuration mode will corrupt any data waiting to be readout. In all the chamber cards and the output FIFO.

Bit 4 is a RUN bit and must be set for RDOUT pulses to be honored. If the RUN bit is not set the NCD and CLOCKFAIL bits will not be driven onto the command bus. This allows non-participating units to be left on the command bus by turning off the RUN bit.

Bits 11 through 8 provide a user programmable board ID. These bits are included in the event header words and can be used to identify the 2748VME data was read from. This is especially useful when debugging the system. Note as on 4 bits are available this limits the unique tag words to 16.

CLOCKFAIL (read only bit 7): The CLOCKFAIL bit is set after a stream readout is attempted and a timeout occurs on the returning stream0 clock. This is typically due to no powered stream being present. In addition this bit may be set if spurious clock edges are received from the stream0 clock return when not performing a stream readout. In either case once the bit is set it will remain set until cleared using a software RESET (see above) or a VME bus reset. Once the bit is set it will disable the unit. It is equivalent to locking on the ABORT input so no RDOUT pulses will be processed. The state of CLOCKFAIL will be driven onto the WIRE OR'ed Command bus IF the RUN bit is set. This allows the entire crate of 2748VME units to be checked by a single read of the 2749VME status register. When CLOCKFAIL is set the NCD bit will not

be driven onto the command bus (though it will still be valid when read directly from the 2748VME). The rationale is that if a single stream 0 backplane fails it will not cause the readout of the other cards to lock up.

NCD (NO CURRENT DATA) (read only bit 12): When this bit is set it indicates that the unit does not have a fresh valid event wait to be read out. It is important to note that this bit is immediately set after the first word of an event has been read and will not be reset until the readout of that event is complete and the next event is awaiting readout. This bit is easily used by scanning a wire or of all the 2748VME NCD bits accessible using the 2749VME.

FULL (read only bit 13): This bit indicates that unit is full. BUSY will also lock on which should be used by the trigger system to inhibit further RDOUT pulses.

BUSY (read only bit 15): This bit indicates the unit is unable to accept a further RDOUT pulse as it is either part way through a previously requested stream readout or it is FULL.

Board Count Register 0-3

The number of pairs of MDL108 devices on each stream to be read out must be specified before triggering a readout. This is indicated by dividing the number of wires connected to each stream by sixteen (which in the case of the 2741-16 is equal to the number of cards) and writing it to the appropriate board count register. The maximum number of MDL108s that can be attached to a stream is 32, so the board count should be set between 0 and 16. Note that it is acceptable to turn off a stream for readout by simply writing its board count to zero. It is also permitted to truncate a stream to fewer than the actual number of cards. The cards furthest from the master will never be read. However, the programmer would be responsible for ensuring that ALL the boards were included in the configuration. The number of wires per stream should be a multiple of sixteen (using the 2741M-16Y this is guaranteed as it is a 16 channel unit). Note that the board count registers are 5 bit read write registers. The upper bits should be masked off in software during read. Providing no more than 32 MDL108s are connected to any one stream, there are no further restrictions as to the arrangement of cards. It is important to realize that these registers are not used for downloading or verification of the configuration of the chamber cards. Stream 0 MUST always be connected to a powered master chamber card as the returning data clock is always taken from it for the readout of all streams.

To automatically sense the number of boards on a particular stream simply send out a configuration pattern and wait for it to return. The latency (in 16 bit words) when divided by the number of control words on each card (8) gives the number of cards on the stream.

Page Register (base+0x14)

This register is normally only read. After a master reset to the unit it is cleared. The two pointers being equal indicates the memory buffer is empty but NOT necessarily the output FIFO. For TEST modes it is necessary to write to this register to manually create simulated events for readout. This register can be confusing if used to interpret the number of free buffers available. When the unit is completely empty the first stream readout will be written into page 0. At the end of the stream readout the (base+0x14) would momentarily read 0x10. This would indicate that the

write pointer had advanced. However, the copying of the page into the FIFO would initiate automatically and when this was complete the page register would read 0x11 indicating that the read pointer had caught up with the write pointer. To avoid this confusion the NCD bit should be interrogated. NCD indicates either that the two page pointers are equal OR the FIFO is empty.

Data Format (base+0x20)

The basic data word of the 2748VME is 16 bits. To increase performance during readout, 32 bit reads are supported. If a long 32-bit word is read the upper word (bits 31-16) is the first word of the two and the lower word (bits 15-0) is the second. If the unit is read in 32-bit words the very first word will have the header in the upper bits and the first data word in the lower bits. It is acceptable to mix modes. The only rational reason for doing so would be to read the header word using D16 and then reading the remainder of the data in D32. The word count is always expressed in 16 bit words independent of the width of readout.

Header Word Format

The 16 bit header has the following format:

Bits 7-0	word count (between 0 and 129) (includes header word). This is always the number of 16 bit words independent of the VME access word width.
Bits 11-8	read pointer (this represents the buffer page the event was read from). This is useful as a synchronization check across multiple units.
Bits 15-12	tag field user programmable in mode register. This field can be used to identify a specific board in the crate.

If a data readout is attempted when there is no valid data in the unit (NCD set) a header word with a word count of zero will be read. This is can easily distinguished from a normal empty event which has a header word count of 1.

Data Word Format

Identical to 2748CAM except bit 15 is always zero. There is no trailer word, the header word must be used to determine number of words to read.

Bits 7-0	each indicate whether a particular wire was hit within the MDL108. Note at least one wire will be hit, as chips with no hits are zero suppressed and will not appear in the data stream.
Bits 12-8	The stream specific address of the of the MDL108. Address 0 corresponds to the MDL108 closest to the master (that is the first chip read out).
Bits 14-13	The stream number (0-3)
Bit 15	0

Parity Error

Bits 7-0 0

Bits 11-8 The stream specific address of the MDL108 in error. As above address 0 corresponds to the MDL108 closest to the master. This information can valuable in finding breaks in the stream as the first non-functional board in the stream can be determined.

Bits 14-13 The stream number (0-3)

Bit 15 0

The parity error indicates a transmission error from the stream cards to the 2748CAM. If this occurs, the most likely causes are unmatched stream cable lengths, bad connections or a faulty board. In general if the error occurs beyond the first MDL108 address then the chamber card or its backplane connections are probably faulty.

2749VME INTERFACE

The 2749VME is exclusive an A24 D16 interface with no block transfer support.

VME Address Map:

Offset from base address	bits	function
0x00		CTRL1
	0	Calibrate
	1	Software FCW
0x04		Status Register
	0	BUSY
	1	NCD
	2	CLOCKFAIL
0x08		CTRL0
	5-0	Calibration pulse spacing
	13-8	Test gate width
0x0C		CTRL2
	13-8	Out3 width
0x14	7-0	Scaler (read only)
0x24		Trigger test gate (write only)
0x28		Trigger Abort (write only)
0x2C		Reserved do not write
0x30		Trigger OUT3 pulse (write only)
0x34		Clear scaler (write only)
0x38		Trigger Readout (write only)

Clear Scalers (base+0x34): Clear scaler.

Read Scaler (base+0x14): Read 8 bit scaler, this scaler is incremented by pulses on input 1.

Read Status Register (base+0x04): The BUSY, NCD and CLOCKFAIL bits represent the current state of the corresponding command bus line. BUSY is 1 if any 2748VME on the command bus is busy. NCD is 1 if any 2748VME on the command bus does not have an event waiting to have its header word read. NOTE this does not mean that the any unit is necessarily empty. As soon as the header word is read on a 2748VME unit it asserts its NCD bit. CLOCKFAIL indicates that at least one of the units has an unpowered or non functional backplane connected to stream 0. Note this error will not be caused by a defective slave card. If this bit is set the failing 2748VME is unable to perform stream readout or ANY of its streams.

Readout (base + 0x38): Trigger readout (OR with front panel input).

Abort (base + 0x28): This command will cause TCLR to be pulsed. In addition, it will be passed over the front panel bus to the 2748VME which will clear any readout in progress or data awaiting VME readout. This command has the same effect as a pulse on the front panel ABORT. It is not necessary to OR the TCLR output into the chamber card fast clear as the abort will be fanned out to all the cards via the P2 pulse.

Pulse TGATE (base + 0x24): Triggers single programmable width pulse on TGATE output, preceded by a delay of approximately 13 μs after the VME access.

Pulse OUT3 (base + 0x30): Triggers single programmable width pulse on '3' output. This pulse is generated without a delay after the VME trigger.

CTRL0 (base+0x08)

This 16 bit read write register has the following functions:

bit field	function
5-0	Pulse pair separation of gate pulses during calibration mode. Separation = field * 50 ns. In this mode the gate pulse width is fixed at 50 ns (acceptable values 0 or greater than 3).
7,6	unused
13-8	Width of test pulse generated on TGATE upon (base + 0x24). Width = field * 50 ns. This field should be programmed between 0x03 and 0x3f (150 ns and 3.15 μs).
15,14	unused

The 2749VME allows the use of an external calibration (rather than the 2749VME preset values). This is achieved by writing zero to bit 5-0. A single pulse will be generated on the TGATE output during calibrations. This should not be OR'ed into the experimental gate instead it should be used to trigger the external standard which should generate a double pulse pair with the desired separation. This double pulse pair should be OR'ed into the experimental OR. The delay from the TGATE output to the

first pulse is not important but the second pulse must occur less than 6 μs after the TGATE output.

CTRL1 (base+0x00)

This 1 bit read write register is used for two functions:

bit field	function
0	While set the system will go into continuous CAL mode. All external readouts, aborts etc., must be prevented.
1	Setting this bit is equivalent to asserting the FCW input. Until it is reset any RDOUT from the 2748VME will not complete. It may be aborted or allowed to continue by resetting the bit.

CTRL2 (base+0x0C)

A 16 bit read write register

bit field	function
7-0	unused
13-8	Width of test pulse generated on '3' upon F25•A4•S1. Width = field * 50 ns The field should be programmed between 0x03 and 0x3f (150 ns - 3.15 μs).
15,14	unused

Scaler (base+0x14)

This 8 bit scaler is provided for diagnostic purposes. It is reset by a write to (base + 0x34) and counts the number of pulses at the '1' NIM inputs. This scaler is not latching and if readout while counting, incorrect data may be obtained. The scalers are designed to count at a maximum rate of 10 MHz.

2748VME & 2749VME

Before reading this section the manual describing the PCOS4 system in general should be read. The operation of the 2748VME is broken down into two separate sections. First the 2748VME and the chamber cards must be configured. Then 2749VME then takes over control of the system. It can issue calibration pulses and also trigger the 2748VMEs to read out their respective streams. After each readout (assuming it is not slow cleared) the data must be read from each 2748VME.

CONFIGURATION

The 2749VME should be set up prior to configuring the 2748VMEs. The 2749VME should be setup as follows:

- Write CTRL0 (5-0) (base + 0x08) to desired delay (typically 8-10 * 50 ns).
- If test pulses are required program CTRL0(13-8) (base+0x08) and or CTRL2(13-8) (base+0x0C).
- Ensure that the 2749VME is not in calibration mode by writing zero to CTRL1 (base+0x00).

The 2748VME is configured by the following sequence:

- Write mode register (base+0x10) to mode 2, stream 0
- Assemble chamber configuration data in 16 bit words (see chamber card manual).
- Write data to the stream using a series of writes to (48base+0x24). If a reasonable speed VME system is used (less than 20 μs per cycle) then it will be necessary to poll the status register on either the 2748VME or 2749VME until busy resets before issuing the next write to (48base+0x24). The data will be automatically shifted out to the furthest chamber card from the master.
- Issue P2 (48base+0x28, data=4), to copy the bits from the chamber shift registers to the configuration registers.
- This entire sequence should be repeated with the 3 other streams. The process is identical except that bits 2 and 3 of the mode register should be set to the correct stream.

To check system integrity the data written may optionally be non-destructively verified by the following sequence:

- Corrupt shift register by issuing a number of writes to (48base+0x24,data=2) (to guarantee that you truly read back the registered data and not just the contents of the shift register left over from when you loaded the stream).
- Write mode register (48base+0x10) to mode 2, stream 0.
- Issue P1 (48base+0x28, data=2), to transfer the chamber card configuration registers to their on chip shift registers.

- Write zero to the download register (48base+0x24, data = 0). This will cause the last 16 bits from the chamber card nearest the master to be shifted into the 2748VME; it will also clear the first 16 bits of the furthest chamber card's shift register.

- If a VME master with a cycle time of less than 20 μs is used, it is necessary to poll the status register until busy resets or wait 20 μs before proceeding.

- Read (48base+0x24). This will give the bits shifted in as a 16 bit word. Due to the circular nature of the shift register the first word read out should be the first word that was originally written.

- This sequence should be repeated until all the desired data has been read.

- This entire sequence should be repeated with the 3 other streams. The process is identical except that the mode register should show the correct stream.

- Set the board count registers (48base+0x00, 0x01, 0x02, 0x03) to the correct number of cards for each stream.

- The mode register should be set to mode 0 (or 1 if test mode is desired).

- Set RUN mode (bit 4 of mode register) to allow RDOUT pulses.

Once the streams have been initialized and the 2748VME and 2749VME have been programmed, the system must be calibrated. In normal running mode after the initial calibration (a minimum of 100 ms), the calibration procedure must be repeated periodically. If the temperature of the experiment is stable it can be expected to be only for a few ms every few minutes. The exact frequency of calibration must be determined experimentally. A status bit in the chamber card indicates after calibration that it was successful, please see chamber manual for more detailed information. For more information on the calibration procedure the chamber card manual should be consulted. The calibration is achieved by distributing a pulse pair over the gate line to all 2741 cards. This pulse pair is generated on the 2749VME TGATE output and should be OR'ed into the front end gate that the experimenter distributes to these cards.

- Load the desired calibration pulse pair separation using (49base + 0x08). After calibration the delays of the chamber cards will be adjusted to match the pulse pair separation.

- Under software control (49VME + 0x00) to the 2749VME or via hardware control (2749VME CAL) input, the system must be calibrated. To ensure correct delay settings CAL must initially be enabled for a minimum of 100 ms to stabilize the delay. It is not necessary to continuously pulse the CAL input. Calibrations will free run while the CAL input is high.

- At the end of the desired calibration signal clear the calibrate bit (49VME + 0x00) or CAL signal. After a 15 μs delay the system is

ready for operation. The trigger should not allow any gates until after 15 μs from turning off the CAL signal.

- The success of this operation can be verified (only necessary occasionally) by reading back the configuration stream and checking the PLL lock bit. For more information please see the chamber card manual.

RUN MODE

The unit should be programmed to mode 0 with the RUN bit off. An abort should be broadcast from the 2749VME to clear spurious data in the chamber cards. The RUN bit should be turned on for each card. It is important to note that RDOUT and GATE pulses should be vetoed at this stage as the boards would go out of sync as the are sequentially enabled. When the entire system is enabled RDOUT pulses may be initiated.

It is assumed at this point the configuration process outlined in the previous section has been completed. Note that the PCOS4 system manual should be consulted for the details of gate, clear and other signal distribution between PCOS4, the trigger and the host computer. The following description covers normal operation of the system with a trigger system. For testing the system a number of VME operations can be issued to the 2748VMEs and 2749VMEs to emulate trigger signals.

The 2741s are now live. After a gate is received by the 2741 cards, a coincidence decision will be made for each channel within the chamber cards. The first level trigger processor has two choices, either a READ can be issued to the 2749VME or the event can be cleared by simply pulsing the fast clear fanned out to the chamber cards (the 2748VME and 2749VME are not informed). If the clear option is chosen then a second gate may be issued after a short fast clear interval (see individual chamber card specification). Once an event has been chosen for readout and the READ pulse has been issued to the 2749VME no further gates should be issued until the readout is complete (monitor 2749VME BUSY). Failure to follow this requirement may result in several gate decisions being OR'ed. Shortly after BUSY is deasserted the data is ready for VME readout. Normally this should be determined by polling the NCD flag in the 2749VME.

During the stream readout and also while the data is awaiting VME readout an ABORT may be issued to the 2749VME. This will cause the current stream readout to be aborted and all data latched in the 2741 card and 2748VME to be cleared.

The data in each 2748VME is read by reading a header word from (48base+0x34) and then issuing the required number of reads to (48base+0x20).

GENERAL INSTALLATION

2748VME & 2749VME

The LeCroy 2748VME and 2749VME units are intended for use within a VME crate.

The 2748VME and 2749VME as per the VME specification MUST NOT be plugged into the crate with the crate power switched on. Doing so can cause damage, repair of damage so caused may not be covered under warranty.

Jumper Setting

The only user-selectable jumpers are I1A and I1B which are used for the STRUCK mode interrupt termination. If this mode is used a single link should be connected between I1A and I1B for the appropriate interrupt.

pin 1 - IRQ1
pin 2 - IRQ2
pin 3 - IRQ3
pin 4 - IRQ4
pin 5 - IRQ5
pin 6 - IRQ6
pin 7 - IRQ7
pin 8 - none (default)

Cables

The only cables necessary to connect the 2748VME to the 2741 cards are the stream cables. The recommended way of cabling is to used twist and flat (34 pin) (e.g. Spectrastrip 843-132-2801-034). It is important for error free operation that the 4 stream cables to any one 2748VME are the same length (to within 0.25m), and are less than 20m in length. The restriction on cable length makes it sensible to map the system with one 2748VME for each logical chamber plane. For operation in unusually noisy environments the use of shielded twist and flat may improve reliability. It is mandatory that the ground voltage between the two ends of the cable is less than 2 V (peak). The experimenter should ensure that the chamber and VME crate are connected to the same ground point (preferable using a star system). The line cord ground is NOT adequate. Damage to the 2748VME or chamber cards caused by excessive ground differentials between the detector and the VME crate may not be covered under warranty.

The stream connection between the 2748VME and each chamber card stream consists of 8 differential twisted pairs. The odd numbered pins are the positive signal and the even numbered the negative logic signal. In order to conserve panel space the stream cables are paired at the 2748VME. The numbering of the second stream on each connector is offset by 18 pins. The cabling should be arranged so that each 34 pin combined stream cable is split into 16 conductors from the top, 16 conductors from the bottom and two in the middle. The 2 in the middle are grounded while the two 16 conductor cables become the two stream cables. It is very important that the length of each stream cable is matched to within 0.25m. This is because the returning clock is only sensed on stream 0. It is assumed that all the returning data is synchronous. It should be noted that the closest and furthest refer to the cards positions relative to the board used as a master in each stream (the card the stream cable is plugged into).

Pin Numbers on Chamber Card	Pair	Description
1,2	TCLK	Outgoing clock to chamber card, only present during configuration and readout
3,4	Mode 0	
5,6	Mode 1	
7,8	Pulse 1	
9,10	Pulse 2	
11,12	TDAT	Outgoing data to furthest chamber card
13,14	RCLK	Returning clock, this is not used except for stream 0, which must be connected
15,16	DIN	Returning data from closest chamber card

The command cable between the 2748VME and 2749VME units is a TTL totem pole or Open collector unterminated bus. The pin assignments are as follows (Note: * denotes active low signal).

Pin Numbers	Name	Description
2,4,6,8,10, 12,14,16	GND	Connected to VME 0 V.
1	CLOCKFAIL*	Wire Ored across all 2748VMEís monitored by 2749VME.
3	ABORT*	Broadcast by 2749VME.
5	RDOUT*	Broadcast by 2749VME.
7	CAL*	Broadcast by 2749VME.
9	RESERVED	
11	NCD*	Wire Ored across all 2748VMEís monitored by 2749VME.
13	BUSY*	Wire Ored across all 2748VMEís monitored by 2749VME.
15	RESERVED	

2748VME DATA ENCODING (YALE ALGORITHM)

The data read out from the streams (in data readout modes 0 or 1) is in a continuous bit stream. Each MDL108 generates a 9 bit word. This word corresponds to the 8 latched hit inputs and 1 odd parity bit. The addition of the parity bit ensures that a stream fault is not likely to be confused with an empty stream. In a fault condition either the stream data would be all 1's or all 0's. All 1's would get attention as an all wires hit stream. All 0's will trigger a parity error.

The data from all four streams is simultaneously is read into the 2748VME stream controller. Each 9 bit data chunk is parity checked and zero suppressed during stream readout. The data is assembled in four separate 32 word areas of the buffer memory, one for each stream. The data actually written is of 2 possible types.

bit 15	bit 7-0	Data Word Type
0	0	regular encoded data word
0	0	parity error

The layout of these words is as follows:

Encoded data word

Bits 7-0	each indicate whether a particular wire was hit within the MDL108. Note that at least one wire will be hit, as chips with no hits are zero suppressed and will not appear in the buffer memory. Bit 0 corresponds to the first wire read into the 2748VME.
Bits 12-8	The stream specific address of the of the MDL108. Address 0 corresponds to the closest to the master (that is the first chip read out).
Bits 14-13	The stream number (0-3)
Bit 15	0

Parity error

Bits 7-0	0
Bits 12-8	The stream specific address of the MDL108 in error. Address 0 corresponds to the closest to the master. This information can be valuable in finding breaks in the stream as the first non-functional board in the stream can be determined.
Bit 15	0

2748VME OPERATION

The majority of the logic within the 2748VME is implemented using a XC4010 Xilinx logic cell array (LCA). The event buffering is split between a 16 bit wide RAM and a 16 bit wide FIFO. The register within the unit are implemented using the configurable RAM logic blocks and also flip flops of the XC4010. The LCA part is configured from two 16K serial PROMs at power up.

The XC4010 is synchronized to two different clocks. The low speed configuration control and data shifting, and VME interface are synchronized to the 40 MHz system clock; the outgoing stream clocks are also derived directly from the system clock. The 20 MHz stream readout, memory read and write and all data encoding is synchronized to the stream 0 returned clock. This choice with the requirement that all the stream cables be the same length gives a known timing relationship (independent of cable length) between the returning data on all streams and the clock. This technique greatly simplifies stream readout, as the incoming data is simply clocked with one returning clock. This clock can also be used to operate all the internal logic with no potential timing problems with multiplexing between streams. In order to allow the majority of the chips to function when stream readout has ended and the stream clock has been stopped the chip changes its source of clock from the returning 20 MHz clock to a direct 20 MHz clock which does not leave the Xilinx. Switching between these two clock sources cause a few clock cycles to be missed as readout is started. If readout is started and a returning clock is not detected a clock fail bit is set in the 2748VME and is wire-OR'ed across multiple 2748VME units and can be sensed globally on the 2749VME. This would typically occur if the backplane connected to stream 0 was not powered or defective. It is important to note that the majority of stream card failures would not interrupt the clock return.

The differential signals are driven using DS26C31 drivers, these CMOS versions offer more predictable propagation delay (reducing their contribution to the skew margin). The returning signals are not received using the standard DS26C32 receivers as their contribution to the skew margin would be too great. Instead AD9646 comparators (preceded by attenuators) are used. Even with worst case propagation delays and 0.3 meter variations in stream cable lengths, the four clocks have healthy skew margins to the returning clock.

2749VME OPERATION

Again most of the logic within the 2749VME is contained within a Xilinx logic array; in this case a XC4005. The only external components are the bus drivers, receivers and NIM/TTL converters. The LCA is configured from a 16K serial PROM on powerup.

CAMAC STREAM & SYSTEM CONTROLLER

2748CAM INTRODUCTION

The LeCroy 2748CAM is a CAMAC readout module for PCOS4 chamber cards. It provides the ability to configure and readout each chamber card. In conjunction with the 2749CAM PCOS4 driver unit it is used to calibrate the chamber cards' delays. The 2749CAM provides the interface between the readout system and the experimenter's trigger electronics.

GENERAL DESCRIPTION

Each 2748CAM is capable of reading out up to 256 wires from each of four streams giving a total of 1024 wires per unit. In a 25 slot crate a maximum of 22 2748CAM's and one 2749CAM can be accommodated, allowing a maximum of 22528 wires per CAMAC crate. It should be noted that reduced readout time will be achieved if the number of cards per crate is reduced.

The modules are used with a standard CAMAC controller and crate. A front panel bus connector is provided that can connect a full crate of 2748CAM units to one 2749CAM. The calibration and trigger interface can be handled by the 2749CAM which communicates with the 2748CAM's via the front panel bus.

The modules physical dimensions, power requirements, control and readout protocol are in compliance with ANSI/IEEE standard 583-1982. The only non-compliance is that the Read lines of the 2748CAM are driven using a tri-state driver (due to the steady trend to obsolescence of open collector octal drivers). The driver chosen meets the leakage specifications of the CAMAC standard. The CAMAC interface is 16 bits wide, the remaining 8 lines on the data way will be pulled high by the backplane during read (will readback zero) and will be ignored on write.

The 2748CAM under CAMAC control is used to serially download the configuration information for the chamber cards. It also supports readback to verify the contents. The four streams are configured separately, to allow the thresholds (and other parameters) to be changed on a board by board basis. The data is transferred in 16 bit words. Data is shifted out at a 1.25 MHz rate for configuration.

During delay calibration mode, the 2748CAM generates the necessary signals to arm and enable the increment /decrement of the PLL circuits on each chamber card. The programmable gates (with the desired delay) are created by the 2749CAM and distributed by the user through his main gate fan out. The synchronization of the 2748CAM and 2749CAM signals is achieved using the front panel flat cable bus.

In order to readout the chamber cards, the 2748CAM is triggered into stream readout mode (either by CAMAC command or from the 2749CAM). The 2748CAM then automatically handles the readout of all the streams under its control. The data is zero suppressed and then encoded before being written into a buffer memory. At the end of readout the encoded data can be readout using CAMAC reads. The data from all four streams is merged into one set of data. The number of chamber cards connected to each stream is programmable. This allows less than the maximum wires to be connected to each 2748CAM. Using this feature the chamber cards may be segmenting with one 2748CAM connected to each logical chamber plane, greatly simplifying cabling. The

data is readout from the stream serially at 20 MHz. The stream readout time for the 2748CAM is.

maximum number of wires on any single stream x 9 / 8 x 50 ns + 1 μs

It is important to realize that the stream readout time is independent of the number of wires hit and is determined by the stream with the most wires, hence to reduce readout time the streams should be evenly populated. To achieve higher performance, more 2748CAM should be used with fewer chamber cards per stream.

The crystal controlled timebase within the 2749CAM is derived from a 100 ppm crystal. Including all other instabilities within the system this allows the calibration pulse pair spacing to be set with a stability of < 0.5 ns. This is more than adequate to set up the delays on the chamber cards. The 2749CAM is capable under CAMAC control of providing a variety of test signals which can used to verify system operation with the minimum of external circuitry. The 2749CAM includes two simple (non-latching) 8 bit scalers, that can be used for monitoring the hit outputs of a 2748CAM. Note for a system with more than two 2748CAMs if this feature is required for a second level trigger a separate CAMAC scaler would be required.

SPECIFICATIONS

Please refer to the Model 2748CAM and 2749CAM technical data sheets for a complete summary of all relevant specifications.

2748CAM FRONT PANEL

The Model 2748CAM front panel provides the user with connectors for system integration and LEDs to assist system debugging.

Displays

Stream activity LED: A four element activity LED is provided, each segment will flash when its corresponding stream contains at least one hit during stream readout. Please note that if 2748CAM clocks are disabled after readout (under 2749CAM control), then LED operation may be affected, as the lights are driven from digital monostables clocked from the system clock. Stream 0 is the top light and stream 3 the bottom.

N LED: As per the CAMAC specification, this red LED is lit whenever the module is addressed from CAMAC.

Connections

The 2748CAM connects to the chamber cards via 4 stream cables. Each of these cables consists of 8 differential pairs. In order to conserve panel space the cables are paired into two 34 pin headers. This leaves 1 pair in the center of the 34 cable that is not used, to reduce noise pickup this pair is grounded at the 2748CAM. It is not intended that this be used as a ground connection between the chamber and the readout crate and hence it should be left disconnected at the far end.

In addition, a front panel lemo is provided which gives a short pulse during stream readout for every MDL108 chip hit. This pulse can be counted using a scaler. A 10-pin connector is provided for connection of the flat cable front panel bus connecting the 2748CAMs to the 2749CAM.

2749CAM FRONT PANEL

The Model 2749CAM front panel provides the user with connectors for system integration and LEDs to assist system debugging.

Displays

Status LED: A four element LED display is used to monitor the following signals. These signals are all pulse stretched to give a visible flash. The LEDs are not marked but in order from top to bottom :

1. Readout: CAMAC or front panel READOUT
2. Abort: CAMAC or front panel ABORT
3. CAL: CAMAC or front panel CAL
4. BUSY: Flat cable bus BUSY signal (this is the OR of BUSY from all the 2748CAMs)

N LED: As per the CAMAC specification, this red LED is lit whenever the module is addressed from CAMAC.

Connections

The 2749CAM connects to the trigger system via a series of NIM signal level lemo cables.

NIM Inputs

The following NIM inputs are terminated in 50 ohms to ground on the 2748CAM.

READ - This edge sensitive NIM signal will cause the 2749CAM to trigger the 2748CAMs into stream readout (assuming they are correctly set up)

ABORT - This edge sensitive NIM signal will cause the 2749CAM to signal the 2748CAMs to abort any stream readout in the progress. If an event is awaiting CAMAC readout, it will be cleared. In addition the 2748CAMs will issue a P2. P2 is a signal distributed over the stream cables to all chamber cards which will clear any event held in the 2741 cards.

CAL - This is a level sensitive NIM input. While active a series of pulse pairs with a programmable spacing will be generated on TGATE, in addition the 2748CAMs will be signaled to send the necessary pulses to the chamber cards before and after the gate pulses. The repetition rate of the pulse pairs is approximately 100 KHz.

1 - This input is connected to an 8 bit scaler that can readout under CAMAC control

2 - This input is connected to second 8 bit scaler

NIM Outputs

The following NIM outputs can sink 16 mA into a single terminated 50 ohm load. They are not designed for use with double terminations.

TGATE - This signal will under program control generate programmable width gate pulses for test purposes or when CAL is active generates calibration pulse pairs. For test use a CAMAC operation triggers a single gate pulse. To allow transients on the CAMAC backplane to decay before the gate pulse is issued, a delay of approximately 12 μs is inserted between the CAMAC operation and the issuing of the gate.

TCLR - This output goes active when either the Abort input active or an internal abort is generated using F25.A1. It may be connected into the experimental trigger (fanned out to front end cards in single buffered system ONLY). For double buffered systems it should not be used.

TBUSY - This output is the OR of the 2748CAM busy lines. It may be monitored to determine when the system is ready for another gate.

3 - This output provides a programmable width pulse immediately on CAMAC trigger.

2748CAM CAMAC INTERFACE

Commands and Functions

In typical operation, the crate controller issues a CAMAC command which includes specifying a station number (N), a subadddress (A), and a function code (F). In response, the module will generate a valid command accepted (X) response. If the command requires a response, the module will act on the command and produce a Q response. For further information on the CAMAC protocol, read “Introduction to CAMAC” found in the LeCroy Research Instrumentation Catalog. The commands recognized by the 2748CAM are listed and briefly described below. A CAMAC X response will be given for all valid commands (except Z·S2 and C·S2). The following commands should not be attempted when the 2748CAM clock is disabled (see 2749CAM CTRL2) : F0·A0, F16·A1, F25·A2, F25·A3, if they are attempted an X response will not be given. In general it is not expected that the 2748CAM will accessed with its clock disabled.

Clear (F9•S1) or (C•S2): Command issues slow reset. If this is not preceded by a readout command, it simply pulses P2 to all the chamber cards which causes any event registered in the chamber cards to be reset. If a readout is in progress or completed, the event ready flag will be reset and the unit returned to an idle state.

Clear LAM (F10•A0•S1): Clears the LAM source within the module.

Disable LAM (F24•A0•S1): Disable the LAM source.

Enable LAM (F26•A0•S1): Enable the LAM source.

Master Reset (Z•S2): Returns module to power up state

Test LAM (F8•A0•S1): Test LAM. A Q response will be generated if the internal LAM source is set.

Read event Data (F0•A0): The unit will readback the next encoded word in the buffer. If the word is valid a Q response will also be given. The next data word will be fetched on the S2 at the end of the cycle, ensuring sufficient time for the next word to be fetched before the next F0•A0. F0•A0 should only be attempted with the 2748CAM in modes 0 or 1.

Read configuration Data (F0·A1): The last 16 bits shifted in from the configuration data is readback. It is important to realize that this command only makes sense when used with F16·A1·S1 as the shifting of the configuration bits back from the stream only occurs when bits are being shifted out to the other end of the stream. The 2748CAM must be in mode 2.

Read memory (F0•A2): This option is provided only for diagnostic purposes. It causes the memory to be read directly at an address specified by the Address Register. For more information on the memory data format see the Theory of Operation. The 2748CAM must be in mode 2.

Read board count register (F1•A0 , F1•A1, F1•A2, F1•A3): These four 5 bit registers show the previously programmed number of boards in their respective streams. This information is used only during automatic stream readout. The unused high order bits will readback high. These registers may only be changed in mode 2. It is important to realize they are ignored during configuration download and readback.

Read mode register (F1·A4): This 4 bit read/write register contains the mode (bits 0,1) and the selected stream (2,3). Note the stream information is only used during downloading of chamber card configuration bits when the 2748CAM is in mode 2. In fact if mode 2 is selected, then all the unselected streams are placed in mode 0, with the selected stream placed in mode 2. At all other times the four streams operate simultaneously.

Read address register (F1·A5): This is only provided for diagnostic use and provides the memory address used in F0·A2. This register may only be accessed in mode 2.

Read double buffer enable (F1.A6): This register is used to enable double buffered mode of the 2748CAM, only bit 0 (the LSB) is used. All other bits read back high and are ignored on write.

Write configuration Data (F16•A1•S1): The word written will be shifted out to the stream selected in the mode register. The unit will be busy for approximately the next 17 us. At the end of this time 16 bits from the other end of stream will have been shifted back into the 2748CAM and if desired can be read back using F0•A1. This is only operational in mode 2.

Write memory (F16·A2): This option is provided only for diagnostic purposes. It causes the memory to be written directly at an address specified by the Address Register. The only use is for memory tests of the 2748CAM. This is only operational in mode 2.

Write board count register (F17·A0·S1 , F17·A1·S1, F17·A2·S1, F17·A3·S1): These 5 bit registers must be programmed with the number of boards in their respective streams. The allowable range is from 0 to 16. This registers can only be accessed in mode 2.

Write mode register (F17·A4·S1): This writes to the mode register as describe under F1·A4.

Write address register (F17.A5.S1): See F1.A5.

Write double buffer enable reg (F17.A6.S1): Enable/disable double buffered mode see below.

P1 (F25·A0): Trigger P1 to all cards. See Operating Instructions. This should only be attempted in mode 2. Note P1 pulses necessary during stream readout are generated automatically by readout.

P2 (F25·A1): Trigger P2 to all cards. See operating Instructions. This should only be attempted in mode 2. Note P2 pulses necessary during stream readout are generated automatically by readout.

Readout (F25·A2): Trigger Readout on 2748CAM. Note normally readout would be broadcast to all 2748CAM's in a crate by triggering 2749CAM. In this case this command does need to be used.

Slow Clear (F25·A0): Trigger slow clear on 2748CAM. Note normally slow clear would be broadcast to all 2748CAMs in a crate by triggering 2749CAM.

Test busy (F27·A0): Give Q response if 2748CAM is performing stream readout or shifting out configuration data.

Test Event Ready (F27·A1): Give Q response if 2748CAM has valid data awaiting F0·A0. This response will occur when queried after the end of stream readout and until the last word has been read

Mode Register (F1/F17·A4)

The mode register is broken into two fields. The two least significant bits (0 and 1) are the mode (0-3). The modes are as follows.

Mode	Function
0	Normal data readout mode
1	Test readout mode: This mode is identical to Mode 0 as far as the 2748CAM is concerned, the mode is echoed to all chamber cards on the four streams which causes them to generate test data. For further information see chamber card manual.
2	Configuration mode: This is used to download and verify setup information in the chamber cards
3	Calibration mode (note: not set directly, see below)

In normal circumstances calibrations are achieved under the control of a 2749CAM. In this case mode 3 on the 2748CAM mode should be 0 or 1. When the 2749CAM is switched into calibrate mode it will automatically pulse the 2748CAM streams to mode 3 during a CAL cycle. However, the mode read back via CAMAC on the 2748CAM would always be that written (that is 0 or 1).

Bits 2 and 3 of the mode register select the stream for configuration. This information is ONLY used in mode 2. When configuration data is written and readback from the chamber cards only one of the streams is placed in mode 2. The 2748CAM forces the other streams into mode 0 which prevents the P1 and P2 pulses corrupting the non-selected chamber cards configuration data. Though it should be noted that switching to configuration mode will corrupt any data waiting to be readout (both in the chamber cards and the 2748CAM memory).

Board Count Register 0-3 (F1/ F17·A0-3)

The number of pairs of MDL108 devices on each stream to be readout must be specified before triggering a readout. This is indicated by dividing the number of wires connected to each stream by sixteen (which in the case of the 2741M-16Y is equal to the number of cards) and writing it to each board count register. The maximum number of MDL108s that can be attached to a stream is 32, so the board count should be set between 0 and 16. Note it is acceptable to turn off a stream for readout by simply writing its board count to zero. It is also permitted to truncate a stream to fewer than the actual number of cards. The cards furthest from the master will never be read. However the programmer would be responsible for ensuring that ALL the boards were included in the configuration. The number of wires per stream should be a multiple of sixteen (using the 2741M-16Y this is guaranteed as it is a 16 channel unit). Note the Board count registers are 5 bit read write registers. The upper bits should be masked off in software during read. Providing no more than 32 MDL108s are connected to any one stream, there are no further restrictions as to the arrangement of cards. It is important to realize that these registers are not used for downloading or verification the configuration of the chamber cards. Stream 0 must always be connected to a powered master chamber card as the returning data clock is always taken from it.

Address Register (F1/F17·A5)

This 7 bit read/write register is provided for diagnostic use only. To test the RAM it is necessary to address it directly (normal Q stop readout F0·A0 does not allow random access). The address register serves this purpose. The RAM location to be addressed is written in the address register and the RAM can be accessed using F0/F16·A2. The upper 17 bits of the address register should be masked off on read. It should be noted that if a data record is examined using this method, the layout is not the same as for Q stop readout mode. For more information see section **Error! Reference source not found.**

Busy and Event Ready Flags

The busy and event ready flags may be sampled at any time using the appropriate F27 commands. The busy flag is set after a F25·A2 (or 2749CAM triggered readout) or F16·A1. It will remain set until the unit is ready for the next operation. The unit should not be addressed except by

F27 polls until the BUSY flag resets. The event ready flag is set at the end of stream readout it is reset at the end of CAMAC readout.

Data Format from F0·A0

Bit 15	Bit 7-0	Data Word Type
0	0	regular encoded data word
0	0	parity error
1	0	final encoded word.
1	0	trailer word

The layout of these words is as follows:

Encoded Data Word

Bits 7-0 each indicate whether a particular wire was hit within the MDL108. Note at least one wire will be hit, as chips with no hits are zero suppressed and will not appear in the buffer memory.

Bits 12-8 The stream specific address of the of the MDL108. Address 0 corresponds to the MDL108 closest to the master (that is the first chip read out).

Bits 14-13 The stream number (0-3)

Bit 15 0 = more words to follow 1= this is the last word

Parity Error

Bits 7-0 0

Bits 12-8 The stream specific address of the MDL108 in error. As above address 0 corresponds to the MDL108 closest to the master. This information can valuable in finding breaks in the stream as the first non functional board in the stream can be determined.

Bit 15 0

The parity error indicates a transmission error from the stream cards to the 2748CAM. If this occurs, the most likely causes are unmatched stream cable lengths, bad connections or a faulty board. In general if the error occurs beyond the first MDL108 address then the chamber card or its backplane connections are probably faulty.

All Streams Empty Trailer Word

Bit 7-0 0

Bits 12-8 The number of MDL108s on the longest stream.

Bit 15 1

In this case as there are no data words, the trailer is a stand alone word marked by setting its 8 most least significant bits to 0.

The only ambiguity with this scheme is, if the only word read from the stream is a parity error. In this case the parity error will not be obvious. This should not be a problem as it extremely unlikely that the faulty chip will evade detection with either real data or test patterns generated in the MDL108. In fact the parity error can be detected rather tediously by checking bits 12-8 of the ambiguous word. If they are less than the number of MDL108s on the stream, a parity error occurred. This checking would not seem necessary in normal use as the most likely cause of parity errors is broken stream cables, missing power etc. Any error will be found as soon as either a test hit or random noise coincidence occurs on the stream.

Double Buffer Enable/Disable Register (F1/F17.A6)

When the LSB of this register is zero, any incoming abort (whether from the command bus or CAMAC) is routed to the 2741 cards (in addition to clearing the current event). When set incoming aborts will not affect the 2741 cards. If a 2741 clear other than that provided automatically after every stream readout is required, it must be provided explicitly by F25.A1.S1 or via the experimenters trigger system. All other bits are ignored on write and read back as ones.

2749CAM CAMAC INTERFACE

Commands and Functions

An X response will be made for any valid CAMAC command (except C·S2 and Z·S2)

Master Reset (Z•S2): Reset all registers, return to power on state

Clear scalers C•S2 or F9•S1: Clear scalers 1 & 2.

Read Scaler 1 (F0·A0): Read 8 bit scaler, this scaler is incremented by pulses in input 1.

Read Scaler 2 (F0•A1): Read 8 bit scaler, this scaler is incremented by pulses in input 2.

Read CTRL0 (F1·A0): Read width/separation register.

Read CTRL1 (F1·A1): Read 2 bit CTRL1 register.

Read CTRL2 (F1·A2): Read width register, scale = 50 ns per unit.

Write CTRL0 (F17•A0•S1): Write CTRL0 (see below).

Write CTRL1 (F17•A1•S1): Write CTRL1 (see below).

Write CTRL2 (F17•A2•S1): Write width for output 3, bit 13-8 pulse width.

Readout (F25. A0·S1): Trigger readout (OR with front panel input).

Abort (F25. A1·S1): This command will cause TCLR to be pulsed (which should be fanned out to all the 2741 cards by the experimenter through the trigger). In addition, it will be passed over the front panel bus to the 2748CAM which will clear any readout in progress or data awaiting CAMAC readout. This command has the same effect as a pulse on the front panel ABORT.

Reserved (F25•A2•S1): For test use only (or'd with front panel CAL input).

Pulse TGATE (F25·A3·S1): Triggers single programmable width pulse on TGATE output. In order to allow transients from CAMAC bus activity to settle before the GATE pulse is issued, it is preceded by a delay of approximately 13 μs after S1.

Pulse OUT3 (F25 A4•S1): Triggers single programmable width pulse on '3' output. This pulse is generated without a delay after S1.

CTRL0

This 16 bit read write register has the following functions:

bit field	function
5-0	Pulse pair separation of gate pulses during calibration mode. Separation = field * 50 ns. In this mode the gate pulse width is fixed at 100 ns.
7,6	unused
13-8	Width of test pulse generated on TGATE upon F25•A3•S1. Width = field * 50 ns.
15,14	unused

Power up state is zero. Bit 23-16 will read back zero and will be ignored on write.

CTRL1

This 2 bit read write register is used for two functions:

bit field	function
0	While set the system will go into continuous CAL mode. All external readouts, aborts etc. must be prevented.
1	While set, the clocks on all the 2748CAMs will be disabled, this is provided as an option to possibly reduce noise during data collection.

Note the 2749CAM clock is a crystal and will continue to run. The only activity that should be attempted in this mode is to apply inputs to the 2741 and issue chamber card gates and clears. Obviously no readouts are possible. It is has not been demonstrated that this option makes any significant effect to 2741 noise.

Power up state is zero. On write bits 23-2 are ignored and on read bit 23-2 should be masked off.

CTRL2

A 16 bit read write register

bit field	function
7-0	unused
13-8	Width of test pulse generated on ‘3’ upon F25•A4•S1. Width = field * 50 ns.
15,14	unused

Scaler1 and Scaler2

These 8 bit scalers are provided for diagnostic purposes. They are reset by F9·S2, C·S2 or Z and count the number of pulses at the ‘1’ and ‘2’ NIM inputs respectively. These scalers are not latching and if readout while counting, incorrect data may be obtained. The scalers are designed to count a maximum rate of 10 MHz.

2748CAM & 2749CAM

Before reading this section the section describing the PCOS4 system in general should be read.

The operation of the 2748CAM is broken down into two separate sections. First the 2748CAM and the chamber cards must be configured. Then 2749CAM then takes over control of the system, it can issue calibration pulses and also trigger the 2748CAMs to readout their respective streams. After each readout (assuming it is not slow cleared) the data must be read from each 2748CAM.

CONFIGURATION

The 2749CAM should be setup prior to configuring the 2748CAMs. The 2749CAM should be setup as follows:

- Write CTRL0 (5-0) (F17•A0•S1) to desired delay (typically 8-10 * 50 ns).
- If test pulses are required program CTRL0(13-8) (F17•A0•S1) and or CTRL2(13-8) (F17•A2•S1).
- Ensure clocks are enabled and the 2749CAM is not in calibration mode by writing zero to CTRL1 (F17•A1•S1).

The 2748CAM is configured by the following sequence:

- Write mode register to mode 2, stream 0 (F17•A4•S1 W=2).
- Assemble chamber configuration data in 16 bit words (see chamber card manual).
- Write data to the stream using a series of F16•A1's. If a reasonable speed CAMAC system is used (less than 20 μs per cycle) then it will be necessary to poll F27•A0 until busy resets (no Q response) before issuing the next CAMAC F16•A1. The data will be automatically shifted out to the furthest chamber card from the master.
- Issue P2 (F25•A1), this will copy the bits from the chamber shift registers to the configuration registers.
- This entire sequence should be repeated with the 3 other streams. The process is identical except that the mode register should be set to the correct stream.

To check system integrity the data written may optionally be non-destructively verified by the following sequence.

- Corrupt shift register by issuing a number of F16•A1•S1's (to guarantee that you truly read back the registered data not just the contents of the shift register left over from when you loaded the stream).
- Write mode register (F17•A4•S1) to mode 2, stream 0.
- Issue P1 (F25•A0), this will transfer the chamber card configuration registers to their on chip shift registers.

- F16•A1•S1. data = 0. This will cause the last 16 bits from the chamber card nearest the master to be shifted into the 2748CAM, it will also clear the first 16 bits of the furthest chamber card's shift register.

- If a CAMAC master with a cycle time of less than 20 μs is used, it is necessary to poll F27•A0 until busy resets (no Q response) or wait 20 μs before proceeding.

- Read F0•A1. This will give the bits shifted in as a 16 bit word. Due to the circular nature of the shift register the first word readout should be the first word that was written originally.

- This F16•A1•S1, F27•A0•S1 F0•A1 sequence should be repeated until all the desired data has been read.

- This entire sequence should be repeated with the 3 other streams. The process is identical except that the mode register should show the correct stream.

- Set the board count registers (F17•A0-3•S1) to the correct number of cards for each stream.

- The mode register should be set to mode 0 (or 1 if test mode is desired)

Once the streams have been initialized and the 2748CAM and 2749CAM have been programmed, the system must be calibrated. In normal running mode with after the initial calibration (a minimum of 100 ms), the calibration must be repeated periodically. If the temperature of the experiment is stable it can be expected to be only for a few ms every few minutes. The exact frequency of calibration must be determined experimentally, a status bit in the chamber card indicates after calibration that it was successful, please see chamber manual for more detailed information. For more information on the calibration procedure the chamber card manual should be consulted.

- Load the desired calibration pulse pair separation using F17•A0•S1. After calibration the delays of the chamber cards will be adjusted to match the pulse pair separation.

- Under software control (F17•A1•S1 to the 2749CAM) or via hardware control (2749CAM CAL) input, the system must be calibrated. To ensure correct delay settings CAL must initially be enabled for a minimum of 100 ms to stabilize the delay. It is not necessary to continuously pulse the CAL input. Calibrations will free run while the CAL input is high.

- At the end of the desired calibration signal clear the calibrate bit (F17•A1•S1) or CAL signal. After a 15us delay the system is ready for operation. The trigger should not allow any gates until after 15us from turning off the CAL signal.

- The success of this operation can be verified (only necessary occasionally) by reading back the configuration stream and checking

the PLL lock bit. For more information please see the chamber card manual.

RUN MODE

It is assumed at this point the configuration process outlined in the previous section has been completed. Note the PCOS4 System section should be consulted for the details of gate, clear and other signal distribution between PCOS4, the trigger and the host computer. The following description covers normal operation of the system with a trigger system. For testing the system a number of CAMAC operations (primarily F25's) can be issued to the 2748CAMs and 2749CAMs to emulate trigger signals.

The 2741s are now live. After a gate is received by the 2741 cards, a coincidence decision will be made for each channel within the chamber cards. The first level trigger processor has two choices, either a READ can be issued to the 2749CAM or the event can be cleared by simply pulsing the fast clear fanned out to the chamber cards (the 2748CAM and 2749CAM are not informed). If the clear option is chosen then a second gate may be issued after a short fast clear interval (see individual chamber card specification). Once an event has been chosen for readout and the READ pulse has been issued to the 2749CAM no further gates should be issued until the readout is complete (monitor 2749CAM BUSY). Failure to follow this requirement may result in several gate decisions being OR'd. Once BUSY is deasserted the data is ready for CAMAC readout (F27•A1 will give Q response). It is acceptable to simply continuously pole the 2748CAMs until stream readout is complete using F27•A1.

As soon as the stream has been read out into the 2748CAM memory a further coincidence gate may be issued to achieve double buffered operation. Double buffering has some noise implications, CAMAC activity can be a major noise source to the chamber. With double buffering CAMAC activity will occur during 2741 live time. It is stressed that normal experimental techniques to improve grounding and screening should solve these problems. During the stream readout and also while the data is awaiting CAMAC readout an ABORT may be issued to the 2749CAM. This will cause the current stream readout to be aborted and all data latched in the 2741 card and 2748CAM to be cleared. It should be noted that ABORT should not normally be used in double buffered applications as 1 or 2 events may be cleared (the one in the 2748CAM and possibly a further coincidence decision in the 2741 cards).

The data in each 2748CAM is read by issuing F0•A0's until no Q response is received. As per the CAMAC specification the last word read (with no Q) contains no valid information. Note F27•A0 (BUSY) will not give a Q response after stream readout is complete (even though an event is now awaiting CAMAC readout in the 2748CAM memory). F27•A1 (EVENT READY) provides the correct indication of an event awaiting CAMAC readout. It will give a Q response after readout until after the F0•A0 that gets no Q response (indicating there are no more words). It will also stop giving Q responses after a slow clear.

A new feature added at ECO1003 of the 2748CAM is the provision of a simple double buffered mode of operation. An additional register (F1/F17•A6) enables this mode of operation. When the LSB of this register is

zero any clear applied to the unit will clear the 2741 cards in addition to any event awaiting CAMAC readout. This operation identical to the of ECO1002 units.

When the LSB is set, an event in the 2741 card and an event awaiting CAMAC become independently clearable. To clear an event in the 2741 cards that has not been transferred to the 2748CAM requires a clear fanned out from the experimenter's trigger directly to the 2741 cards. To clear only the event awaiting CAMAC readout (they may be another one in the 2741 cards) an abort is used. This may be carried out by the 2749CAM using its abort input or CAMAC instruction. It is important to note that the TCLR output of the 2749CAM will pulse if it is given an external or CAMAC abort. In double buffered mode the TCLR output should not be ORed into the experimental fast clear to the 2741 cards. If a separately controllable CAMAC pulse is required to do fast clear then the user NIM output 3 from the 2749CAM may be used.

GENERAL INSTALLATION

2748CAM & 2749CAM

The LeCroy 2748CAM and 2749CAM units are intended for use within a CAMAC crate with the following voltage sources properly connected to the backplane +6.0 V and -6.0 V. Each crate must be controlled by a CAMAC controller such as the LeCroy 8901A. Its purpose is to provide an interface between the 2748CAMs and 2749CAM and the host computer.

The 2748CAM and 2749CAM as per the CAMAC specification MUST NOT be plugged into the crate with the crate power switched on. Doing so can cause damage by the momentary misalignment of the power pins on the rear edge connector. Repair of damage so caused may not be covered under warranty.

Cables

The only cables necessary to connect the 2748CAM to the 2741 cards are the stream cables. The recommended way of cabling is to use twist and flat (34 pin) (e.g. Spectrastrip 843-132-2801-034). For error free operation, it is important that the 4 stream cables to any one 2748CAM are the same length (to within 0.25m), and are less than 20m in length. The restriction on cable length makes it sensible to map the system with one 2748CAM for each logical chamber plane. For operation in unusually noisy environments the use of shielded twist and flat may improve reliability. It is mandatory that the ground voltage between the two ends of the cable is less than 2 V (peak). The experimenter should ensure that the chamber and CAMAC crate are connected to the same ground point (preferable using a star system). The line cord ground is NOT adequate. Damage to the 2748CAM or chamber cards caused by excessive ground differentials between the detector and the CAMAC crate may not be covered under warranty.

The stream connection between the 2748CAM and each chamber card stream consists of 8 differential twisted pairs. The odd numbered pins are the positive signal and the even numbered the negative logic signal. In order to conserve panel space the stream cables are paired at the 2748CAM. The numbering of the second stream on each connector is offset by 18 pins. The cabling should be arranged that each 34 pin combined stream cable is split into 16 conductors from the top, 16 conductors from the bottom and two in the middle. The 2 in the middle are grounded, the two 16 conductor cables become the two stream cables. It is very important that the length of each stream cable is matched to within 0.25m. This is because the returning clock is only sensed on stream 0. It is assumed that all the returning data is synchronous. It should be noted that the closest and furthest refer to the cards position relative to the board used as a master in each stream (the card the stream cable is plugged into).

Pin Numbers on Chamber Card	Pair	Description
1,2	TCLK	Outgoing clock to chamber card, only present during configuration and readout
3,4	Mode 0	
5,6	Mode 1	
7,8	Pulse 1	
9,10	Pulse 2	
11,12	TDAT	Outgoing data to furthest chamber card
13,14	RCLK	Returning clock, this is not used except for stream 0, which must be connected
15,16	DIN	Returning data from closest chamber card

2748CAM DATA ENCODING (YALE ALGORITHM)

The data readout from the streams (in data readout modes 0 or 1) is a continuous bit stream. Each MDL108 generates a 9 bit word. This word corresponds to the 8 latched hit inputs and 1 odd parity bit. The addition of the parity bit ensures that a stream fault is not likely to be confused with an empty stream. In a fault condition either the stream data would be all 1's or all 0's. All 1's would get attention as an all wires hit stream. All 0's will trigger a parity error.

The data from all four streams at once is read into the 2748CAM stream controller. Each 9 bit data chunk is parity checked and zero suppressed during stream readout. The data is assembled in four separate 64 word areas of the buffer memory, one for each stream. The data actually written is of 3 possible types. The INTERNAL data format is described below. However, this format is only accessible to the user through diagnostic read mode (F0•A2). The data format is changed slightly before readout using Q stop mode.

bit 15	bit 7-0	Data Word Type
0	≠ 0	regular encoded data word
0	0	parity error
1		trailer word

The layout of these words is as follows:

- Encoded data word

  Bits 7-0 — each indicate whether a particular wire was hit within the MDL108. Note at least one wire will be hit, as chips with no hits are zero suppressed and will not appear in the buffer memory. Bit 0 corresponds to the first wire read into the 2748CAM.

  Bits 12-8 — The stream specific address of the of the MDL108. Address 0 corresponds to the closest to the master (that is the first chip read out).

  Bits 14-13 — The stream number (0-3)

  Bit 15 — 0

- Parity error

  Bits 7-0 — 0

  Bits 12-8 — The stream specific address of the MDL108 in error. Address 0 corresponds to the closest to the master. This information can valuable in finding breaks in the stream as the first non functional board in the stream can be determined.

  Bit 15 — 0

- Trailer word

In the internal buffer memory format the trailer word is always separate. It is important to note that in the normal Q stop readout mode (F0•A0), the trailer word is combined with the last data word (if possible).

Bits 3-0	0
Bits 5-4	address of next stream containing at least one data word (0 if last interesting stream)
Bits 7-6	0
Bits 12-8	equal to 1 greater than the greatest MDL108 on ANY stream.
Bits 14-13	The stream number (0-3)
Bit 15	1

During CAMAC Q stop readout bits 5 and 4 allow streams containing no useful data to be skipped. This is necessary to ensure that the next word can always be fetched before the next CAMAC operation. If for instance, stream 0 contained data, streams 1 and 2 were empty and stream 3 contained data then without this feature, it would be necessary during Q stop readout to skip over the trailer words of stream 0, stream 1, and stream 2 before finding the next data word. This would be difficult to achieve before the next CAMAC access. With this scheme the maximum number of words to be skipped is 1, the trailer in this case of stream 0.

During Q stop readout (normal operating mode) the data appears as one continuous data stream. The trailer words between each group of data words are suppressed. The data is essentially in the internal format with a few minor changes. The final word from the last stream containing data is marked as a trailer. This is simply indicated by setting bit 15 of the last data word. If there are no data words then the only word readout out has bits 7-0 and with bit 15=1. The only potential ambiguity with this scheme is if the only word readout is a single parity error. In this extremely unlikely case the parity error will not be obvious (in fact, using bits 14-8 it could be determined, but it is not worthwhile). The parity error is provided to detect breaks in the stream readout, this will be detected without ambiguity. As soon as an event is collected the parity error will be apparent.

2748CAM OPERATION

The majority of the logic within the 2748CAM is implemented using two Xilinx logic cell arrays (LCA). A XC3030 is used for the CAMAC decoding and control of Q stop readout. A much larger array the XC4005 is used to provide all the stream interface functions. The RAM is completely under the control of the XC4005. Some of the CAMAC registers are implemented using the configurable RAM logic blocks of the XC4005. The LCA parts are configured from two 8K serial PROMs at power up. A gateable 40 MHz delay line oscillator is the only clock provided on the 2748CAM, a crystal oscillator is not used to allow the option of disabling all clocks on the board to reduce conducted and radiated interference during 2741 live time. Experience to date has suggested that in a well

screened system, any improvement is too small to be measurable, but at least the 2748CAM clocks can at least be easily eliminated as a possible noise source. To disable all the 2748CAM clocks a line on the front panel bus must be asserted. This is achieved by writing to the 2749CAM.

The XC4005 is synchronized to two different clocks. The low speed configuration control and data shifting is synchronized to the 40 MHz system clock; the outgoing stream clocks are also derived directly from the system clock. The 20 MHz stream readout, memory access (during stream readout) and all data encoding is synchronized to the stream 0 returned clock. This choice with the requirement that all the stream cables be the same length gives a known timing relationship (independent of cable length) between the returning data on all streams and the clock. This technique greatly simplifies the stream readout Xilinx, as the incoming data is simply clocked with one returning clock, which can also be used to operate all the internal logic with no potential timing problems with multiplexing between streams.

The differential signals are driven using DS26C31 drivers, these CMOS versions offer more predictable propagation delay (reducing their contribution to the skew margin). The returning signals are not received using the standard DS26C32 receivers as their contribution to the skew margin would be too great. Instead, MVL407 comparators (preceded by attenuators) combined with ECL to TTL level translators are used. The inputs are arranged so that the returning stream 0 clock and data 1, data 2, data 3 are brought through the same MVL407 to improve skew matching. Data 0 has the best incoming relationship to the returning stream 0 clock and hence can afford to go through a separate MVL407. Even with worst case propagation delays and 1 foot variations in stream cable lengths, the four clocks have healthy skew margins to the returning clock.

2749CAM OPERATION

Again most of the logic within the 2749CAM is contained within a Xilinx logic array, in this case a XC4003. The only external components are the bus drivers, receivers and NIM/TTL converters. The LCA is configured from a serial PROM on powerup.