OPERATOR'S MANUAL

MODEL VT960

96-CHANNEL
VME TDC

CE

LeCroy

Innovators in Instrumentation

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CE CONFORMITY

CONDITIONS FOR CE CONFORMITY

Since this product is a subassembly, it is the responsibility of the end user, acting as the system integrator, to ensure that the overall system is CE compliant. This product was demonstrated to meet CE conformity using a CE compliant crate housed in an EMI/RFI shielded enclosure. It is strongly recommended that the system integrator establish these same conditions.

CAUTION

COOLING

It is imperative that the module VT960 TDC be well cooled. Be sure fans move sufficient air to maintain exhaust air temperature at less than 50° C.

INSTALLATION

“Hot” insertion (insertion with crate power turned on) of modules is not recommended in the present VME specification. *Install the modules with the power **off**.*

SPECIFICATIONS

The information contained in this manual is subject to change without notice. The reference for product specification is the Technical Data Sheet effective at the time of purchase.

ELECTROSTATIC SENSITIVITY

While measures have been taken to protect the MTD133 TDC ASIC from electrostatic damage, it is still imperative to follow anti-static procedures when handling this CMOS device. Removal of the MTD133 from its socket will void the product warranty.

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GENERAL INFORMATION

PURPOSE

This manual is intended to provide instruction regarding the setup and operation of the LeCroy Model VT960 Time-to-Digital Converter. In addition, it describes the theory of operation and presents other information regarding its functioning and application.

UNPACKING AND INSPECTION

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the enclosed Packing List and shortages reported promptly. If the shipment is damaged in any way, please notify the Customer Service Department or the local field service office. If the damage is due to mishandling during shipment, you may be requested to assist in contacting the carrier in filing a damage claim.

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LeCroy warrants its instrument products to operate within specifications under normal use and service for a period of one year from the date of shipment. Component products, replacement parts, and repairs are warranted for 90 days. This warranty extends only to the original purchaser. Software is thoroughly tested, but is supplied "as is" with no warranty of any kind covering detailed performance. Accessory products not manufactured by LeCroy are covered by the original equipment manufacturers' warranty only.

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LeCroy offers a selection of customer support services. For example, Maintenance Agreements provide extended warranty that allows the customer to budget maintenance costs after the initial warranty has expired. Other services such as installation, training, on-site repair, and addition of engineering improvements are available through specific Supplemental Support Agreements. Please contact the Customer Service Department for more information.

DOCUMENTATION DISCREPANCIES

LeCroy is committed to providing state-of-the-art instrumentation and is continually refining and improving the performance of its products. While physical modifications can be implemented quite rapidly, the corrected documentation frequently requires more time to produce. Consequently, this manual may not agree in every detail with the accompanying product and the schematics in the Service Documentation. There may be small discrepancies in the values of components for the purposes of pulse shape, timing, offset, etc., and, occasionally, minor logic changes. Where any such inconsistencies exist, please be assured that the unit is correct and incorporates the most up-to-date circuitry.

SOFTWARE LICENSING AGREEMENT

Software products are licensed for a single machine. Under this license you may:

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- Modify the software and/or merge it into another program for your use on a single machine.
- Transfer the software and the license to another party if the other party accepts the terms of this agreement and you relinquish all copies, whether in printed or machine readable form, including all modified or merged versions.

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Products requiring maintenance should be returned to the Customer Service Department or authorized service facility. If under warranty, LeCroy will repair or replace the product at no charge. The purchaser is only responsible for the transportation charges arising from return of the goods to the service facility. For all LeCroy products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired or replaced. The customer will be billed for the parts and labor for the repair as well as for shipping. All products returned for repair should be identified by the model and serial numbers and include a description of the defect or failure, name and phone number of the user. In the case of products returned, a Return Authorization Number is required and may be obtained by contacting the Customer Service Department at (914) 578-6030.

PRODUCT DESCRIPTION

2.1 INTRODUCTION

The LeCroy Model VT960 provides 96 channels of either Common Start or Common Stop multi-hit Time-to-Digital Conversion designed for elementary particle or nuclear physics experiments. All input time signals to be measured, “hits”, are received via differential ECL (dECL) front panel inputs. Time differences between hits and a common reference input are measured with 500 psec LSB, and up to 16 hits within a 32.768 μsec range can be detected. With the CLOCK/2 option activated, the full scale range becomes 65.536 μsec, with 1 nsec resolution. The time measurement is performed using the MTD133, a full custom ASIC developed by LeCroy Corporation.

2.2 GENERAL DESCRIPTION

The VT960 Time-to-Digital Converter features a 500 psec least count and can store up to 16 hits per channel within a 32.768 μsec full scale range. Time data relative to the common input is stored in a LIFO within the MTD133 until it is transferred to the VT960’s buffer memory.

Each VT960 has 96 channels of front-panel hit inputs and a Common input. All inputs are differential ECL (dECL) and are terminated by a balanced 110 ohm impedance matching network.

The VT960 can operate in either Common Start or Common Stop mode. In Common Start mode, the common input receives a start pulse and the individual channels can register up to 16 subsequent hits during a programmable Common Start Timeout window. In Common Stop mode, the 96 front panel inputs accept hits until a common input latches a stop pulse. In both modes, if more than 16 hits occur per channel, only the last 16 hits are retained.

Each channel can be programmed to detect rising and/or falling edges (hits). The number of hits to store is also programmable with a maximum of 16. Selected edges can be detected with a separation of as little as 10 nsec. If multiple common input pulses are received, only the first is registered.

Operation of the VT960 can be divided into four phases: programming, acquisition, buffering and readout. Once the control/status registers have been programmed the module is in acquisition mode and ready to latch hits. In Common Start mode, the acquisition phase begins when the module latches a start and ends after a user programmable common start timeout. No hits will be recorded after the programmed hit window expires. A front-panel dECL input is also provided to allow the use of an external timeout if desired. The maximum acquisition time, however, is internally restricted to 32.768 μsec, regardless of the application of an external timeout. Immediately following the acquisition phase, the time data is transferred to a 16 event circular buffer, awaiting readout to VME. Readout of the event just buffered can occur as quickly as 500 nsec after the end of buffering. The module automatically returns to acquisition mode once all the time data for a particular event has been safely buffered. Readout of events previously stored in the buffer memory may occur simultaneously with acquisition or buffering without any performance penalty.

In both Common Start and Common Stop modes, a programmable fast clear window begins immediately following the end of acquisition. During the fast clear window (FCW), a user can safely clear an event (e.g. based on a experiment trigger decision) and return to acquisition mode,

thus, saving the time necessary for buffering and reading out the event. The FCW can range from 800 nsec to 400 μsec.

The data for each event stored in the multi-event circular buffer is preceded by a header word identifying the address (geographic or logical), the buffer number, and the word count for the event. A parity bit is set, such that the total number of bits set to 1, in the word, is an even number. The timing measurements of the VT960 are stored as 32-bit words. The least significant 16-bit word is the time measurement data. The most significant 16-bit word contains the channel number, phase (leading or trailing), even parity, buffer number (modulo 4), and the geographic address.

The functionality of the VT960 can be tested using either an internal tester or a front panel dECL test input. The internal tester can be programmed to produce 1, 2, 4 or 8 pulses of width 125, 250, 500, or 1000 nsec. When there are several pulses, the pulse separation is equal to the pulse width. Either leading, trailing, or both edges of the pulses can be selected for detection, creating up to 16 internal hits per channel. Testing can be performed in either Common Start or Common Stop modes.

2.3 SPECIFICATIONS

Please refer to the Model VT960 technical data sheet in the front of this manual for a complete summary of all relevant specifications.

2.4 FRONT PANEL

The VT960's front panel provides connectors for system integration and LEDs to indicate the module status and assist system debugging. Cables necessary for proper installation can be purchased from LeCroy. See Section 3.2 for more information regarding cabling.

2.4.1 Displays

Eight colored LEDs reside on the front panel of the VT960 to indicate the status of operations. A brief description of each is listed below: LEDs blink for at least 100 msec to aid in viewing.

A - ACTIVE: This yellow LED is lit whenever the TDC module is available to accept VME cycles and blinks ‘OFF’ when a cycle with a valid address is received.

P - POWER: This red LED is lit when all power supplies are on and within specification, no fuses blown.

R - RUN: This green LED, when lit, indicates the internal logic is running. During and shortly after VME SYSRST*, internal logic is not running.

H - HALT: This red LED, when lit, indicates the internal logic is halted. During and shortly after VME SYSRST*, internal logic is halted.

NE - NOT EMPTY: This yellow LED is lit whenever the TDC module has at least one event in the buffer.

F - FULL: This red LED is lit whenever the module has sixteen events in the buffer.

ST - START: This green LED, when lit, indicates the common input mode is in common start. It blinks momentarily 'OFF' when a common input is received.

SP - STOP: This red LED, when lit, indicates the common input mode is in common stop. It blinks momentarily 'OFF' when a common input is received.

2.4.2 Inputs

All front-panel inputs to the VT960 are differential ECL compatible with the ECLine standard. In the quiescent state, the "+" input is at least 200 mV more negative than the "-" input. Each pair of differential inputs is terminated with an effective 112 ohms. When inputs are connected with a logic value of "0" the (+) input sits at -1.7 V, and the (-) input at -0.7 V.

All hit inputs are received via six 34-pin connectors. A 3M connector type 3414-6034 will mate with the TDC header and provide strain relief. Pin 33 is connected to circuit ground, and Pin 34 is connected to chassis ground. The circuit ground and the chassis ground are connected to each other on the printed circuit board through 100 ohms. The hit inputs are numbered from bottom to top in ascending order. Four control inputs are differentially received via an 8-pin header located at the top of the front panel.

The control signals can be connected by single pair headers, AMP part number 5-87456-2, or they can all be connected simultaneously by a 8-position connector, AMP part number 87456-2. A brief description of each input follows below.

TIM: A dECL input used to receive the Common Start Timeout pulse. When operating in Common Start mode, it is necessary to define a period of time when the TDC will register hits. The beginning of this period starts with receipt of the Common Start. The end of this time occurs when the module receives the timeout pulse. Front panel input of this signal is selected by setting the Common Start Time Out Register (offset 0x10B0) to 0. This signal may be daisy chained on the front panel if the 112 ohm input termination are switched off from all except the last module in the chain. This signal can also be provided by the on-board programmable timer. If the front panel source for this signal is selected but does not arrive, the module will still time out after 32 μsec.

CLR: A dECL input used to issue fast clears to the module. A clear pulse can be issued at any time inside the Fast Clear Window or when buffering is not in progress, and should be at least 40 nsec wide. When a clear is issued, the data of an unbuffered event is cleared. The module returns to acquisition mode 250 nsec after the trailing edge of the pulse. (Note: There is no output signal coinciding with the module's return to the ready state.) The control and status registers are not affected by a clear. The front panel CLR input is always enabled as a possible source of this signal. CLR may be daisy chained on the front panel if the 112 ohm input termination is switched off disabled for all except the last module in the chain. A CLR input arriving outside the Fast Clear window has no effect.

COM: A dECL input which receives the common input pulse. Any pulse, whether it be a start or a stop, received via the COM input is global to all 96 channels. In Common Start mode the pulse acts as a global start for every channel, and in Common Stop mode it acts as a global stop for every channel. Front panel input of this signal is selected by setting Control Signal Source Register bit 5 to zero. This signal may be daisy chained on the front panel if the 112 ohm input termination are switched off for all except the last module in the chain.

IN: All 96 dECL inputs are used to receive individual channel hits. In Common Start mode the stop pulses are received via the connectors marked IN, and in Common Stop mode the start pulses are received. A rising edge on the (+) (rising from -1.7 V to -0.7 V) will generate a data word that is marked as a rising edge. Alternatively, if the transition on the (+) input is negative-going (falling from -0.7 V to -1.7 V), the hit will be marked as a falling edge. The (-) edge should have the complimentary signal, as per the dECL standard.

Jumper J8 controls a diode biasing network on the 96 hit input pins. The inputs accept “voltage” signals when there is a link between 2 and 3 (normal dECL, default), and to accept “current” signal when there is a link between 1 and 2 (biasing active).

2.4.3 Outputs

The one front panel output from the VT960 is differential ECL. This output is terminated with 112 ohms to -2 V.

BIP: Buffering in Progress (BIP) is a single dECL signal provided to aid data acquisition logic. While BIP is true, the current event’s data is being buffered and the data from this event is not yet ready for readout via VME. BIP will also become true when all buffers are full and no further events can be accepted. In the event of a fast clear, BIP will go false within 75 nsec of the rising edge of the fast clear pulse. Buffered events may still be read out via VME at any time. Jumper J1 allows selection of external or internal BIP for synchronization of modules in an event for readout: when there is a link between 1 and 2, the “BIP input” is taken from the connector, when there is a link between 2 and 3, the “BIP input” is simply derived from the internal logic. The position of J1 is immaterial if the BIP signal is not bussed (e.g. in a “wire-or” fashion).

2.4.4 Termination Control

The switch array SW1 is used to select the presence or absence of termination resistors on COM, TIM, CLR and BIP. When these signals are bussed, only modules located at the end of a bus should have termination resistors present. When a switch is moved towards the rear (“ON”), a termination resistor is made electrically present. Switches of SW1 numbered 1, 2, 3, 4, 5, 6, 7, and 8 control the electrical presence of a termination on CLR+, CLR-, COM+, COM-, TIM-, TIM+, BIP- and BIP+ respectively.

2.5 GENERAL OPERATION

The operation of the VT960 can be divided into four unique phases. The first phase includes the setup steps necessary for proper VT960 operation. This includes installation of the module and programming of the control registers. The module will not latch hits until the control registers have been programmed. Once the setup phase is completed, the module is in acquisition mode and ready to accept hits. The module remains in acquisition mode until either a Common Start Timeout or a Common Stop occurs, depending on the acquisition mode programmed.

Following acquisition mode, the module buffers the data into a multiple event data buffer. It can take a maximum of 78 μsec for an event to be buffered, depending on the number of hits in the event. While the data is being buffered, the Buffering In Progress (BIP) signal is true. The user can begin the final phase, readout, 500 nsec after the buffering has finished. However, previously buffered events can be readout while the most current event is being buffered, without a penalty in buffering speed.

2.5.1 Setup

Note that if the VME crate does not provide VIPA GA lines on the outer row of P1, you must set the base address Dip switch, SW5. Only switches 1 to 5 are used, switch 6 is not used at this time. If the VIPA GA lines are not present, the switch setting is latched at power on time and is used as the base address of the module. As per the VME specification, the VT960 should be inserted in the VME crate with the power off. No special precautions are required when attaching the front panel connectors. If it is desired to daisy chain the COM or CLR signals, the terminations for these signals must be switched off on all except the last unit in the daisy chain.

After the CSR registers are programmed, the unit is ready to acquire data. Data may be taken immediately if the power-up default values of the CSR registers are suitable for the application. The power-up defaults are:

- MTD Mode = Common Stop: both edges enabled; geographic header word; 250 MHz clock
- Common Start Timeout = 32768 nsec
- Fast Clear Window = 524288 nsec
- Internal Tester Control = disabled; 1 test pulse; 125 nsec test clock
- A32 Base Address = 0
- Full scale range = 32768 nsec
- LIFO depth = 16
- Read Pointer = 0
- Write Pointer = 0
- Unread Event Buffer Register = 0

When more than one module is present, the Logical (A32) Base Address must be programmed and unique for each module before readout of data. One scheme is to set this Base address to 0x20000 times the slot number.

2.6 CONTROL AND STATUS REGISTERS

All CSRs are in a special A24 address space. They can be accessed at their respective offsets from the CR/CSR base address with the hex 2F address modifier. All registers can be accessed in D32, D16, or D08. Since the registers are aligned on the least significant bytes, access to the registers in D08 takes place at an address offset equal to the quoted D32 offset, plus 3. Similarly, D16 accesses can be done at the quoted offset, plus 2.

2.6.1 Base Address Register

0x7FFFC: Base Address Register (BAR) for CR/CSR Access (5 bits, 1 byte)

Bit	Description
7	MSB
6	:
5	:
4	:
3	LSB

The value of this register at power-up is determined by the geographic address (i.e., the slot number) provided by the VME crate via the VIPA-GA lines. It can be written: if the new value is different from the original one, the base address is changed, and subsequent accesses must be made at the new base address.

2.6.2 Bit Set Register

0x7FFF8: Bit Set Register (1 byte)

Bit	Action when writing a "1" to the bit	Meaning when read as "1"
7	RESET Module	Module has been RESET
6	No effect	Will always read 0
5	No effect	Will always read 0
4	Enable Logical addressing	Logical addressing enabled
3	No effect	Will always read 0
2	No effect	Will always read 0
1	No effect	Will always read 0
0	No effect	Will always read 0

2.6.3 Bit Clear Register

0x7FFF4: Bit Clear Register (1 byte)

Bit	Action when writing a "1" to the bit	Meaning when read as "1"
7	Clear bit 7, stop indicating module has been reset.	Module has been RESET
6	No effect	Will always read 0
5	No effect	Will always read 0
4	Disable Logical addressing	Logical addressing enabled
3	No effect	Will always read 0
2	No effect	Will always read 0
1	No effect	Will always read 0
0	No effect	Will always read 0

For both the Bit Set and Bit Clear register, writing a "0" on any bit causes no action. Also note that at power-up, both bits 4 and 7 are cleared.

2.6.4 User Bit Set Register

0x7FFEC: User Bit Set Register (1 byte, 3 bits)

Bit	Action when writing a "1" to the bit	Meaning when read as "1"
7	No effect	Will always read 0
6	No effect	Will always read 0
5	No effect	Will always read 0
4	No effect	Will always read 0
3	No effect	Will always read 0
2	Generate a COM pulse	A COM pulse was generated
1	Generate a FAST CLEAR pulse	An FC pulse was generated
0	Generate a TEST pulse	A TEST cycle was generated

2.6.5 User Bit Clear Register

0x7FFE8: User Bit Clear Register (1 byte, 3 bits)

Bit	Action when writing a "1" to the bit	Meaning when read as "1"
7	No effect	Will always read 0
6	No effect	Will always read 0
5	No effect	Will always read 0
4	No effect	Will always read 0
3	No effect	Will always read 0
2	Clear bit 2 (stop indicating a COM was generated)	A COM pulse was generated
1	Clear bit 1 (stop indicating an FC was generated)	An FC pulse was generated
0	Clear bit 0 (stop indicating a TEST cycle was generated)	A TEST cycle was generated

For both the User Bit Set and User Bit Clear register, writing a "0" to any particular bit causes no action. At power-up, these registers read as 0.

2.6.6 Function 0 Address Decode Register, byte 3 (Least Significant Byte)

0x7FF6F: This register contains bits 0-7 of the base address of the data space. It is zero by default. It is allowed to write to this register, but its value will remain zero, since the A32 base address has to be a multiple of 0x20000.

2.6.7 Function 0 Address Decode Register, byte 2

0x7FF6B: This register contains bits 8-15 of the base address of the data space. It is zero by default. It is allowed to write to this register, but its value will remain zero, as the base address has to be a multiple of 0x20000.

Function 0 Address Decode Register, byte 1

0x7FF67: This register contains bits 16-23 of the base address of the data space. It is zero by default. It is allowed to write any value to this register, but it will always read back rounded to a multiple of two, because the A32 base address has to be a multiple of 0x20000.

2.6.9 Function 0 Address Decode Register, byte 0

0x7FF63: This register contains bits 24-31 of the base address of the data space. It is zero by default. **Note:** The function 0 address decode register belongs to the recommended way to describe the AM codes and functions available on a module under the VITA-25 VME-64x proposed standard, see http://www.vita.com/vso/draftstd/vme64x_d19.pdf for details.

2.6.10 MTD Mode Register

0x101B4: MTD Mode Register (4 bits, 1 byte)

Bit	Description
5	1 = Logical address appears in header word 0 = Geographical address appears in header word (default)
4	1 = CLOCK/2 enabled 0 = CLOCK/2 disabled (default)
3	1 = Enable Falling Edge Acquisition (default) 0 = Disable Falling Edge Acquisition
2	1 = Enable Rising Edge Acquisition (default) 0 = Disable Rising Edge Acquisition
1	1 = Enable Commons (default) 0 = Commons disabled
0	0 = Common Stop (default) 1 = Common Start

Common Start Timeout Register

0x101B0: Common Start Time Out Register (4 bits, 1 byte)

Bit values [3-2-1-0]	Description
0000	Front Panel
0001	64 ns
0010	128 ns
0011	256 ns
0100	512 ns
0101	1024 ns
0110	2048 ns
0111	4096 ns
1000	8192 ns
1001	16384 ns
1010	32768 ns
1011	32768 ns
1100	32768 ns
1101	32768 ns
1110	32768 ns
1111	32768 ns (default)

Note: These times are to be multiplied by two when the CLOCK/2 option is activated.

2.6.12 Fast Clear Window Register

0x101AC: Fast Clear Window Register (4 bits, 1 byte)

Bit values [3-2-1-0]	Description
0000	1024 ns
0001	2048 ns
0010	3072 ns
0011	4096 ns
0100	6144 ns
0101	8192 ns
0110	12228 ns
0111	16384 ns
1000	24576 ns
1001	32768 ns
1010	49152 ns
1011	65536 ns
1100	98304 ns
1101	131072 ns
1110	262144 ns
1111	524288 ns (default)

Note: These times are to be multiplied by 2 when the CLOCK/2 option is activated.

2.6.13 Internal Tester Control Register

0x101A0: Internal Tester Control Register (5 bits, 1 byte)

Bit	Description
4	1 = Enable Internal Tester 0 = Disable Internal Tester

Bits 3 & 2	Description
00	1 pulse
01	2 pulses
10	4 pulses
11	8 pulses

Bits 1 & 0	Description
00	125 ns
01	250 ns
10	1000 ns
11	2000 ns

Important: Bit 4 should be cleared before making external data acquisition, since tester mode may interfere with the normal acquisition of events. All bits are 0 by default.

2.6.14 Read Buffer Pointer Register

0x1019C: Read Buffer Pointer Register (32 bits, 4 bytes) Read Only. An attempt to write to this register will cause a Bus Error. Will only change as the result of an Advance Read Pointer Command.

2.6.15 Write Buffer Pointer Register

0x10198: Write Buffer Pointer Register (32 bits, 4 bytes) Read Only. An attempt to write to this register will cause a Bus Error. Will only change as the result of the module accepting events.

2.6.16 Advance Read Pointer Register

0x10194: Advance Read Pointer Register (1 bit, 1 byte) (Write Only)

Bit	Description
0	1 = advance read pointer (pulse) 0 = no action
1	1 = reset Read Pointer, Write Pointer & Unread Event Buffer Register (pulse) 0 = no action

A Bus Error will be generated if a read of this register is attempted.

2.6.17 Unread Event Buffer Register

0x10190: Unread Event Buffer Register (16 bits, 2 bytes)

Bit	Description
15	Buffer 15 1 = unread 0 = read
:	:
0	Buffer 0 1 = unread 0 = read

These status bits are set when a valid event is taken, and reset when the read pointer advances past the bit number. For example, if this register is read after 5 events are taken and 2 advance read pointer commands are accepted, a value of hexadecimal 001C and be expected in this register. In addition, all bits can be set or reset explicitly by the user, if so desired.

2.6.18 Control Signal Source Register

0x1018C: Control Signal Source Register (7 bits, 1 byte)

Bit	Description
6	source of COM 0 = Front Panel (default); 1 = VIPA backplane
5	source of Fast Clear 0 = Front Panel (default); 1 = VIPA backplane
4	source of BIP 0 = Front Panel (default); 1 = VIPA backplane
3	EXT_BIP_EN, external BIP synchronization 0 = disable 1= enable

2	Drive COM on backplane 0 = NO (default); 1 = YES
1	Drive Fast Clear on backplane 0 = NO (default); 1 = YES
0	Drive BIP on backplane 0 = NO (default); 1 = YES

2.6.19 Interrupt Vector Register

0x10188: (32 bits, 4 bytes) Writing to this address specifies the interrupt vector that the interrupted master will receive when an interrupt occurs. It will be issued on the bus during a properly addressed IACK cycle.

2.6.20 Interrupt Enable Register

0x10184: When this is set, an IRQ1 signal will be generated when all event buffers are occupied by taken events, in other words, when the FULL LED turns on. Clearing this bit will also clear the interrupt request if one was issued.

Bit	Description
0	1 = Level-1 Interrupts Enabled 0 = Interrupts Disabled (default)

2.6.21 Sparsification Control Register

0x10183: Sparsification Control Register (2 bits, 1 byte).

Bit	Description
0	1 = Sparsification Enabled 0 = Sparsification Disabled (default)
1	1 = Complex Sparsification Enabled 0 = Simple Sparsification (default)

NB: If bit 0 is not set, the state of bit 1 is irrelevant. The Simple Sparsification algorithm is a simple comparison with a threshold on a channel per channel basis, the hits below threshold being discarded. The Complex Sparsification algorithm is identical, except the hits of a given channel are kept regardless of their value compared to threshold, if the “Hit Count” for the channel is 1, 2, or 3. Setting the LIFO depth to 1, the full scale range to a small value, and enabling complex sparsification, provides a means to achieve considerable data reduction when operating this module in conjunction with the MQT300A.

2.6.22 Sparsification Threshold Registers

0x1017E, 0x1017A … 0x10006, 0x10002: Sparsification Threshold Registers, 14 bits, 2 bytes. The units are 500 ps, identical to the time data. (channel 0 = 0x10002, channel 1 = 0x10006, etc.

There is one such register per channel. Hits whose time data is larger than the threshold are kept, on a channel-per-channel basis.

Note: Bit 1 of the Mode register (at offset 0x101b4) must be cleared to properly access these registers. Failure to clear this bit will result in

inconsistent values being read, and no write access to the sparsification constants. After the constants are checked or modified, Bit 1 of the Mode register must be set again, for further data taking to take place.

2.6.23 Configuration ROM

0x0106F, … 0x00003: Configuration ROM bytes. The content of these locations is specified by the VME64 and VME64x standards of the VME International Trade Association. Of particular interest, is the module serial number, hex-encoded in the bytes located at offsets 0x1043, 0x1047, 0x104B, and 0x104F, and the ASCII test information string, stored starting at 0x1057.

2.6.24 Register Summary

Hex. Offset (D32)	(D08)	function	power-on/reset value	modifiable bits
00000	00003	Config. ROM (begin)	ROM check-sum	none
0119C	0119F	Config. ROM (end)	FF	none
10000	10002	Sparsification threshold 0	0000	0 through 13
1017C	1017E	Sparsification threshold 95	0000	0 through 13
10180	10183	Sparsification Control	00	0 and 1
10184	10187	Interrupt Enable	00	0
10188	10188	Interrupt Vector	00000000	0 through 31
1018c	1018f	Signal Source/destination	00	0 through 6
10190	10192	Unread events	0000	0 through 15
10194	10197	Advance Read pointer	Write-only register	0 and 1
10198	10198	Write Pointer	00000000	none-R/O register
1019C	1019C	Read Pointer	00000000	none-R/O register
101A0	101A3	Tester configuration	00	0 through 4
101A4	101A6	Full Scale Range	0FFF	0 through 11
101A8	101AB	LIFO depth	00	0 through 3
101AC	101AF	Fast Clear Window	0F	0 through 3
101B0	101B3	Common Start Timeout	0F	0 through 3
101B4	101B7	MTD mode	0E	0 through 5
7FFE8	7FFEB	F0 Address decode, byte 0	00	0 through 7
7FFE8	7FFEB	F0 Address decode, byte 1	00	1 through 7
7FFE8	7FFEB	F0 Address decode, byte 2	00	none
7FFE8	7FFEB	F0 Address decode, byte 3	00	none
7FFE8	7FFEB	User Bit Clear	00	0 through 2
7FFEC	7FFEF	User Bit Set	00	0 through 2
7FFF4	7FFF7	Bit Clear	00	4 and 7
7FFF8	7FFFB	Bit Set	00	4 and 7
7FFFC	7FFFF	CR/CSR base address	Determined by slot no.	3 through 7

2.7 DATA SPACE

Data memory in the VT960 TDC is organized in a 32K word circular buffer with sixteen 2K word pages. Data resulting from an event is stored in one of the sixteen 2048 word buffers. Each event buffer contains enough addresses to hold the maximum data resulting from a single event (1537 words = 96 ch * 16 hits/ch + header). An event is defined as the occurrence of a Common Start or Stop.

In the power-up or reset state, both the read and write pointers are at 0. Once an event occurs and is buffered the write buffer number is automatically incremented. The Write Pointer Buffer Register and the Read Pointer Buffer Register, at offsets hexadecimal 1098 and 109C respectively, are read-only registers that can be used to monitor the position of the read and write buffers. The Read Pointer Buffer Register is modified by writing to the Advance Read Buffer Register (hexadecimal 1094) while the Write Pointer Buffer Register is incremented by the MTD133 readout circuitry.

The Read Pointer and the Write Pointer values are internally used to determine the state of the unit memory. On power-up the unit is data

buffer is “empty”, with both pointers indicating the zero page address. While the buffer is empty it is not possible to advance the Read Pointer. The RAM is written to as a FIFO. Each time a data event is taken the data is written to the RAM and the write pointer is advanced. The unit will continue to buffer events until the write pointer is again equal to the read pointer. The unit is then in a “FULL” condition, and no more events will be taken until the read pointer is advanced, freeing up the data space for more events.

Any location within the 32 Kword data space is directly accessible via VME at any time, while logical addressing is enabled. Thus, during an acquisition, the Read Pointer will typically be read to determine at which address the ‘next event’ is located. After the readout of an event is completed, the Read Pointer Buffer Register should be incremented via a write to the Advance Read Buffer Register. Failure to do so would eventually result in the “FULL” condition and halt the acquisition.

It is permitted to read the data in any A32 mode, including A32 D64 block transfers, and D08, D16, and D32, block or single-cycle transfers, user or supervisor. Write data to the module (for the purpose of later testing the readout) is permitted in any non-block-transfer A32 mode. It is permitted to write to the header word address, but the value written will be ignored, and the header word will keep its previous value.

2.7.1 Header Word Format

The first word (address 0) of each buffer contains a header word for the event data which follows and is normally the first word readout during a block transfer. This header word contains the word count for that event as well as parity, buffer number, and geographic address of the module. The parity bit is high or low so as to make the total number of ones in the header word even.

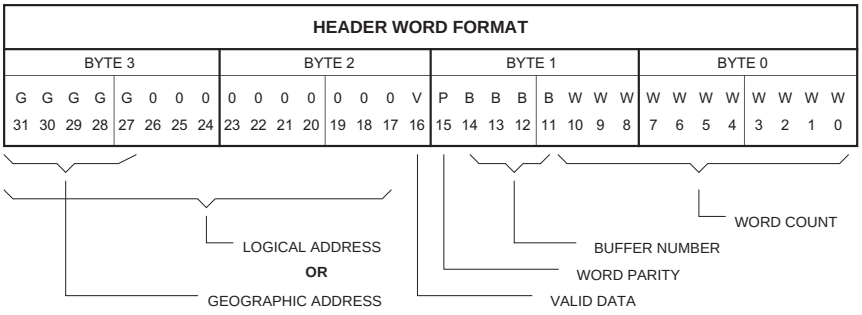

Figure 2-1 VT960 Header Word

2.7.2 Data Word Format

The VT960 hit data is read out as a 32-bit data word. The 16 least significant bits are the time data, the next bit is the hit phase (denoting leading or trailing edge), and the next 7 bits are the channel identification. The most significant byte contains the geographic address, parity, and the buffer number (modulo 4). The hit phase is zero for a rising edge hit, and one for a falling edge hit. Here again, the parity bit is high or low so as to make the total number of high bits in the word even.

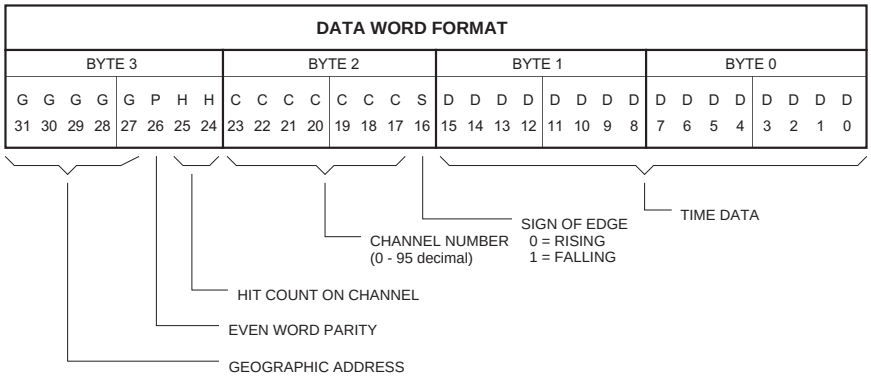

Figure 2-2 VT960 Data Word

2.8 READOUT

2.8.1 Single Read from Data Space

Reading of the data stored in the multi-event buffer can be done using random read cycles. However, first the correct number of words to read must be ascertained. Using the Read Buffer Pointer, select the desired event to read. The first location of this buffer, the header word, should be read to find out how many words are in the event. Bits <10:0> of the header word contain the word count for the event. This word count is the number of data words plus 1 for the header word itself. With this information the correct number of words for the event can be read by repeated reads.

2.8.2 Block Transfer Read from Data Space

Block transfers are the preferred way to read data from the VT960, and this is obtained by issuing the proper AM code in Data Space. A block transfer is typically set up by sending the start address and length in bytes of the transfer to a Block Transfer Manager that manages this transfer efficiently. The start address should be equal to the Logical Address of the module plus the buffer number times 8192(213). The length of the transfer (in bytes) is four times the event length as given by the header.

2.9 TESTER

An on-board tester is provided for easy verification of the unit's functionality. When a "1" is written to bit 0 of the User Bit Set register, an internal test cycle is generated if the internal tester is enabled. The Internal Tester Control Register sets the enable and the number of square wave pulses. The number of pulses generated can be 1, 2, 4, or 8, as programmed. The width of the pulses is 125 ns, 250 ns, 1000 ns or 2000 ns. By enabling both rising and falling edge detection (MTD Mode Register bit3 and bit2 = 1), and setting the tester to 8 pulses, it is possible to generate 16 measurements on all 96 channels.

Since the clock generating the test pulses is asynchronous to the acquisition clock, the tester pulse measurements will have a non-zero standard deviation, typically less than one count. This is, however, usually larger than that attainable using a high quality external source.

2.10 FAST CLEARS

A fast clear can be applied any time during the fast clear window. This will cause the event just recorded in the front end not to be buffered. The write pointer for the buffer will not be incremented. The buffering situation will be as though the cleared event never took place. This action requires 250 nsec from the falling edge of the fast clear pulse before the module is ready to accept another event. Fast clears can be applied either from the front panel input or via the VIPA J0; the choice depends on Control Signal Source Register bit 5. The application of a Fast Clear during the Fast Clear Window will terminate the Fast Clear Window.

2.11 Addressing the VT960

The VME module has distinct addressing modes for the its control and for its data readout.

The control of the modules, together with the readout of its status, proceeds through read and writes in the special A24 addressing space, which is characterized by an address modifier of hexadecimal 2F.

The A32 addressing space becomes available after writing to the Enable Logical Addressing Register; the A32 addressing space is characterized by address modifiers in the 00 to 0F hexadecimal range.

The data appears in the form of a “Random Access Memory” (RAM) memory bank; it can be re-read as many times as wished, and can be read out in any order. It is divided into 16 event buffers. The first word of each event buffer is reserved to a header, which indicates how many hits follow; this is limited to 2047 by the binary coding, and it will never exceed 1536=96*16 because each of the 96 channels can only record up to 16 hits.

The 15 higher bits of the address, A17 to A31, control the access to the module. The module only responds if the 15 upper bits match the upper 15 bits of the module Logical Address Register (Lower 4 bytes).

In the readout of several VT960 modules over the VME back plane, these 15 upper bits of the address are used to select the slot: for this reason, the Logical Address Registers of several modules in the same crate must all be different. Alternatively, if the Logical address of several modules are identical, only one of them should have the Logical addressing enabled, to avoid bus conflicts.

Bits A19-A23 of the Logical Address can be equal to bits A19-A23 of the Base Address Register if so desired. In such a case, the address modifier decides if the cycle is addressed to the data or CR/CSR space.

The contents of the Base Address register (offset hexadecimal 7FFFC) can be modified. It is initially set by the geographical address from the VME back plane. In the absence of a geographical address it is initially set by the dip-switch settings.

The example program which follows illustrates how a VME readout may be organized. The actual implementation (the VME_PORT structure and the VMERead and VMEWrite routines this program refers to) will vary from application to application:

```
#define BaseAddressMSB_off 0x7FF60
#define BaseAddressNMSB_off 0x7FF64
#define BitSetRegister_off 0x7FFF8
#define UnreadEvents_off 0x10190
#define AdvanceReadPointer_off 0x10194
#define ReadPointer_off 0x1019C
#define WritePointer_off 0x10198
long CrCsrBaseAddress;
unsigned long BaseAddress;
unsigned long BaseAddressMSB; // most significant byte of the base address
unsigned long BaseAddressNMSB;// next most significant byte
long ReadPointer;
long WritePointer;
long UnreadEventPattern;
long EvData[16][1537];
long EvDataSize[16];
float MeanTime_ns[16];
long NumberOfBytes;
long One=1;
long Enable_Module_Addressing 0x10;
long Header;
int j,k;
VME_PORT CrCsr;
VME_PORT A32;

CrCsrBaseAddress = SLOT_NUMBER * 0x800001;
VMEWrite(CrCsr, CrCsrBaseAddress+BitSetRegister_off, &Enable_Module_Addressing, 4);
VMERead(CrCsr, CrCsrBaseAddress+BaseAddressMSB_off, &BaseAddressMSB, 4);
VMERead(CrCsr, CrCsrBaseAddress+BaseAddressNMSB_off, &BaseAddressNMSB, 4);
VMERead(CrCsr, CrCsrBaseAddress+WritePointer_off, &WritePointer, 4);
VMERead(CrCsr, CrCsrBaseAddress+ReadPointer_off, &ReadPointer, 4);
VMERead(CrCsr, CrCsrBaseAddress+UnreadEvents_off, &UnreadEventPattern, 4);
BaseAddress = 0x1000000 * BaseAddressMSB + 0x10000 * BaseAddressNMSB
j=ReadPointer;
do {
   if ( UnreadEventPattern & (1<<j) ) {
     VMERead(A32, BaseAddress +j*0x2000, &Header, 4);
     EvDataSize[j]= Header & 0x7FF;
     VMERead(A32, BaseAddress +j*0x2000, EvData[j], 4*EvDataSize[j]);
     MeanTime_ns[j] = 0.0;
     for (k=1; k< EvDataSize[j]; k++) {
      MeanTime_ns[j] += ( EvData[j][k]/2.0 ) / (EvDataSize[j]-1);
     }
   }
   VMEWrite(CrCsr, CrCsrBaseAddress+Advance_Read_Pointer_off, &One, 4);
   j=(j+1)%16;
   } while (j!=WritePointer);
```

INSTALLATION

3.1 GENERAL

The LeCroy Model VT960 Time to Digital Converter is intended for use within a 9U VME crate with the VIPA/VITA backplane, and with the following voltage sources properly connected to the backplane: +5.0 V, -5.2 V, -2.0 V, +12.0 V, and -12.0 V.

With the power off and the Dip switch set to a unique value, the VT960 is inserted into one of the slots of the VME crate. The edge connector of the module should mate with the bus connector with modest pressure.

3.2 CABLES

The use of twisted-pair cables generally results in lower cabling costs and typically higher density and is usually adequate for digital signals. Thus, the VT960 was designed to accept 34 conductor ribbon cable. If using twisted-pairs, care should be taken to install high quality, shielded cables to minimize the effects of noise and crosstalk. Many of such cables can be purchased from LeCroy Corporation. In particular, there are two types of 34 conductor multiwire cables available, one for short connections using flat cable and the second for long connections using twisted and flat ribbon cable.

The polarity of the connector is uncommon, so care should be taken to avoid inserting the cable connector upside down.

The model numbers of such cables are as follows:

STC-DC /34/L - flat multiwire cable for short interconnections

LTC-DC /34-L or DC2 /34-L - twisted-pair multiwire cable for long interconnection

STP-DC /02-L - single twisted-pair cable, 3 ft maximum length

Note: The L is the length in feet that must be specified by the user.

All inputs are differential ECL and terminated by 112 ohms. The terminations are SIP components and may be easily replaced to accommodate other characteristic impedances.

4.1 GENERAL DESCRIPTION OF BUFFER ARCHITECTURE

The buffer memory on the VT960 is a 128K bytes SRAM structure with a word width of 32 bits. The memory is constructed out of four 32K x 8 SRAM chips. Access to the buffer memory from the module's front end (i.e. MTD readout) and from VME is completely interleaved, resulting in a synchronous dual-ported memory.

Both the readout of events from the MTD133s into the buffer and the readout of the buffer memory to VME via efficient block transfers (i.e. A32 D64) can proceed at a rate of up to 20 MHz. It is important to note that front end/VME access to the memory is synchronous and interleaved 2:1. This means that the maximum transfer rate to VME is half of the 40 MHz system timebase. Additionally, since the VME interfacing circuits are operating from the same clock as the memory control circuits, DTACK response times are also a function of the 40 MHz timebase.

Figure 4-1 shows a simplified block diagram of the VT960 paths. Event data is read out of the MTD133Bs through a pipeline at 20 MHz into the buffer memory. Sparsification of the data (if enabled) is performed as the data is pipelined into the buffer memory. Events are read out to VME through a two stage pipeline at speeds up to 20 MHz, depending on the Master. The VME readout pipeline stages are required to maintain the maximum transfer rate to the asynchronous VME. The addresses for front-end and VME access are multiplexed at a rate of 40 MHz.

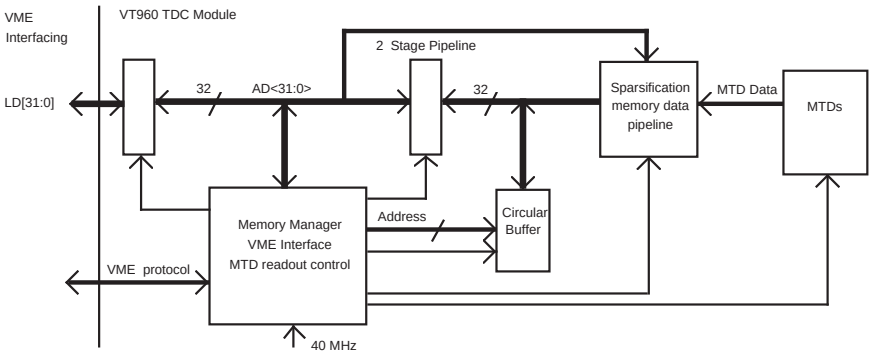

Figure 4-1 Simplified VT960 Interface/Buffer Block Diagram

4.1.1 Multi-Event Buffer Memory Organization

The 128 kbytes memory is logically partitioned into pages, each representing a separate event buffer. For the VT960, there are sixteen pages or buffers, each having 8 kbytes. Since there are a maximum of 1536 data words per event, each page of memory can hold one complete event.

4.1.2 Buffer Memory Pointers

The sixteen individual buffers are logically organized as a circular buffer structure. Two pointers are maintained into the circular buffer memory - MTD Write Pointer (WP) and VME Read Pointer (RP). The WP indicates to which buffer position data is being written to or will get written to. The RP, which is *not* strictly needed for perform a readout, keeps track of which buffer has been read. When the WP is equal to the RP, the circular buffer is either empty or full. To resolve this potential ambiguity, a table of

valid and unread data is kept. Whenever the write pointer is incremented following the successful acquisition of an event, the validity bit is set for the buffer the write pointer is leaving. Whenever the RP is incremented, via an “Advance Read Pointer” VME command, the validity/unread bit for the event it was pointing to is cleared. It is possible to verify at any time which elements of the circular buffer contain valid events not readout yet by reading the bit pattern of validity bits in the CR/CSR area at offset 0x10190.

4.2 ACQUISITION AND BUFFERING

4.2.1 Readout of MTDs

Readout of event time data from the MTDs begins either upon receipt of a common hit (in common stop mode) or at the end of the common start timeout period (in common start mode). During the time that the module is buffering event data, the signal Buffering In Progress (BIP) is asserted. Data words are written into the buffer currently pointed to by WP. If the module receives a Fast Clear during its programmed Fast Clear Window, the event just buffered (or being buffered) is discarded - WP is not incremented. The next event (if not fast-cleared itself) will simply over-write the same buffer.

4.2.2 Organization of Data in Events

As data words are written to memory, the address within the element of the circular buffer pointed to by WP is incremented (starting at address 4) until all data words have been read out of the MTDs. BIP is then deasserted and a 4-byte header word (which contains the address of the last data word) is built; this header word, constructed within the memory controller itself, appears at address 0. In this manner, all events, once completely buffered, consist of a header word in the first memory locations of a given buffer (page) followed by the data words for that event. Further, the header word contains the absolute memory location just beyond the last data word for that event, reflecting the complete word count for that event including the header word itself. If an event occurs which has no data words - a null event - a header word with a word count of one is still written and the MTD Write Pointer is advanced to the beginning of the next buffer.

4.3 VME Readout Schemes

In order to facilitate system integration and minimize dead time, an interrupt can be generated whenever the circular becomes full. A programmable four-byte interrupt vector is generated when an appropriate interrupt acknowledge cycle follows. The interrupt is cleared by the acknowledge cycle, but not the “full” condition. A readout must intervene to clear that condition.

If several units are to be read out in parallel, the default base address for the data (0) within the A32 address space should be changed. With the address space of each next module offset by 128K (0x20000), it is possible to build an uninterrupted address space containing all the data of all the modules. For example, with 3 modules, set the base addresses to 0, 0x20000, and 0x40000 for a continuous data space.

If several modules are in the same VME crate, and their A32 base addresses are identical, (for instance, if they are all left to the default value of 0), then it is imperative, in order to avoid VME bus contention, that only one of the modules has its A32 addressing enabled at any given time. This is controlled by setting bit 4 of either the Bit Set or Bit Clear registers in the CR/CSR area.

4.3.1 Readout of Data Space

All aligned VME readout modes are allowed: D08, D16, D32, in both User and Supervisor mode. The transfers can be done by single read-outs at the individual addresses, or via a block transfer. In addition, the special A32 D64 multiplexed block transfer mode is supported. Whatever the mode, the correspondence between the address (A[31:0]) and the data is the same.

- A[31:17] specify the module to be addressed, only the module with a matching base address will answer.
- A[16:13] specify which of the sixteen elements of the circular buffer will answer.
- A[12:2] specifies which 32-bit header or data word is being addressed; if A[12:2] is zero, the header word is retrieved. Otherwise, a data word is retrieved. This data word is valid if the address is less than the event length specified in the event header.
- A[1:0] specify the byte(s) to be read when D08 or D16 readout is being used. When D32 readout is used, A[1:0] should be zero, as unaligned transfers are not supported.

For comparison, the addressing structure of CR/CSR space is as follows:

- A[31:24] are not decoded.
- A[23:19] specifies which of the modules will respond based on its (geographic) base address.
- A[18:2] specifies which register is being accessed.
- A[1:0] specify the byte(s) to be read when D08 or D16 readout is being used. When D32 readout is used, A[1:0] should be zero, as unaligned transfers are not supported.

Re-reads of any particular buffer are possible without limitation.

It is also possible to write to any memory location with the exception of header word locations. Writes to these addresses are ignored. Be aware that writing to the memory does affect the position of the read pointer.

4.4 MULTI-RANGING ADC COMPATIBILITY

The VT960 is designed to provide the necessary interface and readout features to provide compatibility with single and multi-range Charge-to-Time converting front ends. The VT960 provides the time encoding function of the Charge-to-Time converter output pulse as well as all VME readout and interface functions. In general, Charge-to-Time converters such as the LeCroy MQT300 always generate an output pulse, even at pedestal. This guarantees that non-zero time data is recorded by the VT960 on every channel.

4.4.1 Configuration Considerations

When the VT960 is used in a multi-ranging ADC application (e.g. LeCroy MQT300), the TDC is programmed to operate in Common Start mode. The common start timeout is used to set the full scale rundown time of the front end charge-to-time conversion. Either the VT960 internal programmed Common Start Timeout or front panel TIM input may be used, as appropriate.

A 2-bit hit count field has been provided in the VT960 data word format. This field indicates (modulo 4) how many edges were registered in the MTD133B's LIFO. By programming the MTD133B LIFO depth to one (via offset 0x101a8 of the CR/CSR area), it is possible to readout only one word from each channel while also knowing the total number of hits that channel received. This feature provides a second level of data reduction from the multi-ranging MQT300.

Since it is critical to know how many edges were registered during the common start event, care must be taken in the application of the common start timeout. In Common Start Mode, the MTD133Bs are returned to acquisition mode after buffering is completed. Once the TDC is in acquisition, the MTD133B's internal hit counter will be incremented on every transition on its channel inputs independent of the Common input. This means that edges arriving before the Common Start will increment the hit count and potentially result in misinterpretation of the range information. It is therefore strongly recommended that the front panel TIM input is used to control the common start event. The front panel TIM input is both edge and level sensitive; buffering of the event begins on the rising edge of the TIM input and the MTD133B's LIFO and hit counter are held in reset while the front panel input is asserted. This allows the user to control when the TDC will begin registering hits after the current event has been buffered. The MTD133B hit counter and LIFO are always cleared at the end of buffering so edges received during buffering will have no effect.

4.4.2 Sparse Data Readout

In a mode similar to the LeCroy FASTBUS ADC Model 1881M, a sparse data readout scheme can be used to prevent unwanted data from being buffered. The VT960 allows the user to program 96 constants (14 bits each), one per channel, which can be compared to the measurement values. Only data exceeding these individual thresholds is buffered, reducing both dead time and the quantity of data that must be transferred over VME to the host computer.

In the so-called simple sparsification mode, the sparsification threshold is applied to all hits.

In the complex sparsification mode, the sparsification threshold is only applied to events which correspond to the low range of the multi-ranging MQT300. These events are identified by four transitions, the last transition containing the charge information for the low range. The MTD133B LIFO depth must be programmed to one. Such settings provide maximum data reduction of the MQT300 data, including a charge threshold which can be high, without any loss of meaningful data.

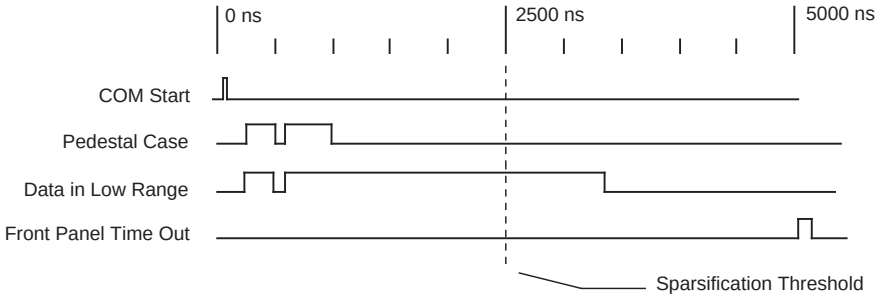

Figure 4-2 Example: MQT300 Low Range Data