VME1X2A / LT1
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Dear Valued Customer:

Thank you for your purchase of an MVME162 or MVME172 VME single board computer. The IndustryPack interface device used on these products has some deviations (commonly called errata) from the original design specification of which you should be aware. This letter will document the errata and the specific versions of the MVME162 and MVME172 series which are affected.

Errata 1

Errata 1 exists in all MVME162-4*xx* and MVME162-5*xx* series which have a board artwork revision of “D” or lower. The board artwork number is etched in copper and can be located on the non-component side of the printed circuit board. The following artwork revisions are affected:

84-W8960B01A
84-W8960B01B
84-W8960B01C
84-W8960B01D

Errata Definition

Bits 0 and 1 of Control Register 2 for each IndustryPack DMA channel defines a snoop control function. According to the Programmer's Reference Guide, these bits define the state of the snoop signals for each DMA channel while that DMA channel is local bus master. Due to a flaw in the IP2 ASIC, the hardware does not always work this way. When either or both snoop control bits are set to values other than 0, they may return to 0 during the IndustryPack DMA cycle if the address is updated during that bus tenure.

The revision “E” artwork does not have the local bus snoop signals connected to the IP2 ASIC. The function has been replaced by two jumpers and an interface circuit so that the state of the jumpers can define the state of the snoop control

signals during IP DMA cycles. For customers who have boards that are not built from the revision “E” artwork, the following two workarounds are suggested:

Workaround #1

Do not program the snoop control bits in Control Register 2 to values other than 00. That is, the control bits for IP DMA channel A, B, C, and D must all be set to zero. Since this has certain performance implications, the second workaround is suggested.

Workaround #2

This solution does not put restrictions on the setting of the snoop control bits but does restrict the starting DMA address and the byte count. The starting local bus DMA address must be a cache line boundary. Therefore the starting address must be divisible by 16 with a remainder of zero. The byte count must also be divisible by 16 with a remainder of zero. This will guarantee that the DMA process will start and end on a cache line boundary. For these boundary conditions, the snoop control logic in the IP2 ASIC will function correctly.

Errata 2

Errata 2 exists in the following MVME162 and MVME172 series products:

MVME162-4*xx* Series
MVME162-5*xx* Series
MVME162-7*xx* Series
MVME162-8*xx* Series
MVME172-2*xx* Series
MVME172-3*xx* Series
MVME172-4*xx* Series
MVME172-5*xx* Series

Errata Definition

DMA command chaining feature does function correctly for certain configurations. There are two failure modes relating to the command chaining feature:

Failure Mode # 1

The system crashes when the IP bus is strapped for 32 MHz and command chaining is enabled.

Workaround

The workaround for this problem requires that the MVME162 or MVME172 uses a DRAM memory module which allows a zero wait state cache burst for the second, third, and fourth beat. The only MVME162 and MVME172 versions that meet this criteria are ones that use Error Checking and Correction (ECC) memory modules. The following MVME162 and MVME172 versions support ECC memory:

MVME162-23*x*	MVME172-32*x*
MVME162-24*x*	MVME172-33*x*
MVME172-23*x*	MVME162-34*x*
MVME172-24*x*	MVME162-35*x*
MVME162-25*x*	MVME172-34*x*
MVME162-26*x*	MVME172-35*x*
MVME172-25*x*	MVME162-74*x*
MVME172-26*x*	MVME162-76*x*
MVME162-32*x*	MVME162-83*x*
MVME162-33*x*	MVME162-85*x*

There is one MVME162-5*xx* series parity combination that meets this work-around criteria: that is the MVME162-53*x* series with a 25 MHz processor and 16MB of non-parity memory. This is not an ideal solution since it requires the IndustryPack bus to operate at 25 MHz.

Failure Mode #2

Command chaining is not functional when the address-based DMA (aDMA) mode is required.

Workaround

There is no workaround for this problem. The command chaining mode is functional for the standard or compelled DMA (sDMA) mode of operation only.

We hope this does not cause you any inconvenience. If you have additional questions, please contact your Motorola Computer Group Sales representative.