

MVME Series

**IPMC712/761 I/O Module
Installation and Use**

VIPMCA/IH2

April 2005 Edition

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Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.



To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution



Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.

CE Notice (European Community)

Motorola products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 "Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment"; this product tested to Equipment Class B

EN50082-1:1997 "Electromagnetic Compatibility—Generic Immunity Standard, Part 1. Residential, Commercial and Light Industry"

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Motorola, Inc.
Embedded Communications Computing
2900 South Diablo Way
Tempe, Arizona 85282

Contents

About This Book	xiii
Summary of Changes	xiii
Comments and Suggestions	xiv
Terminology	xiv
Conventions Used in This Manual	xv
1 Product Features	1
General Functionality	1
IPMC Mode	1
Design Features	1
PCI Bus Interface	1
Configurable Switches	2
PCI-to-ISA Bridge (PIB)	2
SCSI	2
ISA Local Resource Bus	8
PCI-to-ISA Bridge (PIB)	8
Super I/O	8
ESCC	8
CIO	8
Static ROM (SROM)	8
Input/Output Modes	9
LEDs	9
PCI Signaling Voltage Level	9
RS232 Interface	9
2 Installing the IPMC Module	11
Packaging	11
Configuring the IPMC Modules	11
Installing IPMC Modules on Host Board	11
Before You Install or Remove a Board	12
Observe ESD Precautions	12
Watch for Bent Pins or Other Damage	13
Use Caution When Installing or Removing Boards	13
Preserve EMI Compliance	13
Recognize Different Injector/Ejector Lever Types	14
Verify Slot Usage	14

3	Programming	15
	Programming Details	15
	PCI Local Bus	15
	The PCI-to-ISA Bridge (PIB)	15
	The SCSI Controller	15
	IDSEL Address Assignments for PCI Local Bus	17
	PCI Arbitration Assignments on Host Boards	18
	MVME5100	18
	MVME5500	18
	MVME6100	18
	Interrupt Assignments	19
	MVME5100 IPMC Module Interrupt Assignments	19
	MVME5500 IPMC Module Interrupt Assignments	20
	MVME6100 IPMC Module Interrupt Assignments	20
	ISA Local Resource Bus	21
	PCI-to-ISA Bridge (PIB)	21
	Super I/O	21
	ISA DMA Channels	21
	Z8536 CIO Port Pins	22
	ISA DMA Connections/Assignments	22
	Interrupt Routing to PIB	23
	Vital Product Data (VPD)	24
4	Connector Pin Assignments	25
	IPMC712 Connector	25
	IPMC761 Connector	26
	PCI Interface and I/O Connectors	27
A	Specifications	33
	General Specifications	33
	Power Requirements	34
B	Related Documentation	35
	Motorola Documents	35
	Manufacturers' Documents	36
	Related Specifications	37

List of Figures

Figure 1-1. IPMC761 with Default Switch Setting	3
Figure 1-2. IPMC761 Functional Block Diagram	4
Figure 1-3. IPMC712 with Default Switch Settings	5
Figure 1-4. IPMC712 Functional Block Layout	6
Figure 1-5. IPMC712 Serial Port 4 Clock Configuration	7
Figure 2-1. IPMC Installation	12
Figure 2-2. Injector/Ejector Lever Types	14
Figure 3-1. GPIO Switch Settings (S1)	16
Figure 3-2. IDSEL Switch Settings (S2)	16

List of Tables

Table 3-1. GPIO Pin Assignments	16
Table 3-2. IDSEL Mapping for PCI Devices	17
Table 3-3. On-Board PCI Device Identification	17
Table 3-4. PCI Arbitration Assignments	18
Table 3-5. Hawk MPIC Interrupt Assignments	19
Table 3-6. MVME5500 Interrupts	20
Table 3-7. MVME6100 Interrupts	20
Table 3-8. Strap Pins Configuration	21
Table 3-9. PIB DMA Channel Assignments	21
Table 3-10. Z8536 CIO Port Pins Assignment	22
Table 3-11. DMA Connection/Assignments	22
Table 3-12. PIB Interrupt Assignments	23
Table 4-1. IPMC712 Connector	25
Table 4-2. IPMC761 Connector	26
Table 4-3. PCI Connector Pin Assignments (P11)	27
Table 4-4. PCI Connector Pin Assignments (P12)	28
Table 4-5. PCI Connector Pin Assignments (P13)	29
Table 4-6. PCI Connector Pin Assignments (P14)	30
Table A-1. IPMC Specifications	33
Table A-2. Power Consumption	34
Table B-1. Motorola Documents	35
Table B-2. Manufacturers' Documents	36
Table B-3. Related Specifications	37

About This Book

The *IPMC712/761 I/O Module Installation and Use* manual provides the information you will need to install, use, and program your IPMC712 or IPMC761 module. The IPMC712 and IPMC761 are optional I/O modules installed on the MVME5100, MVME5500, and MVME6100 Single Board Computers (SBCs). Their design utilizes the PowerPlus II architecture.

The IPMC712 is a variation of the IPMC761. The primary differences between the two modules are in the physical interfaces of the Ethernet port and serial ports 3 and 4. These differences along with others are discussed in the following chapters of this manual.

As of the printing date of this manual, these I/O module models are available:

Model Number	Product Description and I/O Features
IPMC712-002	Multifunction rear I/O PMC module; Ultra-Wide SCSI, one parallel port, three asynchronous and one synchronous/asynchronous serial port
IPMC761-002	Multifunction rear I/O PMC module; Ultra-Wide SCSI, one parallel port, two asynchronous and two synchronous/asynchronous serial ports

This manual is organized as follows:

- Chapter 1, *Product Features*
- Chapter 2, *Installing the IPMC Module*
- Chapter 3, *Programming*
- Chapter 4, *Connector Pin Assignments*
- Appendix A, *Specifications*
- Appendix B, *Related Documentation*

Summary of Changes

This is the second edition of the *IPMC712/761 I/O Module Installation and Use* manual. The following table describes the changes in this edition.

Date	Changes
April 2005	Added support information for the MVME6100, MVME5500 Added information for the new S2 dip switch for IDSEL selection Updated component layout graphics of both modules

Comments and Suggestions

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In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Terminology

A character precedes a data or address parameter to specify the numeric format, as follows (if not specified, the format is hexadecimal. An asterisk (*) following a signal name for signals that are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following a signal name for signals that are edge significant denotes that the # actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

Data and address sizes are defined as follows:

0x Specifies a hexadecimal number
% Specifies a binary number
& Specifies a decimal number

Byte	8 bits, numbered 0 through 7, with bit 0 being the least significant.
Half word	16 bits, numbered 0 through 15, with bit 0 being the least significant.
Word	32 bits, numbered 0 through 31, with bit 0 being the least significant.
Double word	64 bits, numbered 0 through 63, with bit 0 being the least significant.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<Enter>, <Return> or <CR>

represents the carriage return or Enter key.

Ctrl

represents the Control key. Execute control characters by pressing the **Ctrl** key and the letter simultaneously, for example, **Ctrl-d**.

The IPMC712 and IPMC761 are optional modules that provide backward compatibility with earlier Motorola products using the MVME761 or MVME712M rear transition modules.

General Functionality

Both models are designed around a PMC form factor and both modules incorporate a PCI-to-ISA bridge, Ultra-wide SCSI adapter, and Super I/O functionality. Both modules are single wide, standard length, standard height PMC boards. They attach to the host board PCI bus via the PMC P11, P12, P13, P14, and P15 connectors.

- One single-ended ultra-wide SCSI port
- One parallel port
- Four serial ports (2 or 3 asynchronous and 1 or 2 synchronous/asynchronous, depending on the module)

With this PMC card configuration, the memory mezzanine, one PMC slot, and the PMCSpan are still available, providing support for additional product customization.

IPMC Mode

In IPMC mode, the MVME 6100, MVME5500, and MVME5100 support legacy MVME761 or MVME712M rear transition modules (with limited PMC I/O) when an IPMC712 or IPMC761 module is installed in PMC slot 1. In this configuration, PMC slot 2 contains some signals that are reserved for extended SCSI.

Design Features

The following sections describe the basic features that are incorporated in the design of both IPMC modules.

PCI Bus Interface

Both modules contain four EIA-E700 AAAB connectors, which provide a 32-bit PCI interface to an IEEE P1386.1 PMC-compliant host board such as the MVME6100, MVME5500, or MVME5100.

Connectors P11-P13 on each module provide the 32-bit PCI interface while P14 provides an I/O path from the module to the host board.

Signals routed to P14 include: narrow SCSI, parallel port, COM1 and COM2 synchronous serial ports, COM3 and COM4 synchronous serial ports, power, and P2 mux signals. The remaining SCSI data lines are routed to P15.

The on-board PCI devices on each module are as follows:

- Winbond PCI-to-ISA Bridge (PIB)
- LSI SCSI device (SYM53C895A)

Configurable Switches

S1 Switch

A 1x4 switch (S1) is provided on each module for configuring GPIO pins 2 and 3. The factory default setting is for Ultra-Speed and Ultra-Wide SCSI. Refer to [Table 3-1 on page 16](#) for the GPIO pin assignments and to [Figure 3-1 on page 16](#) for the default switch settings.

S2 Switch

There is a 1x2 switch (S2) on each module that is in line with the PCI-to-ISA bridge for selecting either AD[11] IDSEL or IDSELB for connection to the Winbond chip, depending on the IPMC module you are using.

Note The S2 is not dependent on either IPMC module. It is dependent on either the MVME5100, MVME550, or MVME6100 host board. The IPMC modules are shipped configured for the MVME5100/MVME550.

Details on IDSEL mapping and PCI arbitration assignments for these SBCs can be found in [Chapter 3, Programming](#). An illustration showing the S2 switch settings can be found in [Figure 3-2 on page 16](#).

PCI-to-ISA Bridge (PIB)

The PIB provides the bridging functions between PCI local bus and the ISA local resource bus. The following are a few of the features of the PIB.

SCSI

The SCSI controller is an LSI Logic SYM53C895A device. The SCSI clock frequency is 40 MHz. The SCSI controller features:

- 32-bit PCI Interface with 64-bit addressing
- 8KB internal SCRIPTS RAM
- Improved PCI caching design (improves PCI bus efficiency)

The SCSI device maintains backward compatibility with the MVME761 rear transition module and P2 adapter card. It is also Ultra-wide capable and has a performance of 40MB/s synchronous transfer rate across a 16-bit bus.

Note SCSI signals leading to connector P15 go through zero ohm resistors (R92-R100) before terminating at P15. When the host board's PMC slot 2 is populated, and there is an IPMC module in slot 1, there exists a possibility for contention on these signals. This can be avoided by not installing the zero ohm jumpers.

Figure 1-1. IPMC761 with Default Switch Setting

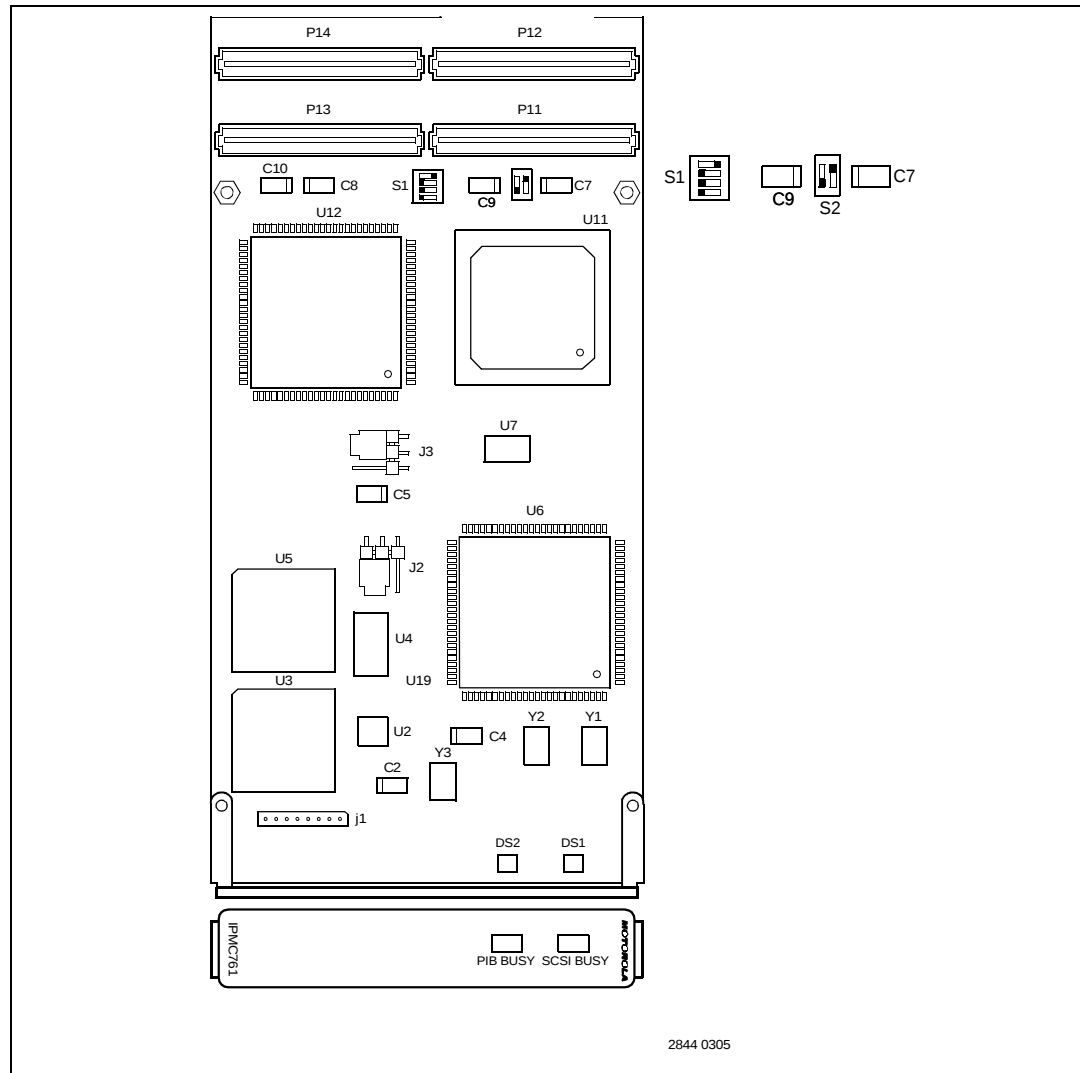


Figure 1-2. IPMC761 Functional Block Diagram

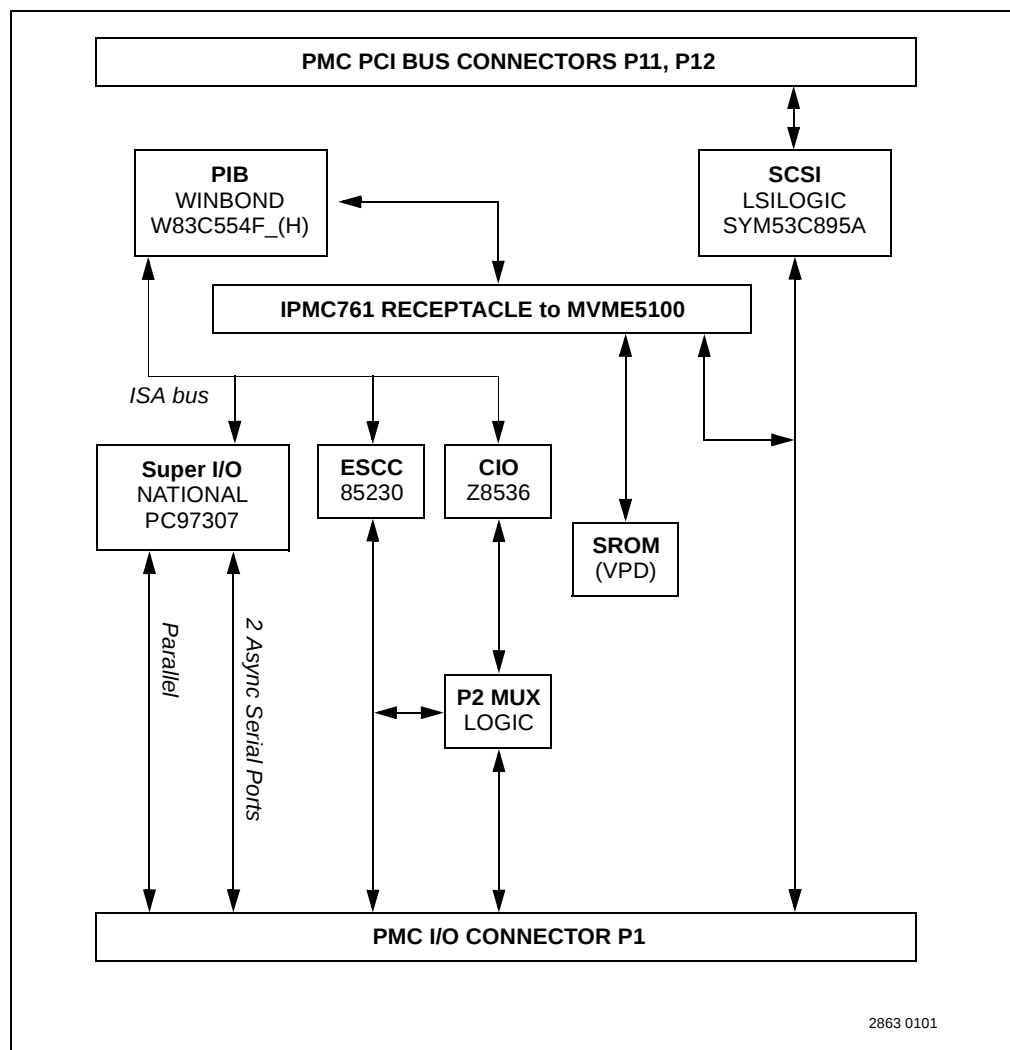


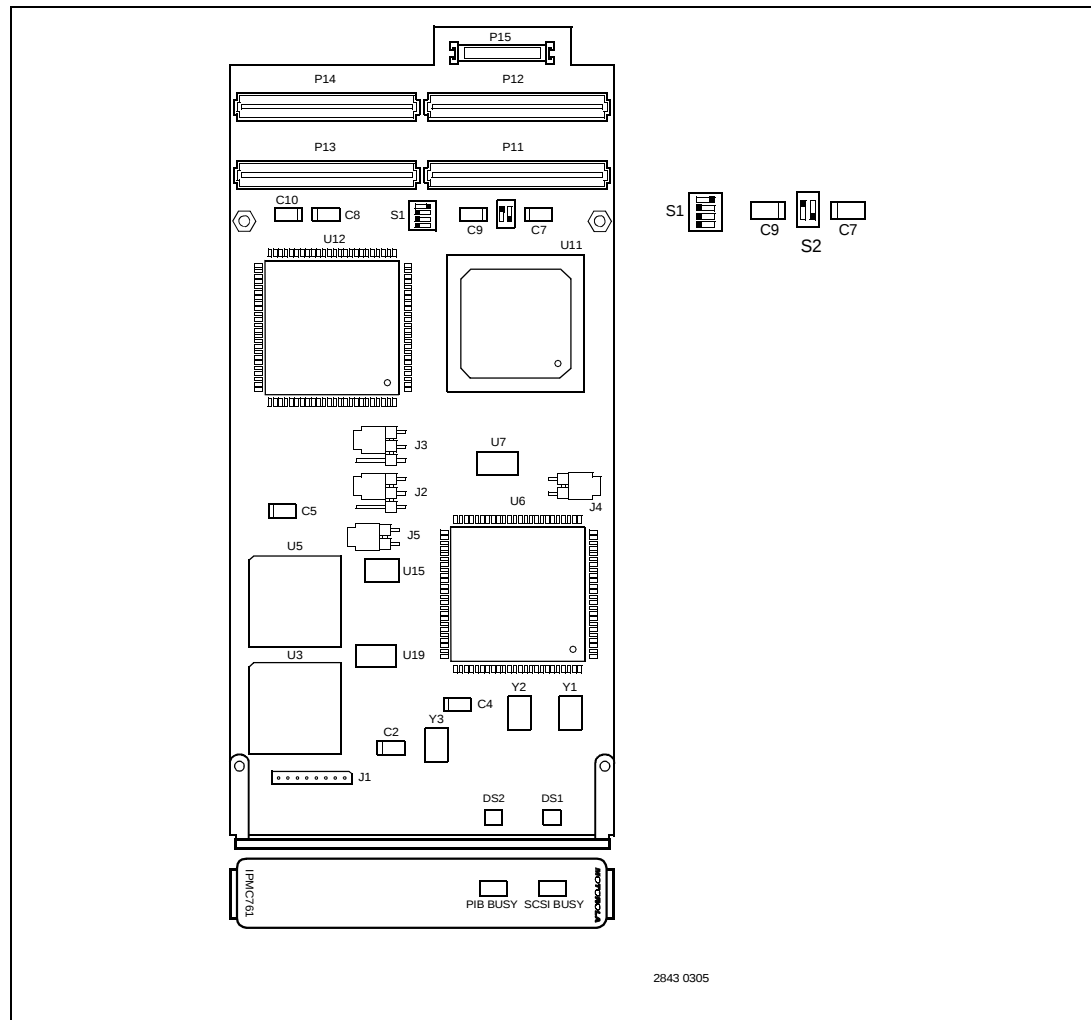
Figure 1-3. IPMC712 with Default Switch Settings

Figure 1-4. IPMC712 Functional Block Layout

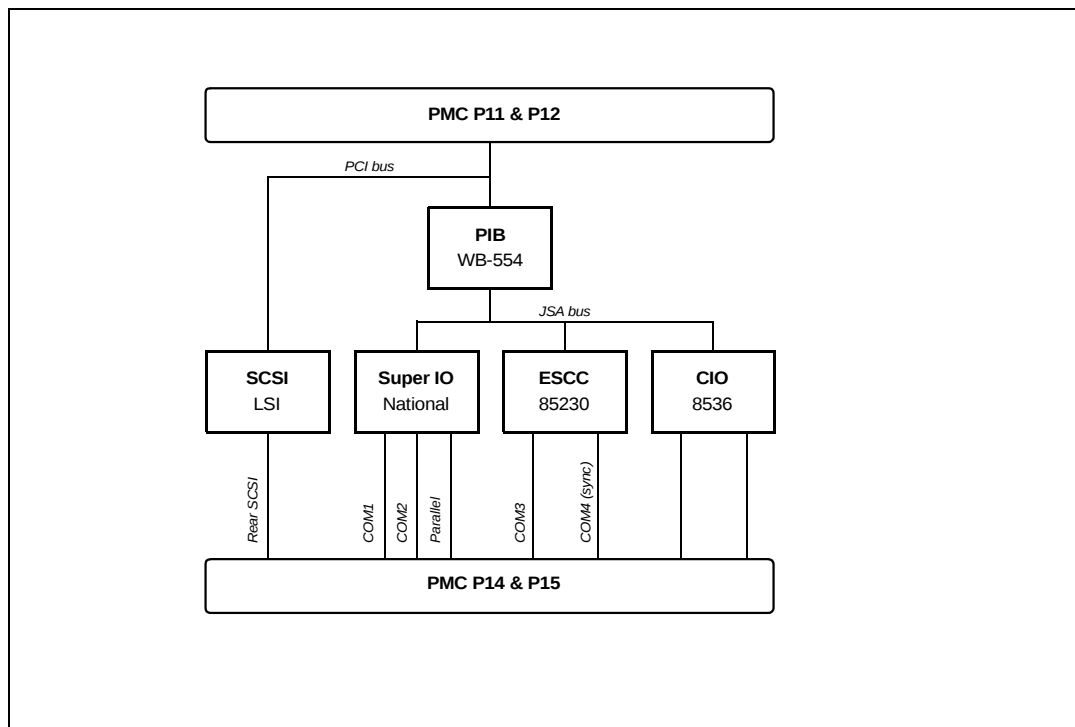
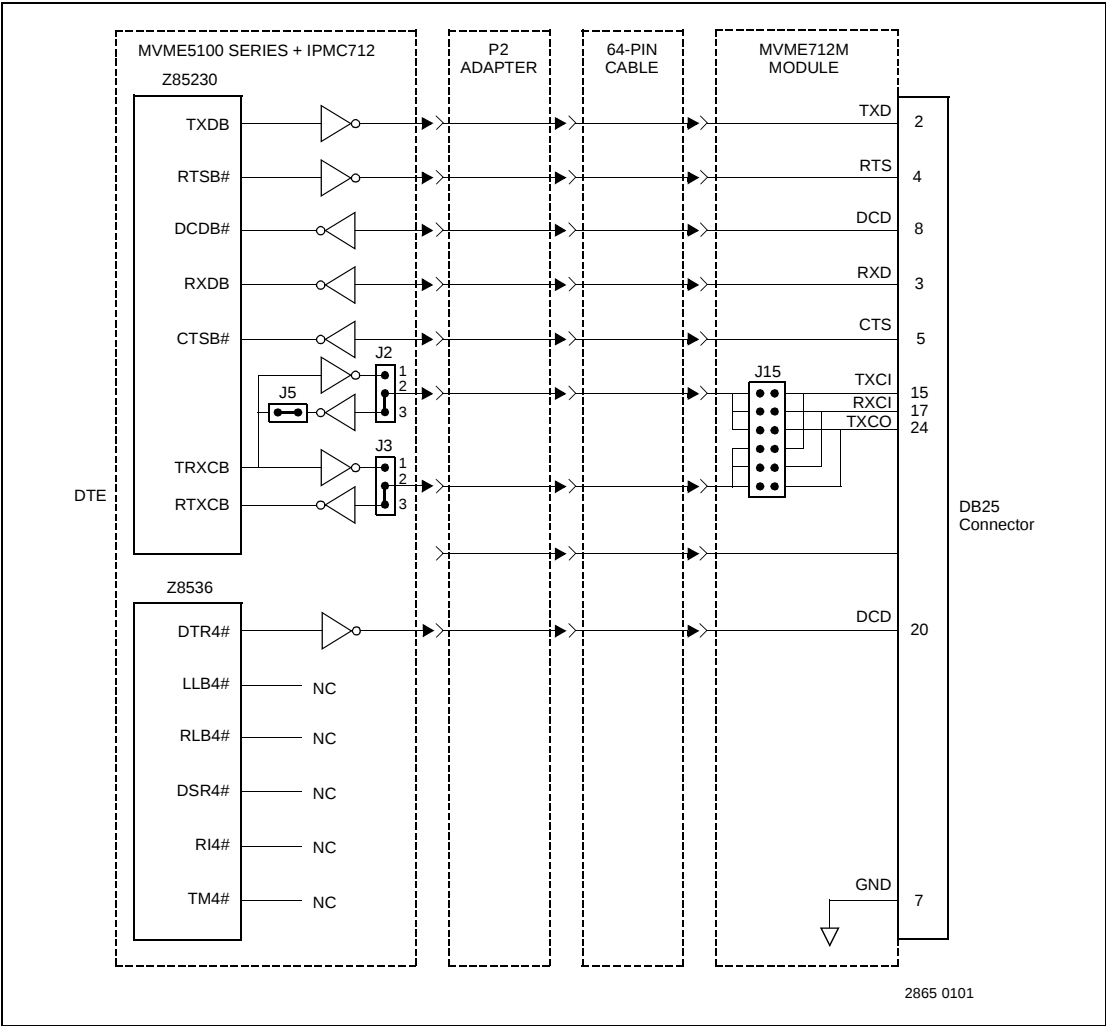


Figure 1-5. IPMC712 Serial Port 4 Clock Configuration



ISA Local Resource Bus

PCI-to-ISA Bridge (PIB)

The PIB (W83C554F) contains the ISA Bridge I/O Registers necessary for various functions. These registers are also accessible from the PCI bus.

Super I/O

The Super I/O device (PC97307) provides the following functions on the IPMC:

- Two synchronous serial ports (COM1 and COM2)
- Parallel printer port

ESCC

Two DTE synchronous/asynchronous serial ports are provided by the ESCC device (Z85230). Since the Z85230 device does not have all modem control lines, a Z8536 CIO device (described below) is used to provide the missing lines.

A PAL device is used to perform decode for the Z85230 and the Z8536 for register accesses and pseudo interrupt acknowledge cycles in the ISA I/O space. DMA supports for the Z85230 is provided by the PIB.

The clock input to the Z85230 PCLK pin is a 10 MHz clock. The Z85230 supplies an interrupt vector during a pseudo interrupt acknowledge cycle. The vector is modified based upon the interrupt source within the device.

All modem control lines from the ESCC are multiplexed/demultiplexed through connector P2 by the P2MX function due to pin limitation of the connector.

CIO

The CIO device (Z8536) is used to provide the modem control lines not provided by the Z85230 ESCC. In addition, the device has three independent 16-bit counters/timers. The clock input to the Z8536 PCLK pin is a 5 MHz clock.

Static ROM (SRAM)

Both modules contains one +3.3V, 256 x 8 serial EEPROM device (AT24C02) onboard. This device provides for Vital Product Data (VPD) storage of the module hardware configuration. The serial EEPROM is accessed through the I²C port in the Hawk ASIC. Its I²C address is \$A4.

Input/Output Modes

Both modules are designed to be plugged into PMC slot 1 of the MVME6100, MVME5500, or MVME5100. As stated earlier, these SBCs have two P2 I/O modes (IPMC and PMC) that are user configurable by setting four jumpers on the board itself.

The jumpers route the on-board Ethernet port 2 to row C of connector P2. When used, both modules are backwards compatible with the MVME761 rear transition module and P2 adapter card (excluding PMC I/O routing) used on the MVME2600/2700.

LEDs

Both modules use two LEDs to provide PMC status.

- The module's green SCSI LED is lit when the SCSI device is Master
- The module's green PIB LED is lit when the PCI bus grant to the PIB is asserted

PCI Signaling Voltage Level

Both modules will operate with only +5V signaling levels.

RS232 Interface

On the IPMC712 module, the four serial ports are used to communicate at RS232 voltage levels (P14). The first three ports are fixed asynchronous ports, while the remaining port can be configured as either a synchronous or an asynchronous port.

For additional handshaking signals, the IPMC712 module has the following features:

- Port 1 has RTS and CTS
- Ports 2, 3, and 4 have RTS, CTS, DTR, DCD
- Port 4 has configurable serial clock signals RTxC and TRxC

Jumpers J2, J3 and J5 determine the sources for these two signals, refer to [Figure 1-5 on page 7](#).

This chapter discusses the configuration and installation of IPMC modules on an MVME6100, MVME5500, or MVME5100 SBC.

For additional information pertaining to the MVME5100 SBC, refer to the information contained in the *MVME5100 Single Board Computer Installation and Use* manual before proceeding with these instructions contained in this chapter.

Packaging

As a precautionary measure, IPMC modules are sealed in an anti-static package to protect them from static discharge. Observe standard handling practices of static sensitive equipment.

Configuring the IPMC Modules

There are two user configurable switches on the IPMC712 and IPMC761 I/O modules. Switches S1 and S2 are described in [Chapter 3, Programming](#).

Installing IPMC Modules on Host Board

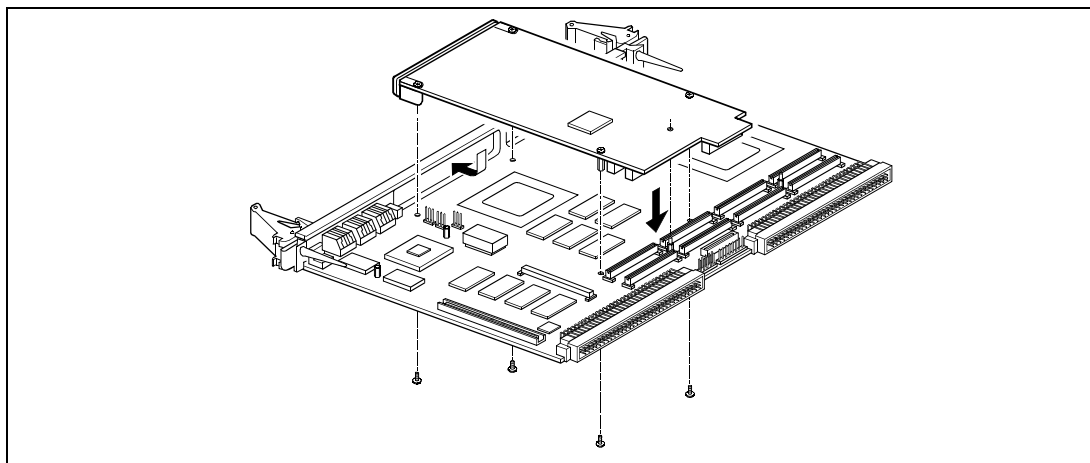
Both the IPMC712 and the IPMC761 modules are installed on PMC slot 1 of the host board. As a general reminder, IPMC modules must be installed on the host board prior to installing it into the VME chassis.

To install an IPMC module, refer to the following figure and proceed as follows:

1. Inspect the host board and the IPMC module for evidence of any damage to the PCB itself or for evidence of any damage on the mating connectors.
2. If the host board is installed in a VMEbus card slot, carefully remove it and place it with connectors P1 and P2 facing you.

3. Remove the filler plate from the host board's front panel. Position the IPMC module over the center area of the slot 1 connectors as follows:

Figure 2-1. IPMC Installation



4. Line up the IPMC module's front panel into the IPMC filler cutout slot on the host board's front panel.
5. Align connectors P11, P12, P13, P14, and P15 on the IPMC module with the mating connectors on the host board and press firmly into place.
6. Insert the appropriate number of Phillips screws (typically 4) from the bottom of the host board into the standoffs on the IPMC module and tighten the screws.

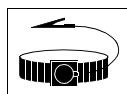
The host board is now ready to be installed into a VME chassis.

Before You Install or Remove a Board

Boards may be damaged if improperly installed or handled. Please read and follow the guidelines in this section to protect your equipment.

Observe ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Watch for Bent Pins or Other Damage



Bent pins or loose components can cause damage to the board, the backplane, or other system components. Carefully inspect your board and the backplane for both pin and component integrity before installation.

ECC and our suppliers take significant steps to ensure there are no bent pins on the backplane or connector damage to the boards prior to leaving our factory. Bent pins caused by improper installation or by boards with damaged connectors could void the warranty for the backplane or boards.

If a system contains one or more crushed pins, power off the system and contact your local sales representative to schedule delivery of a replacement chassis assembly.

Use Caution When Installing or Removing Boards

When first installing boards in an empty chassis, we recommend that you start at the left of the card cage and work to the right when cards are vertically aligned; in horizontally aligned cages, work from bottom to top.

When inserting or removing a board in a slot adjacent to other boards, use extra caution to avoid damage to the pins and components located on the primary or secondary sides of the boards.

Preserve EMI Compliance

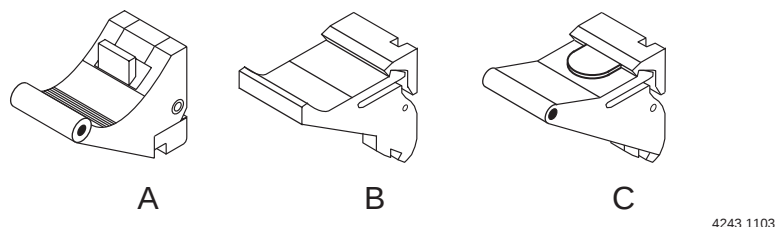


To preserve compliance with applicable standards and regulations for electromagnetic interference (EMI), during operation all front and rear openings on the chassis or board faceplates must be filled with an appropriate card or covered with a filler panel. If the EMI barrier is open, devices may cause or be susceptible to excessive interference.

Recognize Different Injector/Ejector Lever Types

The modules you install may have different ejector handles and latching mechanisms. The following illustration shows the typical board ejector handles used with ECC payload cards: (A) Elma Latching, (B) Rittal Type II, (C) Rittal Type IV. All handles are compliant with the CompactPCI specification and are designed to meet the IEEE1101.10 standards.

Figure 2-2. Injector/Ejector Lever Types



Each lever type has a latching mechanism to prevent the lever from being opened accidentally. You must press the lever release before you can open the lever. *Never force the lever.* If the lever does not open easily, you may not have pressed firmly enough on the release. If the lever does not close easily, the board may not be properly seated in the chassis.

To open a lever, press the release and move the lever outward away from the faceplate.

To close a lever, move the lever inward toward the faceplate until the latch engages.

Verify Slot Usage



Prevent possible damage to module components by verifying the proper slot usage for your configuration.

Programing Details

The overall design of the IPMC712 and IPMC761 is based on the PowerPlus II architecture. The programming characteristics for both modules conforms to the PowerPlusII Programming Specification.

Note The PowerPlus II Programming Specification covers a large variety of programming configurations, many of which are not applicable to either module. This chapter describes those aspects of the specification that are unique to both modules.

PCI Local Bus

The on-board PCI devices on the IPMC712 and the IPMC761 are the PCI-to-ISA Bridge and the SCSI controller.

The PCI-to-ISA Bridge (PIB)

The PCI-to-ISA Bridge (PIB) provides the bridging functions between PCI local bus and the ISA local resource bus. Other features contained in the PIB are:

- 8259 Interrupt Controller
- ISA DMA support
- Timers and counters

The SCSI Controller

The SCSI controller's clock speed is 40 MHz. The presence of the SCSI device can be positively determined by reading the Device ID PCI Configuration Register 0x02 - 0x03. The Device ID is 0x0012.

The General Purpose I/O (GPIO) pin assignments for the SCSI Controller are shown in the table below. A 1x4 switch (S1) is provided to configure GPIO pins 2 and 3. The factory default setting shall be for Ultra-Speed and Ultra-Wide SCSI.

Table 3-1. GPIO Pin Assignments

GPIO Pin	Direction	Level	Usage
GPIO1_MASTER_1	output	1	SCSI LED; SCSI is not MASTER.
		0	SCSI is MASTER.
GPIO2	input	1	SCSI speed; selectable by switch S1. S1 pin 1 in off position selects Ultra-Speed.
		0	S1 pin 1 in ON position selects Ultra-FAST (default).
GPIO3	input	1	SCSI bus width; selectable by switch S1. S1 pin 2 in off position selects Wide-SCSI.
		0	S1 pin 2 in ON position selects Narrow-SCSI.
0, 4, 5, 6, 7, 8	-	-	Not used.

Figure 3-1. GPIO Switch Settings (S1)

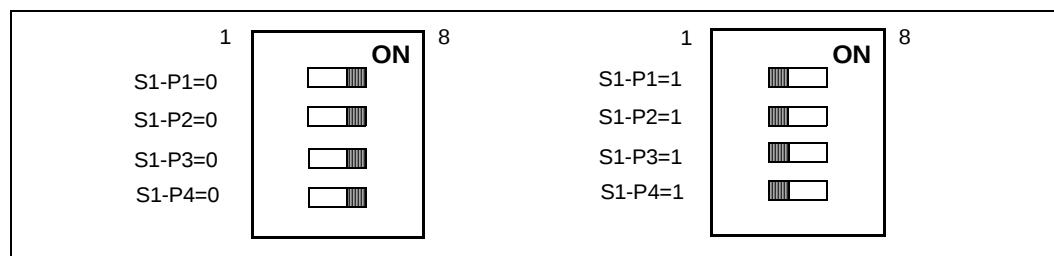
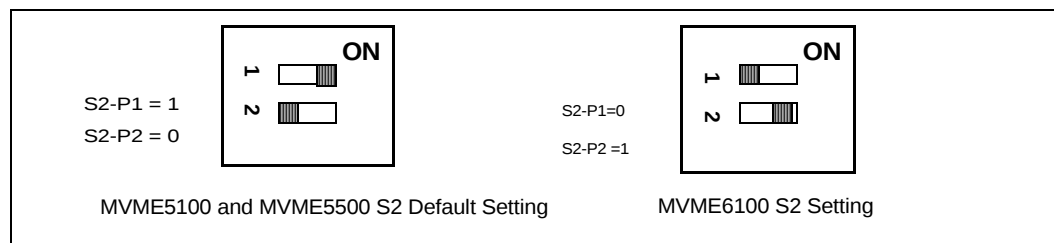


Figure 3-2. IDSEL Switch Settings (S2)



IDSEL Address Assignments for PCI Local Bus

Legacy IDSEL assignment for the PCI-to-ISA Bridge (PIB) is maintained to ensure software compatibility between MVME2700 and MVME5100 while functioning in IPMC mode. The IPMC712 and IPMC761 boards have a switch (S2) that allows you to configure the board for the correct IDSEL connection to the Winbond chip, as described below:

- Connection to IDSEL, AD[11] on PMC connector pin P11-48 is selected when using the IPMC 712/761 with ECC VME boards MVME5100 and MVME5500 (boards released *prior* to the MVME6100)
- Connection to IDSELB, AD[16] on PMC connector pin P12-34 is selected when using the IPMC712/761 with the MVME6100 board and all boards released *subsequently*

The IDSEL assignments for both modules are shown below:

Table 3-2. IDSEL Mapping for PCI Devices

Device Number Field	PCI Address Line	IDSEL Connection
0b0_1011	AD11	PCI/ISA Bridge
0b1_0000	AD16	PMC Slot 1 SCSI Device

The following table shows the Vendor ID, the Device ID, and Revision ID for each of the planar PCI devices on the IPMC712 and IPMC761:

Table 3-3. On-Board PCI Device Identification

Device	Device	Vendor ID	Device ID	Revision ID
SCSI Controller	LSI SYM53C895A	0x1000h	0x0012h	0x00h
PCI-ISA Bridge	W83C554F	0x10ADh	0x0565h	XXh

PCI Arbitration Assignments on Host Boards

The IPMC module PCI arbitration is provided by the host board.

MVME5100

The **MVME5100** PCI arbitration is performed by the Hawk ASIC on the host board which supports eight external PCI masters. Included is the Hawk itself and seven external PCI masters. The arbitration assignments for the IPMC712 and IPMC761, when installed on the MVME5100, are as follows:

Table 3-4. PCI Arbitration Assignments

PCI Bus Request	PCI Master(s)
Request 1 (PARBI1)	PMC Slot 1 (SCSI device on the module in PMC Slot 1)
Request 2 (PARBI2)	PIB device on the module in PMC Slot 1

MVME5500

The **MVME5500** IPMC module PCI arbitration is performed using logic implemented in Programmable Logic Devices (PLDs). These arbiters use a rotating priority scheme for fairness and bus parking and will always be on the GT-64260B. There are no software programmable modes to these arbiters.

MVME6100

The **MVME6100** IPMC module PCI arbitration is performed by the MV64360 ASIC. The internal PCI arbiter REQ#/GNT# signals are multiplexed on the MV64360 MPP[31:0] pins. The internal PCI arbiter is disabled by default (the MPP pins function as general purpose inputs). Software will configure the MPP pins to function as request/grant pairs for the internal PCI arbiter.

The IPMC module arbitration pairs for the MVME6100 are assigned to the MPP pins as follows;

- MPP pin 8, PCI Bus Grant (PIB device on IPMC module)
- MPP pin 9, PCI Bus Request (PIB device on IPMC module)
- MPP pin 12, PCI Bus Grant (SCSI device on IPMC module)
- MPP pin 13, PCI Bus Request (SCSI device on IPMC module)

Interrupt Assignments

The interrupt architecture for the IPMC712 and IPMC761 is fully compliant with the PowerPlusII Programming Specification for a single processor board configuration.

MVME5100 IPMC Module Interrupt Assignments

Legacy interrupt assignment for the PCI-to-ISA Bridge (PIB) is maintained to ensure software compatibility between MVME5100 and IPMC761 while in IPMC mode. This is accomplished by using the on-board IPMC761 connector to route the PIB's interrupt to external interrupt 0 of the Hawk's MPIC.

The MVME5100 Ethernet port 2 is routed to the PIB's IRQ10 input. The SCSI interrupt on the IPMC761 is also routed to the PIB at IRQ14. The SCSI device is connected to the INTA# pin J11-04 of PMC Slot 1. Interrupts are routed to the Hawk from on-board resources as specified by the module's programming.

The Hawk interrupt assignments are shown below:

Table 3-5. Hawk MPIC Interrupt Assignments

MPICI RQ	Edge/Level	Polarity	Interrupt Source	Notes
IRQ0	Level	High	PIB (8259) in PMC Slot 1	1
IRQ9	Level	Low	SCSI Controller interrupt shall be connected to INTA# pin J11-04	2

Notes

1. This interrupt provided for software compatibility with MVME2700.
2. MVME5100 Hawk MPIC IRQ9 interrupt sources may be one of the following: PCI-PMC1 INTA#, PMC2 INTB#, or PCIX INTA#.

MVME5500 IPMC Module Interrupt Assignments

Legacy Interrupt assignments were not maintained on the MVME5500 due to the vastly different host bridge device (GT-64260) used. The MVME5500 uses the GT-64260 interrupt controller to handle interrupts internal to the GT-64260 as well as the external interrupt sources. The GT-64260 uses general purpose pins that are configured by software to act as interrupt inputs. The following are the IPMC module-related interrupt assignments.

Table 3-6. MVME5500 Interrupts

GPP PIN	Edge/Level	Polarity	Interrupt Source
11	Level	Low	IPMC PIB (8259) Int in Slot 1
8	Level	Low	SCSI Controller Interrupt
Connected to INTA# pin J11-04			

Note The MVME5500 does not have any Ethernet interrupts routed back to the IPMC PIB device.

MVME6100 IPMC Module Interrupt Assignments

Legacy Interrupt assignments were not maintained on the MVME6100 because of the vastly different host bridge device (MV64360).

The MVME6100 uses the interrupt controller integrated into MV64360 to manage the MV64360 internal interrupts as well as the external interrupt requests. The IPMC module interrupts are routed to the MV64360 MPP pins as follows;

Table 3-7. MVME6100 Interrupts

GPP PIN	Edge/Level	Polarity	Interrupt Source
5	Level	High	IPMC PIB (8259) Int in Slot 1
16	Level	Low	SCSI Controller Interrupt
Connected to INTA# pin J11-04			

Note The MVME6100 does not have any Ethernet interrupts routed back to the IPMC PIB device.

ISA Local Resource Bus

The ISA devices on the IPMC712 and IPMC761 are as follows:

- PCI-to-ISA Bridge
- Super I/O

PCI-to-ISA Bridge (PIB)

The PIB contains ISA Bridge I/O Registers for various functions. These registers are accessible from the PCI bus.

Super I/O

The Super I/O device provides the following functions:

- Two serial ports (asynchronous)
- Parallel port interface

The device's hardware configuration is based on two strap-pins: BADDR0 and BADDR1. During reset, strapping options shown on BADDR0 and BADDR1 pins determine the device's operation. Clock speed is 48 MHz. The following table shows the hardware strapping for the Super I/O device:

Table 3-8. Strap Pins Configuration

Pins	Reset Configuration
BADDR1 BADDR0	1,1 - Index Register 002Eh, Data Register 002Fh, PnP motherboard mode, Wake up in Config state

ISA DMA Channels

The following table lists PIB DMA Channel Assignments not used.

Table 3-9. PIB DMA Channel Assignments

PIB Priority	PIB Label	Controller	DMA Assignment
Highest	Channel 2	DMA1	Not used on module

Z8536 CIO Port Pins

The following table lists port pins not used by the IPMC761 module.

Notes

1. The Hawk External Register Set interface now provides these functions.
2. On the IPMC712, pins PA0 through PA4, PA6, PA7, PB0 through PB4 are not used on the Z8536 CIO.

Table 3-10. Z8536 CIO Port Pins Assignment

Port Pin	Signal Name	Direction	Descriptions
PA6	BRDFAIL	Output	Not used on module
PB6	FUSE	Input	Not used on module
PB7	ABORT_	Input	Not used on module
PC1	Reserved	I/O	Not used on module
PC2	BASETYP0	Input	Not used on module
PC3	BASETYP1	Input	

ISA DMA Connections/Assignments

The following table shows the DMA connections/assignments between the PC97307 and the PIB.

Table 3-11. DMA Connection/Assignments

Channel	Connection	Level	Usage
0	SCC W//REQA	high	Serial Port 3 RX
1	SCC DTR//REQA	high	Serial Port 3 TX
2	SIO DRQ2/DACK2	high	User SIO configurable, suggested use is parallel port
3	SIO DRQ3/DACK3	high	User SIO configurable, suggested use is parallel port
4	None		PIB Internal DMA cascade
5	SCC W//REQB	high	Serial Port 4 RX
6	SCC DTR//REQB	high	Serial Port 4 TX
7	None		

Interrupt Routing to PIB

Module interrupts and MVME5100 Ethernet Port 2 interrupts go through the 8259 pair and into the PIB. The output of the PIB then goes to the Hawk MPIC on the MVME5100. The table below lists the ISA interrupts routed to the PIB.

Table 3-12. PIB Interrupt Assignments

PRI	ISA IRQ	Controller	Edge/Level	Polarity	Interrupt Source	Notes
1	IRQ0	INT1	Edge	High	Timer 1 / Counter 0	1
3-10	IRQ2		Edge	High	Cascade Interrupt from INT2	
4	IRQ9	INT2	Level	High	Z8536 CIO	2,3
					Z85230 ESCC	
5	IRQ10	INT2	Level	Low	PCI-Ethernet Interrupt (from MVME5100 Port 2)	2,4
9	IRQ14	INT2	Level	Low	PCI-SCSI Interrupt	2
11	IRQ3	INT1	Edge	High	COM2 (Async Serial Port 2)	
12	IRQ4		Edge	High	COM1 (Async Serial Port 1)	
15	IRQ7		Edge	High	Parallel Port Interrupt	

Notes

1. Internally generated by the PIB.
2. After a reset, all ISA IRQ interrupt lines default to edge-sensitive mode.
3. Interrupts from the Z8536 and Z85230 devices are externally wired. External logic will determine which device to acknowledge during a pseudo IACK cycle. The Z8536 CIO has higher priority than the Z85230 ESCC. This IRQ MUST be programmed for level-sensitive mode.
4. This interrupt is routed from the MVME5100 through the IPMC connector to the module's PIB to allow backward compatibility to other products.

Vital Product Data (VPD)

To access VPD information for each SBC, access the registers through the I²C interface as follows:

- MVME5100 - via the Hawk ASIC; IPMC761's VPD address is \$A4.
- MVME5500 - via the Discovery1 device GT64260
- MVME6100 - via the Discovery2 device MV64360

This chapter provides connector pin assignments for the IPMC712 and IPMC761 modules.

IPMC712 Connector

This connector provides the on-board interface of the IPMC712 I/O signals. The pin assignments for this connector are as follows:

Table 4-1. IPMC712 Connector

Pin	Signal Description	Signal Description	Pin
1	I2CSCL	I2CSDA	2
3	GND	GND	4
5	JDB8#	GND	6
7	GND	JDB9#	8
9	JDB10#	+3.3V	10
11	+3.3V	JDB11#	12
13	JDB12#	GND	14
15	GND	JDB13#	16
17	JDB14#	+3.3V	18
19	+3.3V	JDB15#	20
21	JDBP1#	GND	22
23	GND	LANINT2_L	24
25	PIB_INT	+3.3V	26
27	+3.3V	PIB_PMCREQ#	28
29	PIB_PMCGNT#	GND	30
31	GND	+3.3V	32
33	+5.0v	+5.0v	34
35	GND	GND	36
37	+5.0v	+5.0v	38
39	GND	GND	40

IPMC761 Connector

connector provides the on-board interface of the IPMC761 I/O signals. The pin assignments for this connector are as follows:

Table 4-2. IPMC761 Connector

Pin	Signal Description	Signal Description	Pin
1	I2CSCL	I2CSDA	2
3	GND	GND	4
5	DB8#	GND	6
7	GND	DB9#	8
9	DB10#	+3.3V	10
11	+3.3V	DB11#	12
13	DB12#	GND	14
15	GND	DB13#	16
17	DB14#	+3.3V	18
19	+3.3V	DB15#	20
21	DBP1#	GND	22
23	GND	LANINT2_L	24
25	PIB_INT	+3.3V	26
27	+3.3V	PIB_PMCREQ#	28
29	PIB_PMCNT#	GND	30
31	GND	+3.3V	32
33	+5.0v	+5.0v	34
35	GND	GND	36
37	+5.0v	+5.0v	38
39	GND	GND	40

PCI Interface and I/O Connectors

There are four 64-pin connectors on the IPMC761 (P11, P12, P13, and P14) which provide 32-bit PCI interface and P2 Input/Output (I/O) for the host board. The pin assignments are as follows:

Table 4-3. PCI Connector Pin Assignments (P11)

Pin	Signal Description	Signal Description	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	PMCPRSNT1#	+5V	8
9	INTD#	Not Used	10
11	GND	Not Used	12
13	CLK	GND	14
15	GND	PMCGNT1#	16
17	PMCREQ1#	+5V	18
19	+5V (Vio)	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3#	26
27	AD22	AD21	28
29	AD19	+5V	30
31	+5V (Vio)	AD17	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	GND	44
45	+5V (Vio)	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0#	52
53	AD06	AD05	54
55	AD04	GND	56

Table 4-3. PCI Connector Pin Assignments (P11) (continued)

Pin	Signal Description	Signal Description	Pin
57	+5V (Vio)	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64#	64

Table 4-4. PCI Connector Pin Assignments (P12)

Pin	Signal Description	Signal Description	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	Not Used	8
9	Not Used	Not Used	10
11	Not Used	+3.3V	12
13	RST#	Not Used	14
15	+3.3V	Not Used	16
17	Not Used	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL1	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2#	32
33	GND	Not Used	34
35	TDRY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD14	AD13	46
47	GND	AD10	48
49	AD08	+3.3V	50
51	AD07	Not Used	52
53	+3.3V	Not Used	54
55	Not Used	GND	56

Table 4-4. PCI Connector Pin Assignments (P12) (continued)

Pin	Signal Description	Signal Description	Pin
57	Not Used	Not Used	58
59	GND	Not Used	60
61	ACK64#	+3.3V	62
63	GND	Not Used	64

Table 4-5. PCI Connector Pin Assignments (P13)

Pin	Signal Description	Signal Description	Pin
1	Reserved	GND	2
3	GND	Not Used	4
5	Not Used	Not Used	6
7	Not Used	GND	8
9	+5V (Vio)	Not Used	10
11	Not Used	Not Used	12
13	Not Used	GND	14
15	GND	Not Used	16
17	Not Used	Not Used	18
19	Not Used	GND	20
21	+5V (Vio)	Not Used	22
23	Not Used	Not Used	24
25	Not Used	GND	26
27	GND	Not Used	28
29	Not Used	Not Used	30
31	Not Used	GND	32
33	GND	Not Used	34
35	Not Used	Not Used	36
37	Not Used	GND	38
39	+5V (Vio)	Not Used	40
41	Not Used	Not Used	42
43	Not Used	GND	44
45	GND	Not Used	46
47	Not Used	Not Used	48
49	Not Used	GND	50
51	GND	Not Used	52
53	Not Used	Not Used	54
55	Not Used	GND	56

Table 4-5. PCI Connector Pin Assignments (P13) (continued)

Pin	Signal Description	Signal Description	Pin
57	+5V (Vio)	Not Used	58
59	Reserved	Reserved	60
61	Reserved	GND	62
63	GND	Reserved	64

Table 4-6. PCI Connector Pin Assignments (P14)

Pin	Signal Description	Signal Description	Pin
1	Not Used	DB0#	2
3	Not Used	DB1#	4
5	Not Used	DB2#	6
7	Not Used	DB3#	8
9	Not Used	DB4#	10
11	Not Used	DB5#	12
13	Not Used	DB6#	14
15	PRSTB#	DB7#	16
17	PRD0	DBP#	18
19	PRD1	ATN#	20
21	PRD2	BSY#	22
23	PRD3	ACK#	24
25	PRD4	RST#	26
27	PRD5	MSG#	28
29	PRD6	SEL#	30
31	PRD7	D/C#	32
33	PRACK#	REQ#	34
35	PRBSY	O/I#	36
37	PRPE	AFD#	38
39	PRSEL	SLIN#	40
41	INIT#	TXD3	42
43	PRFLT#	RXD3	44
45	TXD1_232	RTXC3	46
47	RXD1_232	TRXC3	48
49	RTS1_232	TXD4	50
51	CTS1_232	RXD4	52
53	TXD2_232	RTXC4	54
55	RXD2_232	TRXC4	56

Table 4-6. PCI Connector Pin Assignments (P14) (continued)

Pin	Signal Description	Signal Description	Pin
57	RTS2_232	Not Used	58
59	CTS2_232	Not Used	60
61	MDO	MSYNC#	62
63	MDI	MCLK	64



General Specifications

The following table provides general specifications for the IPMC712 and IPMC761 module.

Table A-1. IPMC Specifications

Main Characteristic	Function	Specification
PMC Interface	Address/Data	A32/D32/D64, PMC PN1, PN2, PN3, PN4 Connectors
	PCI Bus Clock	33 MHz
	Signaling	5 Volts
	Module Type	Basic, Single-Wide; P2 I/O
SCSI Bus	Controller	Symbios 53C895A
	PCI Local Bus DMA	Yes, with PCI Local Bus Burst
	Asynchronous Transfer Rate	5.0MB/s
	Ultra-SCSI Transfer Rate	20.0MB/s (8-Bit Mode), 40.0MB/s (16-Bit Mode)
	Connector	Routed to P2, 50 or 68 Pin on P2
Synchronous Serial Ports	Controller	85230/8536
	Number of Ports	2
	Configuration	TTL to P2 (Both Ports), SIM on MVME761
	Baud Rate (BPS Max)	2.5M Synchronous, 38.4K Asynchronous
	Connector	Routed to P2, HD-26 on MVME761
Asynchronous Serial Ports	Controller	16C550 UART
	Number of Ports	2 (16550 Compatible)
	Configuration	EIA-574 DTE
	Asynchronous Baud Rate (BPS Max)	38.4 EIA-232, 115Kbps Raw Transfer Rate
	Connector	Routed to P2, DB-9 on MVME761
Parallel Ports	Controller	PC97307
	Configuration	8-Bit Bi-Directional, Full IEEE 1284 Support, Centronics Compatible
	Modes	Master Only
	Connector	Routed to P2, HD-36 on MVME761

Power Requirements

The table below lists the typical and maximum power consumption of the IPMC712 and IPMC761 modules.

Table A-2. Power Consumption

Supply Voltage	Amps (Typical)	Amps (Maximum)
+5V ($\pm 5\%$)	0.5 A	N/A
+12V ($\pm 10\%$)	0.2 A	0.5 A
-12V ($\pm 10\%$)	0.1 A	0.3 A



Motorola Documents

The Motorola publications listed below are referenced in this manual. You can obtain paper or electronic copies of Motorola Embedded Communications Computing publications by:

- Contacting your local Motorola sales office
- Visiting the Embedded Communications Computing World Wide Web literature site, <http://www.motorola.com/computer/literature>

Table B-1. Motorola Documents

Document Title	Motorola Publication Number
MVME5100 Single Board Computer Installation and Use	V5100A/IH
MVME5100 Single Board Computer Programmer's Reference Guide	V5100A/PG
MVME5500 Single Board Computer Installation and Use	V5500A/IH
MVME5500 Single Board Computer Programmer's Reference Guide	V5500A/PG
MVME6100 Single Board Computer Installation and Use	V6100A/IH
MVME6100 Single Board Computer Programmer's Reference Guide	V6100A/PG
MVME2600 Single Board Computer Installation and Use	V2600A/IH
MVME2600 Single Board Computer Programmer's Reference Guide	V2600A/PG
MVME2700 Single Board Computer Installation and Use	V2700A/IH
MVME2700 Single Board Computer Programmer's Reference Guide	V2700A/PG
MOTLoad Firmware Package User's Manual	MOTLODA/UM
PPCBUG Firmware Package User's Manual, Part 1 of 2	PPCBUGA1/UM
PPCBUG Firmware Package User's Manual, Part 2 of 2	PPCBUGA2/UM
PPCBUG Diagnostics User's Manual	PPCDIAA/UM

To obtain the most up-to-date product information in PDF or HTML format, visit <http://www.motorola.com/computer/literature>.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets or user's manuals. For your convenience, a source for the listed document is also provided.

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Table B-2. Manufacturers' Documents

Document Title	Publication Number
WebSite: Motorola Literature Distribution Center E-mail: ldcfomotorola@hibbertco.com Telephone: (800) 441-2447 or (303) 675-2140	
MPC750 RISC Microprocessor Users Manual	MPC750UM/AD
MPC7400 RISC Microprocessor Users Manual	MPC7400UM/D
PowerPlus II Vital Product Data Engineering Specification	Revision 0.1
Tundra Semiconductor Corporation Universe II User Manual	8091142_MD300_01.pdf
MV64360 System Controller for PowerPC Processors Data Sheet Marvell Technologies, Ltd. Web Site: http://www.marvell.com/	MV-S100414-00C

Note In many cases, the information is preliminary and the revision levels of the documents are subject to change without notice.

Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided.

Table B-3. Related Specifications

Document Title and Source	Publication Number
PCI Special Interest Group Peripheral Component Interconnect (PCI) Local Bus Specification,	PCI Specification Revision 2.0, 2.1, 2.2
Institute of Electrical and Electronics Engineers, Inc. (IEEE)	
IEEE - Common Mezzanine Card Specification (CMC)	P1386, Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC)	P1386.1, Draft 2.0
Bidirectional Parallel Port Interface Specification	IEEE Standard 1284
ANSI ANSI Small Computer System Interface-2 (SCSI-2), Draft Document Global Engineering Documents	X3.131.1990
VMEbus International Trade Association (VITA) VME64 Specification	ANSI/VITA 1-1994

A

address assignments PCI local bus (IDSEL) 17
arbitration assignments (host boards) 18
arbitration pairs, MVME6100 18
architecture xiii, 15
ASICs 8

B

backward compatibility 2, 9
basic features 1
block diagram, IPMC712 6
block diagram, IPMC761 4
board ejector handles 14
bus grants 18

C

caching 2
CIO device 8
CIO port pins 22
clock configuration, IPMC712 7
clock input 8
clock speed, SCSI 15
clock speed, Super I/O 21
comments, sending xiv
compliance, IEEE P1386.1 1
configuring the module 11
connectors
 EIA-E700 1
 IPMC761 25, 26
 P1 and P2 25, 26, 27
controller, SCSI 2
conventions used in the manual xv

D

device ID, PCI device 17
device ID, SCSI 15
devices
 CIO 8
 ESCC 8
 ISA 21
 PCI 15
 PIB 2, 21
 SCSI 2, 15
 Super I/O 8
DMA channel assignments 21
DMA connections 21
DMA support 8, 15
DTE 8

E

EEPROM device 8

EIA-E700 1
ejector levers 14
ESCC 8
ESD precautions 12
Ethernet port interrupts 23
extended SCSI 1

F

form factor 1
functionality 1

G

GPIO pin assignments 16
green PIB LED 9
green SCSI LED 9

H

handshaking signals 9
Hawk ASIC 8, 18
headers, configurable 11

I

I/O
 narrow SCSI 2
 parallel 2
 serial 2
I/O connector pin assignments 26
I/O modes 9
I/O ports 1
IDSEL mapping 17
IDSEL settings 2, 16
inspecting the module 11
installation
 hardware 11
 PMC module onto host board 11
installation precautions 12
installing the IPMC 11
interfaces
 Hawk external register set 22
 parallel 21
 PCI bus 1, 26
 SCSI 2
 serial 21
interrupt assignments
 for MVME5500 20
 for MVME6100 20
 Hawk MPIC for MVME5100 19
interrupt routing to PIB 23
IPMC mode 1, 9
IPMC specifications 33
IPMC712 pin assignments 25

IPMC761 pin assignments [26](#)
ISA Bridge I/O Registers [8](#)
ISA local resource bus [8, 21](#)

J

jumpering, clock signals [9](#)

L

LEDs [9](#)
local buses [2](#)
local resource bus [8](#)

M

manual conventions [xv](#)
manufacturers' manuals [36](#)
mapping to IDSEL [17](#)
max power consumption [34](#)
mechanical layouts [5](#)
memory support [1](#)
model numbers [xiii](#)
modem control lines [8](#)
modes, I/O [9](#)
modes, programmable [18](#)
module interrupts [23](#)
Motorola manuals [35](#)
MPP pins [18](#)

P

P1 and P2 connectors [25, 26, 27](#)
packaging [11](#)
parallel port [8](#)
PCI arbitration, MVME5100, MVME5500,
MVME6100 [18](#)
PCI bus grant [9](#)
PCI device identification [17](#)
PCI interface [26](#)
PCI Signaling Voltage Level [9](#)
PCI-ISA Bridge [2](#)
PCI-to-ISA bridge [2, 8, 15](#)
PIB [2, 8](#)
pin assignments [25](#)
pin assignments, GPIO [16](#)
PLDs [18](#)
PMC mode [9](#)
PMC support [1](#)
power consumption [34](#)
power requirements [34](#)
product description [xiii](#)
programmable modes [18](#)
programming model [15](#)
publications, related [35](#)

R

register access [8](#)
registers, ISA bridge [21](#)
related specifications [37](#)
revision history [xiii](#)
revision ID, PCI device [17](#)

RS232 Interface [9](#)

S

S1 switch [2, 16](#)
S2 switch [16](#)
SCRIPTS RAM [2](#)
SCSI as master [9](#)
SCSI controller [2](#)
SCSI data lines [2](#)
SCSI device [2](#)
SCSI extended [1](#)
SCSI signals [3](#)
selecting IDSEL settings [16](#)
selecting SCSI bus width [16](#)
selecting SCSI master [16](#)
selecting SCSI speed [16](#)
serial port 4, clock [7](#)
serial port configuration [8](#)
serial ports [8](#)
settings for IDSEL [2](#)
signaling levels [9](#)
signals, mux [2](#)
signals, SCSI [3](#)
specification, related [37](#)
specifications for IPMCs [33](#)
static ROM [8](#)
strap pin configuration [21](#)
strapping options [21](#)
suggestions, submitting [xiv](#)
Super I/O [8, 21](#)
super I/O [21](#)
switch settings [11](#)
switches
S1 (GPIO) [2, 16](#)
S2 (IDSEL) [16](#)
synchronous transfer rate [2](#)

T

termination of SCSI signals [3](#)
terminology used in this manual [xiv](#)
transition modules, compatibility [2](#)
typeface, meaning of [xv](#)

U

user documentation [35](#)

V

variants [xiii](#)
vendor ID, PCI device [17](#)
Vital Product Data (VPD) [8](#)
voltage levels [9](#)

W

Winbond PCI-to-ISA Bridge [2](#)

Z

zero ohm jumpers [3](#)