Hall A

Phillips Scientific

32 Channel 225 MHz Scaler

CAMAC MODEL 7132 7132H

FEATURES

* 7132 Features NIM/TTL with LEMO's, 7132H Differential ECL Header Inputs
* 32 Scalers, 24-Bits long or 16 Scalers, 48-Bits long
* Scalers may be Read Out or Preset Individually or in Q Block Mode
* Fast Clear and Inhibit Inputs
* LAM on Overflow on Any Scaler
* Programmable Inhibit on Overflow
* Done Output on Overflow
* Built-in Test Features

DESCRIPTION

The Model 7132/7132H scaler implements thirty-two scalers, 24-bits long, or sixteen scalers, 48-bits long in a single width CAMAC module. The high density, versatility and 225 MHz count rate are unmatched. Each scaler consists of a presettable up counter with NIM/TTL or differential ECL inputs. Clear, Inhibit and Test inputs are common to all 32 scalers. When any counter overflows, LAM and/or Done may be generated. When Inhibit on Overflow is enabled, a channel may be programmed to inhibit itself and other channels from counting. Any counter may be preset with the 1's complement of a desired count; this configures it as a programmable countdown scaler or programmable timer function.

FRONT PANEL INPUTS

Lemo Inputs (7132) : Accepts positive TTL and negative NIM level signals. TTL threshold typically +1.2Volts; NIM threshold typically –500mVolt.

NIM : Input impedance 50 ohm, ±10%; Inputs protected to ±8VDC.

TTL : Input impedance 1000 ohm, ±10%; Inputs protected to ±8VDC.

Bridged NIM Inputs : Available as an option on control inputs; (Clear, Inhibit and Test). Useful for daisy-chaining multiple 7132 modules; Input impedance 1K ohm; Will not respond to TTL level inputs. Specify when ordering.

ECL Inputs (7132H) : Two dual row x 17 pin headers; Accepts differential ECL inputs; 200mVolt threshold. Removable 110 ohm input termination.

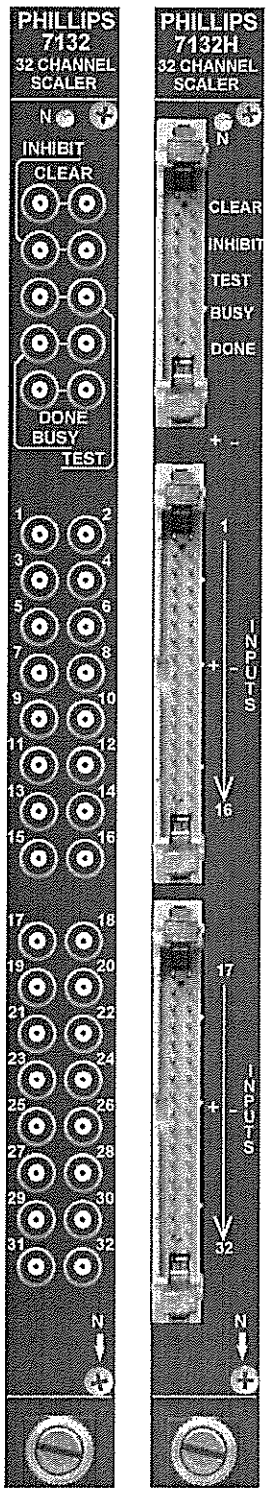
Input Channel 1 to 32 : Clock inputs to scalers normally configured as 32, 24-bit scalers. When configured as sixteen 48-bit scalers, the inputs are fed to the odd numbered channels. Minimum input pulse width 2.0nSec.

Count Rate : NIM/ ECL : Greater than 225 MHz.
TTL : Greater than 50 MHz.

Fast Clear : Clears all scalers; May be applied at any time. Minimum input width 20nSec. Requires 30nSec for next scaler Clock input to be recognized after the trailing-edge of Clear input.

Inhibit Input : Inhibits all scalers from counting inputs within 1.5nSec. Minimum input width is 4nSec. Allow 20nSec after Inhibit trailing-edge to recognize the next scaler Clock input. Will not inhibit counting of CAMAC initiated test counts or front panel test inputs.

Test Function : Common to all channels; Used to clock all scalers when the module is inhibited by CAMAC I or the front panel Inhibit. Minimum pulse width 5nSec; Maximum frequency 100MHz.



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FRONT PANEL OUTPUTS

7132 : *LEMO output connectors; NIM current-switching bridged outputs –32mA, (–1.6Volts into a single 50 ohm load and –800mV into two 50 ohm loads).*

7132H : *Differential ECL header outputs. Capable of driving two 110 ohm loads.*

DONE Output : *Pulsed on overflow for those channels selected by the Done On Overflow Register. Latency time from clock to Done Output is 100nSec typical; Pulse width 64nSec min. to 96nSec max.*

BUSY Output : *Active when the module is inhibited from the front panel Inhibit or from CAMAC and during any CAMAC operation. When the Configuration Register is written to or reset, Busy will be active for up to 300 mSec.*

TEST FEATURES

Front End Check : *All scalers are clocked with the front panel Test input. The module must be inhibited from the front panel Inhibit or from CAMAC. This ensures that the scaler inputs are not being clocked by external events during a test sequence.*

CAMAC Check : *A programmed number of 32 MHz clocks equal to the number stored in the Test Count Register is applied to all channels. The module must be inhibited from the front panel Inhibit or from CAMAC Inhibit to lock out any external events during a test sequence.*

GENERAL PERFORMANCE

Power Supply Requirements : *+6 Volt @ 1.4 Amps typical; – 6 Volt @ 2.5 Amps typical;* } *Forced air cooling is recommended when operating adjacent modules in a crate.*

Operating Temp. : *0 °C to 60 °C ambient.*

Packaging : *Standard single width CAMAC module in accordance with ESONE Report EUR 4100.*

PROGRAMMING REGISTERS

SCALER BANK SELECTION REGISTER :

Contains the bank of scalers for the next CAMAC command as well as the address and bank of scalers for the next sequential access commands (F4 or F20) as follows:

D24 D10	D9 D5	D4 D2	D1
Not Used	SA4 Sequential Address SA0	Not Used	Scaler Bank

D1: Selects scaler bank; D1 = 0 accesses channels 1 to 16, D1 =1 accesses channels 17 to 32.
D5-D9: Sequential access address, SA [4..0]; Points to the address that the next CAMAC cycle will execute.

TEST COUNT LENGTH REGISTER :

Sets the number of 32 MHz pulses applied to all scalers at the test command. Up to 255 pulses may be programmed, using D [8..1].

LAM MASK REGISTER :

Allows LAM to be generated on overflow on selected channels when LAM is enabled. Bits set to 1 allow LAM on overflow for their corresponding channels. Addressing is same as the Inhibit On Overflow Register.

LAM STATUS REGISTER :

Read only; Bits set to 1 indicate overflow for the corresponding channel. This register is 'AND'ed with the Inhibit on Overflow Register to produce Inhibit on Overflow and with the LAM Mask Register to produce LAM when LAM is enabled. Addressing is same as the Inhibit on Overflow Register.

DONE ON OVERFLOW REGISTER :

Enables The Front Panel Done output for each channel in the 7132/7132H. Bits set to 1 enable Done on Overflow for their corresponding channels. Addressing is same as the Inhibit on Overflow Register.

PROGRAMMING REGISTERS (continued)

INHIBIT ON OVERFLOW REGISTER :

Enables inhibit on overflow for selected channels as described in Tables 1 and 2. When Scaler bank 0 is selected (Scalers 1 to 16) each bit enables the corresponding channel. With Scaler bank 1 selected (Scalers 17 to 32), each bit enables the corresponding channel + 16 (bit 1 enables channel 17 and so on). Bits set to 1 enable Inhibit on Overflow for their corresponding channels.

INHIBIT ON OVERFLOW OPERATION :

There are four inhibit on overflow modes, as described below. Inhibit on overflow mode is controlled by setting the appropriate bits in the Control Register. Input to Inhibit on Overflow time (any channel, any configuration): Less then 95nSec.

TABLE 1: THIRTY-TWO 24-BIT SCALERS

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1,2	1-4	1-8	1-16
2	-	-	-	-
3	3,4	-	-	-
4	-	-	-	-
5	5,6	5-8	-	-
6	-	-	-	-
7	7,8	-	-	-
8	-	-	-	-
9	9,10	9-12	9-16	-
10	-	-	-	-
11	11,12	-	-	-
12	-	-	-	-
13	13,14	14-16	-	-
14	-	-	-	-
15	15,16	-	-	-
16	-	-	-	-

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17,18	17-20	17-24	17-32
18	-	-	-	-
19	19,20	-	-	-
20	-	-	-	-
21	21,22	21-24	-	-
22	-	-	-	-
23	23,24	-	-	-
24	-	-	-	-
25	25,26	25-28	25-32	-
26	-	-	-	-
27	27,28	-	-	-
28	-	-	-	-
29	29,30	29-32	-	-
30	-	-	-	-
31	31,32	-	-	-
32	-	-	-	-

TABLE 2: SIXTEEN 48-BIT SCALERS

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1	1,3	1-7	1-15
3	3	-	-	-
5	5	5,7	-	-
7	7	-	-	-
9	9	9,11	9-15	-
11	11	-	-	-
13	13	13,15	-	-
15	15	-	-	-

Overflow on Channel	Inhibits Channels			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17	17,19	17-23	17-31
19	19	-	-	-
21	21	21,23	-	-
23	23	-	-	-
25	25	25,27	25-31	-
27	27	-	-	-
29	29	29,31	-	-
31	31	-	-	-

CONFIGURATION REGISTER FORMAT :

D24 D7	D6 D5	D4 D2	D1
Not Used	Inhibit on Overflow Mode	Not Used	Configuration

D6	D5	Mode	
0	0	0	(Default)
0	1	1	
1	0	2	
1	1	3	

0	Selects 32 24 Bit Scalers	(Default)
1	Selects 16 48 Bit Scalers	

CAMAC DATAWAY OPERATIONS

F(0)·A(X) : 32-Bit Mode: Read scaler (X+1) in the bank selected by the Scaler Bank Selection Register. 48-Bit Mode: Even addresses read the lower 24 bits and odd addresses read the upper 24 bits of a scaler in the bank selected by the Scaler Bank Selection Register.

F(1)·A(0) : Read the Configuration Register.

F(1)·A(1) : Read the Scaler Bank Selection Register.

F(1)·A(2) : Read the Test Count length.

F(1)·A(3) : Read the Inhibit on Overflow Register for the bank selected by the Scaler Bank Selection Register.

F(1)·A(5) : Read the Done on Overflow Register for the bank selected by the Scaler Bank Selection Register.

F(1)·A(12) : Read the LAM Status Register for the bank selected by Scaler Bank Selection Register.

F(1)·A(13) : Read the LAM Mask Register for the bank selected by the Scaler Bank Selection Register.

F(2)·A(X) : Read and Reset Scaler and LAM. See F0·A(X) for addressing.

F(4)·A(15) : Q Block read. Sequentially reads scalers starting at address in Scaler Bank Selection Register. After accessing scaler 32, the next command will return Q=0. The Scaler Bank Selection Register must be reprogrammed to reuse this command.

F(8) : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

F(9)·A(X) : Reset Scaler and LAM. See F0·A(X) for addressing.

F(10)·A(X) : Reset LAM. See F0·A(X) for addressing. Channels which have been inhibited by overflow on the addressed scaler are enabled.

F(11)·A(0) : Clear the Configuration Register. Also clears Inhibit on Overflow Register, LAM Mask, Done on Overflow Register and LAM Status Register. This command requires about 300 mSec to complete operation. Occurs on S2 strobe.

F(11)·A(1) : Reset the Scaler Bank Selection Register. Occurs on S2 strobe.

F(11)·A(2) : Reset the Test Count Length Register. Occurs on S2 strobe.

F(11)·A(3) : Reset Inhibit on Overflow Register. Enables all channels inhibited by overflow. Occurs on S2 strobe.

F(11)·A(4) : Reset all scalers, and LAM. Enables all channels inhibited by overflow. Occurs on S2 strobe.

F(11)·A(5) : Reset Done on Overflow Register. Occurs on S2 strobe.

F(11)·A(12) : Reset the LAM Status Register. Enables all scalers inhibited by overflow. Resets all LAMs. Occurs on S2 strobe.

F(11)·A(13) : Reset the LAM Mask Register. Occurs on S2 strobe.

F(16)·A(X) : Load Scaler. See F(0)·A(X) for addressing. Resets the LAM Status Bit for Scaler on S2 strobe. Any channels previously inhibited by overflow on channel (X+1) will be enabled by the S2 strobe.

F(17)·A(0) : Program the Configuration Register. See F(11)·A(0).

F(17)·A(1) : Write to the Scaler Bank Selection Register.

F(17)·A(2) : Write to the Test Count Length Register.

F(17)·A(3) : Write the Inhibit on Overflow Register.

F(17)·A(5) : Write the Done on Overflow Register.

F(17)·A(13) : Write the LAM Mask Register for the bank selected.

F(20) : Q Block Load. Sequentially loads scalers. See F(4) for addressing.

F(24) : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

F(25)·A(0) : Enables the test clock for the number of counts programmed into the Test Count Length. The module must be inhibited from Front Panel Inhibit or CAMAC I for clocks to be generated.

F(26) : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

Z : Reset all Scalers and LAM's. Enables all Scalers inhibited by overflow. Reset all registers. This command requires about 300 mSec to complete operation.

C : Reset all Scalers and LAM's. Enables all Scalers inhibited by overflow. Resets the Scaler Bank Selection Register to 0.

I : Inhibit the Scalers from counting normal input pulses. Allow test pulses from the front end or internally by CAMAC commands.

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MODEL 7132 32 CHANNEL 225 MHz PRESETTABLE SCALER

(Front Panel Description)

An LED Indicates the Module is Being Addressed via CAMAC.

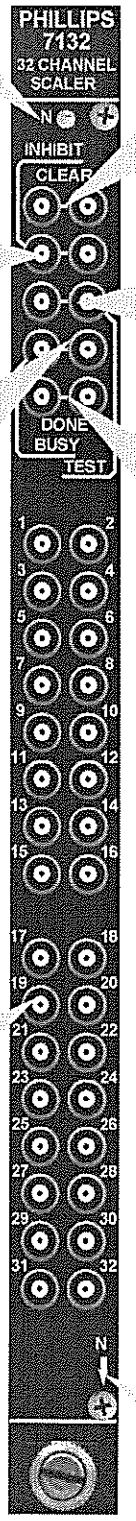
Clear Input, Bridged NIM, Logic Level (-500mV); Allows Easy Daisy Chaining; Clears All Scaler Channels;

Inhibit Bridged NIM Input, (-500mV) Inhibits All Scaler Channels; Enables Test Feature.

Test Input; Bridged NIM, Logic Level (-500mV); Triggers All Enabled Channels. Enabled by CAMAC or Front Panel Inhibit.

Busy Output Active on Inhibit or CAMAC Operation; Bridged NIM Out; -32mA (-1.6V @ 50 ohm, -.8V into Two 50 ohm Loads).

Done Output Pulses on Channel Over-flows; Bridged NIM Out; -32mA (-1.6 V @ 50 ohm, -.8 V into Two 50 ohm Loads)



32 Scaler Inputs; Logic Levels Negative NIM or Positive TTL; NIM=50 ohm, TTL=500 ohm.

Standard #1 CAMAC Packaging in accordance with EUR 4100.

Note:

1). Programmable Registers Permit the Module to be Configured for 32 Channel 24bit or 16 Channel 48bit Operation and Selction of LAM, Done and Inhibit on Overflow Features.

PROGRAMMING

MANUAL

FOR THE

MODEL 7132

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MODEL 7132/7132H
32 CHANNEL CAMAC SCALER
PROGRAMMING MANUAL

1 Scaler Bank Operation

Due to the number of scalers, the scalers and some of the registers controlling them are separated into two banks. Bank 0 contains the scalers 1 to 16 and the bits associated with them in the LAM Mask Register, the Inhibit On Overflow Register and the Done On Overflow Register. Bank 1 contains the scalers 17 to 32 and the bits associated with them in the LAM Mask Register, the Inhibit On Overflow Register and the Done On Overflow Register. Except during sequential access of scalers, the correct Scaler Bank must be selected in the Scaler Bank Selection Register before accessing these registers or the scalers. During sequential access the scalers are accessed sequentially in ascending order. The address and bank of the next scaler to be accessed is found in the Scaler Bank Selection Register.

When the 7132/7132H is configured as 24 bit scalers, the scalers are numbered 1 to 32. When the 7132/7132H is configured as 48 bit scalers, the scalers are odd numbers from 1 to 31.

2 Scaler Operations

2.1 Random Access Read and Write

Scalers are selected by the Bank and CAMAC subaddress as follows.

32 24-Bit Scalers:

	Scaler	
A[X]	Bank 0	Bank 1
0	1	17
1	2	18
2	3	19
3	4	20
4	5	21
5	6	22
6	7	23
7	8	24
8	9	25
9	10	26
10	11	27
11	12	28
12	13	29
13	14	30
14	15	31
15	16	32

16 48-Bit Scalers:

A[X]	Scaler			
	Bank 0		Bank 1	
	Lower 24 Bits	Upper 24 Bits	Lower 24 Bits	Upper 24 Bits
0	1	-	17	-
1	-	1	-	17
2	3	-	19	-
3	-	3	-	19
4	5	-	21	-
5	-	5	-	21
6	7	-	23	-
7	-	7	-	23
8	9	-	25	-
9	-	9	-	25
10	11	-	27	-
11	-	11	-	27
12	13	-	29	-
13	-	13	-	29
14	15	-	31	-
15	-	15	-	31

For example, A(5) will address the upper 24 bits of Scaler 5 in Scaler Bank 0 or the upper 24 bits of Scaler 21 in Bank 1.

2.1.1 Loading Scalers (Random Access)

F(16)·A(X)·W(24..1): Load a scaler with the value contained in W(24..1), Reset LAM for the scaler being loaded and enable any scalers disabled by a previous overflow on the scaler being loaded.

Any Channel inhibited by overflow by a channel that is being loaded will be enabled. The LAM Status bit associated with the scaler will also be reset.

2.1.2 Reading the Scalers (Random Access)

F(0)·A(X)·R(24..1): Read a scaler. The data is returned on R(24..1).

F(2)·A(X)·R(24..1): Read the value in a scaler and reset that scaler and the bit in the LAM Status Register associated with that scaler. Any scalers which had been inhibited by overflow on the scaler being read is enabled. Data is returned on R(24..1). When the 7132/7132H is configured as 48-bit scalers, odd address reads reset the bit in the LAM Status Register for the addressed scaler.

2.2 Q Block Read & Write

The address and bank of the next scaler to be accessed is found in the Scaler Bank Selection Register bits 5 to 9. Bits 5 to 9 of the Scaler Bank Selection Register are incremented at the end of the S1 time. The starting address for a Q Block access may be set by writing the appropriate value in the Scaler Bank Selection Register. The value of bits 5 to 9 in the Scaler Bank Selection Register is the number of the Scaler To Be Accessed minus 1. (See the following table.)

Configured as 32, 24 Bit Scalers				Configured as 16, 48 Bit Scalers			
Bank Selection Register Bits 5 to 9	Scaler To Be Accessed	Bank Selection Register Bits 5 to 9	Scaler To Be Accessed	Bank Selection Register Bits 5 to 9	Scaler To Be Accessed	Bank Selection Register Bits 5 to 9	Scaler To Be Accessed
0	1	16	17	0	1, Lower 24 Bits	16	17, Lower 24 Bits
1	2	17	18	1	1, Upper 24 Bits	17	17, Upper 24 Bits
2	3	18	19	2	3, Lower 24 Bits	18	19, Lower 24 Bits
3	4	19	20	3	3, Upper 24 Bits	19	19, Upper 24 Bits
4	5	20	21	4	5, Lower 24 Bits	20	21, Lower 24 Bits
5	6	21	22	5	5, Upper 24 Bits	21	21, Upper 24 Bits
6	7	22	23	6	7, Lower 24 Bits	22	23, Lower 24 Bits
7	8	23	24	7	7, Upper 24 Bits	23	23, Upper 24 Bits
8	9	24	25	8	9, Lower 24 Bits	24	25, Lower 24 Bits
9	10	25	26	9	9, Upper 24 Bits	25	25, Upper 24 Bits
10	11	26	27	10	11, Lower 24 Bits	26	27, Lower 24 Bits
11	12	27	28	11	11, Upper 24 Bits	27	27, Upper 24 Bits
12	13	28	29	12	13, Lower 24 Bits	28	29, Lower 24 Bits
13	14	29	30	13	13, Upper 24 Bits	29	29, Upper 24 Bits
14	15	30	31	14	15, Lower 24 Bits	30	31, Lower 24 Bits
15	16	31	32	15	15, Upper 24 Bits	31	31, Upper 24 Bits

It is not necessary to set bits 5 to 9 in the Scaler Bank Selection Register before each Q Block access (F4 or F20) unless the value of bits 5 to 9 is 31 (11111). If the value of bits 5 to 9 is not 31, the value of bits 5 to 9 will automatically increment at the end of S1 time during a Q Block access, pointing to the next scaler. When the value of bits 5 to 9 is 31 (11111), all access is to scaler 32, and the 7132 will return Q=0 when a Q Block access is requested. Bits 5 to 9 in the Scaler Bank Selection Register must be reprogrammed, or the Scaler Bank Selection Register must be reset to use a Q Block access again.

2.2.1 Loading Scalers (Q Block Access)

F(20)·W(24..1) Sequentially Load the Scalers with the value contained in W(24..1), Reset LAM for the scaler being loaded and enable any scaler disabled by a previous overflow on the scaler being loaded. The address lines have no effect on this command.

2.2.2 Reading the Scalers (Q Block Access)

F(4)·A(15)·R(24..1) Sequentially Read the Scalers. Data is returned on R(24..1). The address lines have no effect on this command.

2.3 Resetting Scalers

F(9)·A(X): Reset a Scaler and the corresponding bit in the LAM Status Register. Any channels inhibited by overflow in the scaler being reset will be enabled. 48-bit scalers must be reset 24 bits at a time. The scaler to be reset is determined as described below:

Address A[X]	24-Bit Scaler Bank		48-Bit Scaler Bank	
	0	1	0	1
0	1	17	1, Lower 24 Bits	17, Lower 24 Bits
1	2	18	1, Upper 24 Bits	17, Upper 24 Bits
2	3	19	3, Lower 24 Bits	19, Lower 24 Bits
3	4	20	3, Upper 24 Bits	19, Upper 24 Bits
4	5	21	5, Lower 24 Bits	21, Lower 24 Bits
5	6	22	5, Upper 24 Bits	21, Upper 24 Bits
6	7	23	7, Lower 24 Bits	23, Lower 24 Bits
7	8	24	7, Upper 24 Bits	23, Upper 24 Bits
8	9	25	9, Lower 24 Bits	25, Lower 24 Bits
9	10	26	9, Upper 24 Bits	25, Upper 24 Bits
10	11	27	11, Lower 24 Bits	27, Lower 24 Bits
11	12	28	11, Upper 24 Bits	27, Upper 24 Bits
12	13	29	13, Lower 24 Bits	29, Lower 24 Bits
13	14	30	13, Upper 24 Bits	29, Upper 24 Bits
14	15	31	15, Lower 24 Bits	31, Lower 24 Bits
15	16	32	15, Upper 24 Bits	31, Upper 24 Bits

F(11)·A(4): Reset all Scalers, and the LAMs. All scalers are enabled.

3 Registers

The 7132/7132H contains many operational options. These options are controlled through registers. Writing to or resetting the Configuration Register will reset the Inhibit On Overflow Register, the LAM Mask Register, the Done On Overflow Register, the LAM Status Register and all scalers. Any scaler inhibited by overflow will be enabled.

3.1 Scaler Bank Selection

W9 W5	W4 W2	W1
Pointer to Scaler for Sequential Access	Not Used	Scaler Bank

W1 = 0 Random Operations affect Scalers 1 to 16, or Scaler Bank 0.

W1 = 1 Random Operations affect Scalers 17 to 32, or Scaler Bank 1.

3.1.1 Set the Scaler Bank Selection

F(17)·A(1)·W(1..9): Select the bank of scalers for the next scaler read (F0, F2), scaler write (F16), scaler reset (F9), Done On Overflow Register (F1·A5, F17·A5), LAM Mask operations (F1·A13, F17·A13), Inhibit On Overflow Register (F1·A3, F17·A3) and LAM Status Reads (F1·A12) and set the pointer to the next scaler for sequential access (F4, F20).

3.1.2 Read the Scaler Bank Selection

F(1)·A(1)·R(1..9): Read the bank of scalers selected for the next scaler read (F0, F2), scaler write (F16), scaler reset (F9), Done On Overflow Register (F1·A5, F17A), Inhibit On Overflow Register (F1·A3, F17·A3), LAM Mask operations (F1·A13, F17·A13) and LAM Status Reads (F1·A12) and the pointer to the next scaler for sequential access (F4, F20).

3.1.3 Reset the Scaler Bank Selection

F(11)·A(1): Resets the Scaler Bank Selection to the default value of Bank 0, Sequential Address Pointer to 0.

3.2 Configuration Register

The 7132/7132H may be configured as thirty-two 24-bit scalers or sixteen 48-bit scalers. The 7132/7132H may also be configured to allow one channel to inhibit itself and 1, 3, 7 or 15 other channels on overflow (when configured as thirty-two 24-bit scalers) or 0, 1, 3 and 7 other channels (when configured as sixteen 48-bit scalers). These options are selected in the Configuration Register. Setting or resetting the Configuration Register will reset the Inhibit On Overflow Register, the LAM Mask Register and the LAM Status Register and all scalers. Any scaler inhibited by overflow will be enabled.

Bits assigned as follows:

D24 D7	D6 D5	D4 D2	D1
Not Used	Inhibit on Overflow Mode	Not Used	Configuration

D6	D5	Mode	
0	0	0	(Default)
0	1	1	
1	0	2	
1	1	3	

0	Selects 32 24 Bit Scalers	(Default)
1	Selects 16 48 Bit Scalers	

Inhibit On Overflow is controlled as shown below:

FOR 32 24-BIT SCALERS

Overflow on Channel	Inhibits Scalers			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1,2	1-4	1-8	1-16
2	-	-	-	-
3	3,4	-	-	-
4	-	-	-	-
5	5,6	5-8	-	-
6	-	-	-	-
7	7,8	-	-	-
8	-	-	-	-
9	9,10	9-12	9-16	-
10	-	-	-	-
11	11,12	-	-	-
12	-	-	-	-
13	13,14	14-16	-	-
14	-	-	-	-
15	15,16	-	-	-
16	-	-	-	-

Overflow on Channel	Inhibits Scalers			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17,18	17-20	17-24	17-32
18	-	-	-	-
19	19,20	-	-	-
20	-	-	-	-
21	21,22	21-24	-	-
22	-	-	-	-
23	23,24	-	-	-
24	-	-	-	-
25	25,26	25-28	25-32	-
26	-	-	-	-
27	27,28	-	-	-
28	-	-	-	-
29	29,30	29-32	-	-
30	-	-	-	-
31	31,32	-	-	-
32	-	-	-	-

FOR 16 48-BIT SCALERS

Overflow on Channel	Inhibits Scalers			
	Mode 0	Mode 1	Mode 2	Mode 3
1	1	1,3	1-7	1-15
3	3	-	-	-
5	5	5,7	-	-
7	7	-	-	-
9	9	9,11	9-15	-
11	11	-	-	-
13	13	13,15	-	-
15	15	-	-	-

Overflow on Channel	Inhibits Scalers			
	Mode 0	Mode 1	Mode 2	Mode 3
17	17	17,19	17-23	17-31
19	19	-	-	-
21	21	21,23	-	-
23	23	-	-	-
25	25	25,27	25-31	-
27	27	-	-	-
29	29	29,31	-	-
31	31	-	-	-

3.2.1 Set the Configuration Register

F(17)·A(0)·W(1..6): Set the configuration of the scalers and the inhibit on overflow mode as described above. Sets the Done On Overflow, Inhibit On Overflow and LAM Mask Registers to 0

3.2.2 Read the Configuration Register

F(1)·A(0)R(1..6): Reads the configuration of the scalers and the inhibit on overflow mode as described above.

3.2.3 Reset the Configuration Register

F(11)·A(0): Reset the Configuration Register to all zero, giving thirty-two 24-bit scalers and inhibit on overflow mode 0. Done On Overflow, Inhibit On Overflow and LAM Mask Registers are all reset to 0.

3.3 Inhibit On Overflow Register

When configured as thirty-two 24-bit scalers, each pair of odd/even channels (i.e., channels 1 and 2, channels 3 and 4) may be enabled to inhibit on overflow as described in paragraph 3.2. When configured as sixteen 48-bit scalers, each channel may be enabled to inhibit on overflow as described in paragraph 3.2. This option is controlled by the Inhibit On Overflow Register.

A channel inhibited by overflow may be enabled in one of four ways:

1) Writing to or resetting the Configuration Register will reset the Inhibit On Overflow Register and enable all channels inhibited by overflow.
2) Resetting the LAM Status bit associated with the channel whose overflow caused the affected channel to be inhibited will enable that channel.
3) Loading the Scaler which caused the inhibit on overflow.
4) Reading the Scaler which caused the inhibit on overflow with a CAMAC F2 operation.

The 7132/7132H contains one Inhibit On Overflow Register for each bank of Scalers. The correct scaler bank must be selected in the Scaler Bank Selection Register before reading or writing one of the Inhibit On Overflow Registers. The command to reset the Inhibit on Overflow Register operates on both Inhibit On Overflow Registers.

Inhibit on Overflow for a specific pair of scalers is enabled by setting the appropriate bit in the Inhibit on Overflow Register as follows:

Inhibit on Overflow Register Bit	24-Bit Scaler Bank		48-Bit Scaler Bank	
	0	1	0	1
1	1,2	17,18	1	17
2	-	-	-	-
3	3,4	19,20	3	19
4	-	-	-	-
5	5,6	21,22	5	21
6	-	-	-	-
7	7,8	23,24	7	23
8	-	-	-	-
9	9.1	25,26	9	25
10	-	-	-	-
11	11,12	27,28	11	27
12	-	-	-	-
13	13,14	29,30	13	29
14	-	-	-	-
15	15,16	31,32	15	31
16	-	-	-	-

3.3.1 Load the Inhibit On Overflow Register

F(17)·A(3)W(16..1): Load the Inhibit On Overflow Register for the bank of scalers selected in the Scaler Bank Selection Register.

3.3.2 Read the Inhibit On Overflow Register

F(1)·A(3)R(16..1): Read the Inhibit On Overflow Register for the bank of scalers selected in the Scaler Bank Selection Register.

3.3.3 Reset the Inhibit On Overflow Register

F(11)·A(3): Resets both Inhibit On Overflow Registers to zero. Enables all scalers which were inhibited by overflow.

3.4 LAM Mask Register

Every channel, regardless of the 7132/7132H configuration, may be programmed to cause LAM on overflow. This is controlled by the LAM Mask Register. The channel causing a LAM is determined by reading the LAM Status Registers. Writing to or resetting the Configuration Register will reset the LAM Mask Register.

The 7132/7132H contains one LAM Mask Register and one LAM Status Register for each bank of scalers. The correct Scaler Bank must be selected in the Scaler Bank Selection Register before reading or writing one of the LAM Mask Registers. The command to reset the LAM Mask Registers operates on both LAM Mask Registers.

LAM on overflow for a specific scaler is enabled by setting the appropriate bit in the LAM Mask Register as follows:

LAM Mask Register Bit	24-Bit Scaler Bank		48-Bit Scaler Bank	
	0	1	0	1
1	1	17	1	17
2	2	18	-	-
3	3	19	3	19
4	4	20	-	-
5	5	21	5	21
6	6	22	-	-
7	7	23	7	23
8	8	24	-	-
9	9	25	9	25
10	10	26	-	-
11	11	27	11	27
12	12	28	-	-
13	13	29	13	29
14	14	30	-	-
15	15	31	15	31
16	16	32	-	-

3.4.1 Load the LAM Mask Register

F(17)A·(13)W(16..1): Load LAM Mask for scalers in bank selected by F17·A1.

3.4.2 Read the LAM Mask Register

F(1)·A(13)·R(16..1): Read LAM Mask for scalers in bank selected by F17·A1.

3.4.3 Reset the LAM Mask Register

F(11)·A(13): Resets the LAM Mask Register to zero. No LAMs will be generated.

3.5 LAM Status Register

Every channel, regardless of the 7132/7132H configuration or the setting in the LAM Mask Register, will set the appropriate bit in the LAM Status Register on overflow. The 7132/7132H contains a LAM Status Register for each bank of scalers. The correct scaler bank must be selected in the Scaler Bank Selection Register before reading one of the LAM Status Registers. The command to reset all LAMs resets all bits in both LAM Status Registers. Writing to or resetting the Configuration Register will reset the LAM Status Register. Loading a scaler with a bit set in the LAM Status Register will reset that bit in the LAM Status Register.

The scaler(s) which have overflowed may be determined by the bits set in the LAM Status Registers as follows:

LAM Status Register Bit	24-Bit Scaler Bank		48-Bit Scaler Bank	
	0	1	0	1
1	1	17	1	17
2	2	18	-	-
3	3	19	3	19
4	4	20	-	-
5	5	21	5	21
6	6	22	-	-
7	7	23	7	23
8	8	24	-	-
9	9	25	9	25
10	10	26	-	-
11	11	27	11	27
12	12	28	-	-
13	13	29	13	29
14	14	30	-	-
15	15	31	15	31
16	16	32	-	-

3.5.1 Read the LAM Status Register

F(1)·A(12)·R(16..1): Read LAM Status Register for scalers in bank selected by F17·A1.

3.5.2 Reset the LAM Status Register

There are four ways to reset the LAM Status Register. F(10)·A(X) will reset one bit in the LAM Status Register selected by the Scaler Bank Selection Register and the address [A(X)] to zero while F(11)·A(13) completely resets both LAM Status Registers to zero. Loading a scaler or an F2 read of a scaler with its bit set in the LAM Status Register will reset that bit in the LAM Status Register. Any channels which have been inhibited by overflow on the channel for which LAM is reset will be enabled.

F(10)·A(X): Resets LAM for the channel addressed by A(X) in the LAM Status Register to zero.

F(11)·A(12): Resets the LAM Status Register to zero. No LAMS will be generated.

3.6 Done On Overflow Register

Every channel, regardless of the 7132/7132H configuration, may be programmed to cause a pulse on the DONE output on overflow. This is controlled by the Done On Overflow Register. Writing to or resetting the Configuration Register will reset the Done On Overflow Register. Any scaler inhibited by overflow will be enabled.

The 7132/7132H contains one Done On Overflow Register for each bank of scalers. The correct scaler bank must be selected in the Scaler Bank Selection Register before reading or writing one of the Done On Overflow Registers. The command to reset the Done On Overflow Register operates on both Done On Overflow Registers.

Done On Overflow for a specific scaler is enabled by setting the appropriate bit in the Done On Overflow Register as follows:

Done on Overflow Register Bit	24-Bit Scaler Bank		48-Bit Scaler Bank	
	0	1	0	1
1	1	17	1	17
2	2	18	-	-
3	3	19	3	19
4	4	20	-	-
5	5	21	5	21
6	6	22	-	-
7	7	23	7	23
8	8	24	-	-
9	9	25	9	25
10	10	26	-	-
11	11	27	11	27
12	12	28	-	-
13	13	29	13	29
14	14	30	-	-
15	15	31	15	31
16	16	32	-	-

3.6.1 Load the Done On Overflow Register

F(17)·A(5)·W(16..1): Loads the Done On Overflow Register for the bank selected in the Scaler Bank Selection Register.

3.6.2 Read the Done On Overflow Register

F(1)·A(5)·R(16..1): Read the Done On Overflow Register.

3.6.3 Reset the Done On Overflow Register

F(11)·A(5): Resets both Done Overflow Registers to zero. There will be no Pulses on Overflow for any Channel.

3.7 Test Count Length Register

The 7132/7132H contains a 32 MHz burst generator for internal test. The burst generator will put out a burst of 1 to 255 pulses at 32 MHz which is applied to all the scalers. The Test Count Length Register is programmed for the desired burst length. It is important to note that a test with the internal burst generator cannot be performed unless the module is inhibited by CAMAC inhibit or Front Panel Inhibit.

The Test Count Length Register is 8 bits. This register may be accessed from both Scaler Bank 0 or Scaler Bank 1.

3.7.1 Load the Test Count Register

F(17)·A(2)·W(8..1): Load the Test Count Length Register with the W(8..1). This will set the number of pulses produced by F25·A(0) .

3.7.2 Read the Test Count Register

F(1)·A(2)·R(8..1): Read the test count register. Data is returned on R(8..1).

3.7.3 Reset the Test Count Register

F(11)·A(2): Reset the test count register to zero. F25·A(0) will produce no pulse.

4 Test Functions

4.1 Initiate Internal Test

F(25)·A(0): A burst of pulses equal to the number in the Test Count Register is applied to all channels not inhibited by an overflow condition. The 7132/7132H must be inhibited by CAMAC I or through the front panel for this command to execute.

5 LAM

5.1 Disable LAM

F(24): Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.

5.2 Enable LAM

F(26): Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.

5.3 Test LAM

F(8): Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.

6 CAMAC NON-DATAWAY COMMANDS

Z: Reset all scalers and LAMs. Enables all scalers inhibited by overflow. Reset all registers. This command requires about 300 mSec to complete operation.

C: Reset all Scalers and LAMS. Enables all Scalers inhibited by overflow. Resets the Scaler Bank Selection Register to 0.

I: Inhibit all Scalers from counting normal input pulses. Enables test via CAMAC or the front panel Test input.

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