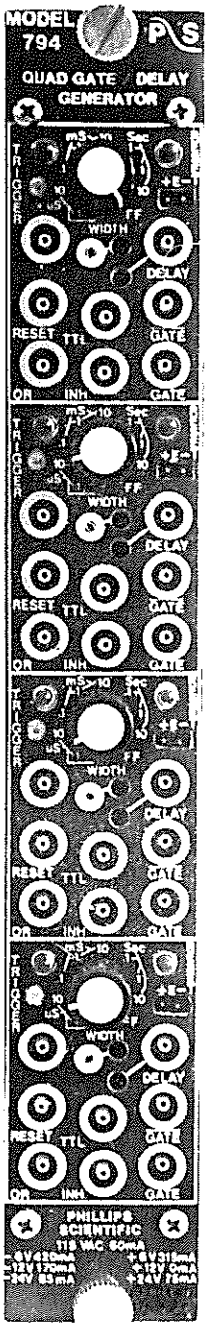
Phillips Scientific | Quad Gate/Delay Generator | NIM MODEL 794

Hall A

FEATURES

* Four Independent Gate/Delay Channels
* Wide Range, 50 nSec to over 10 Sec
* NIM, TTL Inputs; NIM, TTL, ECL Outputs
* Deadtimeless Operation
* Set/Reset Flip-Flop Mode
* Remote Programming via a 0 Volt to 10 Volt Input
* Easily Configured as an Oscillator or a Pulser
* Provides Bin Gate for Host NIMBIN



GENERAL DESCRIPTION

The Quad Gate/Delay Generator, Model 794, complies fully with the NIM specification TID-20893 and is packaged in a single width module. In monostable mode, Gate/Delay periods may be adjusted either locally or remotely from less than 50 nSec to more than 10 seconds. Each channel also operates in a Set/Reset flip flop mode. A bright LED indicates an active gate condition. Versatile input and output structures provide compatibility with NIM, ECL, and TTL standards. Further flexibility is afforded by programming jumpers mounted on the printed circuit board. These jumpers allow selected inputs and outputs to be assigned alternate logic functions or polarities.

TIME-BASE DESCRIPTION

The model 794 time-base circuit is non-updating and exhibits essentially no deadtime. Monostable Gate/Delay periods are selected by a combination of the RANGE switch and an analog programming input. A monitor test point provides a 0 to 1 Volt output which is proportional to the Gate/Delay period. Setting the Gate/Delay period with an oscilloscope is easily accomplished by pushing the TRIGGER pushbutton. Depressing this switch for more than 0.5 seconds causes the time-base to retrigger at a 1 KHz rate. In the bistable mode, the Gate/Delay period is equal to the interval between the arrival of the trigger and reset functions. The DELAY output always occurs at the trailing edge of the GATE output. The DELAY output width may be adjusted by a front panel potentiometer

INPUT DESCRIPTION

There are three ways to trigger the Model 794: (1) TRIGGER input; (2) OR input; (3) TRIGGER pushbutton. These functions are enabled in both monostable and bistable modes.

The TRIGGER input is compatible with both TTL levels and negative NIM logic. This input presents a high impedance to positive signals and 50 ohms to negative signals. The time-base triggers on the leading edge of the input pulse regardless of its polarity. The gate period is independent of the TRIGGER pulse width.

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INPUT DESCRIPTION (Continued)

OR is a negative NIM logic input which is configured with program jumpers. The OR input is always logically OR'ed with the time base output. Assuming a quiescent time-base, the GATE output width is equal to the OR input width. A program jumper enables an alternate OR mode in which the OR input also triggers the time-base. This mode produces a GATE output equal to the width of the OR input or the preset time whichever is greater. An additional jumper allows OR to be a high impedance or 50 ohms. Note that the high impedance input OR allows multiple channels or multiple modules to be triggered from a single output.

The TRIGGER pushbutton offers two operating modes for manual triggering. A single output is executed by pushing and releasing the switch in less than 0.5 seconds. This produces a single trigger pulse. Retrigger mode is executed by pushing and holding the switch for more than 0.5 seconds.

In the bistable mode, the channel is triggered or set and remains in that state until reset by the negative NIM compatible RESET input or the RESET pushbutton. The TRIGGER and OR inputs are inhibited from setting the channel when RESET is present. The RESET input is enabled only in the bistable mode.

INHIBIT is a negative NIM compatible input. All outputs are forced to their quiescent state whenever INHIBIT is present. GATE transitions resulting from INHIBIT do not generate DELAY outputs.

A special feature of the Model 794 is the analog PROGRAMMING input. Enabled by program jumpers, each input accepts 0 to +10 Volt levels and produces a 5% to 105% adjustment of the selected range. The analog voltage is received differentially to relieve the noise and common mode offsets associated with long cable runs.

OUTPUT DESCRIPTION

Each channel has five (5) outputs. GATE, $\overline{\text{GATE}}$, and DELAY are negative NIM current source outputs governed by the trigger rules described above. TTL is a TTL compatible output which can be assigned to either the GATE or DELAY function. A second jumper associated with TTL provides a true or complement feature. ECL is a differential ECL output conforming to CERN note EP 79-01 and is jumper programmed to be identical to either GATE or DELAY.

BIN GATE DESCRIPTION

The model 794 is capable of driving the bin gate of the host bin. A switch mounted on the rear panel enables or disables the BIN GATE feature. Individual channels are selected to supply this gate signal via program jumpers. More than one channel may be selected resulting in a Bin Gate which is the logical OR of the selected channels.

MANUAL CONTROL SUMMARY

Range Switch

A ten position rotary switch selects one of eight full scale times for the monostable mode. The remaining two positions are for bistable mode. RANGE positions are: 1μSec, 10 μSec, 0.1 mSec, 10 mSec, 0.1 Sec, 10 Sec, and two FF positions.

Trigger Pushbutton

Provides a manual trigger function. Single trigger mode is implemented by pressing and releasing in less than 0.5 seconds. Retrigger mode is implemented pressing and holding for more than 0.5 seconds.

Reset Pushbutton

Provides a manual reset function.

MANUAL CONTROL SUMMARY (Continued)

Time Vernier Potentiometer

Adjusts the monostable time-base form approximately 5.0% to 105.0% of the selected range in local programming mode. The potentiometer is disabled in remote programming and bistable modes.

Delay Width

Adjusts the width of the delay output from 10 nSec to 100 nSec.

INPUT CHARACTERISTICS

All inputs are LEMO style connectors. Negative NIM Inputs are 50 ohms, LOGIC 0 = ±1 mA; LOGIC 1 = -14 mA to -18 mA.

TRIGGER : A high impedance for positive logic levels. Positive LOGIC 0 less than 0.5 V; LOGIC 1 greater than 1.5 V. Negative NIM for negative logic levels.

OR : Negative NIM when jumpered as 50 ohm impedance. For high impedance; LOGIC 0 = ±50 mV; LOGIC 1 = -0.7 to -0.9 V.

OR is shipped as high impedance input OR.

INHIBIT : Negative NIM input.

RESET : Negative NIM input. Enabled only in bistable mode.

ANALOG PROGRAM : A high impedance, differential, analog input.
Maximum input voltage: Differential = -6 V to +12 V
Common Mode = ±6 V

Recommended Input Voltage: Differential = 0 to +10.0 V
Common Mode = ±0.5 V

OUTPUT CHARACTERISTICS

ECL is a two pin header, 0.025" posts on 0.1" centers. All other outputs are LEMO style connectors. Negative NIM outputs are current source type, LOGIC 0 = 0 mA typ. LOGIC 1 = -16 mA typ.

GATE : Negative NIM output.

$\overline{\text{GATE}}$: Negative NIM output. The complement of GATE.

DELAY : Negative NIM output.

TTL : A TTL compatible output. LOGIC 1 = 2.7 V, min. @ 45 mA maximum, LOGIC 0 = 0.5 V maximum @ -100 mA maximum. TTL is jumper selected to be GATE, DELAY or their complements.

TTL is shipped as GATE.

ECL OUTPUTS : A differential 100 ohm line driver. Jumper selected as GATE or DELAY.

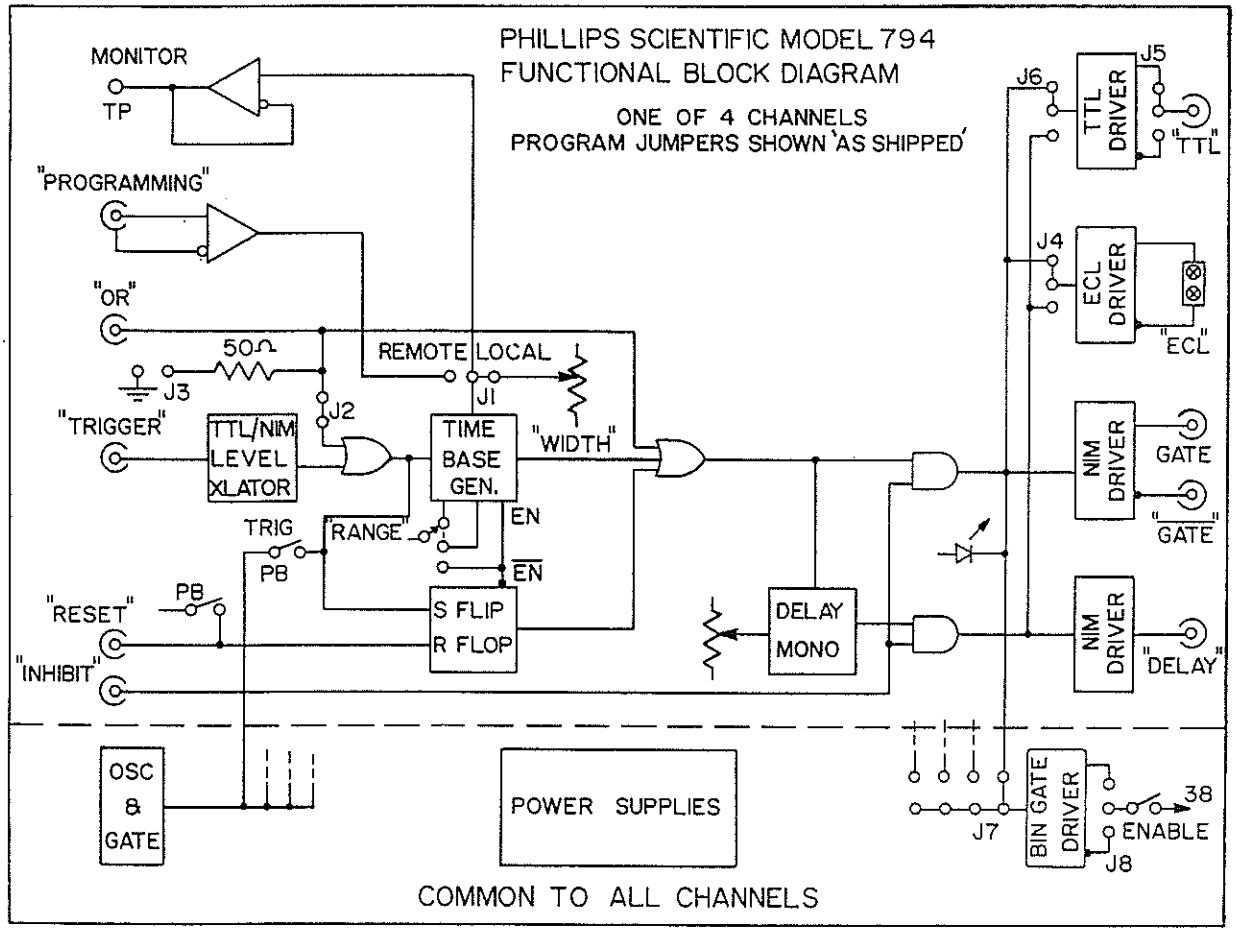
ECL + : Quiescently LOGIC 0 = -1.7 V, typ. LOGIC 1 = -0.90 V typ.

ECL - : Quiescently LOGIC 0 = -0.90 V typ. LOGIC 1 = -1.7 V typ.

ECL is shipped as GATE.

PERFORMANCE SUMMARY

Propagation Delay	:	TRIGGER to: GATE = 11 nSec max. TTL = 20 nSec max. ECL = 11 nSec max.	RESET to: GATE = 11 nSec max. TTL = 20 nSec max. ECL = 11 nSec max.
		OR to: GATE = 8 nSec max. TTL = 15 nSec max. ECL = 8 nSec max.	INHIBIT to: GATE = 6 nSec max. TTL = 15 nSec max. ECL = 8 nSec max.
Dead Time	:	The channel may be triggered immediately upon the completion of the GATE logic 1 to logic 0 transition.	
Time Jitter	:	Less than 0.03% of range.	
Temperature Range	:	0°C to 70°C ambient.	
Temperature Stability	:	Less than 400 ppm/°C from 20°C to 50°C.	
Power Supply Rejection:		GATE width will not change by more than 0.04% of setting for a ±5% change in any power supply.	
Power Supply Requirements	:	- 6V @ 400 mA -12V @ 165 mA -24V @ 85 mA	+ 6 V @ 325 mA +12 V @ 0 mA +24 V @ 75 mA



5/93

Hall A

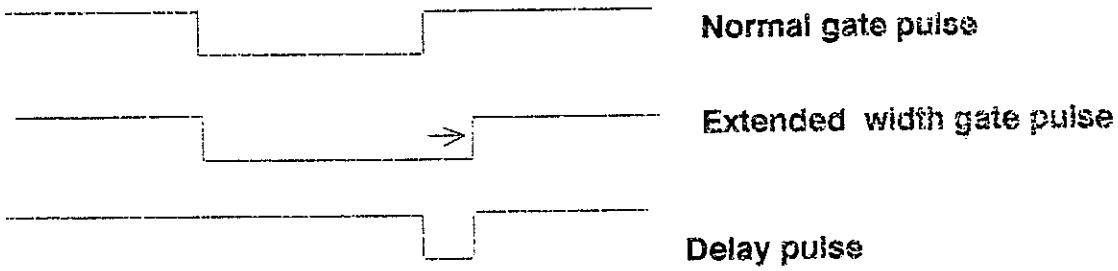
Model # 794 Quad Gate/Delay Unit

Serial No. 12585

WITH NEW EXTENDED WIDTH JUMPER OPTION IN EACH CHANNEL

Jumper (JE) not installed - Normal gate width, delay occures after gate pulse

Jumper (JE) installed - Gate width is extended to include delay width



This unit has been shipped ✓ with jumpers installed / without jumpers installed

(User may change jumper settings)

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MOD. 794 GATE/DELAY UNIT QC CHECK-OFF

DATE: 8-17-93 S/N: 12585

TECH: Nayana ECO: 2002

MODIFICTIONS: _____

TEST	CH. A	CH. B	CH. C	CH. D	UNITS
DELAY O/P	✓	✓	✓	✓	
GATE O/P	✓	✓	✓	✓	
/GATE O/P	✓	✓	✓	✓	
TTL GATE	✓	✓	✓	✓	
/TTL GATE (J5)	✓	✓	✓	✓	
TTL DELAY (J6)	✓	✓	✓	✓	
/TTL DELAY(J5)	✓	✓	✓	✓	
ECL GATE	✓	✓	✓	✓	
/ECL GATE	✓	✓	✓	✓	
ECL DELAY (J4)	✓	✓	✓	✓	
BIN GATE (J7)	✓	✓	✓	✓	
/BIN GATE (J8)	✓	✓	✓	✓	
FF TRIG. PB	✓	✓	✓	✓	
FF RESET PB	✓	✓	✓	✓	
FF TRIG I/P	✓	✓	✓	✓	
INHIBIT I/P	✓	✓	✓	✓	
RESET I/P	✓	✓	✓	✓	
O/P "OR"(J2)	✓	✓	✓	✓	
INP. "OR"(J2)	✓	✓	✓	✓	

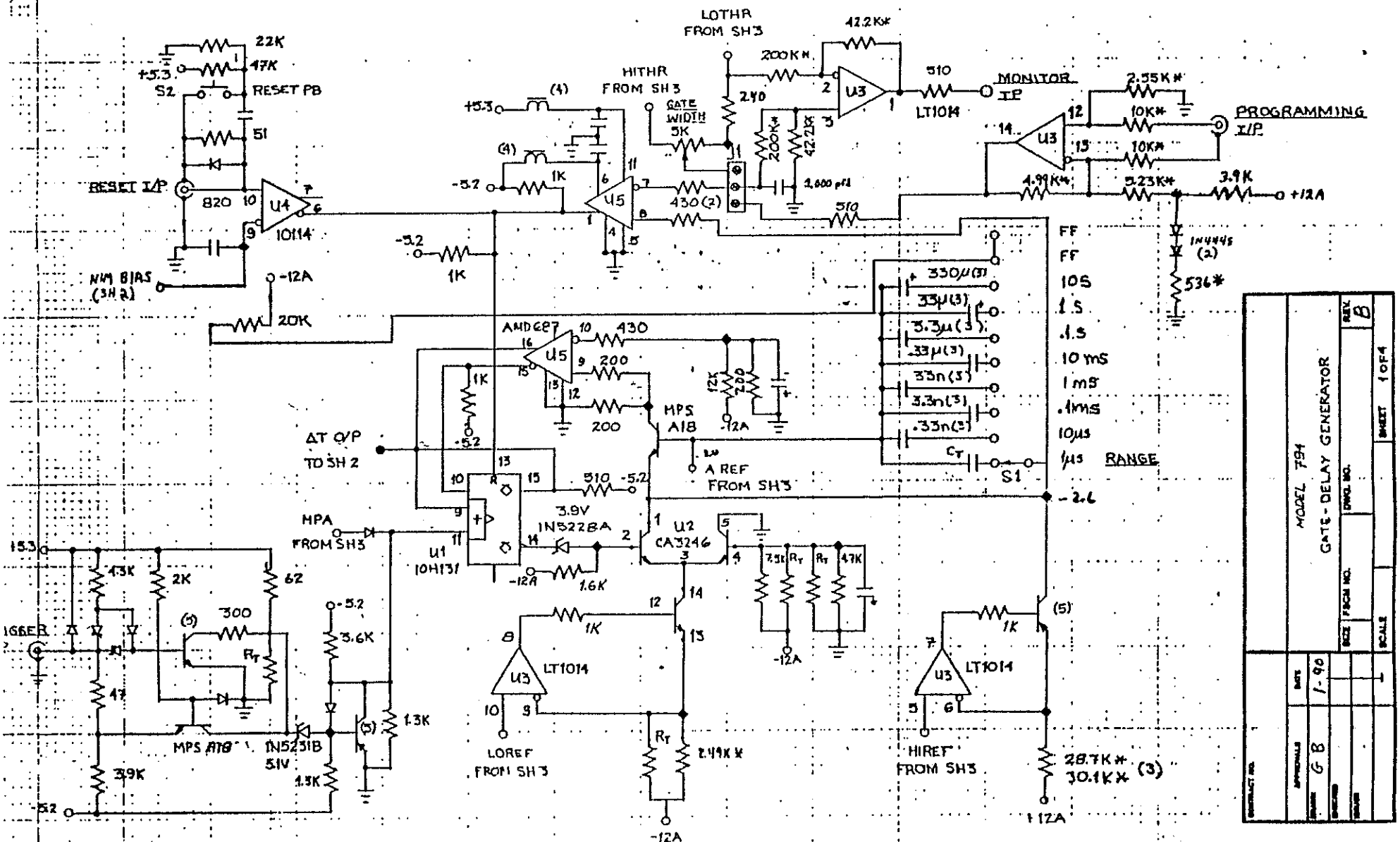
MODEL 794 CALIBRATION CHECK-OFF

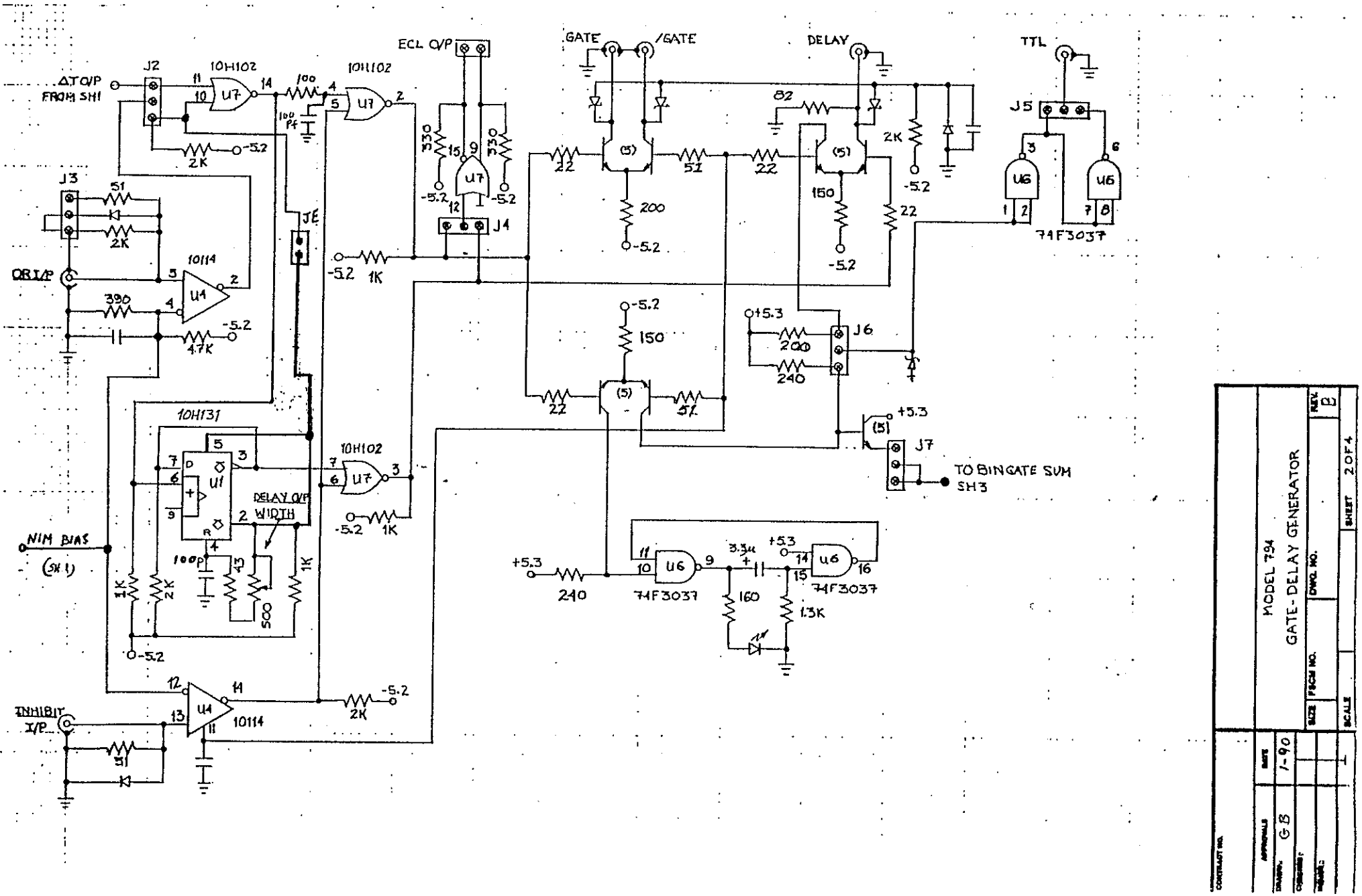
DATE: 8-17-93 S/N: 12585

TECH: Ndyand ECO: 2002

MODIFICTIONS: _____

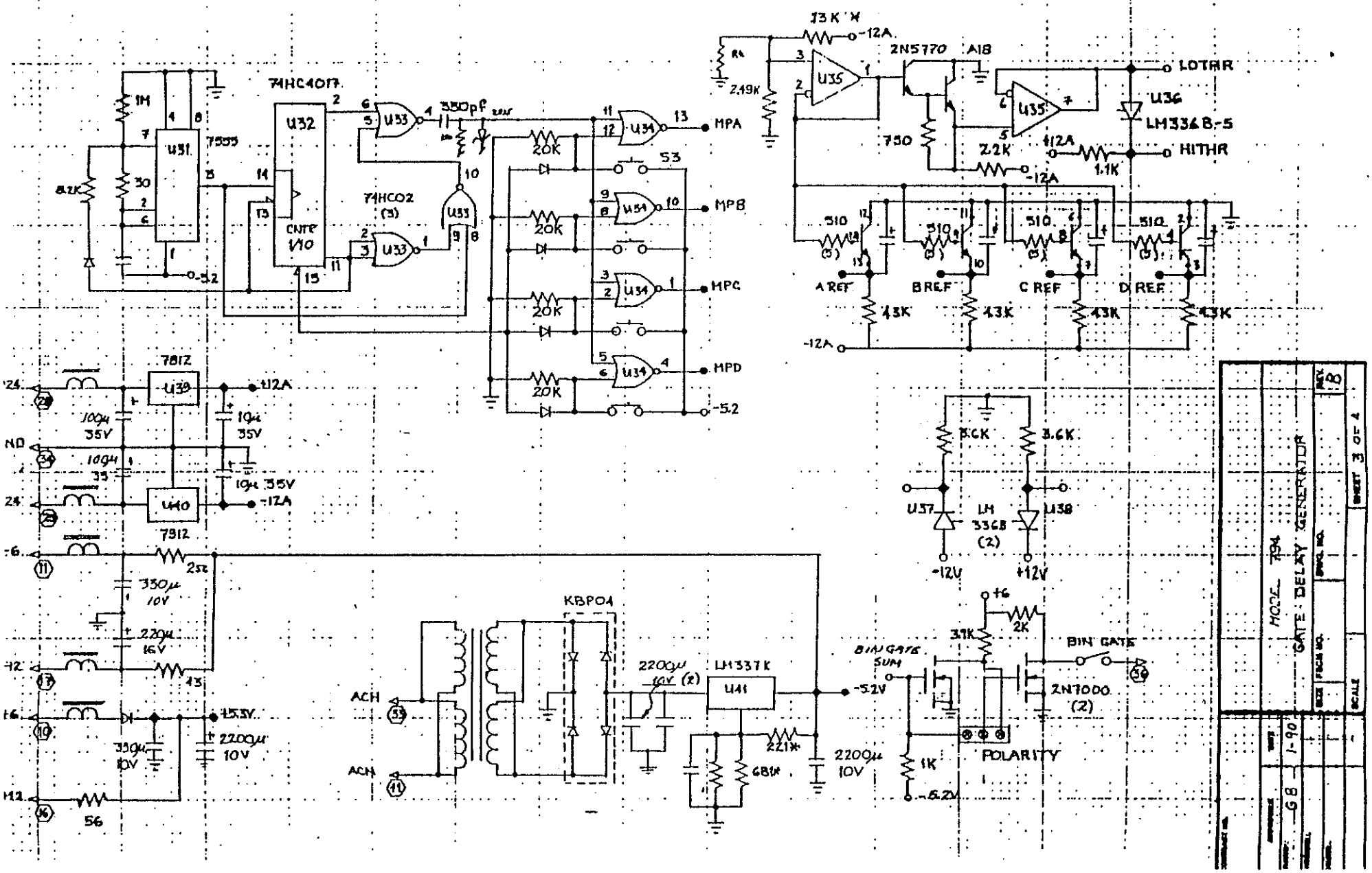
JUMPER ASS'Y	CH. A	CH. B	CH. C	CH. D	LOCATION
J1 LOC./REMO.	✓	✓	✓	✓	LOC.
J2 I/P O/P OR	✓	✓	✓	✓	INP.
J3 50/2Kohm	✓	✓	✓	✓	2 Kohm
J4 ECL G/DEL	✓	✓	✓	✓	GATE
J5 TTL NOR/COM	✓	✓	✓	✓	NORM.
J6 TTL G/DEL	✓	✓	✓	✓	GATE
J7 BIN E/D	✓	✓	✓	✓	DISABLED
J8 BIN NOR/COM	✓	✓	✓	✓	NORM.


LOTHR FROM SH3
42.2K*
200K*
HITHR FROM SH3
GATE WIDTH 5K
240
510
MONITOR I/P
LT1014
2.55K*
10K*
PROGRAMMING I/P
10K*
4.99K*
5.23K*
3.9K
+12A
22K
47K
+5.3
S2
RESET PB
51
RESET I/P
820
U4
10114
NM BIAS (3H2)
-12A
20K
1K
-5.2
200K*
42.2K*
1,600 pfd
430 (2)
510
536*
1N4445 (2)
330μ(3)
33μ(3)
3.3μ(3)
.33μ(3)
33n(3)
3.3n(3)
.33n(3)
CT
S1
FF
FF
10S
1 S
.1 S
10 mS
1 mS
.1mS
10μS
1μS RANGE
-2.6
AMDEB7
430
200
12K
MPS A18
ΔT O/P TO SH 2
A REF FROM SH3
510
3.9V
1N5228A
1.6K
MPA FROM SH3
U1
10H131
U2
CA3246
3.5K
47K
LT1014
LOREF FROM SH3
HIREF FROM SH3
28.7K* 30.1K* (3)
+12A
MODEL 794
GATE-DELAY GENERATOR
REV. B
SHEET 1 OF 4
DWG. NO.
SIZE
FSCM NO.
SCALE
DATE 1-96
APPROVALS
DRAWN G B
CHECKED
ENGINEER
ISSUED
PRODUCT NO.



MODEL 794
GATE-DELAY GENERATOR

CONTRACT NO.				REV. D	
			DWG. NO.		SHEET 2 OF 4
			SIZE	FSCM NO.	SCALE
	APPROVALS	DATE			
	DRAWN G.B	1-90			
	CHECKED				
	ENGR				
	MFGR				

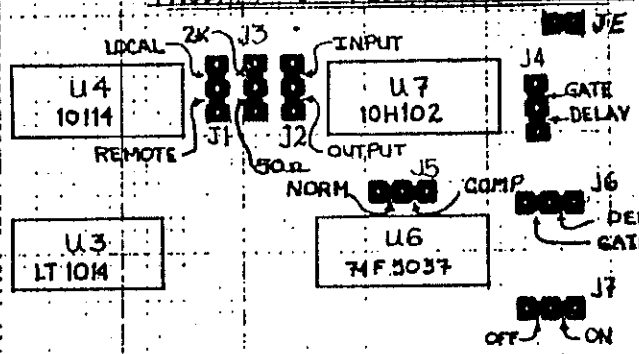

74HC4017
U32
U31
7555
1M
8.2K
30
CNTR 1/10
74HC02 (3)
U33
350pf
MPA
MPB
MPC
MPD
S3
20K
-5.2
13K W
-12A
2N5770
A18
U35
Z.19K
750
2.2K
1.1K
+12A
LOTHR
HITHR
U36
LM336B-5
510
A REF
B REF
C REF
D REF
43K
7812
U39
7912
U40
+12A
-12A
100µ 35V
10µ 35V
2Ω
330µ 10V
220µ 16V
43
56
+5.3V
2200µ 10V
KBP04
ACH
ACN
2200µ 10V (2)
LM337K
U41
221K
681
8.6K
U37
U38
LM 336B (2)
-12V
+12V
+6
2K
3.3K
BIN GATE SUM
BIN GATE
2N7000 (2)
POLARITY
1K
-6.2V
-5.2V
HOZ 754 GATE DELAY GENERATOR
SHEET 3 OF 4
1-90
G8

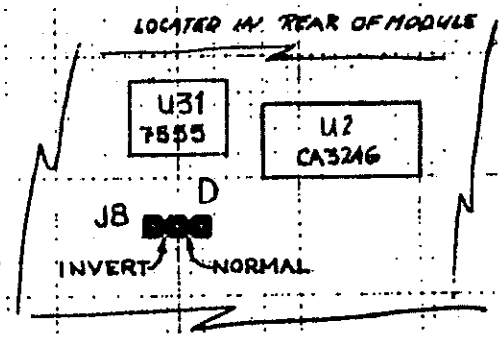
DEVICE	DESIGNATION	+5.2	-5.2	+12R	-12R	GND
10114	U4		8			1,16
10H102	U7		8			1,16
10H131	U1		8			1,16
74F3037	U6	13,12	1			4,5
74HC02	U33, U33		7			14
74HC4017	U32		8			16
7555	U31		4			8
AM687	U5	11	6			3,14
LF412	U35			8	4	
LT1014	U3			4	11	

NOTES

1) RESISTORS ARE 1/8 W. CF UNLESS OTHERWISE SPECIFIED
2) UNMARKED CAPS ARE 0.1μF MONO
3) INDICATES A SELECTED COMPONENT
4) 3.9μH BEAD W/ 2 TURNS OF #26 WIRE
5) INDICATES SURFACE MOUNT COMPONENT
6) * - INDICATES 1/3 W. CF, 1% RESISTOR
7) ⬡ = NIM BLOCK PIN

PROGRAM JUMPER CONFIGURATION



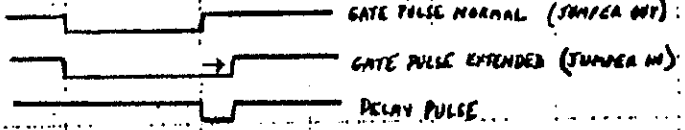


PROGRAM JUMPER SUMMARY

J1 SELECTS GATE WIDTH CONTROL VIA THE FRONT PANEL POT OR REAR PANEL PROG. INPUT
J2 SELECTS "INPUT OR" MODE OR "OUTPUT OR" MODE
J3 SELECTS 50 OHM OR 'HI Z' 'OR" INPUT
J4 ASSIGNS "ECL" OUTPUT TO GATE OR DELAY
J5 ASSIGNS "TTL" OUTPUT TO NORMAL OR COMPLEMENT
J6 ASSIGNS "TTL" OUTPUT TO GATE OR DELAY
J7 CONNECTS THE CHANNEL TO THE 'BIN GATE' DRIVER
J8 SELECTS 'NORMAL' OR INVERTED" BIN GATE

JE EXTENDED WIDTH JUMPER

JUMPER OUT - NORMAL GATE WIDTH (DELAY PULSE OCCURES AFTER GATE WIDTH)
JUMPER IN - GATE WIDTH IS EXTENDED TO INCLUDE DELAY WIDTH



MODEL 794
GATE - DELAY GENERATOR
SIZE B
SHEET 4 OF 4
DWG. NO.
FSCM NO.
SCALE
DATE 1-90
DRAWN GB