PME PIO-1
Manual

Rev. 1

Issue 3

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Radstone Technology PLC
Water Lane,
Towcester,
Northants.,
NN12 6JN

Telephone: 0327 359444
Facsimile: 0327 359662
Telex: 31628 RADSTN G

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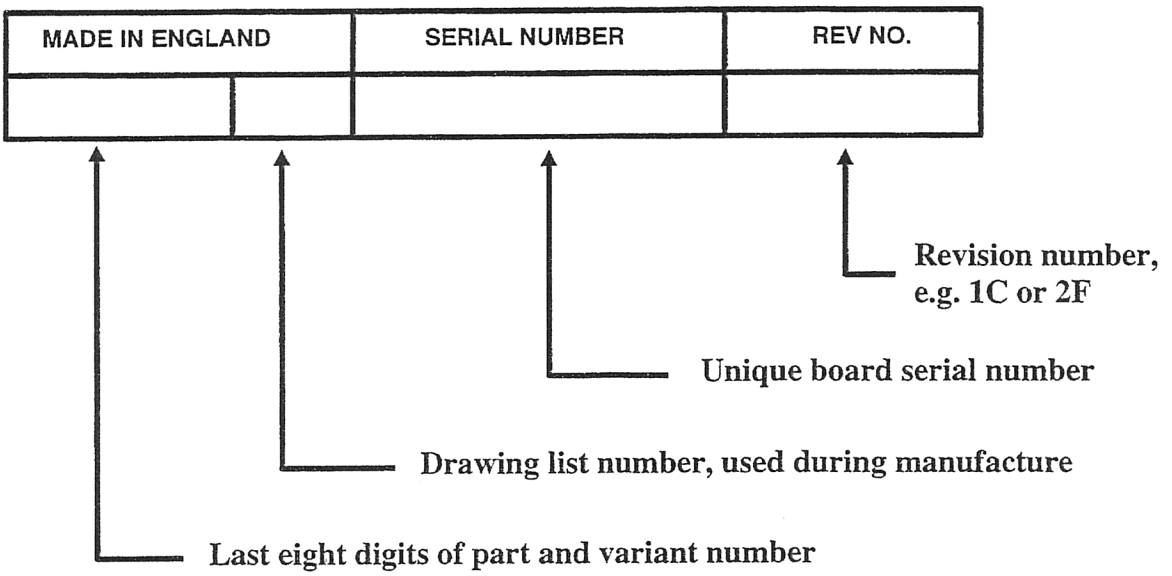
Board Identification

Radstone PME boards are identified by a label fitted to the component side of the board.



This publication describes the PME PIO-1 at revision state Rev. 1 (all letter codes).

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Chapter 1 - Introduction

This manual describes the features and functions of the PIO-1 Parallel I/O board. Throughout the text, this manual adopts the following conventions:

1) An asterisk shows an active *low* signal, e.g. DTACK*.

2) A prefix of '0x' shows a hexadecimal address or value, e.g. 0x0F.

3) MSB means most significant bit. LSB means least significant bit.

Overview

The PIO-1 is a highly configurable I/O board providing a direct interface for many VMEbus-based data acquisition and control systems. Typical applications include handling inputs from push buttons, panel switches, pressure switches, proximity and limit switches, photo-detectors and alarm trip switches. The PIO-1 outputs may directly control solenoids, motors, relays, control valves, programmable controllers, indicators, alarms, etc.

To provide the required combination of inputs and outputs at the best possible price, several options are available for the PIO-1. Basic options are 16 or 32 channels user configurable as either input or output. This feature is one that particularly differentiates the PIO-1 from most other boards of this type, which only offer a fixed number of inputs or outputs.

The PIO-1 adopted stringent design rules. These ensure a robust design with a high degree of immunity to the type of electrical interference and vibration found in typical industrial environments.

The PIO-1 has the following features:

- 16 or 32 I/O channels with relay-controlled outputs and opto-coupled inputs
- Trigger mode allows all channels to be switched simultaneously
- VMEbus interrupt generated on change of channel states
- 300V isolation between channels
- 1000V isolation between channels and VMEbus
- Channel connections made via the front panel
- Front panel status display
- VMEbus A24:D16 slave

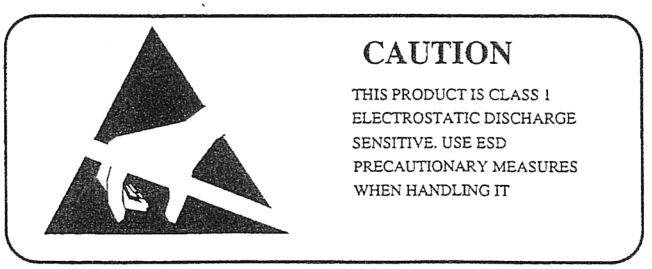
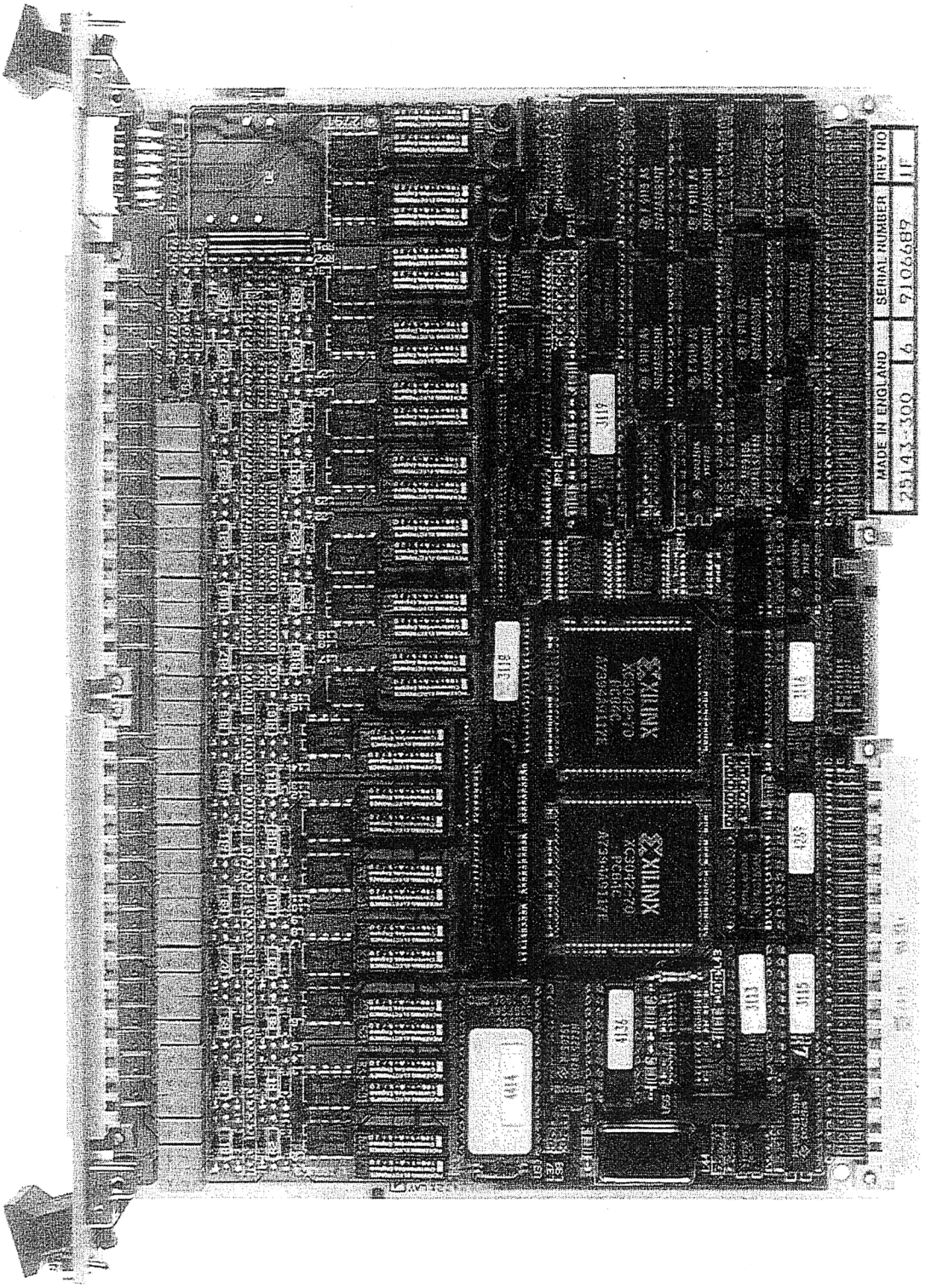


Figure 1. PIO-1 Parallel Input/Output Board



The PIO-1 is available with 16 or 32 channels, and is supplied with channels configured as input/output. Most equipment found in data acquisition and control systems operates with one of four DC voltages: 5, 12, 24 or 48 volts. The PIO-1 input channels can be further configured for either +5, +12, +24 or +48 volt inputs to cope with any of these 'standard' voltages or for detection of external contact closures.

The input circuitry uses an optical coupler, which in fact detects current rather than voltage. The desired operating voltage should be specified at order time, and an appropriate value resistor is then fitted to each input circuit. Plant inputs may often be in 'contact pairs', rather than voltage levels. The PIO-1's optional internal DC/DC converter can be linked to supply a 5V power source to channels detecting remote contact closures. The contact closure detection option is available on channels 17 to 32. On-board resistors between the input lines and the 5V supply provide TTL level generation. They also give 'contact wetting' (i.e. sufficient current flow through the contacts to avoid significant build-up of oxidation).

Plant inputs often include sets of relay contacts that, as they change from one stable state to another, tend to 'chatter' or change state frequently in a short period. This is due to their mechanical properties. Another common problem is pick-up, where electromagnetic interference from a cable induces a signal in other nearby cables. These phenomena can potentially cause false readings at plant inputs. The 'debounce' circuitry on the PIO-1 overcomes this problem by double-sampling each input node, and requires that both samples are equal before accepting them as a valid reading. The parameters for the debounce logic are user configurable via links that allow selection of three different sampling rates: 500, 250 and 50 Hz. When configured as an input board, any change of state in an I/O cell can be polled or can be link-configured to generate a VME interrupt.

Each channel output can be software controlled either individually, or simultaneously with the other channels. Multiple PIO-1s on the same VMEbus backplane can be simultaneously triggered to output.

The I/O signals are brought out to standard DIN41612 connectors on the front panel. The front panel can be single width, for use with a ribbon cable, or double width with a screw terminal connector. The front panel has a matrix of 32 LEDs fitted to act as a channel status indicator. Further indicators are: a Power-on (Ready) indicator, a Trigger mode indicator and an Interrupt mode indicator. For ease of insertion and removal from the VME card frame, the front panel has card-ejector handles fitted.

The PIO-1 operates as a VMEbus A24:D16, D08 (EO) slave. The PIO-1 is double Eurocard size and fully conforms to the VMEbus Specification ANSI/IEEE Std. 1014 - 1987.

Product Codes and Part Numbers

To order a PIO-1, specify the product code, followed by (a list of) the Processor OPtions (POPs) required. The following table shows the product codes:

Product Code	Board Type	Number of Channels
PME PIO-1/300	Input/output	32
PME PIO-1/301	Input/output	16

Chose the required input voltage POP number from the following list:

Input Voltage Range	POP Number
5V DC	2
12V DC	3
24V DC	4
48V DC	5
28 V DC	10

Further POPs can be selected from the following list:

5V DC input power option	POP number 6
Double width front panel option (default single width)	POP number 7

Note: Other variants and POPs are available on request.

Examples

PME PIO-1/300, POP 4 is a 32-channel input/output board with 24V inputs and a single width front panel.

PME PIO-1/301, POP2, POP 6, POP 7 is a 16-channel input/output board with 5V inputs, an internal DC/DC converter for contact-only inputs, and a double width front panel.

Chapter 2 - Specifications

General Specification

I/O channels	Logic Cell Array	50MHz Xilinx XC 3042
	Configuration PROM	32k x 8 EPROM
	Opto-coupler (input)	HCPL 2731
	Reed relay (output)	5V coil (with internal protection diode). 1 normally open or 1 normally closed contact. External magnetic shield
	Fuse	0.75 Amp/channel single in-line socket mounted fuse
	Transient Voltage Suppressor	60V suppressor
Front panel	Status LEDs	A 7 x 5 dot matrix display showing the status of each channel, the Trigger mode indicator, the Interrupt mode indicator and whether the Logic Cell Arrays are being configured (Ready)
	Connectors	Two 32-pin DIN 41612 ribbon cable connectors (using rows a and c even numbered pins) on a single width front panel
		Screw terminal connector on a double width front panel, allowing plant cables to be wired directly
		Two card-ejector handles for easy card removal and insertion into the card frame (only on the single width panel)
DC/DC converter		+5V DC to DC converter with 1000V isolation
VMEbus interface		A24, A16:D16, D08 (EO) slave fully conforming to ANSI/IEEE Std. 1014 - 1987
Power requirements		+5V @ 2.3A (typical) 32 relays active = 3.0A
Weight		0.7 kg

Environmental Specification

Operating Environment

The PIO-1 will operate under the following conditions:

Temperature range: 0 to +55°C ambient air temperature

Cooling requirement: A linear airflow of 2.5 meters/second (8.5 feet/second) across the board is recommended

Relative humidity: Up to 95% without condensation

Thermal shock: ±5°C/minute

Altitude: -300 to +3,000 metres (-1000 to +10,000 feet approximately)

Vibration: 10 to 100 Hz with 2g acceleration

Mechanical shock: 20g for 6ms (half sine) when mounted in a suitable racking system

Storage Environment

The PIO-1 may be stored or transported without damage within the following limitations:

Temperature range: -40 to 85°C

Relative humidity: Up to 95% without condensation

Thermal shock: ±10°C/minute

Altitude: -300 to +16,000 metres (-1000 to +50,000 feet approximately)

Vibration: 10 to 500 Hz with 2g acceleration

Mechanical shock: 20g for 6ms (half sine)

Mean Time Between Failures (MTBF)

The following table shows the calculated MTBF for the PIO-1 variants. The failure rates used in this calculation were derived from the British Telecom Reliability Handbook HRD3 with MIL-HDBK-217D and in-house data.

Variant	MTBF (Hours)
/100 (32 output only channels) *	38, 915
/101 (16 output only channels, open contacts) *	69, 632
/103 (16 output only channels, closed contacts)*	69, 632
/200 (32 input only channels) *	203, 747
/201 (16 input only channels) *	251, 183
/300 (32 input/output channels)	37, 820
/301 (16 input/output channels)	66, 929

* = Only available on request

Mechanical Specification

The PIO-1 is constructed on a multi-layer double Eurocard printed circuit board and conforms to the dimensions specified in ANSI/IEEE Std. 1014 - 1987. Some ICs are stacked. Dimensions shown below are in millimeters, with inches (in parentheses) for reference only.

Figure 2. VME Dimensions

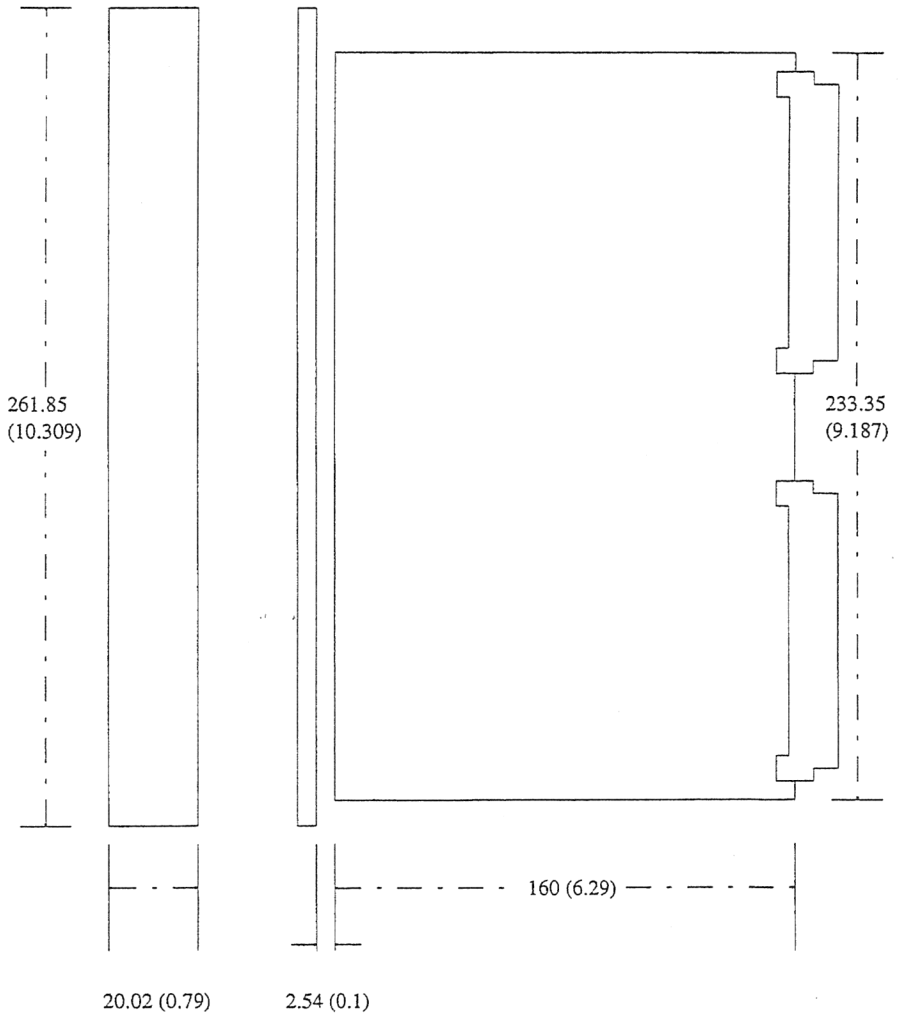


Figure 3. PIO-1 Single Width Front Panel

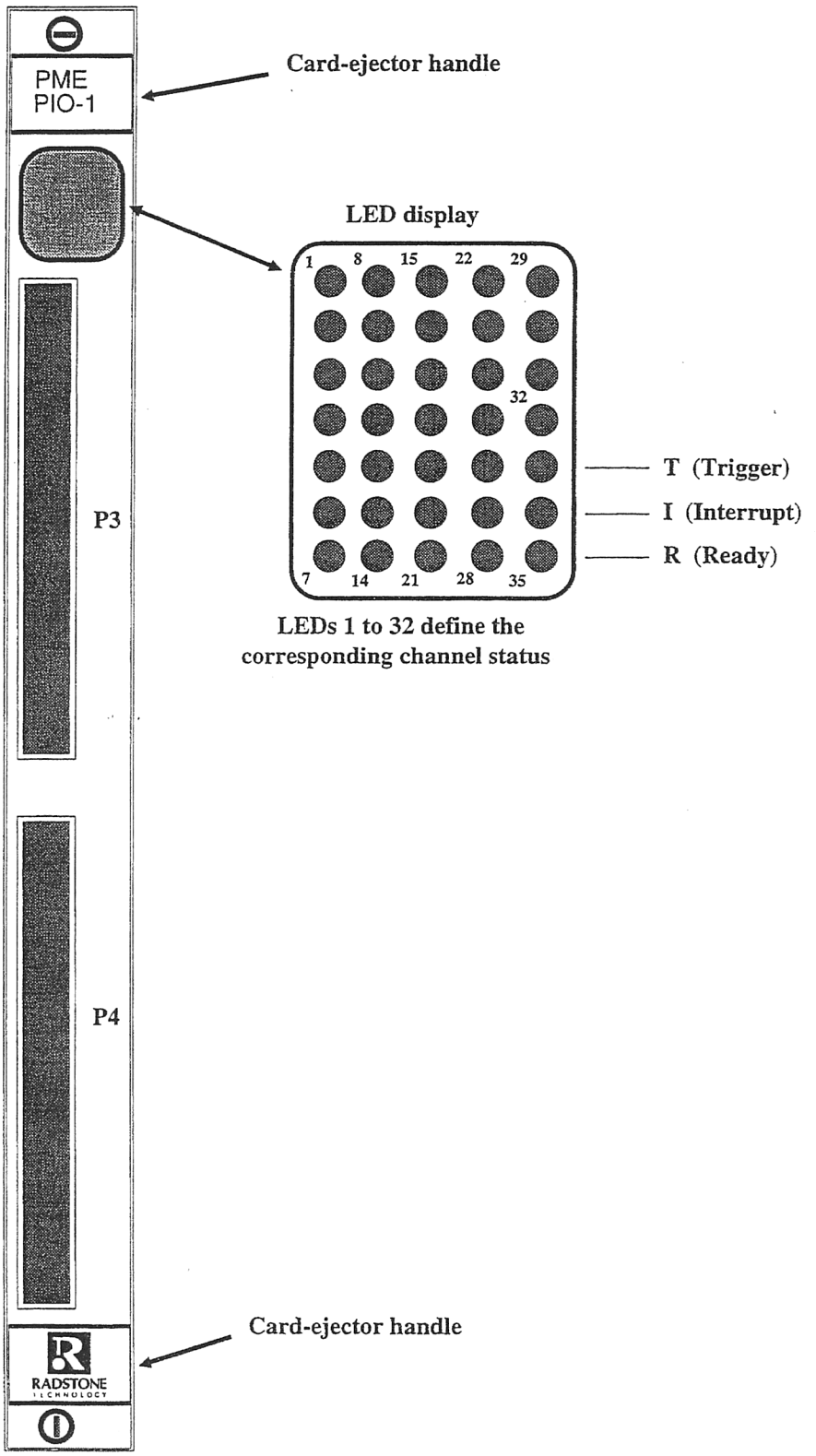
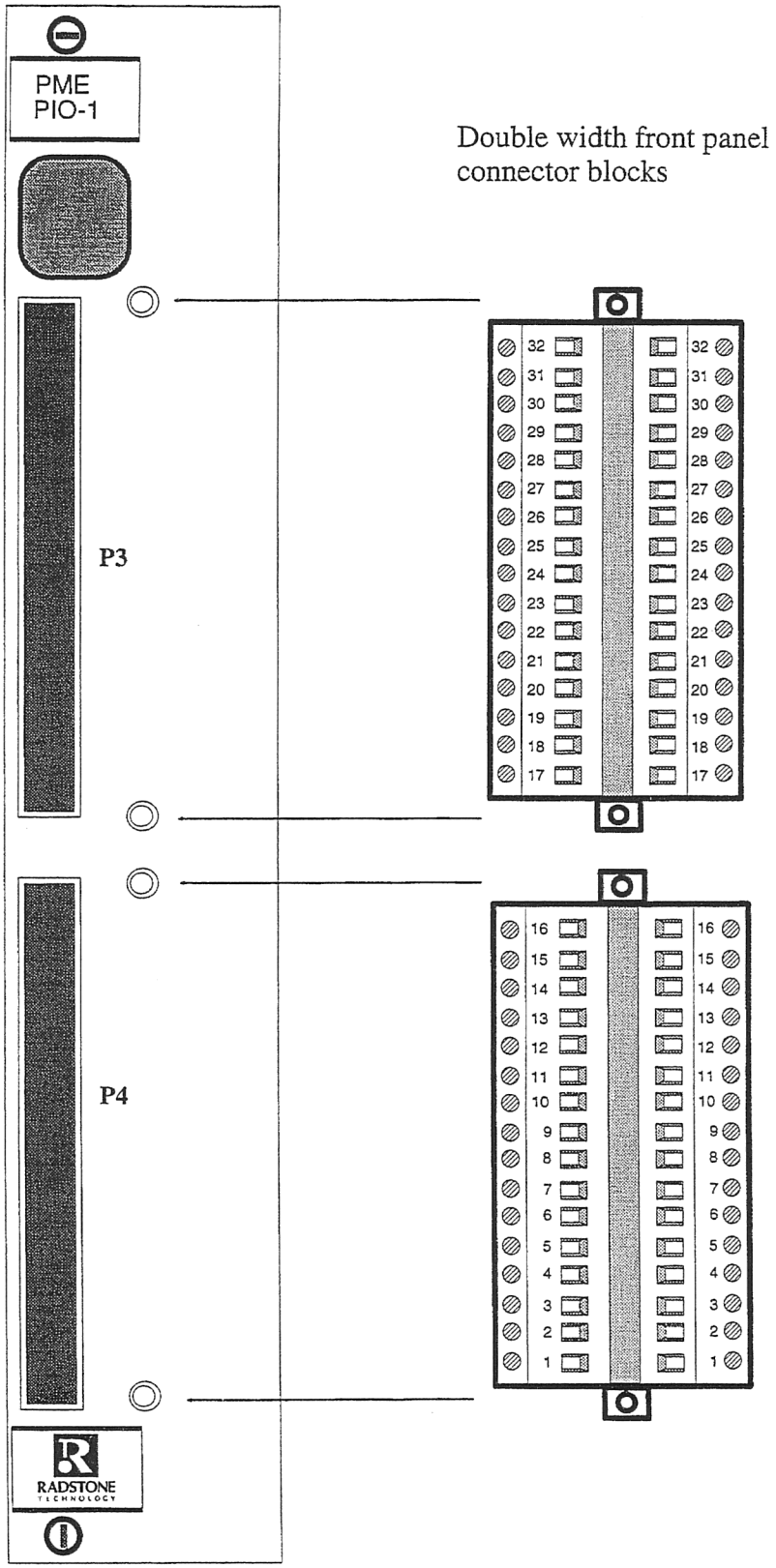


Figure 4. Double Width Front Panel



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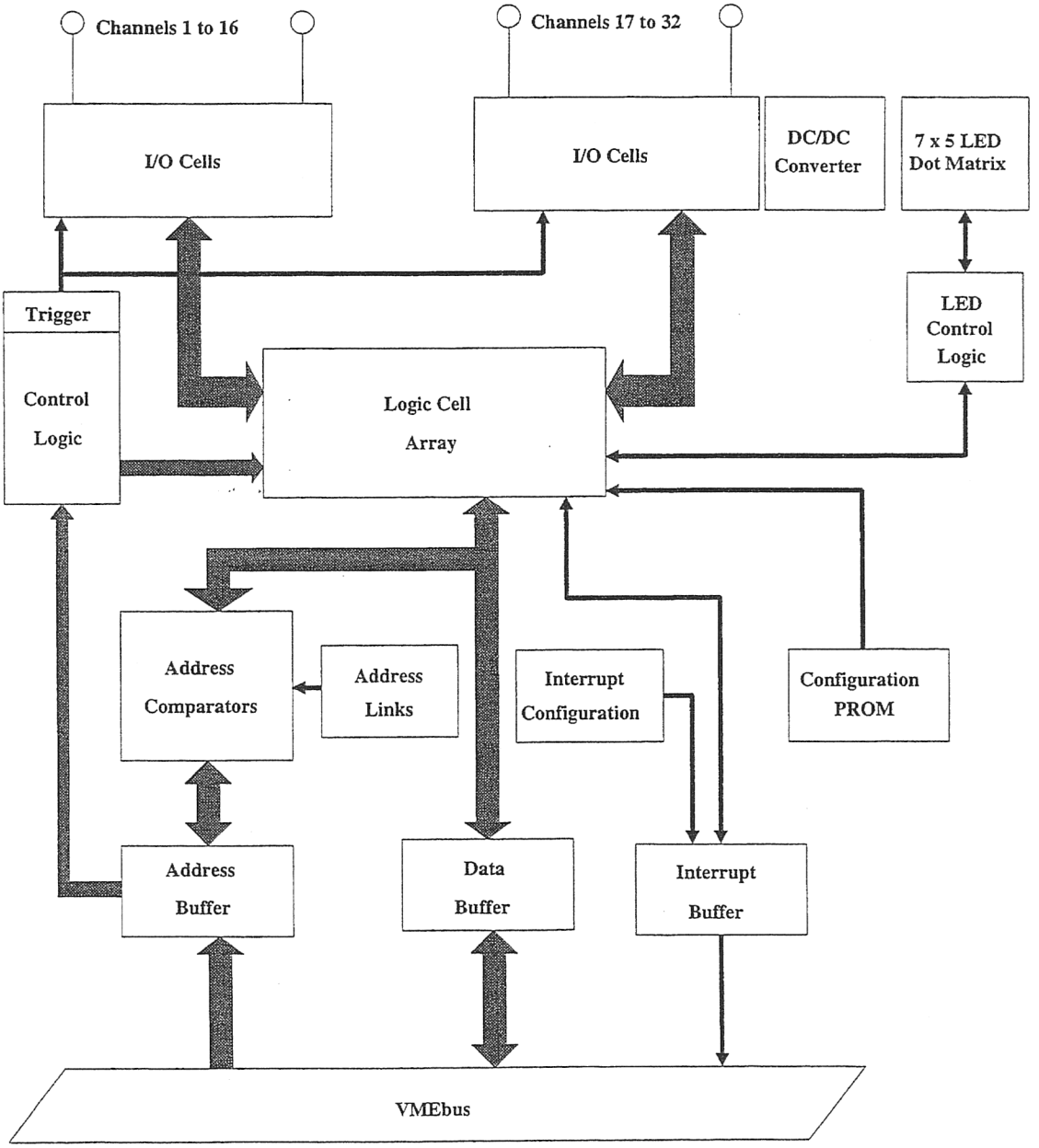
Chapter 3 - Functional Description

This chapter describes the PIO-1's functional operation.

Figure 5. PIO-1 Block Diagram



PIO-1 Addressing

Following a VME reset, the PIO-1 responds to A16/D16 VMEbus cycles. A Host processor configures the PIO-1 to the required mode of operation. The A16 base address is link-configured on delivery. Links LK41 and LK42 set the Address Modifier (default 0x2D - VME Short I/O Address Space) while links LK33 and LK34 configure the Address lines A08 to A15 (default 0xFFEExx). Once the PIO-1 is up and running, you can dynamically reposition the PIO-1's base address by writing to the two Global Address registers (identified below). The "Software Interface" section of this chapter gives a more detailed description of the memory mapping for the PIO-1. Offsets from the base address give locations for the registers listed below:

Offset	Register
0x00	Card type
0x01	Population
0x02	Revision state
0x03	Not used
0x04	Global Address A08 to A15
0x05	Global Address A16 to A23
0x06	Not used (Global Address A24 to A31)
0x07	Global Address Modifiers (AM00 to AM05)
0x08 to 0x0B	Not used
0x0C	Interrupt level
0x0D	Interrupt vector
0x0E and 0x0F	Not used
0x10	Global Trigger Address A08 to A15
0x11 and 0x12	Not used
0x13	Global Trigger Address Modifiers

Card Type (Offset 0x00)

This read-only register identifies the type of board within the Radstone I/O range.

Population (Offset 0x01)

This read-only register defines the PIO-1's population (number of channels) and the channels' configuration (output or input and input voltage). This register is set up using links LK39 and LK40. These links are factory set to suit the variant ordered (see Chapter 4 - Configuration).

Revision State (Offset 0x02)

This read-only register defines the PIO-1's revision state. This register is set up using links LK35 and LK36. These links are factory set to suit the PIO-1's revision state at the time of manufacture and so no absolute default values can be supplied in this manual. After initial installation, you can use LK35 and LK36 as a special read-only register for whatever purpose you require (see Chapter 4 - Configuration).

Global Address Registers (Offset 0x04 to 0x06)

These write-only registers dynamically configure the PIO-1's base address on a 256-byte boundary in the VME A24 Global Address space. Address lines A24 to A31 are not used in this configuration.

Global Address Modifiers (Offset 0x07)

This write-only register dynamically sets up the PIO-1's Address Modifier (AM) code. Data bits 00 to 05 correspond to AM codes AM00 to AM05. Writing to this location enables standard (A24) address mode, so write to this I/O port last.

Interrupt Level (Offset 0x0C)

This register defines whether, and at what level, the card generates an interrupt on a change of state of an input channel, as the following table shows:

Contents	Meaning
00	Interrupts disabled (default)
01	Level 1
02	Level 2
03 07	Level 3 . . Level 7

Interrupt Vector (Offset 0x0D)

This write-only register gives the interrupt vector address when the PIO-1 is configured to interrupt.

Global Trigger Address (Offset 0x10)

This write-only register defines Trigger Address bits A08 to A15. Global Address bits A16 to A23 (offset 0x05) define Trigger Address bits A16 to A23. Trigger Address bits A00 to A07 are 'don't care' (not decoded).

If multiple PIO-1s in the same VME rack have the same trigger address, then an access to this address triggers all the PIO-1s to operate simultaneously. This is similar to an address broadcast. See the following section for how to enable/disable Trigger Mode and Chapter 4 for details of LK43, the Trigger/DTACK* link.

Global Trigger Address Modifiers (Offset 0x13)

Data bits 00 to 05 of this write-only register correspond to Address Modifier codes AM00 to AM05 when defining the cycle type during accesses to the Global Trigger Address register. Data bit 07 is the Trigger Mode control bit (logic 1 = Trigger Mode enabled).

I/O Cell Configuration

Addressing the Global Address register with the appropriate offset, using A01 to A07, defines the I/O cells' configuration. The following table lists the registers and offsets:

Offset	Register
0x00	Data channels 09 to 16
0x01	Data channels 01 to 08
0x02	Data channels 25 to 32
0x03	Data channels 17 to 24
0x04 to 0x07	Not used
0x08	Interrupt Status channels 09 to 16
0x09	Interrupt Status channels 01 to 08
0x0A	Interrupt Status channels 25 to 32
0x0B	Interrupt Status channels 17 to 24
0x10	Interrupt Mask channels 09 to 16
0x11	Interrupt Mask channels 01 to 08
0x12	Interrupt Mask channels 25 to 32
0x13	Interrupt Mask channels 17 to 24

Data Registers (Offset 0x00 to 0x03)

Writing to these registers controls the corresponding output relays. Logic 0 releases the relay and logic 1 operates the relay, depending on the Trigger Mode control bit (see the Global Trigger Address Modifiers section). Reading from these registers shows the opto-coupler's state for the corresponding channels. Logic 1 shows that the opto-coupler is on and logic 0 shows that the opto-coupler is off.

Interrupt Status Registers (Offset 0x08 to 0x0B)

If there is a change detected in an I/O cell and the PIO-1 is configured to generate an interrupt, then these read-only registers record the interrupt. At any time, any or all of the channels can detect a change, but only one interrupt is generated on the VMEbus. Once an interrupt has been serviced, the corresponding register is read and then reset ready for the next change. Since these registers record all the changes, this method ensures that no interrupts are missed. If there is a change detected after an interrupt service routine has started, then it is stored until after the register has been reset. A new VMEbus interrupt is then generated, and the bit set in the appropriate register.

Interrupt Mask Registers (0x10 to 0x13)

These write-only registers define whether a channel should interrupt on a change of state in an I/O cell and if so, on what conditions. Each channel can be programmed independently. The interrupt mask requires two write accesses to program it: the first access defines the LSB and the second defines the MSB.

Contents	Meaning
00	Do not interrupt
01	Interrupt on a low to high transition
10	Interrupt on a high to low transition
11	Interrupt on any transition

Logic Cell Array

The Logic Cell Array (LCA), with links LK35 and LK36 and the Configuration EPROM, defines the PIO-1's configuration. This is the number and functions of the I/O channels, and the input voltage. A configuration program, held in EPROM and loaded into static memory cells in the device at power-up, configures the LCA's logic functions and interconnections.

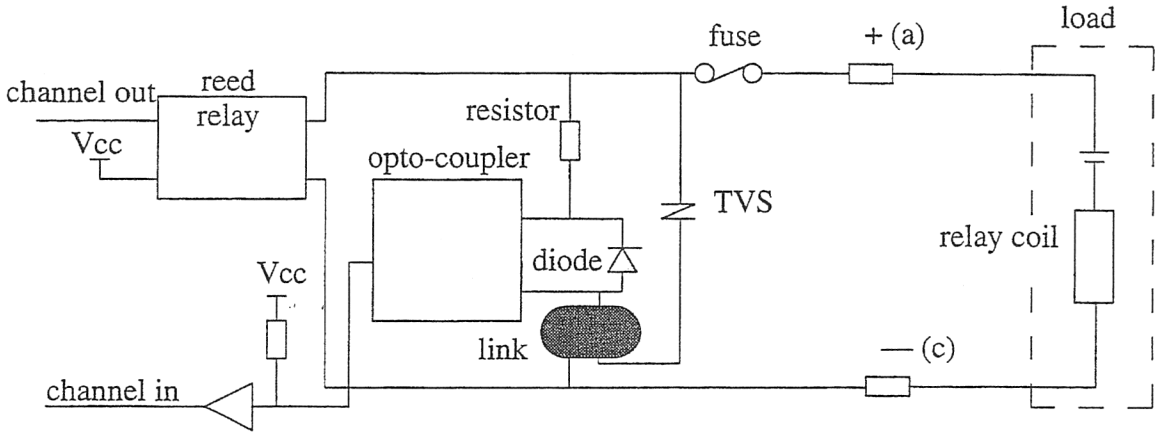
I/O Cells

Radstone configures all cells as input/output. You can then configure each cell as:

Input (with or without self power)
Output (monitored or not)

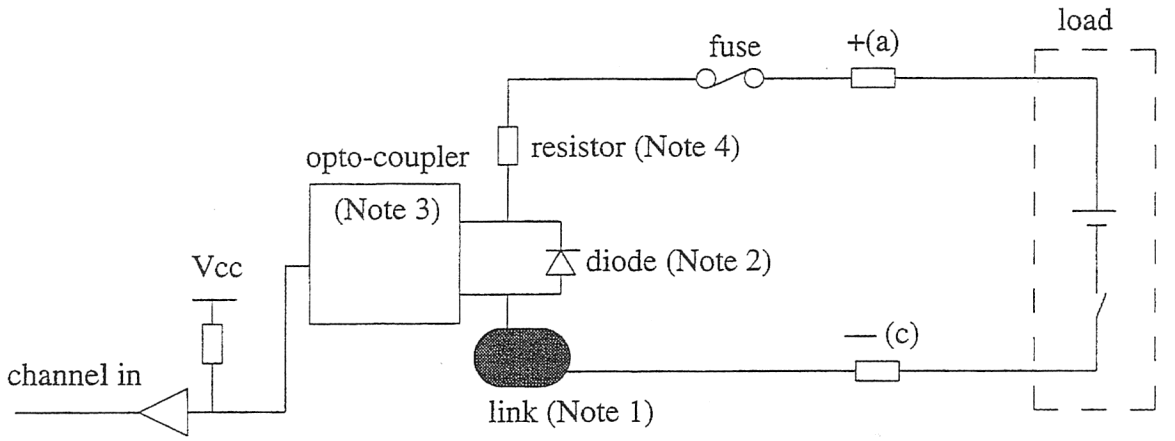
Channels 1 to 16 have two pin links, which are connected (pin 1 to pin 2) or not as required. Channels 17 to 32 can be linked in several positions (pin 1 to pin 2, pin 2 to pin 3, etc.). Figure 10 in Chapter 4 identifies the pin number layout.

Figure 6. Input/Output Circuit



To configure the cells as inputs, see Figure 7 (or Figure 8 for self powered input).
To configure the cells as outputs (monitored or not), see Figure 9.

Figure 7. Input Circuit



Notes:

1) a) Channels 1 to 16 - Fit the link to enable the input cell.
b) Channels 17 to 32 - Fit the link between pin 2 and pin 5 to enable the input cell.

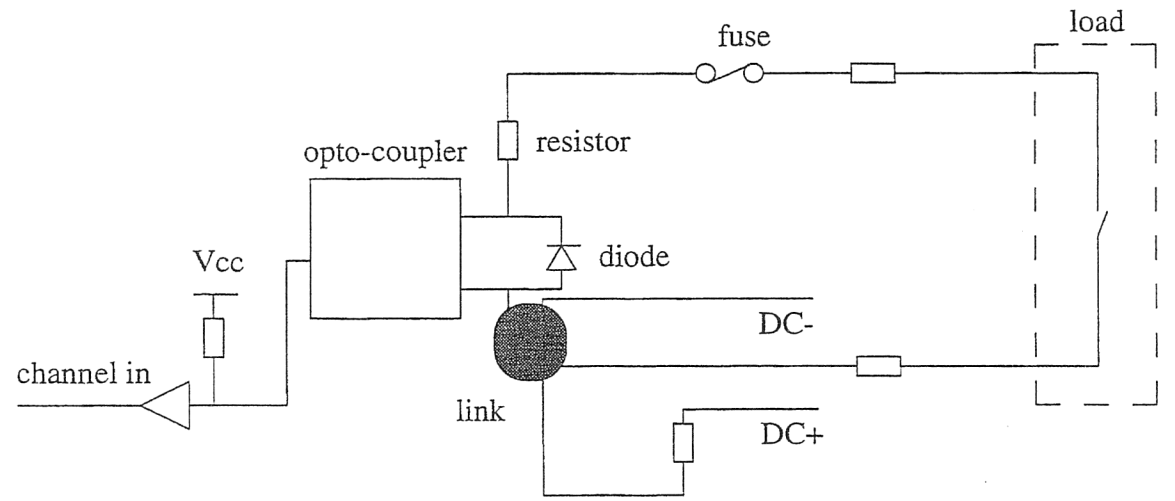
2) The diode protects the opto-coupler from reverse voltages caused by contact bounce in the load.

3) The opto-coupler is a dual, low input current, high gain device (HCPL 2731). The LED has a 400% minimum current transfer ratio at 0.3mA with a forward voltage drop of 1.4V.

4) The resistor value depends on the configured input voltage (i.e. +5V, +12V, +24V or +48V). It ensures that the forward current to the opto-coupler is maintained at approximately 0.3mA.

5) The input terminals are polarised so that the opto-coupler can function correctly.

Figure 8. Self Powered Input on Channels 17 to 32

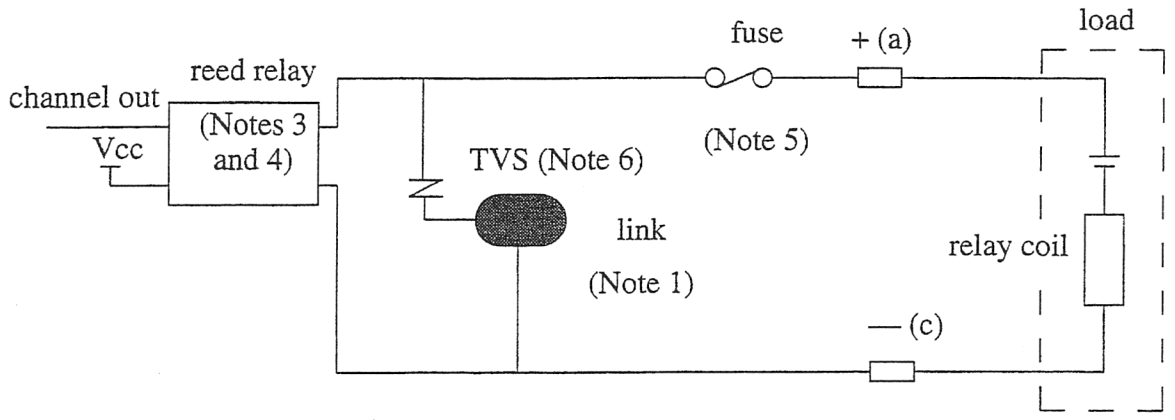


Notes:

1) If the load is purely a set of contacts, the opto-coupler requires a power supply. Channels 17 to 32 provide this option, where a 5V DC/DC converter may be added by connecting pin 4 to pin 5 and pin 2 to pin 3 (assuming that POP 5 was requested).

2) In this configuration, the input terminals are not polarised.

Figure 9. Output Circuit



Notes:

1) a) Channels 1 to 16 - Fit the link to make the cell become a monitored output cell. Leave the link out for a non monitored output cell.

   b) Channels 17 to 32 -Fit the link between pins 1 & 2 and pins 5 & 6 to make the cell become a monitored output cell. Fit the link between pin 5 and pin 6 only for a non monitored output cell.

2) The monitored output cell works in the opposite way to the input cell. In the quiescent state, the opto-coupler draws a small leakage current (0.3mA), large enough to turn the opto-coupler on, but not large enough to energise the relay coil.

3) The operation of the reed relay short circuits the output terminals, the load relay coil energises and the opto-coupler turns off. The opto-coupler turns on when the reed relay turns off.

4) The reed relay contacts are normally open, and close to give a short circuit to the output terminals. (This includes variants /100 and /101, available only on request). Alternatively (variant /103, also available only on request), they can be normally closed, and open to give an open circuit to the output terminals.

5) A 0.75A fuse protects the relay contacts from excessive currents drawn by the load.

6) The Transient Voltage Suppressor (TVS) protects the relay contacts from high back-EMF voltages. The suppressor switches on at a rated voltage of 60V.

7) The output terminals are polarised to ensure correct TVS operation.

DC to DC Converter

A 5V to 5V DC converter provides a potential to the opto-coupler when the input load is only a pair of contacts. This facility is link-selectable on channels 17 to 32 (see Note 1 under Figure 8) and must be requested as a POP (POP 5).

Software Interface

The PIO-1 has hard wired links (see Chapter 4 - Configuration) to enable it to be addressed as an A16:D16 slave on the VMEbus. Using this address, the PIO-1 can be dynamically located anywhere on the A24:D16 VMEbus.

Integration of the PIO-1 into a VMEbus system requires three areas to be covered:

1) How does the host system recognise what this board is ?

2) How does it set up the operating parameters ?

3) How does the host control the PIO-1 ?

The host discovers the type of board that is connected by reading the Card Type register in the A16 address space.

At power-up or after a SYSRESET*, the PIO-1 only responds in the A16 address space. This is the set-up area while the I/O area is disabled in the A24 space. All output/input nodes are disabled and the PIO-1 goes through a self-test and initialisation routine. During this time, the PIO-1 holds the SYSFAIL* line to the host low. When the host sees this line go high, it can set up the PIO-1.

The host then interrogates the Population and Revision State registers to discover the PIO-1's population and revision status. Once the host knows what it is talking to, it can set up the operating parameters by writing to the registers that define:

- The A24 address space that the PIO-1 occupies in VMEbus address space
- The interrupt level to which the PIO-1 responds after a change of state
- The interrupt vector number
- The circumstances under which any individual node generates an interrupt:
  00 = do not interrupt
  01 = interrupt on a low to high transition
  10 = interrupt on a high to low transition
  11 = interrupt on any transition
- If the PIO-1 is to use Trigger mode, an A24 Trigger address
- The Trigger Address Modifier code. This register also contains the Trigger Mode control bit
- The Address Modifier that the PIO-1 recognises. Note that writing to this register makes the PIO-1 active, so make this the last operation.

Once the host has set up the above functions, the PIO-1 will operate in the way you have configured it. If, for example, you have configured the PIO-1 so that all input nodes generate interrupts on any transitions, then it continuously senses all channels and generates an interrupt on any change of state. There are no scan rate limitations involved.

If the PIO-1 has output nodes, then a write to the data registers operates the output cells provided you have not enabled Trigger mode. If you have enabled Trigger mode, then you must address the appropriate location to trigger the output cells.

If you have configured the PIO-1 as either an input or an output monitor, then a read of the data registers tells you the target equipment's state.

The following tables identify the location and addressing requirements for all the registers mentioned above:

A16 Address Space

Offset	Definition	Access
0x00	Card type - default data = 0xFF	Read only
0x01	POP number - LK39 and LK40	Read only
0x02	Revision state - LK35 and LK36	Read only
0x03	Not used - any access causes a bus error	
0x04	Global Address A08 to A15	Write only
0x05	Global Address A16 to A23	Write only
0x06	Not used - any access causes a bus error	
0x07	Global Address Modifiers (AM00 to AM05)	Write only
0x08 to 0x0B	Not used - any access causes a bus error	
0x0C	Interrupt level - 0x00 = disabled; 01 = level 1; etc	Write only
0x0D	Interrupt vector	Write only
0x0E and 0x0F	Not used - any access causes a bus error	
0x10	Global Trigger Address A08 to A15	Write only
0x11 and 0x12	Not used - any access causes a bus error	
0x13	Global Trigger AM - AM00 to AM05 (Data 07 = Trigger Mode control bit)	Write only
0x14 to 0x1F	Not used - any access causes a bus error	

A24 Address Space

The PIO-1 is a slave to the VMEbus with D16 and D08 (EO) capabilities. Due to the way in which the VMEbus organises the addresses, byte 0 is always on the most significant data lines. Take care when accessing the PIO-1 in either word or byte mode.

The PIO-1 always routes data line D00 to channel 1 (or channel 17), D01 to channel 2 (or channel 18), D02 to channel 3 (or channel 19) etc. up to D15 to channel 16 (or channel 32).

Byte Mode

Offset	Definition	Access
0x00	Data Register - Channels 09 to 16	Read/write
0x01	Data Register - Channels 01 to 08	Read/write
0x02	Data Register - Channels 25 to 32	Read/write
0x03	Data Register - Channels 17 to 24	Read/write
0x04 to 0x07	Not used - any access causes a bus error	
0x08	Interrupt Status Register - Channels 09 to 16	Read only
0x09	Interrupt Status Register - Channels 01 to 08	Read only
0x0A	Interrupt Status Register - Channels 25 to 32	Read only
0x0B	Interrupt Status Register - Channels 17 to 24	Read only
0x0C to 0x0F	Not used - any access causes a bus error	
0x10	Interrupt Mask register - Channels 09 to 16	Write only
0x11	Interrupt Mask register - Channels 01 to 08	Write only
0x12	Interrupt Mask register - Channels 25 to 32	Write only
0x13	Interrupt Mask register - Channels 17 to 24	Write only
0x14 to 0x1F	Not used - any access causes a bus error	

Word Mode

Offset	Definition	Access
0x00	Data Register - Channels 01 to 16	Read/write
0x02	Data Registers - Channels 17 to 32	Read/write
0x08	Interrupt Status Register - Channels 01 to 16	Read only
0x0A	Interrupt Status Register - Channels 17 to 32	Read only
0x10	Interrupt Mask Register - Channels 01 to 16	Write only *
0x12	Interrupt Mask Register - Channels 17 to 32	Write only *

* Each channel requires two writes to program it. The first write programs the LSB and the second write programs the MSB

00 = Do not interrupt
01 = Interrupt on low to high transition
10 = Interrupt on high to low transition
11 = Interrupt on any transition.

Examples

1) To operate the relay on channel 1 using byte mode, write 0x01 as data to offset 0x01.

2) To operate the relay on channel 1 using word mode, write 0x0001 as data to offset 0x00.

3) To set the Interrupt mask on channels 01 to 08 as follows:

Channels 1, 4 and 8	do not interrupt
Channels 2 and 7	interrupt on positive transition
Channel 3	interrupt on negative transition
Channels 5 and 6	interrupt on either transition

Channel	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	
First write	0	1	1	1	0	0	1	0	= 0x72
Second write	0	0	1	1	0	1	0	0	= 0x34

write	0x72 as data to offset 0x11
and then write	0x34 as data to offset 0x11

Notes:

1) Half populated boards, i.e. variant 301 (and variants 101, 103 and 201, available only on request) only have channels 01 to 08 and 17 to 24.

2) When the PIO-1 is configured as input, the Data registers are read-only.

3) When the PIO-1 is configured as output, the Data registers are write-only. Every write operates on the whole of that byte. For instance, to activate channels 1 and 3 together and then channel 6 subsequently:

write	0x05 as data to offset 0x01 (channels 1 and 3)
and then write	0x25 as data to offset 0x01 (channels 1, 3 and 6)

It is the user's responsibility to maintain records of the active channels (there is a form for this provided at the end of this manual).

4) In the monitored output configuration, the opto-coupler turns *on* when the output relay turns *off*. Writing a logic '1' to the relay turns it on and the opto-coupler turns off. In the quiescent condition, when the opto-coupler is on, it draws a very small current (approximately 0.3 mA) through the load. It is anticipated that a current of this magnitude, although sufficient to turn the opto-coupler on, is not sufficient to affect the load.

5) When using a double width front panel, link the unoccupied backplane slot across the Bus Grant and Interrupt Acknowledge lines.

PIO-1 Driver Software

OS9 is the most widely used operating system in today's VMEbus market and Radstone Technology supports it extensively. Those familiar with OS-9 will be aware that it contains several device managers, which have been included to make the writing of device drivers easier.

These managers are limited to helping devices, e.g. serial comms (SCF), rotating media (RBF) and tape drives (SBF). Radstone has therefore written a new device handler that ideally suits 16/32-bit event driven boards, e.g. the PIO-1. The latest release of Radstone's OS-9 includes this device handler, ready configured for the PIO-1. Also included is a library of functions providing a simple mechanism for configuring, reading from and writing to the PIO-1. The handler is in source form to help you understand both the PIO-1 and the way to use OS-9 to its best advantage for your application.

Example Code for Driving the PIO-1

As the PIO-1 communicates (mostly) in 16-bit words, any 32-bit I/O requires two 16-bit operations. The following examples are in two formats: 680x0 machine code and in the C programming language. They assume that the following variables have already been declared and correctly assigned:

680X0

```
MaskOffset  equ < offset to Mask registers in PIO-1 >
DataOffset  equ < offset to Data registers in PIO-1 >
   vsect
Top16Databits          dc.w 1     Stores top 16 channels data
Bottom16Databits       dc.w 1     Stores bottom 16 channels data
Configured_address     dc.1 1     Address of PIO-1 on VMEbus
Trigger_address        dc.1 1     Trigger address on VMEbus

Top16bitsLow           dc.w 1     Low bits for top 16 channels' interrupt masks
Top16bitsHigh          dc.w 1     High bits for top 16 channels' interrupt masks
Bottom16bitsHigh       dc.w 1     Low bits for bottom 16 channels' interrupt masks
Bottom16bitsLow        dc.w 1     High bits for bottom 16 channels' interrupt masks
ends
```

C

```
#define MaskOffset < offset to Mask registers in PIO-1 >
#define DataOffset < offset to Data registers in PIO-1 >

   short
*Configured_address,      /* Address of PIO-1 on VMEbus */
*Trigger_address,         /* Trigger address on VMEbus */
*Data_ptr,                /* A pointer to the DATA variable declared below */
Top16bitsLow,             /* Low bits for top 16 channels' interrupt masks */
Top16bitsHigh,            /* High bits for top 16 channels' interrupt masks */
Bottom16bitsHigh,         /* Low bits for bottom 16 channels' interrupt masks */
Bottom16bitsLow;          /* High bits for bottom 16 channels' interrupt masks */

unsigned
DATA;                     /* stores all 32 bits of channel data */
```

Writing to the PIO-1

In 680X0:

```
move.l    Configured_address(a6),a0      get the card address
add.l     #Data_Offset,a0                add the offset to the data registers
move.w    Top16DataBits(a6),(a0)         put the top 16 bits into PIO-1
move.w    Bottom16DataBits(a6),1(a0)     put the bottom 16 bits into PIO-1
```

In C:

```
/* put the top 16 bits into PIO-1 */
*( Configured_address + DataOffset ) = *Data_ptr;
/* put the bottom 16 bits into PIO-1 */
*( Configured_address + DataOffset + 1 ) = *( Data_ptr + 1 );
```

Reading from the PIO-1

In 680X0:

```
move.l    Configured_address(a6),a0      get the card address
add.l     #Data_Offset,a0                add the offset to the data registers
move.l    (a0),Top16Bits(a6)             read the top 16 bits from PIO-1
move.w    1(a0),Bottom16Bits(a6)         read the bottom 16 bits from PIO-1
```

In C:

```
/* read the top 16 bits from PIO-1 */
*Data_Ptr = *( Configured_address + DataOffset );
/* read the bottom 16 bits from PIO-1 */
*Data Ptr = *( Configured_address + DataOffset + 1 );
```

Triggering Data to Outputs if Trigger Mode is On

In 680X0:

Any instruction that accesses `Trigger_address` will do. A suggested instruction is:

```
move.l          Trigger_address(a6),a0
tst.b           (a0)
```

In C:

Again, anything that accesses `Trigger_address` will do. A suggested instruction is:

<some unsigned variable> = `*Trigger_address;`

The rest of the PIO-1 operations are for configuration. The most difficult operation is setting the interrupt masks, as it requires 4 writes, compared with 1 for all other configuration operations.

Setting the Interrupt Masks

In 680X0:

```
move.l    Configured_address(a6),a0
add.l     #Mask_Offset,a0            get address of interrupt mask registers
move.w    Top16Bitslow(a6),(a0)      set low bit of top 16 channels' masks
move.w    Top16Bitshigh(a6),(a0)     set top bit of top 16 channels' masks
move.w    Bottom16Bitslow(a6),(a0)   set low bit of bottom 16 channels' masks
move.w    Bottom16Bitshigh(a6)(a0)   set top bit of bottom 16 channels' masks
```

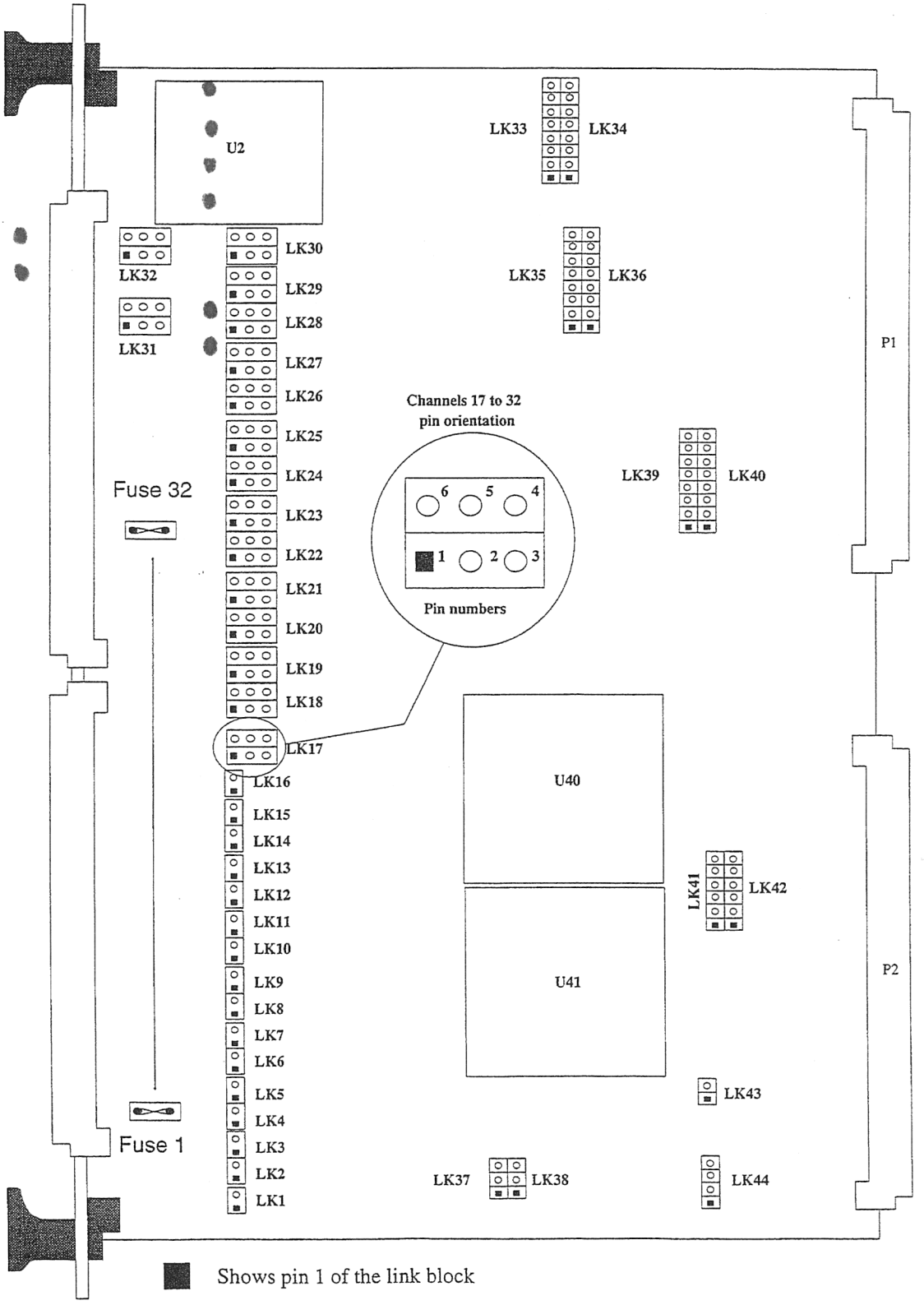
In C:

```
*(Configured_address + Mask_Offset) = Top16Bitslow;
*(Configured_address + Mask_Offset) = Top16Bitshigh;
*(Configured_address + Mask_Offset + 1) = Bottom16Bitslow;
*(Configured_address + Mask_Offset + 1) = Bottom16Bitslow;
```

Chapter 4 - Configuration

This chapter shows the possible configurations of the user links on the PIO-1. The following diagram shows the links' positions and orientations:

Figure 10. Link Location Diagram



I/O Addresses and Address Modifiers

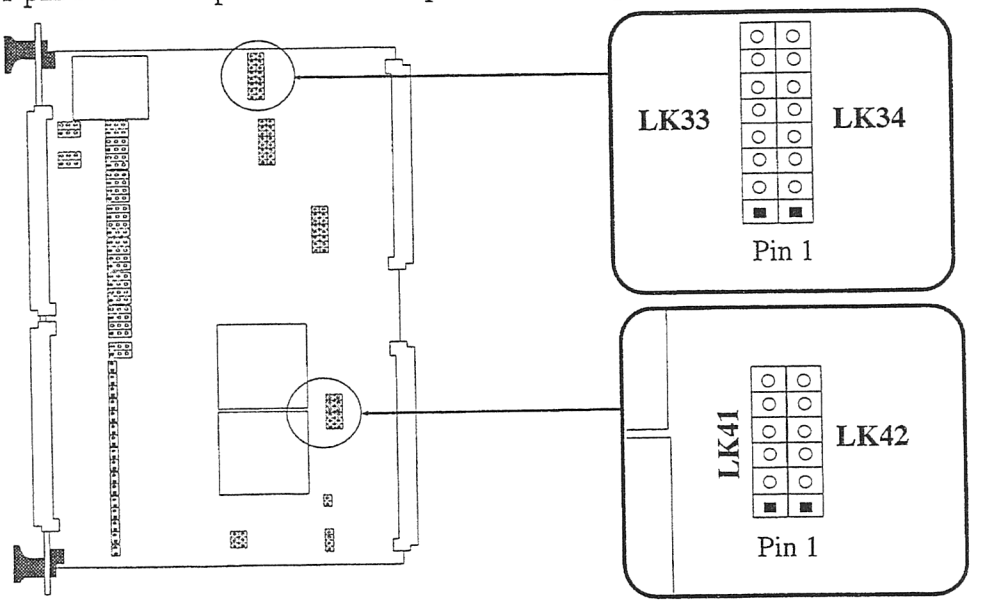
You can map the PIO-1 anywhere in the VME short I/O address space. This mapping uses LK33 and LK34 to set address bits A08 to A15, and LK41 and LK42 to set the Address Modifier codes AM00 to AM05, as the following tables show:

Address Bit	Link Configuration		Link In	Link Out
	LK33	LK34		
A08	Pin 8	Pin 8	Logic 0 ●	Logic 1
A09	Pin 7	Pin 7	Logic 0 ●	Logic 1
A10	Pin 6	Pin 6	Logic 0 ●	Logic 1
A11	Pin 5	Pin 5	Logic 0 ●	Logic 1
A12	Pin 4	Pin 4	Logic 0	Logic 1 ●
A13	Pin 3	Pin 3	Logic 0	Logic 1 ●
A14	Pin 2	Pin 2	Logic 0 ●	Logic 1
A15	Pin 1	Pin 1	Logic 0 ●	Logic 1

Address Modifier Code Bit	Link Configuration		Link In	Link Out
	LK41	LK42		
AM00	Pin 6	Pin 6	Logic 0	Logic 1
AM01	Pin 5	Pin 5	Logic 0	Logic 1
AM02	Pin 4	Pin 4	Logic 0	Logic 1
AM03	Pin 3	Pin 3	Logic 0	Logic 1
AM04	Pin 2	Pin 2	Logic 0	Logic 1
AM05	Pin 1	Pin 1	Logic 0	Logic 1

For example, to set the PIO-1 in the short supervisory I/O address space of 0xEExx (the default setting), insert the following links:

LK33 pin 4 to LK34 pin 4 and LK33 pin 8 to LK34 pin 8 (i.e. 0xEE)
LK41 pin 2 to LK42 pin 2 and LK41 pin 5 to LK42 pin 5 (i.e. 0x2D)



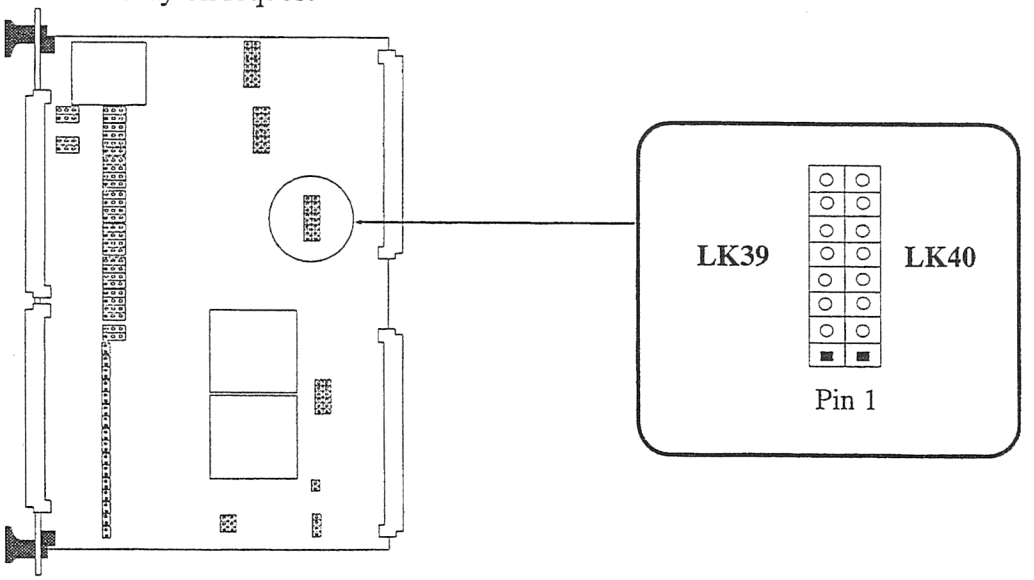
I/O Configuration (LK39 and LK40)

These links are factory fitted according to the PIO-1's build standard. The following table shows how they define the PIO-1's population and I/O configuration:

Variant	Input or Output	Number of Channels	LK39 and LK40 pin configuration, pin 1 to pin 1, pin 2 to pin 2 etc.							
			8-8	7-7	6-6	5-5	4-4	3-3	2-2	1-1
/100*	Output only (open)	32	In	In	Out	In	In	In	In	In
/101*	Output only (open)	16	In	In	Out	In	In	In	In	Out
/103*	Output only (closed)	16	In	Out	Out	In	In	In	In	Out
/200*	Input only	32	In	In	In	Out	POP dependant, see below			In
/201*	Input only	16	In	In	In	Out				Out
/300	Both (default)	32	In	In	Out	Out				In
/301	Both	16	In	In	Out	Out				Out

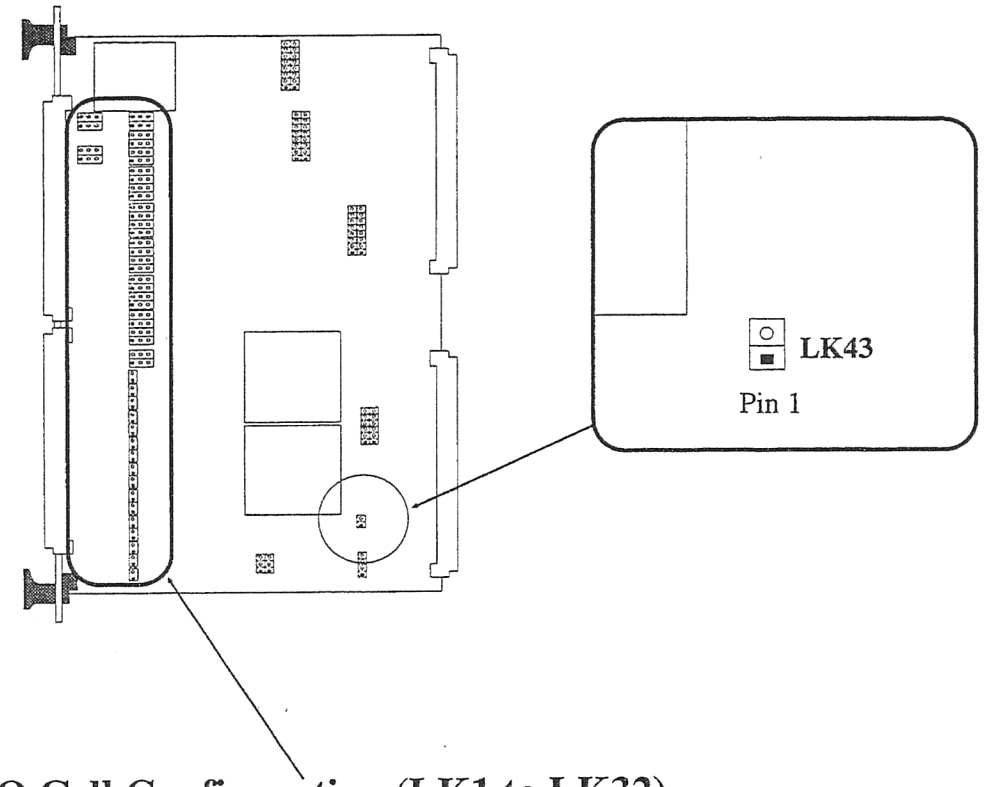
POP	Input Voltage	LK39 and LK40 pin configuration, pin 2 to pin 2 etc.		
		4 to 4	3 to 3	2 to 2
2	5V	In	In	Out
3	12V	In	Out	In
4	24V	In	Out	Out
5	48V	Out	In	In
9*	5V and 12V	Out	In	Out
10	28V	Out	Out	In
11*	5V and 24V	Out	Out	Out

* = Available only on request



Trigger Address (LK43)

When using multiple PIO-1s in the same system, they can be configured to trigger simultaneously to output data. If you require this facility, then only one PIO-1 should have LK43 inserted to enable DTACK* to the VMEbus. This should preferably be the last PIO-1 (rightmost) in the rack.



I/O Cell Configuration (LK1 to LK32)

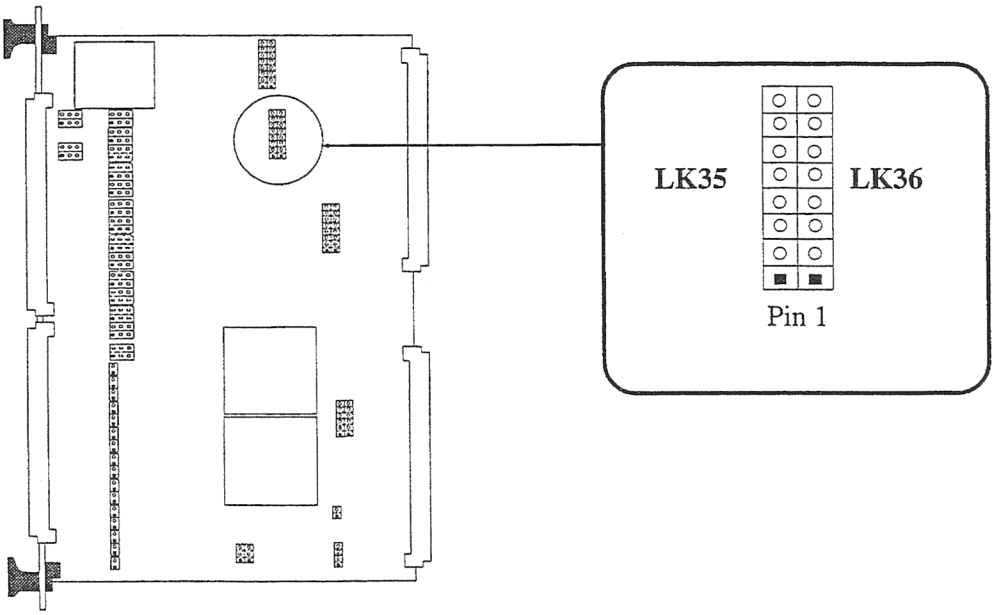
Links LK1 to LK32 configure the I/O cells on channels 1 to 32 respectively. Links LK1 to LK16 are 2 pin links and so are either connected or not connected. Links LK17 to LK32 are 6 pin links. These can be linked in various ways, depending on whether the cell is input, self powered input, output, input and output or monitored output. Depending on the variant and POPs requested, Radstone may factory configure certain of links LK1 to LK32. Chapter 3 fully describes the linking, in the 'I/O Cells' section.

Revision State (LK35 and LK36)

Radstone Technology sets the default revision state to reflect the PIO-1's build status, using links LK35 and LK36. Once you have read, identified and recorded the PIO-1's revision state below, you can use LK35 and LK36 for any purpose that you wish. The following table allows you to create a permanent record of how you have configured these links:

Revision State =

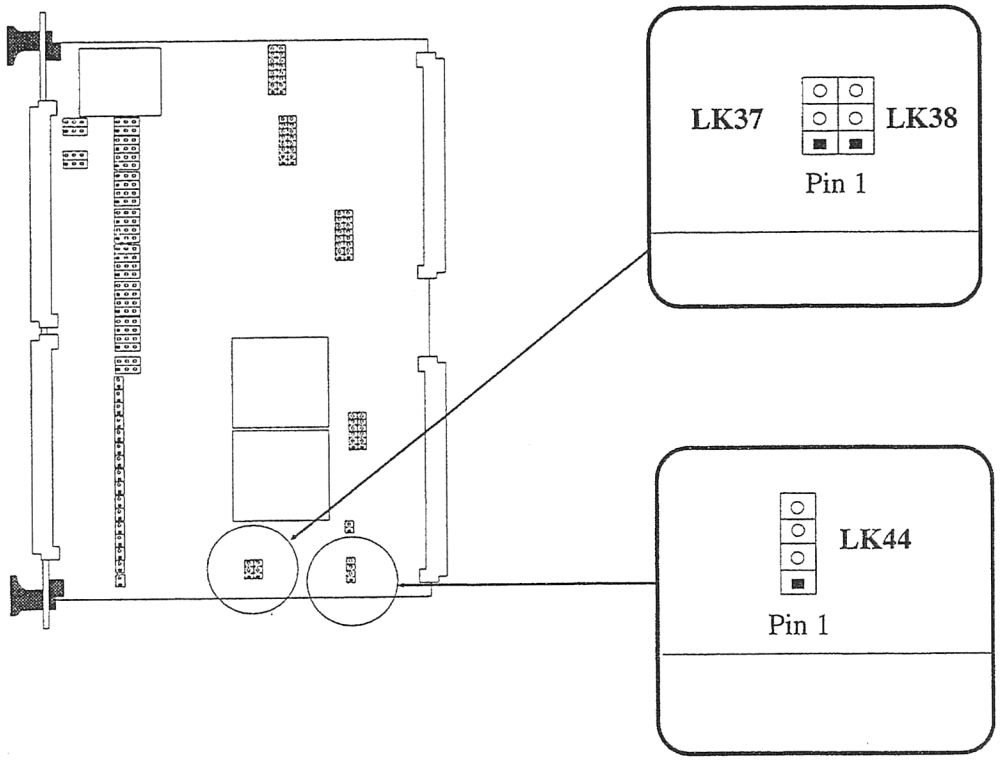
LK35 and LK36 Pin Configuration pin 1 to pin 1, pin 2 to pin 2 etc.								Function
8-8	7-7	6-6	5-5	4-4	3-3	2-2	1-1	



Debounce Clock (LK44)

The LCA has a multiple input stage to verify that any changes that occur are genuine and not transitions caused by such events as contact bounce. The rate at which this verification takes place is link selectable via LK44.

Pin 1 to 4 250Hz (default)
Pin 2 to 4 500Hz
Pin 3 to 4 50Hz



LCA Configuration (LK37 and LK38)

Power-up automatically configures the PIO-1 from the on-board configuration PROM. To select the correct configuration program, leave links LK37 and LK38 at their default settings, i.e. LK37 pin 2 to 3 and LK38 pin 2 to 3.

Chapter 5 - Connector Pinouts

In Figures 11 and 12, the signals enclosed in braces { } are not active on the PIO-1. However, they are passed on to the next VME slot.

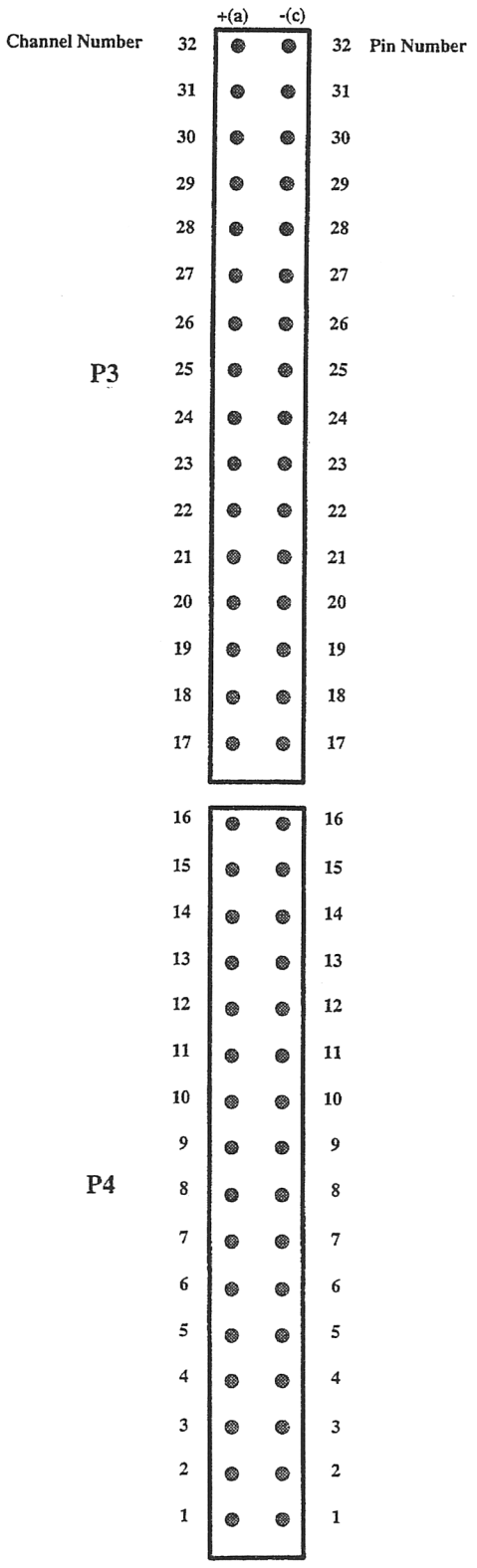
Figure 11. VME Connector P1

Pin	Row a Signal	Row b Signal	Row c Signal
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	**D03**	**{BG0IN*}**	**D11**
5	**D04**	**{BG0OUT*}**	**D12**
6	**D05**	**{BG1IN*}**	**D13**
7	D06	{BG1OUT*}	D14
8	D07	{BG2IN*}	D15
9	GND	{BG2OUT*}	GND
10	**SYSCLK**	**{BG3IN*}**	**SYSFAIL***
11	**GND**	**{BG3OUT*}**	**BERR***
12	**DS1***	**BR0***	**SYSRESET***
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	**DTACK***	**AM0**	**A22**
17	**GND**	**AM1**	**A21**
18	**AS***	**AM2**	**A20**
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	Not Used	A17
22	**IACKOUT***	**Not Used**	**A16**
23	**AM4**	**GND**	**A15**
24	**A07**	**IRQ7***	**A14**
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	**A03**	**IRQ3***	**A10**
29	**A02**	**IRQ2***	**A09**
30	**A01**	**IRQ1***	**A08**
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

Figure 12. VME Connector P2

Pin	Row a	Row b	Row c
1	No connection	{+5V}	No connection
2	No connection	{GND}	No connection
3	No connection	{RESERVED}	No connection
4	**No connection**	**{A24}**	**No connection**
5	**No connection**	**{A25}**	**No connection**
6	**No connection**	**{A26}**	**No connection**
7	No connection	{A27}	No connection
8	No connection	{A28}	No connection
9	No connection	{A29}	No connection
10	**No connection**	**{A30}**	**No connection**
11	**No connection**	**{A31}**	**No connection**
12	**No connection**	**{GND}**	**No connection**
13	No connection	{+5V}	No connection
14	No connection	{D16}	No connection
15	No connection	{D17}	No connection
16	**No connection**	**{D18}**	**No connection**
17	**No connection**	**{D19}**	**No connection**
18	**No connection**	**{D20}**	**No connection**
19	No connection	{D21}	No connection
20	No connection	{D22}	No connection
21	No connection	{D23}	No connection
22	**No connection**	**{GND}**	**No connection**
23	**No connection**	**{D24}**	**No connection**
24	**No connection**	**{D25}**	**No connection**
25	No connection	{D26}	No connection
26	No connection	{D27}	No connection
27	No connection	{D28}	No connection
28	**No connection**	**{D29}**	**No connection**
29	**No connection**	**{D30}**	**No connection**
30	**No connection**	**{D31}**	**No connection**
31	No connection	{GND}	No connection
32	{0V}	{+5V}	{0V}

Figure 13. Front Panel Connectors P3 and P4



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Active Channel Record

Channel Number	Active ?
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
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20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
31	
32	

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If your Company has already entered a Confidentiality Agreement for PME products with Radstone Technology, no signature is required.

Confidentiality Agreement

In consideration of our supplying you with information concerning the PME product range for the purpose of allowing all user functions to be fully understood it is agreed as follows:

1. As used in this agreement:

   (a) "our information" shall mean all documents, ideas, know-how and other information supplied by us to you (whether disclosed to you orally, in documentary or other material form, by demonstration or otherwise) for the purpose referred to above;

   (b) "proper use" shall mean use solely for the purpose referred to above; and

   (c) "third party" shall include any parent, subsidiary or affiliated company of your Company.

2. All our information shall be treated by you as confidential, shall not be used by you except for proper use, shall not be disclosed to any person within your Company who is not directly concerned in its proper use, and shall not be disclosed to any third party without our prior written consent, except for such information as you can prove to our reasonable satisfaction:

   (a) is already known to you at the date hereof and is or becomes free of restriction on disclosure and use (and you have advised us of the fact), or

   (b) is generally known or freely available to the public (except by reason of any breach by you of your obligations hereunder), or

   (c) has been disclosed to you, free of restriction on disclosure and use, by a third party who was entitled to make such unrestricted disclosure.

Continued

3. You will take such precautions and make such arrangements as are reasonably necessary to protect our information (and in any event no less than those you would take and make to protect your own confidential information). You will inform such of your employees as are concerned in its proper use of the confidential nature of our information, and you will prohibit each of them from making copies of any of it.

4. In the event that you do not purchase or discontinue purchase of the product you will promptly, and in any event not later than 3 months after such event, and without further request return to us all the documents and other material containing our information.

5. This Agreement shall be governed by and construed in accordance with the law of England.

..... For and on behalf of
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Signed .....

Name .....

Title .....

Date .....

Address .....

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2. All our information shall be treated by you as confidential, shall not be used by you except for proper use, shall not be disclosed to any person within your Company who is not directly concerned in its proper use, and shall not be disclosed to any third party without our prior written consent, except for such information as you can prove to our reasonable satisfaction:

   (a) is already known to you at the date hereof and is or becomes free of restriction on disclosure and use (and you have advised us of the fact), or

   (b) is generally known or freely available to the public (except by reason of any breach by you of your obligations hereunder), or

   (c) has been disclosed to you, free of restriction on disclosure and use, by a third party who was entitled to make such unrestricted disclosure.

Continued

3. You will take such precautions and make such arrangements as are reasonably necessary to protect our information (and in any event no less than those you would take and make to protect your own confidential information). You will inform such of your employees as are concerned in its proper use of the confidential nature of our information, and you will prohibit each of them from making copies of any of it.

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