Technical Manual

STR200

FASTBUS
Scaler Module

Version:.....

Serial Number:.....

STRUCK

STR200

FASTBUS SCALER MODULE

This single-width, four layer Module is a FASTBUS implementation of a general-purpose multichannel pulse counter, as needed for data acquisition and control tasks in HEP experiments. The STR200 accepts pulses via two front panel ECL ports, using standard differential ECL levels with a popular 34 pin connector pin layout.

MODULE FEATURES

CHANNELS PER MODULE	The STR200 contains 32 independent scaler channels.
CHANNEL RANGE	Each channel provides 32 bits of scaling. (Due to its large range the module does not handle any overflow.)
SCALER FUNCTION	Up-counter without preset.
INPUT RATE	The scaler responds to pulses from DC up to 100MHz.
INPUT LEVEL	Two front panel ECL ports are employed to accept 32 input sources using standard differential ECL level, 100 Ohm impedance (high impedance by a simple user option). Plugging a cable into the scaler with a logical 0 signal does not generate a count. NIM input level on request.
COUNT-ENABLE	Each scaler channel is controlled by an individual count-enable condition, which is generated by a logical AND of a common external count-enable, and one corresponding bit from CSR Register 12hex. One separate front panel connector is employed to accept the common count-enable using differential ECL-level. Assert false level ⇒ counting is inhibited Assert true level7 ⇒ counting is only enabled if CSR(23h) bits are also set If no signal present ⇒ counting is enabled.
READ-ON-FLY	The module has read-on-fly capability (i.e. counters with "shadow" registers). Only the upper 24 bits are assumed to be valid during a read-on-fly; the lower four bits may be in transition. However, if no input pulses are asserted during a read then all 32 bits are valid. No counts are missed due to read-on-fly.
SCALER CLEAR	Each scaler channel can be cleared by an individual clear condition that is generated by a logical OR of seven signal sources: — Front panel FAST CLEAR (differential. ECL 25ns) common for channels 0-31 — FASTBUS RB*/BH condition common for channels 0-31 — Power on condition common for channels 0-31 — CSR(=) Write AD(30) (=general clear module) common for channels 0-31 — CSR(0) Write AD(31) (=clear scaler only) common for channels 0-31 — CSR(10h) Write: if AD(xx) is asserted, then channel xx is cleared. — Read and Clear if CSR(11h) Bit(xx) is set, then channel xx is cleared after a Block Transfer Read.

SCALER TEST	To perform stand-alone tests without external signal sources, CSR(0) contains two bits: AD(06)/AD(22) ⇒ enable/disable test mode AD(07) ⇒ generate test-increment on Bit 0 and Bit 16 channel 0-31 during CSR(0) write. In combination with selective count-enable and selective clear, proper operation of all channels can be verified "off-line" (even if input signals are connected). Attention: If count-enable is logical 0, only test increment on bit 0 is inhibited.
FASTBUS INTERFACE	The module conforms to FASTBUS Spec. dated December 83 (US NIM). For information about implemented slave functions see next chapter.
FRONT PANEL INDICATOR	"CONN" is active when the module is a connected Slave (without mono-stable stretching).

FASTBUS CONTROL

ADDRESSING MODES:

A primary address connection can be established either by GEOGRAPHICAL, LOGICAL or BROADCAST (general & class-N) addressing mode. The module contains two independent NTA-registers for DSR and CSR-space, each 5 bits wide. These NTA-registers are loaded at primary address time if logical addressing is performed or during a secondary address write cycle. During Block transfer-Read the DSR-NTA is used as an autoincremented address pointer.

Invalid addressing results in SS=7 response either on AK(u) (logical) or on DK(u) (secondary address write).

BROADCAST FUNCTIONS:

A 16 bit Broadcast Class register is provided. Modules which recognize General Broadcast or their Broadcast Class connect to a master without generating AK-Handshake. The module will execute subsequent datacycles (only CSR write cycles recommended). This permits selected groups of modules to perform simultaneous control or test operations.

DATA CYCLES:

The module supports types of datacycles as follows:

Random read/write CSR

Secondary address read/write CSR

Random read/write DSR

Secondary address read/write DSR

Block handshake read DSR

(Block pipelined read DSR) not recommended

Un-supported datacycles result in SS=6 responses.

Blocktransfer address 31 results in SS=2 response.

Un-implemented secondary addresses result in SS=7 responses.

CSR SPACE REGISTER

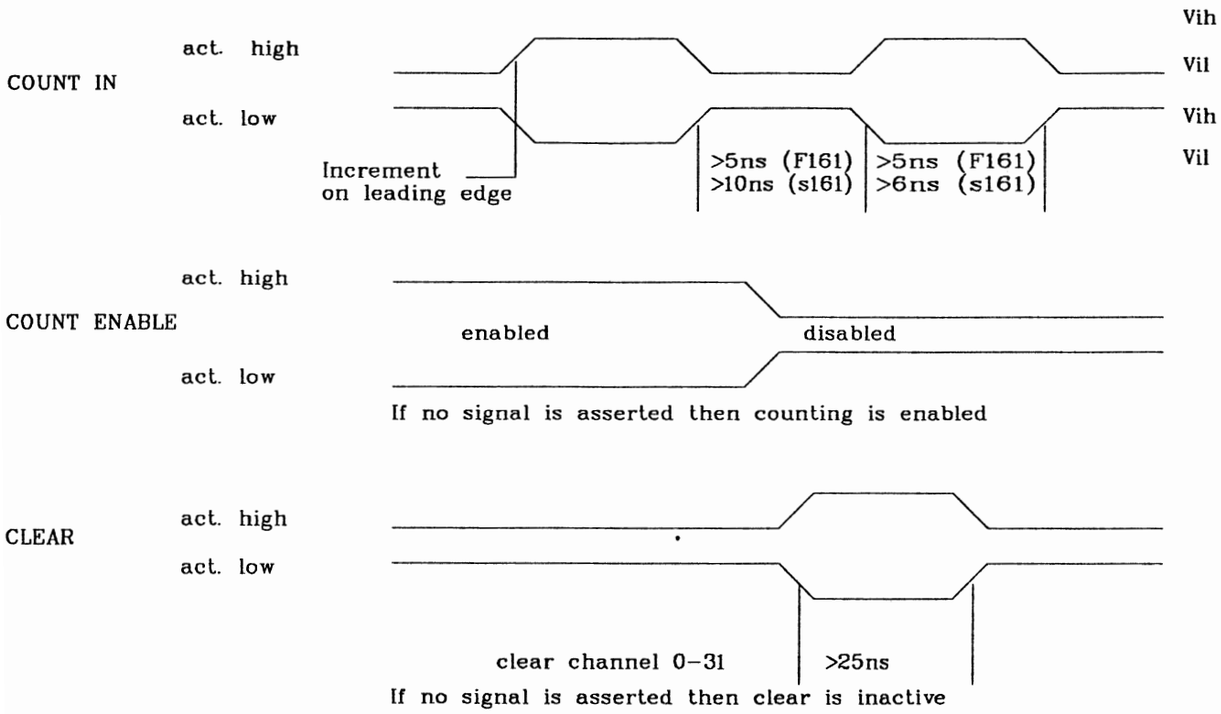
CSR(0) R/W	Module identifier on AD(31:16) ⇒ 6823 hex
	⇒ 26674 dec
	⇒ 64062 oct
	Enable/disable logical address ⇒ AD(01)/AD(17)
	Enable/disable test-mode ⇒ AD(06)/AD(22)
	Increment channel 0-31 upper and lower 16bits only if testmode is enabled ⇒ AD(07)
	General clear ⇒ AD(30)
	Reset channel 031 ⇒ AD(31)
CSR(3) R/W	Logical address register ⇒ AD(31:05)
CSR(7) R/W	Broadcast classN register ⇒ AD(15:00)
CSR(10h) WO	Selective clear of scaler ⇒ AD(31:00)
	Asserting AD(xx) during write clears channel xx.
CSR(11h) R/W	Selective Read & Clear register ⇒ AD(31:00)
	If register bit (xx)=1, then channel xx is reset at the end of a block transfer read (DSR).
CSR(12h) R/W	Selective count enable register ⇒ AD(31:00)
	If register bit(xx)=1, then channel xx is prepared to count. ANDcondition with common frontpanel-signal.

DSR SPACE

DSR(0) RO	Read scaler channel 0 ⇒ AD (31:00)
*	
*	
DSR(31) RO	Read scaler channel 31 ⇒ AD (31:00)

INITIALISATION

GENERAL CLEAR	Power on +
	RB .and. .not BH +
	Write CSR(0) AD(30)
	General clear resets CSR register 7,11h,12h and scaler channels 0-31.
	General clear disables logical address, testmode
SCALER CLEAR	Common front panel signal +
	Write CSR(0) AD(31)


COUNT IN
act. high
act. low
Vih
Vil
Vih
Vil
Increment
on leading edge
>5ns (F161)
>10ns (s161)
>5ns (F161)
>6ns (s161)
COUNT ENABLE
act. high
act. low
enabled
disabled
If no signal is asserted then counting is enabled
CLEAR
act. high
act. low
clear channel 0–31
>25ns
If no signal is asserted then clear is inactive

CONNECTOR PINOUT

1. FASTBUS Connector

— see FB-specification

2. Connector ST0/15 'Input channel 0-15'

Pin#	Signal	Pin#
act. high 1	Inputchannel 0	2 act. low ECL
act. high 3	Inputchannel 1	4 act. low ECL
act. high 5	Inputchannel 2	6 act. low ECL
act. high 7	Inputchannel 3	8 act. low ECL
act. high 9	Inputchannel 4	10 act. low ECL
*		
*		
act. high 31	Inputchannel 15	32 act. low ECL
33	GND	34

3. Connector ST16/31 'Input channel 16-31'

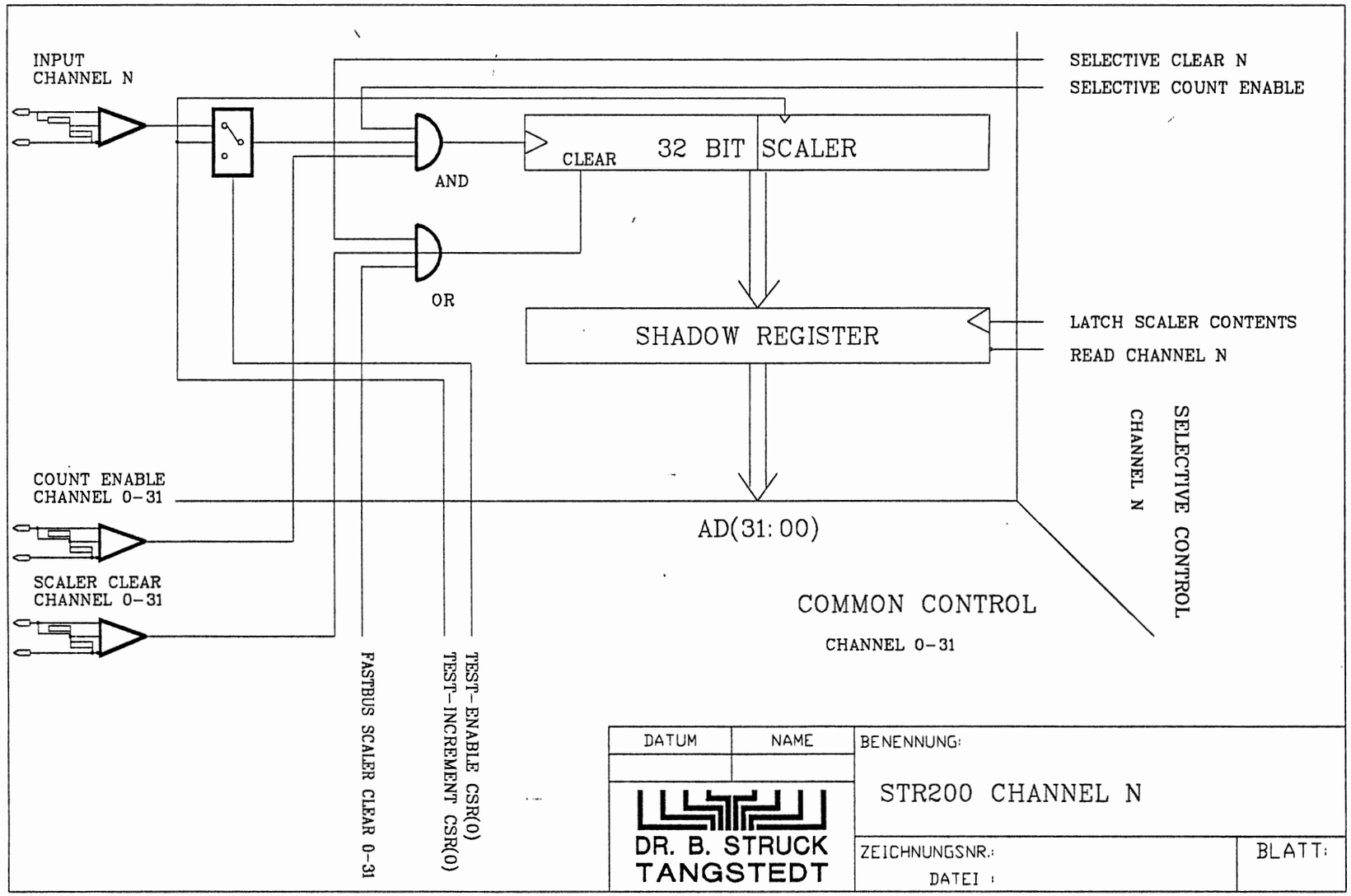
Pin#	Signal	Pin#
act. high 1	Inputchannel 16	2 act. low ECL
act. high 3	Inputchannel 17	4 act. low ECL
act. high 5	Inputchannel 18	6 act. low ECL
act. high 7	Inputchannel 19	8 act. low ECL
act. high 9	Inputchannel 20	10 act. low ECL
*		
*		
act. high 31	Inputchannel 31	32 act. low ECL
33	GND	34

4. Connector ST3 'Count enable'

Pin#	Signal	Pin#
act. high 1	Count enable	2 act. low ECL
act. high 3	GND	4 act. low ECL
act. high 5	GND	6 act. low ECL
act. high 7	Not connected	8 act. low ECL
act. high 9	Not connected	10 act. low ECL

5. Connector ST4 'Clear scaler'

Pin#	Signal	Pin#
act. high 1	Clear scaler	2 act. low ECL
act. high 3	GND	4 act. low ECL
act. high 5	GND	6 act. low ECL
act. high 7	Not connected	8 act. low ECL
act. high 9	NOt connected	10 act. low ECL


INPUT
CHANNEL N
SELECTIVE CLEAR N
SELECTIVE COUNT ENABLE
AND
CLEAR
32 BIT SCALER
OR
SHADOW REGISTER
LATCH SCALER CONTENTS
READ CHANNEL N
SELECTIVE CONTROL
CHANNEL N
COUNT ENABLE
CHANNEL 0-31
AD(31:00)
SCALER CLEAR
CHANNEL 0-31
COMMON CONTROL
CHANNEL 0-31
FASTBUS SCALER CLEAR 0-31
TEST-INCREMENT CSR(0)
TEST-ENABLE CSR(0)
DATUM
NAME
BENENNUNG:
STR200 CHANNEL N
DR. B. STRUCK
TANGSTEDT
ZEICHNUNGSNR.:
DATEI :
BLATT:

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PAL12H6
STR300 100MHZ SCALER                DR.B.STRUCK COMPANY
PAL1 VERSION 2                      R OELSCHLAEGER   29/ 1/85

GA AK MS0 MS1 MS2 AS ASDEL EG RD GND
LOG LOGDEL CKGEO LDNTA CKLOG CKCSR CLRGEO DGEO RESALL VCC

DGEO    = /RD*/MS1*/MS2*/GA
CKGEO   =  EG* ASDEL */AK
CLRGEO  =  AS
CKCSR   =  ASDEL*/AK
CKLOG   =  ASDEL*/AK*/EG
LDNTA   =  LOG*.LOGDEL

DESCRIPTION
THIS PAL GENERATES CLOCK AND D-INPUTS FOR ADDRESS RECOGNITION
STR300 100MHZ SCALER



PAL16R4
STR300 100MHZ SCALER                DR B STRUCK COMPANY
PAL2 VERSION 2                      R OELSCHLAEGER   29/ 1/85

CLASS AK ENLOG MS1 MS2 AD0 NC AD2 RD GND
EQ1 EQ2 EQ3 NC NC DBRDCST DLOG EQ4 AD3 VCC

DLOG    = /RD*/MS1*/MS2* ENLOG * /EQ1 */EQ2 */EQ3 */EQ4
DBRDCST = /RD* MS1*/MS2* AD0   * /AD3 */AD2 +
          /RD* MS1*/MS2* AD0   * /AD3 * AD2 */CLASS

DESCRIPTION
THIS PAL GENERATES D-INPUTS FOR SELECT FLIPFLOPS LOGICAL AND
BRCAECAST



PAL16R4
STR300 100MHZ SCALER                DR B STRUCK COMPANY
PAL3 VERSION 3                      R OELSCHLAEGER   29/ 1/85

LDNTA GEO CSR LOG BRCST SECWC LDNTA SECWD BDS GND
CLR NC IAKN CLSSGT LDNTAD LDNTAC RDRQ SEL DSDEL VCC

SEL     = GEO + LOG + BRCST
IAKN    = GEO*CSR +
          LOG*CSR +
          LOG*/CSR*LDNTA +
          GEO*/CSR*LDNTA
RDRQ    = GEO + LOG
LDNTAC  = CSR*LDNTA + /SECWC*/DSDEL
LDNTAD  =/CSR*LDNTA + /SECWD*/DSDEL
CLSSGT  =/BDS*CLR

DESCRIPTION
THIS PAL GENERATES SIGNALS STEERING ADDRESSING PART
OF THE SCALER
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PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL4 VERSION 3                          R.OELSCHLAEGER   21/10/84

NC NC NC NVA AD4 AD0 AD1 AD2 AD3 GND
NC NC NC NC NVACSR NVCS1 NC NC NC VCC

/NVACSR = /NVA*/AD0*/AD1*/AD2*/AD3*/AD4 +
          /NVA* AD0* AD1*/AD2*/AD3*/AD4 +
          /NVA* AD0* AD1* AD2*/AD3*/AD4 +
          /NVA*/AD0*/AD1*/AD2*/AD3* AD4 +
          /NVA* AD0*/AD1*/AD2*/AD3* AD4 +
          /NVA*/AD0* AD1*/AD2*/AD3* AD4

/NVCS1  =       /AD0*/AD1*/AD2*/AD3*/AD4 +
                 AD0* AD1*/AD2*/AD3*/AD4 +
                 AD0* AD1* AD2*/AD3*/AD4 +
                /AD0*/AD1*/AD2*/AD3* AD4 +
                 AD0*/AD1*/AD2*/AD3* AD4 +
                /AD0* AD1*/AD2*/AD3* AD4
DESCRIPTION
THIS PAL DECODES ADDRESS LINES TO GENERATE NON VALID ADDRESSES
CSR SPACE



PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL5 VERSION 2                          R OELSCHLAEGER   30/01/85

SECRDC SECRDC CSR NVD SSIT SECWC NVC SECWD NC GND
NC NC NC NC NC SE? NC   NC NC VCC

/SE?    = SSIT*CSR +
          *SECWD*NVD +
          /SECWC*NVC +
          /SECRDC*NVD +
          /SECPJC*NVC

DESCRIPTION
TH'S PAL GENERERATES INTERNAL SSI RESPONSE



PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL6 VERSION 1                          R OELSCHLAEGER   21/10/84

AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 GND
AD25 AD26 AD27 AD28 NC ZERO AD29 AD30 AD31 VCC

/ZERO = /AD16*/AD17*/AD18*/AD19*/AD20*/AD21*/AD22*/AD23*/AD24
        */AD25*/AD26*/AD27*/AD28*/AD29*/AD30*/AD31

DESCRIPTION
THIS PAL CHECKS AD  (31:16) FOR ZERO
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PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL7 VERSION 1                          R OELSCHLAEGER   21/10/84

ZERO NC   NC   AD3  AD4  AD5  AD6  AD7  AD8  GND
AD9  AD10 AD11 AD12 NC VLID AD13 AD14 AD15 VCC

/VLID = /AD5 */AD6 */AD7 */AD8 */AD9 */AD10*/AD11*/AD12*/AD13
       */AD14*/AD15*/ZERO

DESCRIPTION
THIS PAL CHECKS AD [31:05] FOR ZERO
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PAL16L8
STR300 100MHZ SCALER                    DR L STRUCK COMPANY
PAL8 VERSION 2                          R OELSCHLAEGER   21/10/84

BDSDEL BDS SEL MS0 AS RESALL DSR MS1 RD GND
BLOCK NC SETPIP SETEL DDS   DDST BLKEND CLRBL CLRBLI VCC

/DDS     =BDS*SEL
/DDST    =SEL*BDS*/BDSDEL*BLOCK +
          SEL*/BDS*BDSDEL*BLOCK
/CLRBL   =SEL*/BDS*BDSDEL*/MS0 +
          /AS                  +
          /RESALL
/SETEL   =SEL*BDS*/BDSDEL*MS0*DSR* RD
/SETPIP =SEL*BDS*/BDSDEL*MS0*MS1*DSR
/BLKEND =BLOCK*/CLRBLI
DESCRIPTION
THIS PAL GENERATES SIGNALS DUE TO DATACYCLES
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PAL16L8
STR200 100MHZ SCALER                    DR.B STRUCK COMPANY
PAL9 VERSION 2                          R OELSCHLAEGER   21/10/84

DS LMS0 LMS1 LMS2 GND DSR BLOCK BRQST DSDEL GND
NC IDK SECWC SECWD SECRDC SECRDD WRC RDC RDD VCC

/RDD     =/DS*/LMS0*/LMS1*/LMS2*LRD*DSR + BLOCK
/RDC     =/DS*/LMS0*/LMS1*/LMS2*LRD*/DSR
/IDK     = /DSDEL* BRQST
/WRC     =/DS*/DSDEL*/LMS0*/LMS1*/LMS2*/LRD*/DSR
/SECRDD =/DS        */LMS0* LMS1*/LMS2* LRD* DSR
/SECRDC =/DS        */LMS0* LMS1*/LMS2* LRD*/DSR
/SECWD   =/DS        */LMS0* LMS1*/LMS2*/LRD* DSR
/SECWC   =/DS        */LMS0* LMS1*/LMS2*/LRD*/DSR

DESCRIPTION
THIS PAL GENERATES DATACYCLE SIGNALS
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PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL10 VERSION 1                         R GELSCHLAEGER   21/10/84

DS LMS0 LMS1 LMS2 LRD DSR BLOCK ENDBL NVD  GND
NVC NC NC NC SS2 SS6 NC NC NC VCC

/SS6    = /DS * LMS1 +
          /DS * /DSR *  LMS0 */LMS1 * /LMS2 +
          /DS * /DSR *  LMS0 * LMS1 * /LMS2 +
          /DS *  DSR * /LMS0 */LMS1 * /LMS2 * /LRD +
          /DS * NVC * /DSR +
          /DS * NVD *  DSR

/SS2    = BLOCK*ENDBL

DESCRIPTION
THIS PAL GENERATES SS RESPONSES DURING DATACYCLES




PAL16L2
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL11 VERSION 2                         R GELSCHLAEGER   21/10/84

WRC NTC0 NTC1 NTC2 NTC3 NTC4 RDC NC NC GND
NC NC NC NC RDC12 RDC11 RDC7 RDC3 RDC0 VCC

/RDC0   = /RDC *  /NTC0*/NTC1*/NTC2*/NTC3*/NTC4
/RDC3   = /RDC *   NTC0* NTC1*/NTC2*/NTC3*/NTC4
/RDC7   = /RDC *   NTC0* NTC1* NTC2*/NTC3*/NTC4
/RDC11  = /RDC *  NTC0*/NTC1*/NTC2*/NTC3* NTC4
/RDC12  = /RDC * /NTC0* NTC1*/NTC2*/NTC3* NTC4

DESCRIPTION
THIS PAL GENERATES CSR READ CYCLES




PAL16L8
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL12 VERSION 2                         R GELSCHLAEGER   21/10/84

WRC NTC0 NTC1 NTC2 NTC3 NTC4 PIPE BWT NC GND
NC NC LDW WRC12 WRC11 WRC10 WRC7 WRC3 WRC0 VCC

/WRC0   = /WRC *  /NTC0*/NTC1*/NTC2*/NTC3*/NTC4
/WRC3   = /WRC *   NTC0* NTC1*/NTC2*/NTC3*/NTC4
/WRC7   = /WRC *   NTC0* NTC1* NTC2*/NTC3*/NTC4
/WRC10  = /WRC *  NTC0*/NTC1*/NTC2*/NTC3* NTC4
/WRC11  = /WRC *  NTC0*/NTC1*/NTC2*/NTC3* NTC4
/WRC12  = /WRC *  /NTC0* NTC1*/NTC2*/NTC3* NTC4
/LDW    = /BWT + PIPE

DESCRIPTION
THIS PAL GENERATES WRITE CYCLES CSR SPACE AND CONTROLSIGNAL
FOR WAIT LATCH
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PAL16L4
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL16 VERSION 1                         R OELSCHLAEGER   21/10/84

AD0 AD1 AD2 AD3 RS0 RS1 RS2 RS3 NC GND
CLNT WRC10 CLBC CL3 CL2 CL1 CL0 NC NC VCC

/CL0    = /CLNT + /WRC10*AD0 + /CLBC* RS0
/CL1    = /CLNT + /WRC10*AD1 + /CLBC* RS1
/CL2    = /CLNT + /WRC10*AD2 + /CLBC* RS2
/CL3    = /CLNT + /WRC10*AD3 + /CLBC* RS3

DESCRIPTION
THIS PAL GENERATES CLEAR PULSES FOR SCALER CHANNELS


PAL16L6
STR200 100MHZ SCALER                    DR B STRUCK COMPANY
PAL16 VERSION 2                         R OELSCHLAEGER   21/10/84

BB BH PON WRC0 AD30 AD31 AD7 EXTCLR NC GND
NC NC CLCNT INC CLBC NC RESPRT RESALL RESALLI VCC

/CLCNT  = AD31*/WRC0 + /RESALLI + EXTCLR
/RESALL = /PON + /BH*RB + /WRC0*AD30
/CLBC   = /PON + /WRC0*AD30
/INC    = /WRC0*AD7
/RESPRT = /PON + /BH*RB

DESCRIPTION
THIS PAL GENERATES RESET SIGNALS AND TESTINCREMENT SIGNAL


PAL16L6
STR200 100MHZ SCALER                    DR.B.STRUCK COMPANY
PAL16 VERSION 1                         R OELSCHLAEGER   21/10/84

RDC11 RDC11 RDC7 RDC3 SECRDD SECRDC RDC RDD RDC0 GND
NC NC NC NC EN1631 EN2115 EN07 NC NC VCC

/EN07    = RDD*RDC*SECRDC*SECRDD
/EN2115  = RDD*RDC3*RDC7*RDC11*RDC12
/EN1631  = RDD*RDC0*RDC11*RDC12*RDC3

DESCRIPTION
THIS PAL GENERATES ENABLE SIGNALS FOR FASTBUS READ BUFFERS


PAL16R4
VERSION 2  R OELSCHLAEGER
FB SCALER PAL IN COUNT CHANNEL

NC ADEL A RQ NC BDEL B NC NC GND
NC GNTBI GNTB CLKB STRB STRA CLKA GNTA GNTAI VCC

CLKA = /A*ADEL
CLKB = /B*BDEL
GNTA = RQ*A + RQ*/ADEL + RQ*GNTAI
GNTB = RQ*B + RQ*/BDEL + RQ*GNTBI
STRA = GNTAI
STRB = GNTBI

DESCRIPTION
THIS PAL IS STEERING THE SHADOW REGISTER OF ONE SCALER CHANNLE
STR200 100 MHZ FB SCALER 32 BIT
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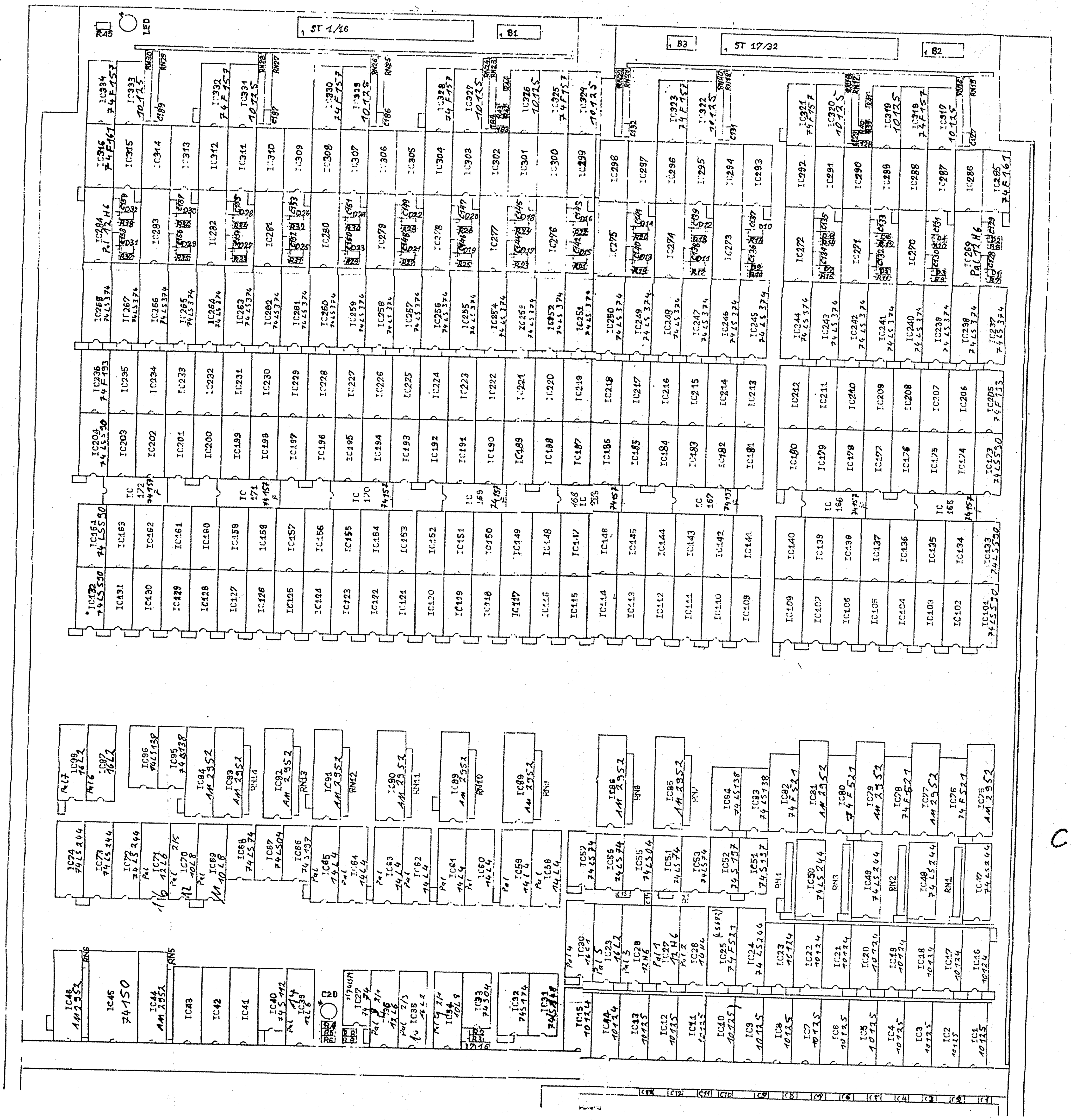
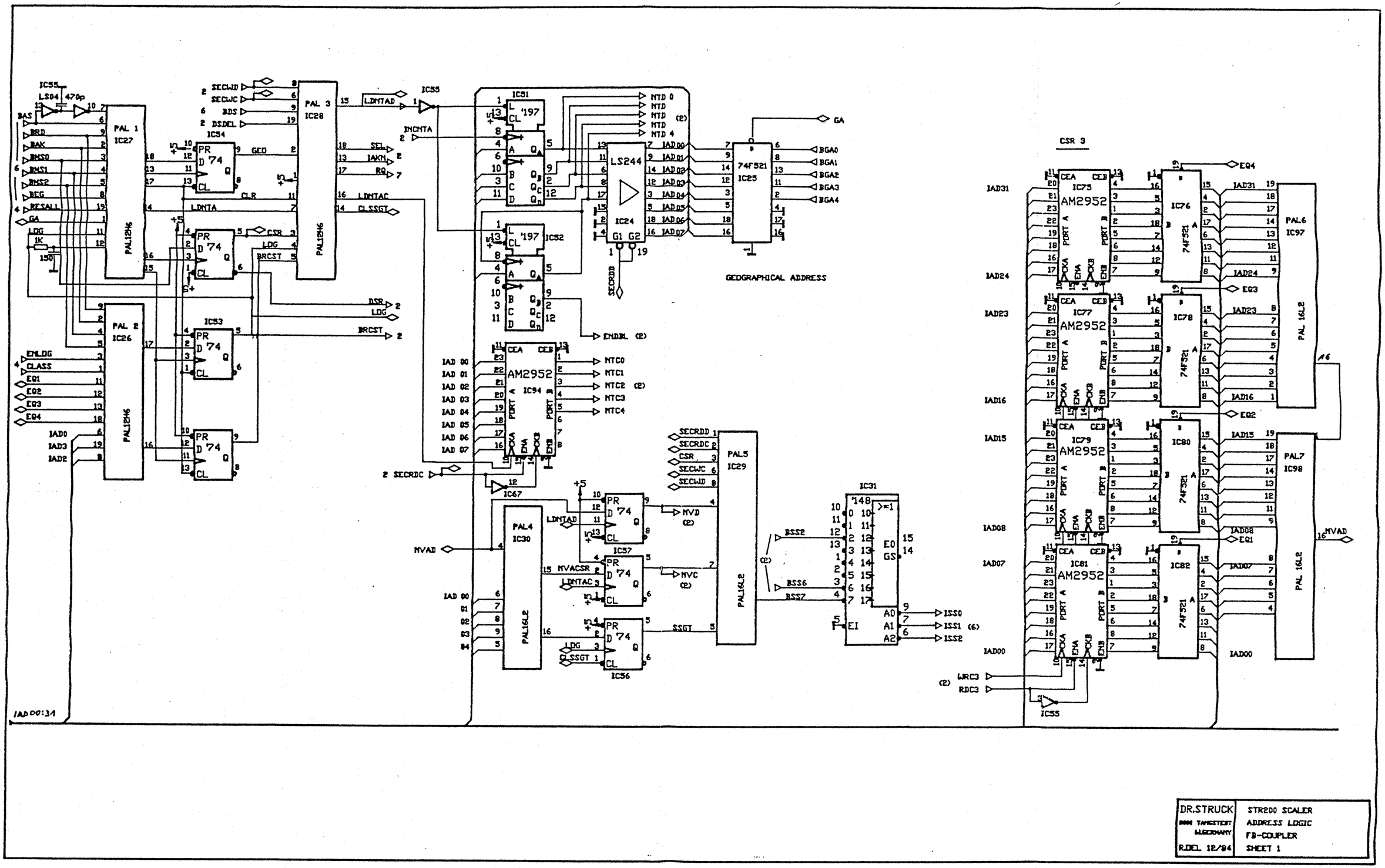
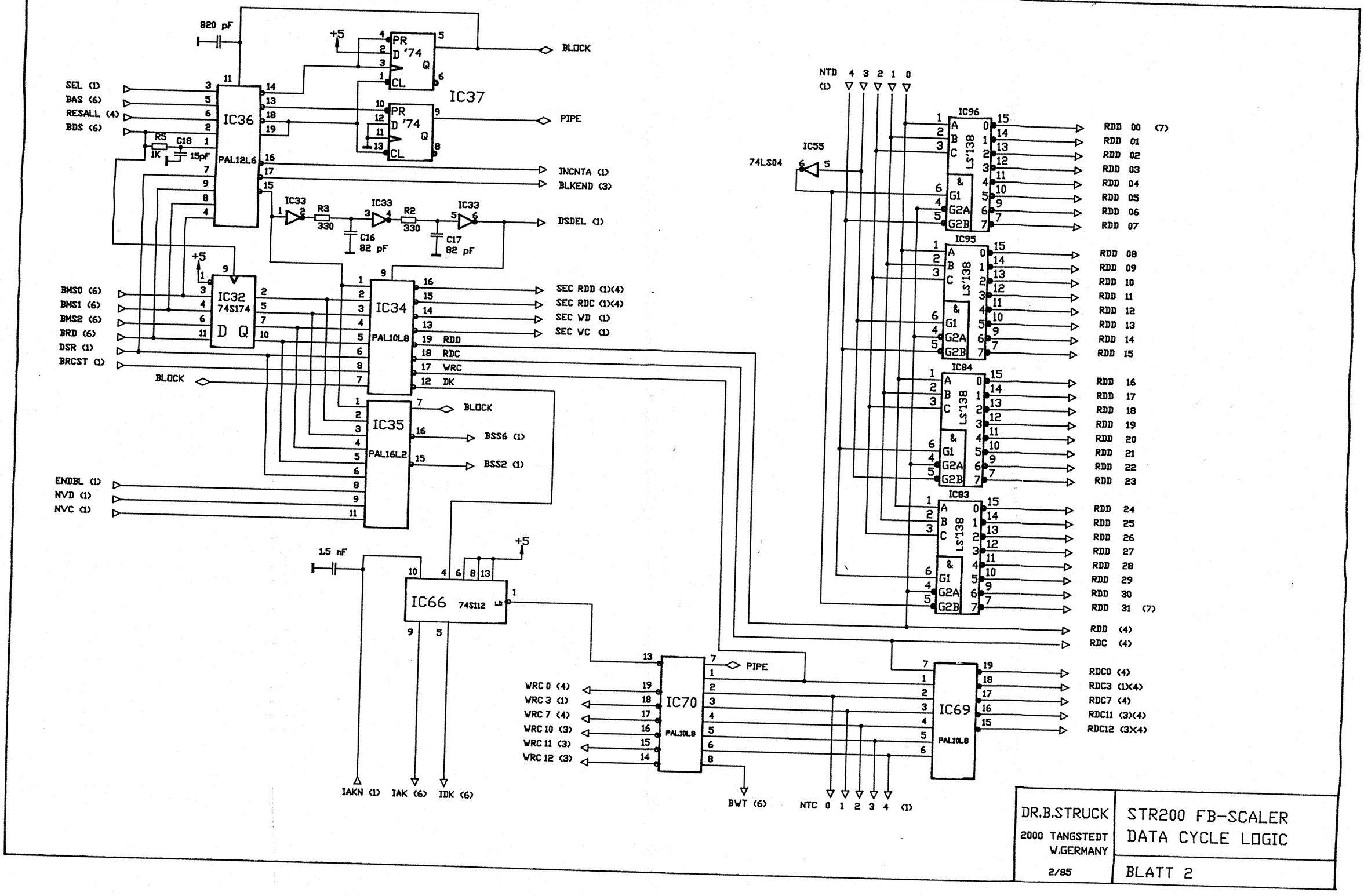


Component Layout
STR200


IC55
LS04
470p
PAL 1
IC27
PAL 2
IC26
PAL 3
IC28
PAL12H6
PAL16L8
PAL4
IC30
PAL5
IC29
PAL6
IC97
PAL7
IC98
IC51
IC52
IC53
IC54
IC56
IC57
IC67
IC24
LS244
74F521
IC25
AM2952
IC94
IC75
IC76
IC77
IC78
IC79
IC80
IC81
IC82
IC31
'148
'197
'74
BAS
BRD
BAK
BMS0
BMS1
BMS2
BEG
RESALL
GA
LDG
1K
150
EMLDG
CLASS
EQ1
EQ2
EQ3
EQ4
IAD0
IAD3
IAD2
SECWD
SECWC
BDS
DSDEL
GEO
CLR
LDNTA
CSR
BRCST
DSR
LDNTAD
INCNTA
SEL
IAKN
RQ
LDNTAC
CLSSGT
NTD 0
NTD
NTD
NTD
NTD 4
IAD 00
IAD 01
IAD 02
IAD 03
IAD 04
IAD 05
IAD 06
IAD 07
SECRDB
ENDBL (2)
NTC0
NTC1
NTC2 (2)
NTC3
NTC4
SECRDD
SECRDC
NVD (2)
NVC (2)
SSGT
NVAD
NVACSR
BSS2
BSS6
BSS7
ISS0
ISS1 (6)
ISS2
BGA0
BGA1
BGA2
BGA3
BGA4
GEOGRAPHICAL ADDRESS
CSR 3
IAD31
IAD24
IAD23
IAD16
IAD15
IAD08
IAD07
IAD00
EQ4
EQ3
EQ2
EQ1
WRC3
RDC3
IAD00:31
DR.STRUCK
STR200 SCALER
ADDRESS LOGIC
FB-COUPLER
R.DEL 12/94
SHEET 1


820 pF
+5
IC37
BLOCK
PIPE
SEL (1)
BAS (6)
RESALL (4)
BDS (6)
IC36
PAL12L6
R5
1K
C18
15pF
INCNTA (1)
BLKEND (3)
IC33
R3
330
R2
330
C16
82 pF
C17
82 pF
DSDEL (1)
IC32
74S174
BMS0 (6)
BMS1 (6)
BMS2 (6)
BRD (6)
DSR (1)
BRCST (1)
IC34
PAL10L8
SEC RDD (1)(4)
SEC RDC (1)(4)
SEC WD (1)
SEC WC (1)
RDD
RDC
WRC
DK
IC35
PAL16L2
BSS6 (1)
BSS2 (1)
ENDBL (1)
NVD (1)
NVC (1)
1.5 nF
IC66
74S112
IAKN (1)
IAK (6)
IDK (6)
IC70
PAL10L8
WRC 0 (4)
WRC 3 (1)
WRC 7 (4)
WRC 10 (3)
WRC 11 (3)
WRC 12 (3)
BWT (6)
IC69
PAL10L8
NTC 0 1 2 3 4 (1)
NTD (1)
IC55
74LS04
IC96
IC95
IC84
IC83
LS'138
RDD 00 (7)
RDD 01
RDD 02
RDD 03
RDD 04
RDD 05
RDD 06
RDD 07
RDD 08
RDD 09
RDD 10
RDD 11
RDD 12
RDD 13
RDD 14
RDD 15
RDD 16
RDD 17
RDD 18
RDD 19
RDD 20
RDD 21
RDD 22
RDD 23
RDD 24
RDD 25
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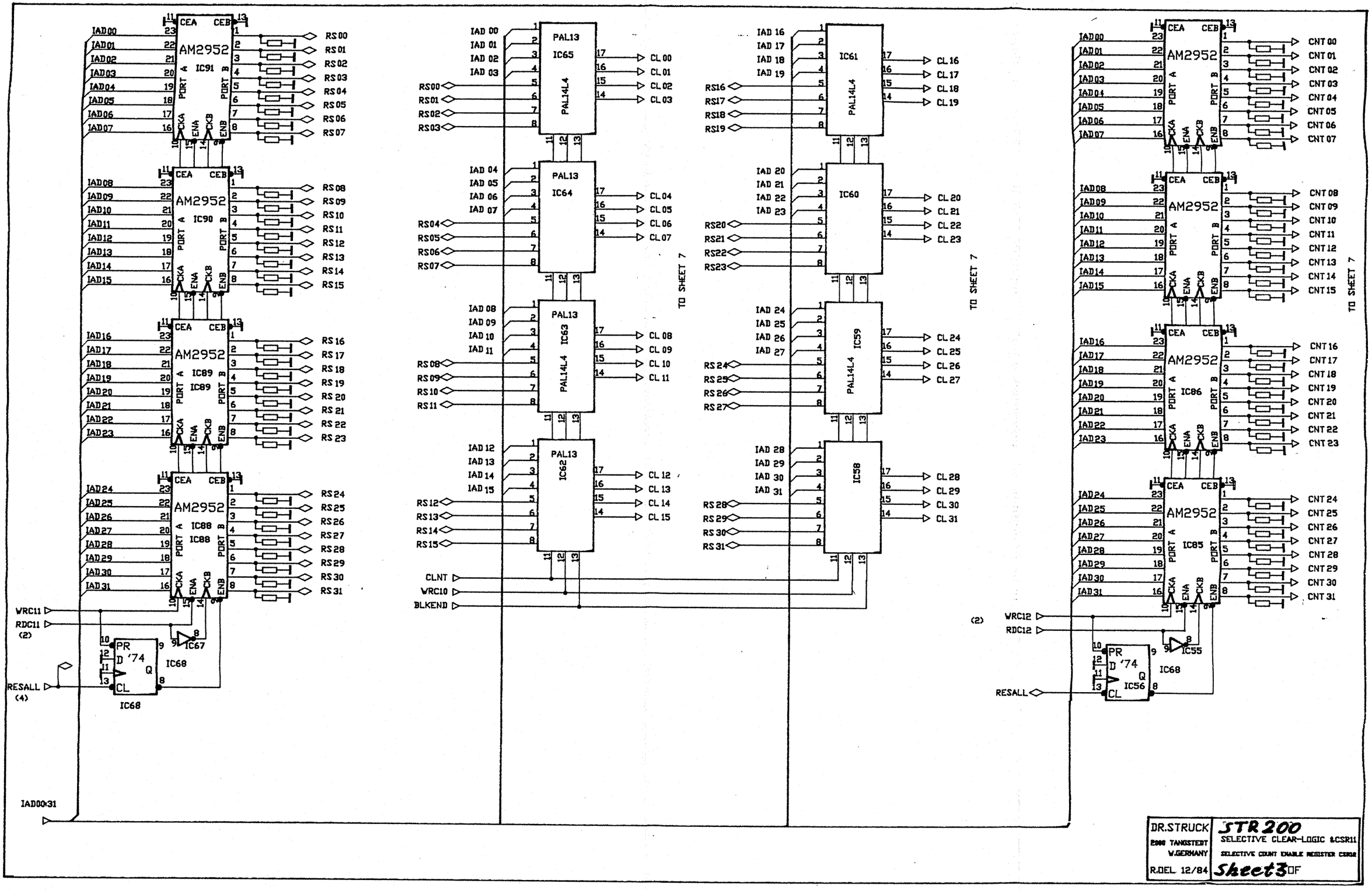
RDD (4)
RDC (4)
RDC0 (4)
RDC3 (1)(4)
RDC7 (4)
RDC11 (3)(4)
RDC12 (3)(4)
DR.B.STRUCK
2000 TANGSTEDT
W.GERMANY
2/85
STR200 FB-SCALER
DATA CYCLE LOGIC
BLATT 2


IC91
IC90
IC89
IC88
IC87
IC86
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IC84
IC83
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IC81
IC80
IC79
IC78
IC77
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PAL13
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CEA
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IAD28
IAD29
IAD30
IAD31
IAD00:31
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CL29
CL30
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CNT01
CNT02
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CNT05
CNT06
CNT07
CNT08
CNT09
CNT10
CNT11
CNT12
CNT13
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CNT16
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CNT18
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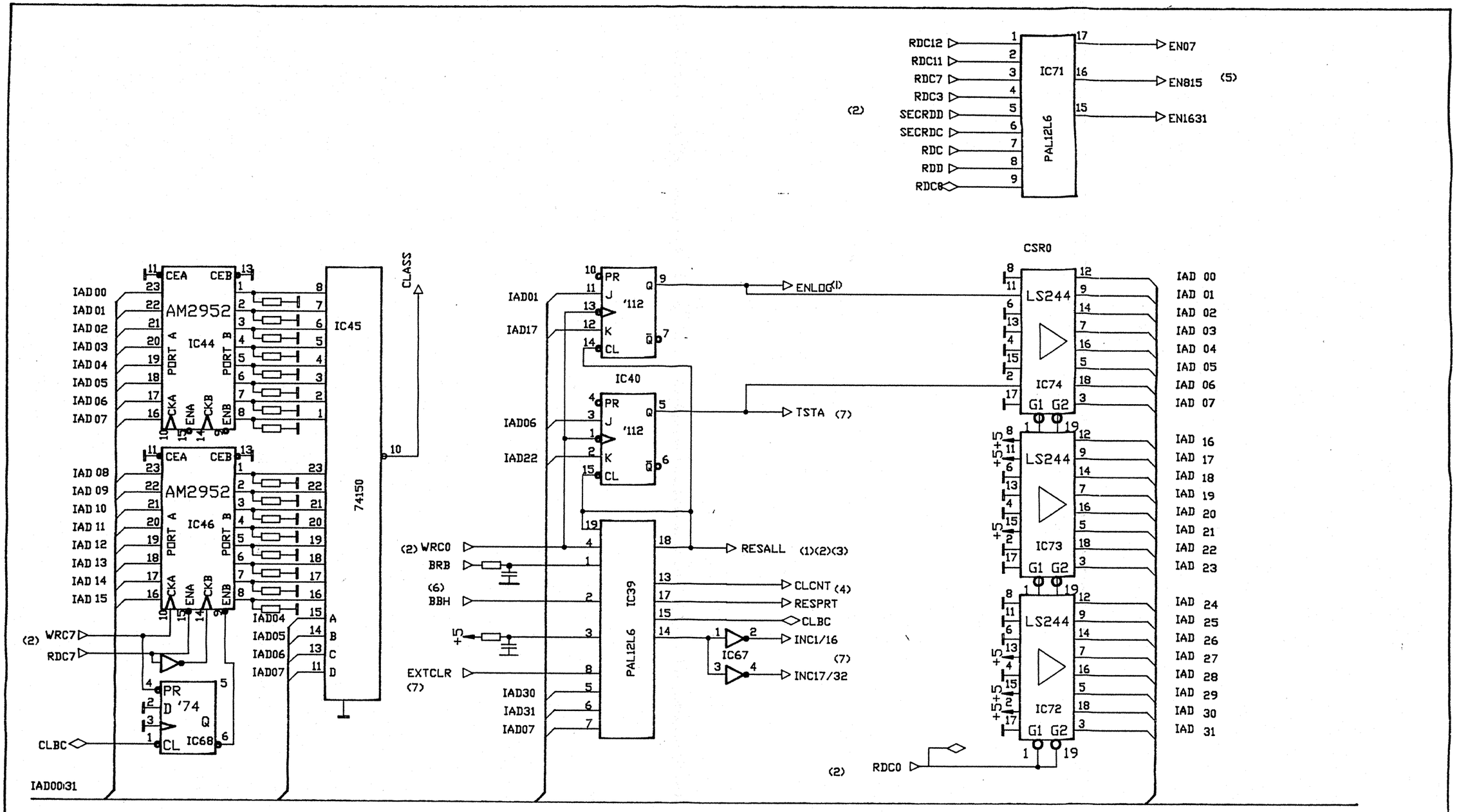
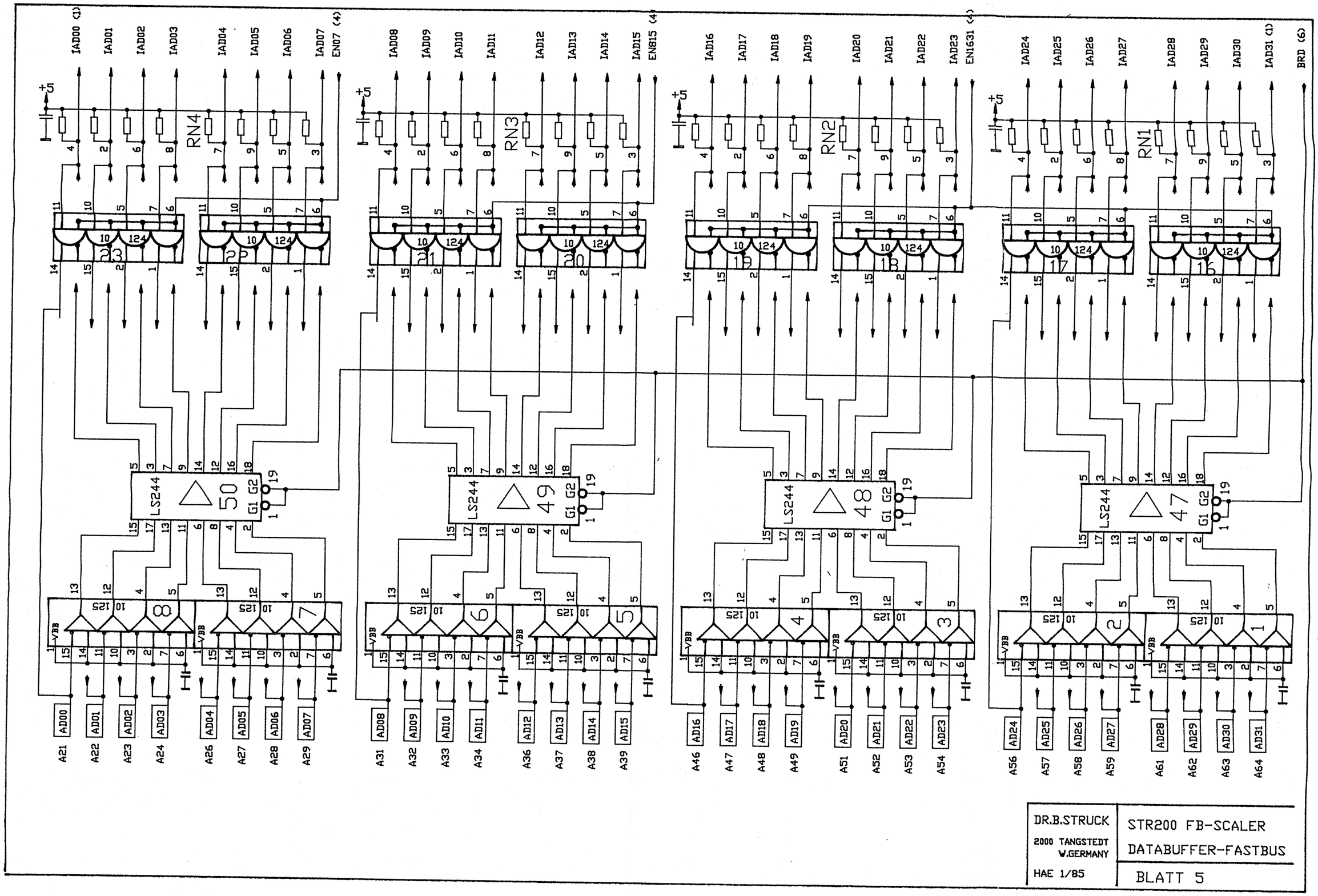
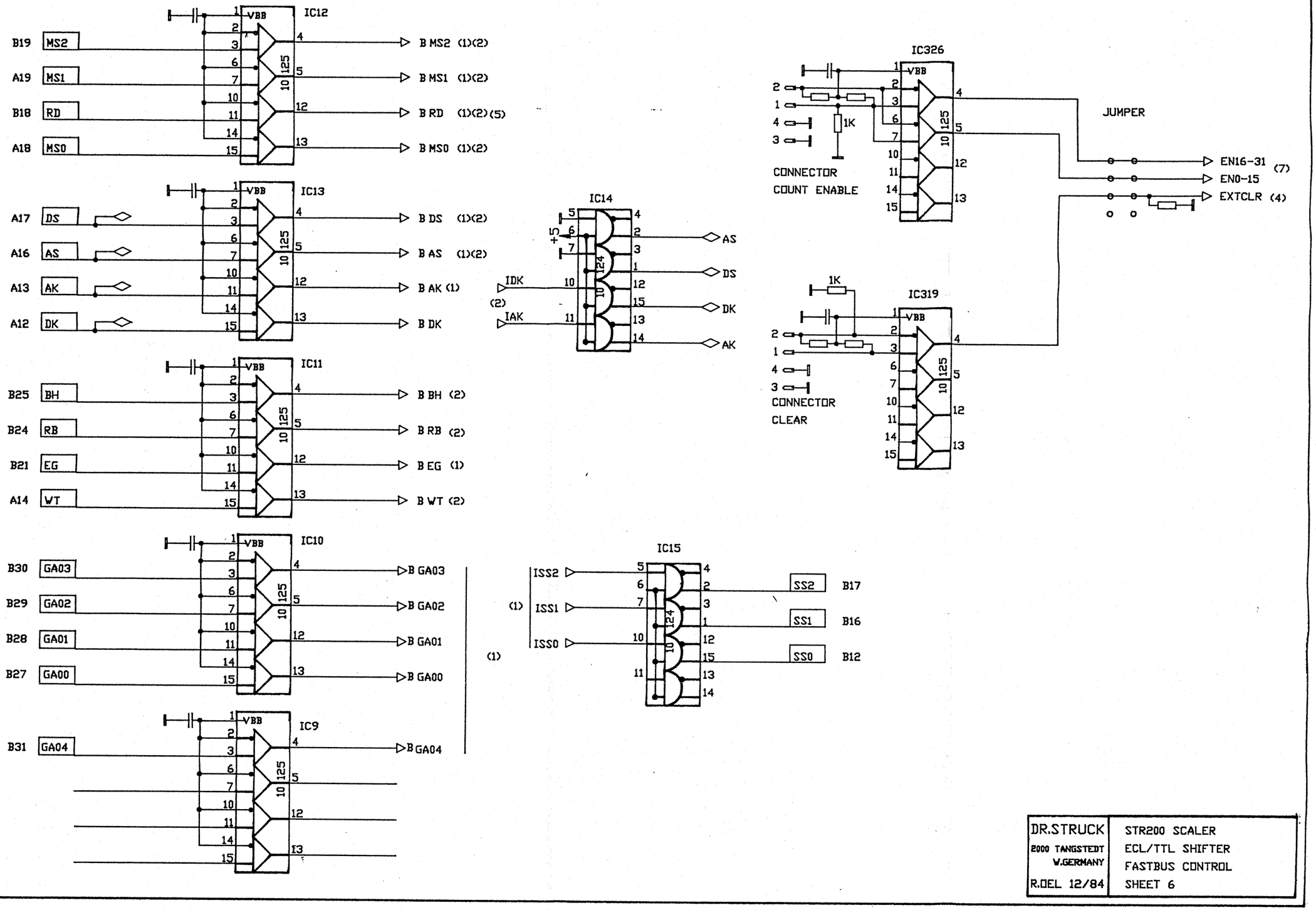
CNT28
CNT29
CNT30
CNT31
WRC11
RDC11
(2)
RESALL
(4)
CLNT
WRC10
BLKEND
WRC12
RDC12
TO SHEET 7
DR.STRUCK
2000 TANGSTEDT
W.GERMANY
R.DEL 12/84
STR200
SELECTIVE CLEAR-LOGIC &CSR11
SELECTIVE COUNT ENABLE REGISTER CSR12
Sheet3 OF



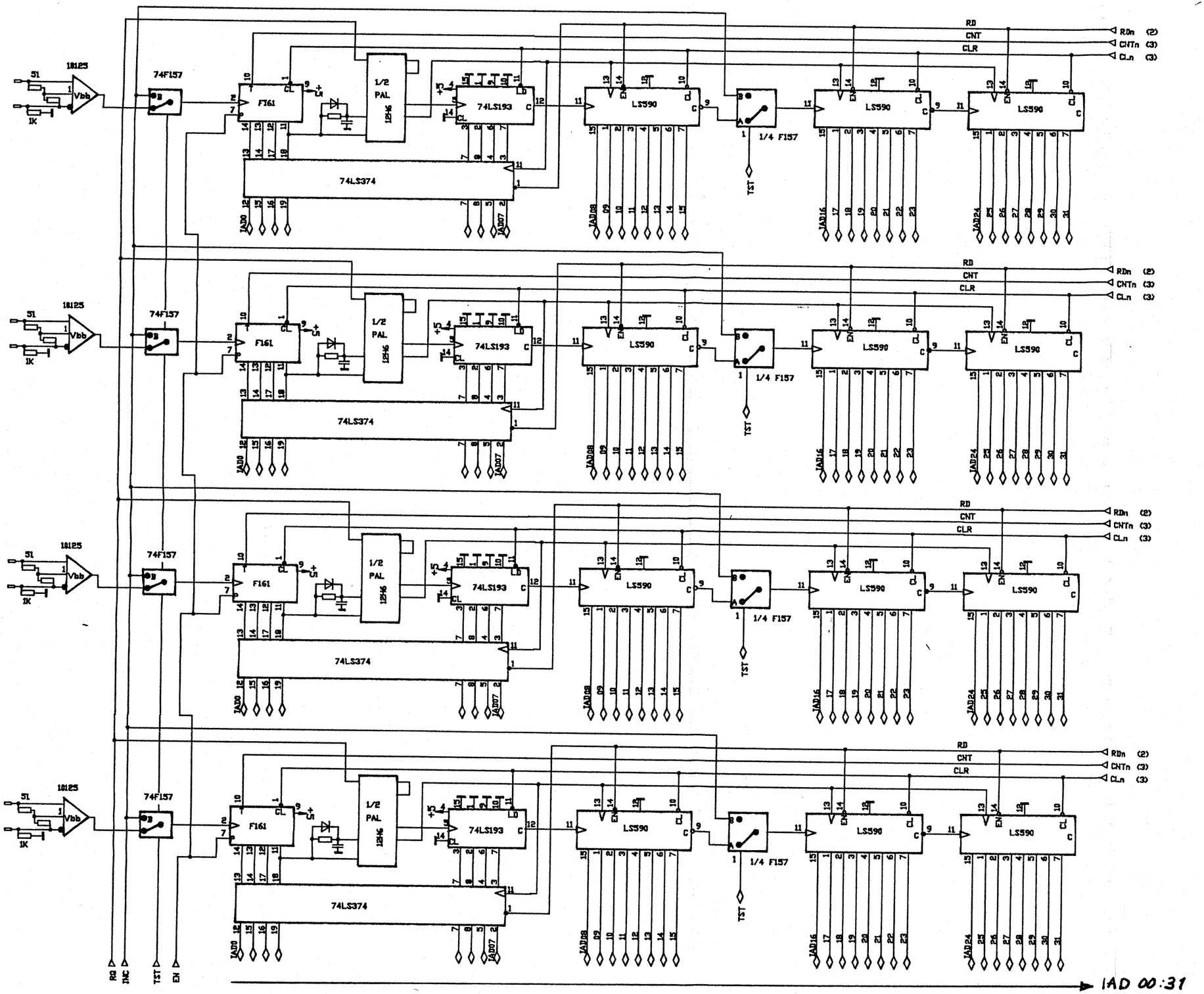
DR.STRUCK 2000 TANGSTEDT W.GERMANY R.DEL 12/84	STR200 SCALER CSR0, CSR7 RESET LOGIC SHEET 4



DR.B.STRUCK 2000 TANGSTEDT W.GERMANY HAE 1/85	STR200 FB-SCALER DATABUFFER-FASTBUS BLATT 5



DR.STRUCK 2000 TANGSTEDT W.GERMANY R.OEL 12/84	STR200 SCALER ECL/TTL SHIFTER FASTBUS CONTROL SHEET 6



STR200
Scaler
4 of 32 channels
Sheet 7