ADM1224F

24-Channel, 12-Bit, ±10 Volt
Differential-ended-input, Multiplexed
Analog-to-Digital Converter IPack

Document No. B-T-MU-ADM1224F-A-0-A1

PRELIMINARY DOCUMENT

FOREWORD

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GLOSSARY

[x:y] Bit-range designation (in descending decimal) , where "x" is the most significant bit down to "y", the least significant bit. (e.g. IPD[15:0] refers to the IPD bus where bit 15 is the most significant bit, bit 0 is the least significant bit, and there are 16 bits).

Accuracy *ABSOLUTE*: The error of an ADC at a given output code is the difference between the theoretical and actual analog input voltages required to produce that code.

RELATIVE: The deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

acquire The process of selecting and capturing an analog signal for the process of developing its digital representation. The capturing operation is usually performed by a sample/hold or track/hold amplifier.

active filter A signal filter that uses an amplifier with conventional passive filter elements to provide a desired fixed or tunable pass or rejection characteristic.

ADC Analog-to-Digital Converter; a device which translates continuous analog signals into proportional discrete digital signals.

aliasing error (*over-simplified*) The unrecoverable error in converted data that occurs when sampling an analog signal whose bandwidth is not limited (*by a low-pass filter*) to less than half of the sampling frequency to an amplitude of at least -72dB for a twelve bit ADC.

analog mux Also known as an analog multiplexer, it provides switching of analog input signals to allow use of a common analog→digital converter.

analog signal A nominally continuous electrical signal that varies in amplitude or frequency in response to changes in physical phenomenon, such as sound, light, heat, position, or pressure.

AREF Analog REFerence, common, or ground.

bipolar mode A configuration that an ADC uses to handle signal spans containing both positive and negative signals. Usually it means offsetting half-scale to become analog zero, and accepting the resulting offset binary code or changing it to two's complement coding.

buffer amp An operational amplifier used after a critical stage to isolate it from the effects of load impedance variations in subsequent stages.

byte 8 contiguous bits on octal boundaries. (e.g. IPD[15:8], and IPD[7:0]).

byte-lane Byte position description. (e.g. IPD[15:8] is the "*high*" byte-lane, also defined as "*byte-lane ONE*"; whereas IPD[7:0] is the "*low*" byte-lane, also defined as "*byte-lane ZERO*").

CAD Computer-Aided Design.

CAE Computer Aided Engineering.

clipper-limiter A device whose output is a function of the instantaneous input amplitude for a range of values lying between two predetermined limits but is approximately constant, at another level, for input values above the range.

CMR Common-Mode Rejection. The ability of an amplifier to cancel a common-mode signal while responding to an out-of-phase signal, often through variation of a ground level.

CMRR Common-Mode Rejection Ratio is the ratio of gain for the differential,or normal-mode, signal to the gain for the common-mode signal.

CMS Common-Mode Signal. A signal applied equally to both ungrounded inputs of a balanced amplifier stage or other differential device.

conversion rate The number of complete conversions an analog-to-digital converter can perform per unit time, usually specified in conversions per second per channel.

CRC Cyclic Redundancy Check.

CVT Current Value Table consisting of twenty-four current value registers.

differential as in input; a circuit that rejects voltages that are the same at both (+ & -) input terminals and amplifies the voltage difference between the two input terminals.

DNL Differential Nonlinearity (*see nonlinearity*).

doublewide An IPack module that is physically and electrically two side-by-side singlewide IPacks.

EPLD Erasable Programmable Logic Device.

endoframe Short pulse driven out the N_STROBE logic signal line to the host carrier indicating when channel #24 has just had its ADC and frame count information written to the CVT; also internally increments the frame counter.

ENOB Effective Number Of Bits. For a sine wave, the signal-to-noise ratio can be expressed in terms of the number of bits.

$$ENOB = (SNR - 1.76) \div 6.02.$$

frame One complete pass through all twenty-four channels.

frame time Time per frame = 70 µs. The reciprocal of this is the sampling-rate per channel.

gain error The deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions.

GRAYbus Gray Code Engine bus (testpoints) designated as: GRAY[6:0].

IAMP Instrumentation Amplifier; differential-input, single-ended output. Usually is a closed-loop fixed-gain amplifier, with very high input impedance, low drift, and high common-mode rejection over a wide range of frequencies.

Id Drain current of MUX; usually in context with ON and OFF leakage current specifications.

Idiff Differential, OFF-state output leakage current for differential multiplexers, where the first channel experiences plus-full-scale on the non-inverting input and minus-full-scale on the inverting input, and the adjacent channel is driven with plus-full-scale on the inverting input and minus-full-scale on the non-inverting input.

ID PROM Identification Programmable Read Only Memory, emulated within the EPLD providing the required identification information about the IPack.

INL Integral Nonlinearity (*see nonlinearity*)

IndustryPack see IPack.

I/O Input/Output.

IPAbus IPack Address bus designated as: IPA[6:1].

IPack Business-card size mezzanine-type boards that provide general and special-purpose input and output functions to and from their host carriers. An open industry standard defines the mechanical and electrical interface to the carrier board, which can be a bus converter or a standalone, embedded host.

IPDbus IPack Data bus designated as: IPD[15:0].

Is Source current of MUX; usually in context with ON and OFF leakage current specifications.

KHz KiloHertz, thousands of cycles per second.

LSB Least Significant Bit = 20 Volts ÷ 4096 = 4.8828 mVolts.

lowpass filter A passive or active filter that transmits alternating current below a given cutoff frequency and substantially attenuates all other currents.

monotonic a specification that guarantees no missing codes such that every code combination appears in an increasing sequence as the analog input level is increased.

MTBF Mean Time Between Failures.

multiplexer see Analog Mux.

MUXAbus MUltipleXer 'A' (address) bus, designated as: MUXA[2:0]. These three signals provide the address that define which of the eight channels, from 1 → 8, that are presented to its subsequent differential amplifier and ADC.

MUXBbus MUltipleXer 'B' (address) bus, designated as: MUXB[2:0]. These three signals provide the address that define which of the eight channels, from 9 → 16, that are presented to its subsequent differential amplifier and ADC.

MUXCbus MUltipleXer 'C'(address) bus, designated as: MUXC[2:0]. These three signals provide the address that define which of the eight channels, from 17 → 24, that are presented to its subsequent differential amplifier and ADC.

nA nanoamperes, or 10^n Amps, where "n" = -9.

nonlinearity *DIFFERENTIAL:* An ideal ADC provides code transitions that are 1LSB apart. Differential nonlinearity is the maximum deviation, expressed in LSBs, from this ideal value.

INTEGRAL: The worst case deviation of a code from a best-fit straight line between "zero" and "full scale".

nS nanoseconds, or 10^n Seconds, where "n" = -9.

offset error The deviation of the actual MSB code change to the ideal of ½LSB below analog common. See "2's complement", below.

ρC picoCoulombs, or 10^n Coulombs, where "n" = -12, unit of electrical charge

PSRR Power Supply Rejection Ratio. Often referred to in amplifier specifications, it is the equivalent change at the input due to variations in the power supply. For an amplifier with a gain of 1, a PSRR of 10mV/V will provide 10mVolts of change on the output for every volt of change on the power supply.

Qinj Charge Injection; also charge transfer. In multiplexers, this is the transfer of charge (energy) from the switch driver to the output capacitance after a switch turns off.

QSOP Quarter-sized Small Outline (surface mount) Packages.

RDSon A Multiplexer's series ON-channel resistance measured between the source ("S") input and the drain ("D") output terminals under specified conditions.

SADDbus SRAM's ADDress bus, designated as: SADD[4:0]. These five address lines provide the proper location addressing function for reads from and writes to the SRAM, which is the CVT.

SAR Successive Approximation (shift) Register type of ADC.

SNR The measured Signal-to-Noise Ratio at the output of the ADC, usually including harmonic distortions, logarithmically expressed in decibels. The ideal is: *SNR = (6.02***N** *- 1.76) dB*, where **N** = bits of resolution.

settling time Also known as the transient response time, the settling time of an ADC is the time required for the ADC to settle to rated accuracy after the application of a full-scale step input in either direction.

single-ended as in input; unbalanced and not differential, and one side of the transmission line or circuit is usually referenced to analog common or ground.

singlewide The most common size (and smallest) physical IPack size (3.9″ by 1.8″).

span The full scale analog input ranged; = ±10.000 Volts.

SRAMDbus Static Random Access Memory Data bus designated as: SRAMD[15:0]. The nibble consisting of SRAMD[15:12] contains the frame count information while the 1½ bytes consisting of SRAMD[11:0] contains the ADC information.

switching time The time required for a multiplexer to switch and slew from one analog input channel to another analog input with a full-scale differential between inputs with a high impedance output load.

2's complement Output coding: 800*hex* @ -10.000 Volts input → FFF*hex* @ ≈-0.005 Volts input; 000*hex* @ 0.000 Volts input → 7FF*hex* @ +9.995 Volts input.

µS microseconds, or 10^{n} where "n" = -6.

VHDL Very High speed integrated circuit Hardware Description Language, used, with synthesis, for EPLD logic development.

VIN+# The non-inverting input for differential inputs applied to the ADM1224F IPack; also the only input for single-ended inputs. # ≡ 1 → 24 channel numbers.

VIN-# The inverting input for differential inputs; or ground (optionally on-board jumpered) for single-ended inputs. # ≡ 1 → 24 channel numbers.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for SYSTRAN's 24-channel, 12-bit, ±10 Volt differential-ended-input, Multiplexed Analog→Digital Converter IndustryPack (also called IPack) board, referred to in this manual as the ADM1224F (part number BHAS-ADM1224F).

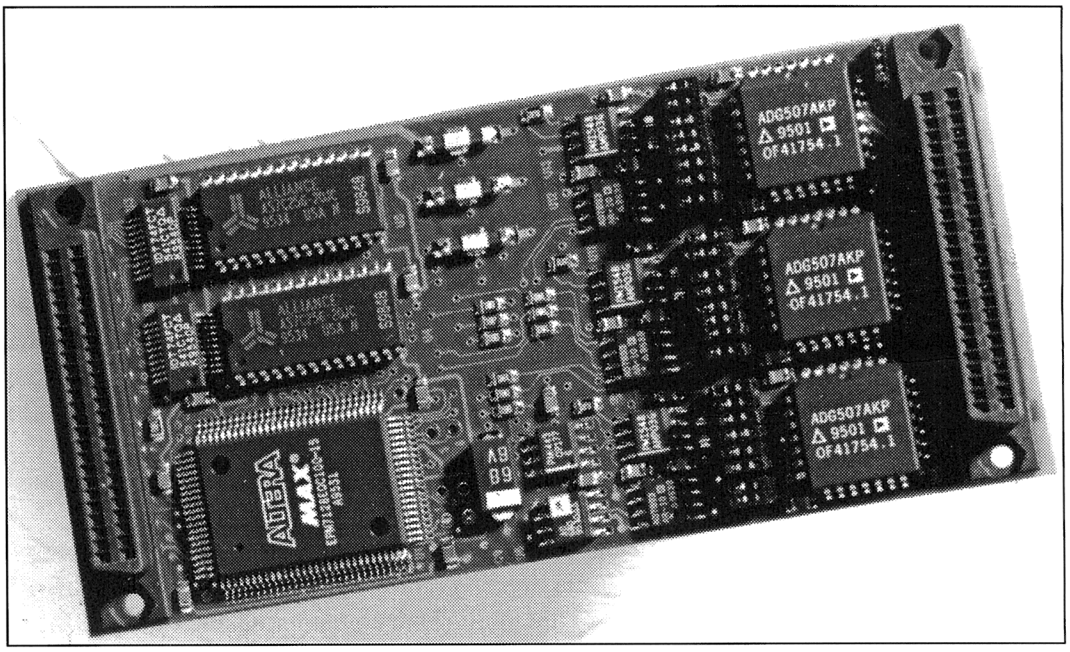


Figure 1-1 ADM1224F Board

1.2 Scope

This reference manual covers the physical and operational description of the ADM1224F, both from hardware and software perspectives. This manual also contains detailed technical information about the ADM1224F's performance characteristics, and some typical applications. The reader should have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The ADM1224F is a singlewide IPack board, conforming both mechanically and electrically to the *IndustryPack Logic Interface Specification, revision 0.7.1.* For a typical (non-SYSTRAN) IPack carrier that holds four IPacks, the ADM1224F can provide up to 96 channels of high-performance ADCs in a single slot on a computer bus backplane, or be mixed with other IPacks for a more customized, modular I/O system solution. Using SYSTRAN's carriers, up to 120 channels of ADCs may be installed in a single VME slot, or (still more) 144 in a single ISA slot.

The ADM1224F is designed to maintain the highest possible accuracy and performance characteristics by minimizing analog errors in the design by using the best (yet, reasonably affordable) components for the tasks to be accomplished. The board level accuracy is also maximized by the inclusion of good ground plane and power filtering design, and by the exclusion of on-board range selectors, gain blocks, offset circuits, anti-aliasing filters, and other special-purpose circuits, thereby providing the user more accuracy for the 12-bits of resolution in the captured and converted data.

1.3.1 The Name

The product name of ADM1224F consists of several descriptive components. The "AD" portion indicates its primary function of performing analog→digital conversions. The "M" indicates that this board has a multiplexed, analog front-end design. This means that several channels share an analog→digital converter, with their channel-switching function being implemented with an analog multiplexer. If there had been dedicated converters per channel, the leading characters would have been "ADC", as they are on the ADC128F1 IPack. The next "12" field indicates the number of bits of resolution (not accuracy). The next "24" indicates how many analog input channels are available. The last "F" indicates that the input range is fixed and that the span is ±10 Volts. There is no embedded designator for the significant feature of differential-ended-inputs.

1.3.2 Features

- Twenty-four multiplexed channels of switched capacitor SAR-based ADCs with all channels sampling and converting at a free-run and completely determinsitic rate of over 14,285 samples/second/channel, with a board total of over 342,857 samples/second.
- All samples provide 12-bits of resolution, and the ADC used has an impressive 11.33 Effective Number Of Bits (not accuracy).
- All twenty-four channels feature true, differential-ended-inputs spanning ±10volts full scale, feeding (gain = 1) instrumentation amplifiers.
- Automatic power-up of all channels sampling and updating the current value table (CVT).
- The CVT provides no-wait, read-on-the-fly IPack accesses to the latest ADC data.
- 4-bit Frame counter data on top of ADC data in CVT, incremented per pass of 24 channels.
- End-of-frame pulse provided via "N_STROBE" signal on Logic Connector per pass of 24 channels.
- Three sets of multiplexers, instrumentation amplifiers, and ADCs time staggered; 1 per 8 channels.
- The ADCs' relative and differential nonlinearities are guaranteed to ±1 LSB (max.).
- Precision +2.500 Volt ADCs' sampling reference optionally sampled as channel #24.
- Analog (ground) reference jumpers to "inverting" inputs on-board for single-ended inputs for all channels.
- All (on-board filtered) power is obtained from the host carrier.
- Gray Code sequence engines used (where possible) for minimum on-board generated digital noise.
- Embedded analog ground plane for "quiet" operations.

- Theoretical output data coding is two's complement: 800 *hex* @ -10.000 Volts input → FFF *hex* @ ≈-0.005 Volts input; 000 *hex* @ 0.000volts input → 7FF *hex* @ +9.995 Volts input.

1.4 Specifications

MECHANICAL: SINGLEWIDE IPACK

- Measurements: 1.800″ x 3.900″ x 0.303″ (connectors, above board)
  4.572 x 9.906 x 0.770 cm
  NOTE: 0.234″ (0.595 cm) maximum component (non-connector) height
- Weight: 1.104 oz., 31.3 grams
- Board thickness: 0.062″ (0.157 cm) nominally, (4 layer)

PROTOCOL: SINGLEWIDE IPACK TRANSFERS

- 8 MHz clock rate
- No WAIT cycles inserted on any valid transfer types
- HOLD cycles supported on all valid transfer types supported
- Complete (no partial) address decoding
- Twenty-four I/O locations:
  - 16-bit read-only, byte lane selects ignored
  - No writes
  - ADC data = IPD[11:0]
  - Frame Counter data = IPD[15:12]
  - Maximum read rate: 4 MTransfers/second, sustained
  - No Acknowledgement for IPA≥18 *hex* or for any write attempts
- Twelve ID locations:
  - 16-bit read-only, byte lane selects ignored
  - No writes
  - ID data = IPD[7:0]
  - Zero-fill = IPD[15:8]
  - SYSTRAN's manufacturer's ID = 45 *hex* = **E** *ASCII*
  - ADM1224F's model number = 6F *hex* = **o** *ASCII*
  - Cyclic Redundancy Check value = **CD** *hex*
  - Maximum read rate: 4 MTransfers/second, sustained
  - No Acknowledgement for IPA≥0C *hex* or for any write attempts
- Memory transfers: not supported; no acknowledgements
- Interrupt Vector transfers: not supported; no acknowledgements
- Interrupt requests: none generated
- DMA activity: none supported
- End-of-frame: ≈63 ns pulse every 70 µs at N_STROBE on Logic Connector

POWER-UP DEFAULT CONDITION

- No accesses permitted or acknowledged during RESET
- All control logic frozen and all counters zeroed during RESET
- Data is not accurate to specification until after ≈25 ms following application of power
- First ADC data entries for channels #1, #9 and #17 following the negation of RESET are indeterminant; valid entries for these channels completed 78.750 µs after the negation of RESET.

AS-SHIPPED CONDITION

- All 24 channels configured as single-ended inputs
- Channel #24 connected to the I/O Connnector; not to the voltage reference

POWER REQUIREMENTS

- Carrier power:
  - +5 Vdc @ 114 mA (all inputs grounded)
  - +12 Vdc @ 9.10 mA (all inputs grounded)
  - -12 Vdc @ 7.79 mA (all inputs grounded)
  - Total: 204 mW
- I/O Connector:
  - Analog (ground) reference common to all analog circuitry; tied to the digital ground on the carrier side of the Logic Connector only (pins 25 and 50)
  - No other I/O Connector power requirements exist

PERFORMANCE CHARACTERISTICS

- Accuracy: Refer to section 5.0 on Performance (histograms & scattergrams)
- Timing: Refer to section 5.0 on Performance (analyzer figures)
- Input Impedance (per channel):
  - Vin+ (Vin- grounded): 50594 Ω, nominal (single-ended configuration)
  - Vin- (Vin+ grounded): 25297 Ω, nominal (inverting single-ended configuration)
  - Differential-ended: 50594 Ω, nominal
- MUX (analog):
  - Analog signal range ±12.000 Volts
  - RDS_{ON} = 280 Ω (typical @ 25°C), 400 Ω (maximum, over temperature)
  - RDS_{ON} match = 5% (typical)
  - I_S = 0.02 nA (OFF, typical input leakage), 50 nA (maximum, over temperature)
  - I_D = 0.04 nA (OFF, typical input leakage), 100 nA (maximum, over temperature)
  - I_D = 0.04 nA (ON, typical input leakage), 100 nA (maximum, over temperature)
  - I_{DIFF} = 25 nA (maximum, over temperature)
  - Q_{INJ} = 4ρC (typical @ 25°C)
  - Maximum continuous current, source or drain, = 20 mA (must be externally limited if overvoltage conditions are possible)
- IAMP (analog):
  - Offset voltage = 25 µV (typical @ 25°C), ±2000 µV (maximum, over temperature)
  - Gain error = 0.001% (typical, full scale, @ 25°C), 0.02% (maximum, full scale, over temperature)
  - CMR = 80dB (minimum @ 25°C), 90dB (typical, over temperature)
  - Slew Rate = 6 V/µs (minimum @ 25°C), 9.5V/µs (typical, over temperature)
  - PSRR = 0.7µV/V (typical @ 25°C), 15 µV/V (maximum, over temperature)
- ADCs (analog):
  - Signal-to-noise (distortion) Ratio = 70 dB minimum for 10 KHz Sine wave input
  - Effective Number of Bits = 11.33
  - Total Harmonic Distortion = -80 dB maximum for 10 KHz Sine wave input
  - Peak Harmonic Distortion = -80 dB maximum for 10 KHz Sine wave input

- Intermodulation Distortion = -80 dB maximum for both 2nd and 3rd order terms (F*a*=9 KHz and F*b*=9.5 KHz)
- Minimum resolution = 12 bits with no missing codes, guaranteed
- Relative accuracy = ±½ LSB (typical), ±1 LSB (maximum)
- Differential nonlinearity = ±1 LSB (typical and maximum)
- Positive full-scale error = ±1½ LSB (typical), ±3 LSB (maximum)
- Bipolar zero (offset) error = ±2 LSB (typical), ±4 LSB (maximum)
- Negative full-scale error = ±1½ LSB (typical), ±3 LSB (maximum)
- Input voltage range = ±10 Volts referenced to "AREF"
- Input resistance = 33 KΩ (typical), 16 KΩ (minimum)
- 1 LSB = 20 Volts ÷ 4096 ≈ 4.88 mV

- REFERENCE (analog):
  - Output voltage = +2.500, ±0.010 Volts (maximum, over temperature)
  - Output voltage drift = 10 ppm/°C (typical), 25 ppm/°C (maximum) = 1.75 mV (typical), 4.375 mV (maximum, over temperature)
  - Output settling time = 25 ms to within 250 µV of final value after application of power

ABSOLUTE MAXIMUM VOLTAGES ‡ :

- Carrier power supplies:
  - +5 Volt supply with respect to ground: -0.3 Volts (minimum), +7.0 Volts (maximum)
  - +12 Volt supply with respect to ground: ≤ +18.0 Volts
  - -12 Volt supply with respect to ground: ≥ -18.0 Volts
- VIN± input range: ±17 Volts (maximum if ±18.0 Volts is supplied by the carrier)
  ±12 Volts (maximum if ±12.0 Volts is supplied by the carrier)
- CMS = ±10volts (maximum, over temperature)

‡ *Stresses above those listed may cause permanent damage to the components on the ADM1224F. Operating the ADM1224F beyond the recommended ratings for extended periods of time may affect reliability.*

MAXIMUM INPUT BANDWIDTH:

- No signal energy ≥ -72 dB in amplitude at frequencies ≥ 7142 Hz to prevent aliasing errors (for single sampling per frame)
- Signals can be supercommutated using even "time" spacing techniques to acquire higher bandwidth signals, to a limit of a maximum frequency of 171.428 KHz (all 24 channels sampling a single signal source; input impedance ≈ 16,865 Ω)

RECOMMENDED OPERATING CONDITIONS:

- Carrier Supply Voltages:
  - +5.00, +0.25/-0.125 Volts, 50 mV maximum peak-to-peak ripple and noise
  - +12.0, +0.60/-0.36 Volts, 50 mV maximum peak-to-peak ripple and noise
  - -12.0, -0.60/+0.36 Volts, 50 mV maximum peak-to-peak ripple and noise
- Input Signals:
  - ±10.000 Volts
  - 7142 Hz (maximum frequency, fundamental and harmonics)
- Recommended carriers: (for "quiet" operations)

- SYSTRAN's VME3SC2 for VME-3U
- SYSTRAN's VMESC5 for VME-6U
- SYSTRAN's ISASC6 for ISA (P.C.'s)

ENVIRONMENTAL SPECIFICATIONS:

- Temperature:
  - Operating: 0°C → +70°C
  - Storage (no bias): -40°C → +85°C
- Humidity (noncondensing): 5% → 95%
- Vibration (operating): 10 G's RMS, 20 Hz → 2000 Hz, random (no jumper shunts installed)
- Shock (operating): 50 G's maximum, all axes (no jumper shunts installed)
- Altitude (operating): 10,000', maximum

MEAN TIME BETWEEN FAILURE (MTBF):

- 1,031,885 hours per MIL-HDBK-217F

1.5 Related Products

Software: 'C' library and OS-9 device driver routines and documentation.
ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.6 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp.(This synopsis is included in this document as Appendix A).
- SYSTRAN I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by GreenSpring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.7 Ordering Process

If you wish to learn more about SYSTRAN products or to place an order, the following contacts are available:

- Phone: **(513) 252-5601**
- E-mail address: **info@systran.com**
- World Wide Web address: **http://www.systran.com/**

1.8 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct any programming questions, any concerns about the functional-fit of this product for your particular application, or any questions not satisfactorily answered by this document, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

Refer to Section 7.0 for warranty and repair information.

1.9 Reliability

SYSTRAN Corporate policy is to provide the highest-quality products in support of a customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

2.0 DESCRIPTION

NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the *IndustryPack Logic Interface Specification Synopsis* included as Appendix A.

2.1 Simplified Block Diagram

Figure 2-1 presents the first of three levels of block diagrams for the ADM1224F IPack.

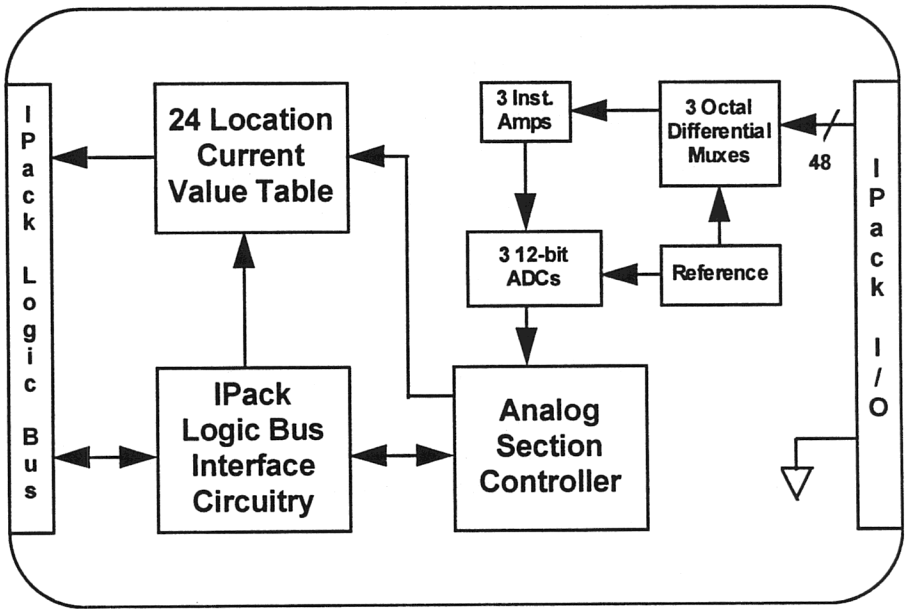


Figure 2-1 ADM1224F Simplified Block Diagram

2.1.1 Simplified Block Descriptions

IPACK LOGIC BUS INTERFACE CIRCUITRY

On the left side of the diagram is the IPack Logic Bus connector through which all transfers between the IPack Carrier and the ADM1224F's registers and data sources are conducted. The block labeled "IPack Logic Bus Interface Circuitry" contains all of the board level access logic that descriminates between valid and invalid access attempts by the carrier, provides the ID PROM data for identification queries, develops the arbitration and access control logic for the SRAM-based current value table, coordinates activities with the analog section controller, and executes all of the IPack transfer sequence/control and data bus interface operations.

24 LOCATION CURRENT VALUE TABLE

This block consists of a pair of Static Random Access Memory (SRAM) devices that function as the Current Value Table (CVT). This table consists of 24 consecutive, 16-bit wide locations that contain the latest (most current) conversion results for all 24 input

channels. From the IPack carrier's perspective, these are read-only, 16-bit only, I/O locations that present all ADC & Frame Count data requests with no wait cycles inserted. The analog section controller coordinates with the IPack Logic Bus Interface Circuitry to perform orderly, error-free deposition of ADC data into the CVT.

ANALOG SECTION CONTROLLER

This block consists of a free-running sequential state machine that controls all of the analog signal selection and conversion activities, data retrieval and serial-to-parallel conversion operations, as well as the writes to the CVT of the conversion results with their appended frame count information. Implied, but not explicitly shown, is a significant connection between the analog section controller and the analog multiplexers.

REFERENCE

The voltage reference is a high-accuracy, buffered source that is the ADCs' conversion analog reference point. This signal is also optionally available as a direct connection into channel #24 for system applications that require continuous monitoring of the voltage reference (hence the connection of the reference to the analog multiplexers box).

3 OCTAL DIFFERENTIAL MUXES

This block depicts the analog signal multiplexers that are configured as three separate eight-to-one-by-two analog signal multiplexers whose channel selections are controlled by the analog section controller's state machine. The input channels are grouped as channels 1 → 8, 9 → 16, and 17 → 24.

3 INST. AMPS

The differential outputs of the three analog multiplexers drive three separate instrumentation amplifiers that convert the inputs to single-ended, buffered signals for the ADCs. When inputs through the multiplexers are configured as differential-ended inputs, these instrumentation amplifiers remove common-mode (noise, offset errors, etc.) signals.

3 12-BIT ADCS

The single-ended outputs of the three instrumentation amplifiers drive the analog inputs to the three 12-bit ADCs. These converters, and their analog signal multiplexers, are time-stagger-controlled by the analog section controller to provide the highest throughput possible with maximum signal settling time (for the highest accuracy possible). The data is retrieved from the ADCs in serial format for eventual deposition of the data into the CVT.

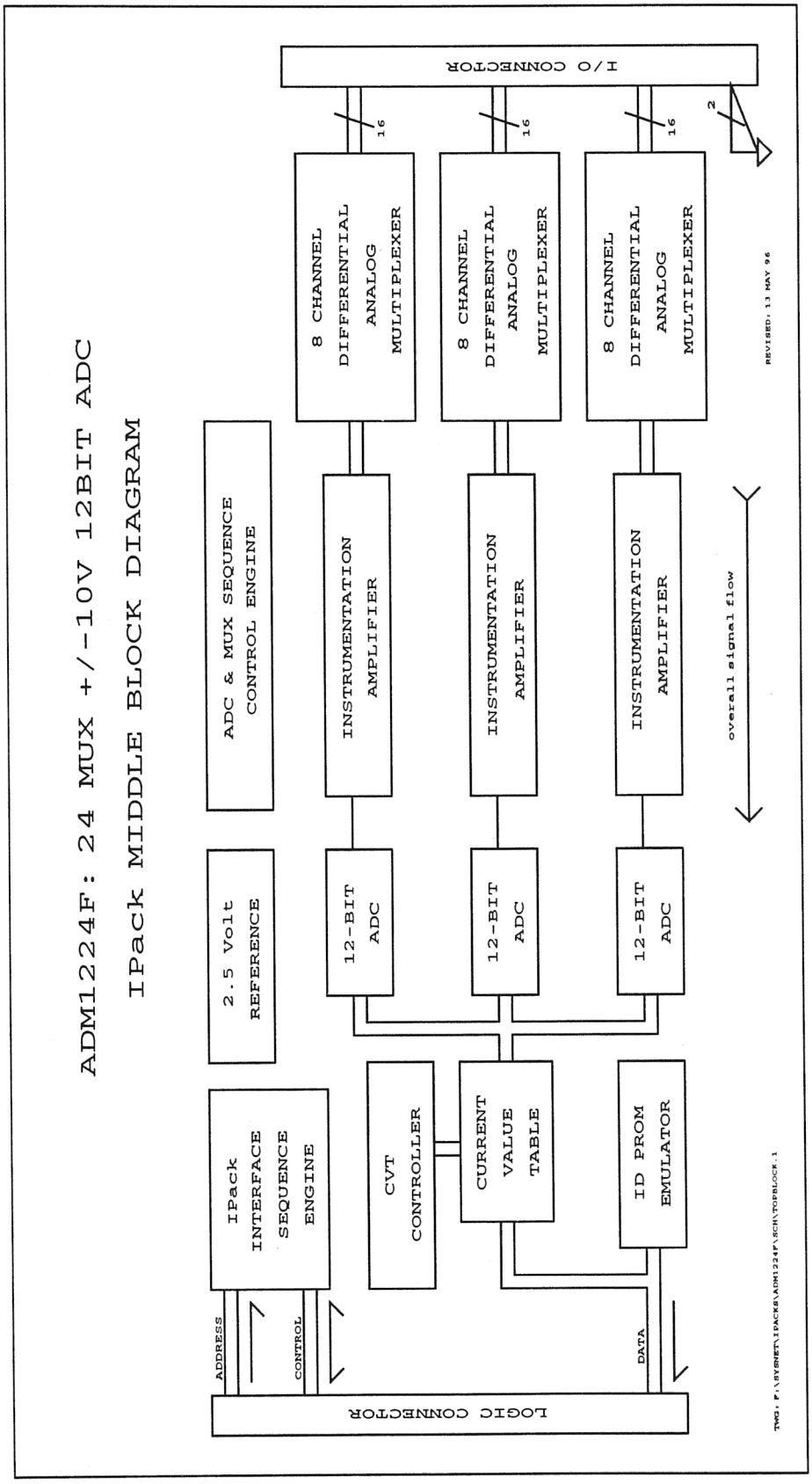


Figure 2-2 ADM1224F Middle Block Diagram

2.2 Middle Block Diagram

Figure 2-2 presents the second, mid-level block diagram of the ADM1224F IPack.

2.2.1 Middle Block Descriptions

LOGIC CONNECTOR

On the left side of the diagram is the IPack Logic Bus connection between the ADM1224F and its carrier. The three groups of information signals (not including power and grounds) perform the interface duties. There are six inbound address signals that provide descriminatory information beyond the select (control) signals, accessing both unique ID and I/O data from the ADM1224F's data sources. The normally bi-directional 16-bit data bus is a simplex read-only bus on the ADM1224F since there are only two types of read accesses possible. The normal control lines consist of four select signals, a read/write control line, reset, clock, and the one outbound acknowledgement signal.

ID PROM EMULATOR

This function, included in the IPack Logic Bus Interface Circuitry block of Figure 2-1, generates the necessary data patterns to emulate an ID PROM during Identification (ID) Transfers from the IPack to its carrier. Emulating the ID information within the EPLD, instead of providing the data from an actual PROM, is possible due to the never changing information presented by it. This technique saves board space, lowers costs, improves reliability, and enables this IPack to provide read accesses to this information without the insertion of wait cycles.

CURRENT VALUE TABLE & CONTROLLER

These two blocks, included in the 24-Location Current Value Table block of Figure 2-1, separate these functions into their respective physical components. The table, itself, is actually a pair of 32 KB SRAM devices configured as 32 KWord locations of write (from the ADCs) and read (to the carrier) locations. Only the first 24 locations are used. This registration technique is several orders of magnitude less expensive than any other technique for storing this much information in this small of area.

The CVT controller is contained within the EPLD. Not shown in figure 2-2 is the tight linkage between the CVT Controller and the ADC & MUX Sequence Control Engine, which requests to perform writes to the CVT, and the IPack Interface Sequence Engine, which requests to perform reads from the CVT. The CVT controller is basically the SRAM's read/write arbitor and timing controller.

ADC & MUX SEQUENCE CONTROL ENGINE

This block defines the primary functionality of that presented as the analog section controller of Figure 2-1. The core of this engine is a seventy state GRAY CODE counter that is continuously driven by the 8 MHz ICLK from the carrier. It provides orderly sequencing of signal selecting, signal tracking and holding, analog-to-digital converting, retrieving results, serial-to-parallel converting, and assistance in the eventual storing of results.

ANALOG CIRCUITRY

The remainder of Figure 2-2 presents the three sets of analog circuits. For each of eight channels there is a dedicated ADC, which is driven by a dedicated, gain = 1, instrumentation amplifier, which is fed signals from its own 8 channel, differential input and differential output full-scale analog multiplexer. This section of Figure 2-2 expands that which was presented in the upper right corner of Figure 2-1. This diagram still lacks

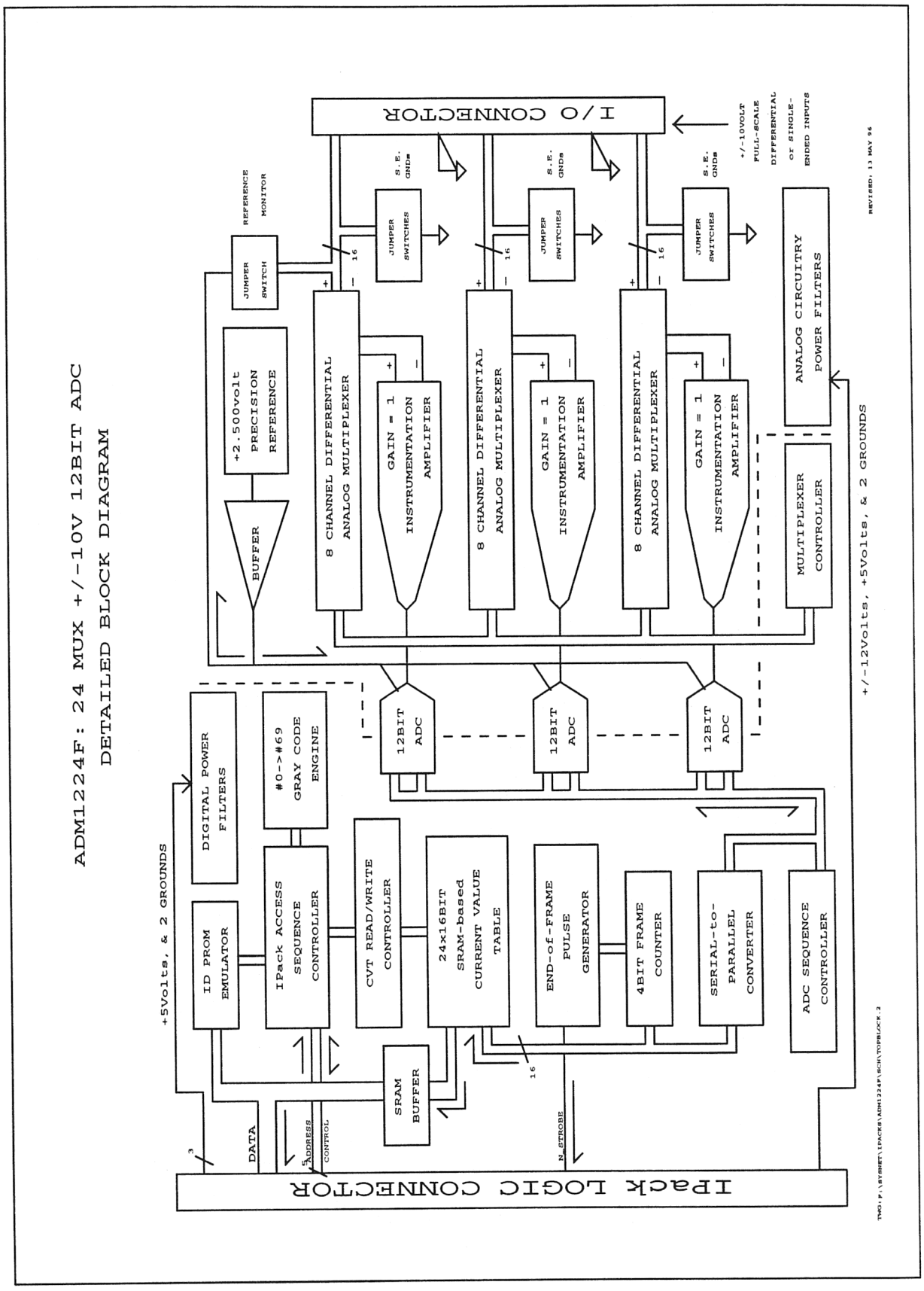


Figure 2-3 ADM1224F Detailed Block Diagram

the details necessary to understand all of the features and functions of the ADM1224F IPack.

2.3 Detailed Block Diagram

Figure 2-3 presents the detailed block diagram of the ADM1224F IPack.

2.3.1 Detailed Block Descriptions

2.3.1.1 Remaining Digital Blocks

Most of the digital logic (left half of Figure 2-3) has been discussed in the previous figures of this section. The following text provides additional information for a few blocks that Figure 2-3 presents.

SRAM BUFFER

This block presents a simple hexadecimal tristatable gate that couples the SRAM's data bus to the IPDbus during CVT read operations. It provides both isolation of buses and extra drive capabilities.

SERIAL-TO-PARALLEL CONVERTER

As mentioned previously, the three ADCs are serial interface devices. All three share a single, 12-bit, serial-to-parallel converter that captures the digitized data in round-robbin fashion. As will be seen in section 2.6, Table 2-1 (page 2-15) the data stream from the ADCs is actually 16-bits in length. The leading nibble of zeroes is discarded. Once the 12 bits of data is assembled in parallel format, the current frame-count value is appended at the highest nibble location, and the 16-bit result is deposited into the current value table by the CVT controller.

4-BIT FRAME COUNTER

A "frame" is defined, for this application, as one complete pass (channel #1 through channel #24) through all 24 channels. The frame counter is provided to enable the user to ascertain an accurate time relationship between the samplings of various channels in any order desired, including at rates slower than the rate at which new data is deposited into the CVT from the ADCs. As with most counters used on the ADM1224F, the frame counter is implemented as a free-running GRAY CODE sequencer, primarily to minimize board level noise (*only one bit changes at a time*). The "frame" count is incremented every 70.0000 μs, ≡ once per pass through all 24 channels. The sequence, in hexadecimal, is:

0, 1, 3, 2, 6, 7, 5, 4, C, D, F, E, A, B, 9 , and 8.

The entire frame count sequence repeats itself every 1.12 ms (70 μs per frame times 16 frames).

END-OF-FRAME PULSE GENERATOR

Every time the frame counter is incremented, a short, ½-ICLK-cycle-width pulse is generated. This low-going pulse occurs every 70 μs on the logic connector's N_STROBE signal line. It can be used for system signalling and synchronization purposes via the carrier's "strobe" connections. One typical use is that of generating an interrupt with the resultant ISR fetching all 24 samples from the CVT.

NOTE: This signal is NOT buffered. Be careful about loading on this line if it is used.

#0 → #69 GRAY CODE ENGINE

This particular counter is the core of all activity on the ADM1224F IPack. It is a modified GRAY CODE sequence engine. A minimum of 69 counts were necessary to accomplish all of the control and data retrieval activities. A full-sweep GRAY CODE engine would naturally include 128 counts to encompass the minimum count of 69. A modification in the single-bit changes near the end of the minimum of 69 counts, and the addition of one count to accomplish single-bit changes only, resulted in the 70-state machine design. The non-standard, hexadecimal sequence occurs during the sequence of:

$$62 \rightarrow 42 \rightarrow 40 \rightarrow 00 \quad \text{instead of} \quad 62 \rightarrow 66 \rightarrow 67 \rightarrow 65 \rightarrow \ldots 80 \rightarrow 00.$$

At one count per ICLK (125 ns per cycle), it takes 8.750 µs per pass through the engine, with eight passes through the engine per frame. Each pass through the engine controls the acquisition and data retrieval processes for one channel each for the three different analog and acquisition paths. The sequencing and associated activities will be covered in greater detail in sections 2.5 and 2.6. For now, it is sufficient to say that for any given pass through this engine, the same multiplexer value is applied to all three analog paths for the conversion process. If the first pass through the engine provides conversion processing for channels 1, 9, and 17; then the fourth pass will provide conversion processing for channels 4, 12, and 20; etc. This topic will be covered in greater detail in sections 2.5 and 2.6.

2.3.1.2 REMAINING ANALOG BLOCKS

Most of the analog circuitry (right half of Figure 2-3) has been discussed in the previous figures of this section. The Following text provides additional information for a few new blocks presented by Figure 2-3.

BUFFER (FOR THE REFERENCE)

This particular (triangular) block is a voltage follower buffer used to provide sufficient drive capability for generating the +2.500 V reference for the three ADCs, and for driving the channel #24 input if that option is exercised.

JUMPER SWITCH (REFERENCE MONITOR)

This is a shunt jumper switch that provides the option of monitoring the +2.500 V ADC reference voltage (defined as VREF ≡ Voltage REFerence) for conversion purposes as channel #24 in place of that which would normally be supplied as channel #24 from the I/O connector. It is also possible to couple the buffered reference voltage as an output to the I/O connector if the need exists. This is slightly risky since the ADCs' reference will then be exposed to all noise sources that may exist at the I/O connector and beyond.

JUMPER SWITCHES (S.E. GNDS)

These blocks represent three groups of eight shunt jumper switches, one group per multiplexer. Each switch provides the user the ability to short the inverting differential-ended input to the analog ground reference (AREF) on a per-channel basis for single-ended input applications. It is possible to convert inverted signals using the ADM1224F by driving the desired signal into the inverting input while grounding the non-inverting input. This application, of course, mandates the removal of these single-ended grounding

shunts for these channels. An example of this would be the case where an analog input swings from 0.000 V → -10.000 V but the application needs the data to be represented as if it were changing from 0.000 V → +10.000 V.

2.3.1.3 POWER FILTERS

As can be seen in Figure 2-3, the power distribution and filtering on the ADM1224F IPack is split between the digital system (upper left area of Figure 2-3) and the analog system (lower portion of Figure 2-3). The IPack's 50-pin logic connector has two pins reserved for +5volt power, four pins for ground return, and one each for ±12 V. One +5 V line and two of the ground return lines are dedicated as digital power lines. The digital power filtering consists of eight decoupling (0.1μF) capacitors. The other +5 V line, ±12 V lines, and the remaining two ground return lines (separately defined as AREF ≡ Analog REFerence) are dedicated as analog power lines. The analog power filter consists of a 68 μF bulk filter for the +5 V input, three T-type L-C-L filters for the +5 & ±12 V sources, and seventeen decoupling (0.1 μF) capacitors. About two thirds of the board has a solid analog ground plane, under all of the analog circuitry and analog power filters, that connects to AREF (analog ground return). The analog and digital grounds are tied together on the carrier-side of the logic connector, as are the two different +5 V power source lines.

2.4 ADM1224F SCHEMATICs

NOTE: Refer to the ADM1224F schematics located in Appendix B while reading this material since individual components are referred to by function name (SRAM, Buffer, ADC, MUX, Connector, etc.), component reference designators (U1, R3, C5, J2, etc.), industry-standard device part numbers (7128, AMP03, AD7893, 74FCT541, etc.), or physical location references. The physical location references are found along the borders of the schematics. The numbers 1 → 6 are found along the top and bottom and go from left → right, respectively. The letters A → F are found along both sides and go from top → bottom, respectively. Location A1 is the top left corner; C3 is slightly up and left of center; F6 is at the bottom right corner; etc.

The following is a short presentation on the schematics of the ADM1224F. There are two pages that comprise the schematic set. The first page presents all of the digital circuitry, combined with the IPack-logic connector, digital-logic filtering, analog-circuitry bulk filtering, and the 25 jumper switch shunts for the analog-input circuitry. The second page presents all of the analog circuitry, combined with the IPack I/O connector, and the remainder of the analog circuitry's filtering.

2.4.1 SCHEMATICS - SHEET 1 - COMPONENTS

The active components on sheet 1 are:

- U1, located at A3 → E3, is an ALTERA 7128 EPLD that contains all of the digital-control logic that supports the carrier and analog-circuitry sequencing activities
- U4, at C4 → D5, is the low byte of the CVT
- U5, at B4 → C5, is the high byte of the CVT
- U2, at C5 → D6, is the lower byte of the SRAM Buffer (see figure 2-3)
- U3, at B5 → B6, is the upper byte SRAM Buffer.

The discrete components on sheet 1 are:

- J1, found at B1 → E1, is the IPack logic connector which interfaces with the host carrier.
- Capacitors C1, C2, C5 and C6, found at A1 → A2, are decoupling capacitors for U1.
- Capacitor C3, located at D6, is a decoupler for U2.
- Capacitor C4, located at A2, is a decoupler for U3.
- Capacitor C7, found at A1, is a decoupler for U4.
- Capacitor C8, located at D6, is a decoupler for U5.
- Resistor R1, located at E4, is a series termination resistor for the ENDOFRAME (end of frame) pulse output that is driven onto the N_STROBE signal line of the logic connector J1.
- R2 → R10, located at A4 → B5, are series termination resistors for the digital interface lines between the 7128 controller EPLD and the three ADCs. Their function is to minimize noise normally generated by switching digital signals.
- H2 → H26, located at F1 → E2 and at F4, are the 25 shorting shunts for the jumper switches that are located on sheet 2 of the schematics.
- The 68 µF tantulum capacitor C9, located at D2, is the bulk power filter for the analog circuitry's +5 V power rail.
- FL1, FL2, and FL3, at D2 → E2, are the T-Type power filters for all three voltage sources for the analog circuitry.

The inventory of elements on sheet 1 of the schematics is complete except for seven non-components. These are the testpoints TP1 → TP7, located at E3 → F3. These "donuts" provide troubleshooting hooks that monitor the actual state of the core GRAY CODE engine.

2.4.2 SCHEMATICS - SHEET 2 - COMPONENTS

The active components on sheet 2 are:

- U14, U15, and U16, at A3 → F4, are the ADG507AKP devices that perform the input signals' selection (multiplexing) duties. MUX'A', referred to as U14, handles channels 1 → 8; MUX'B' ≡ U15 controls channels 9 → 16; U16 selects channels 17 → 24.
- U9, U11, and U13, at A2 → E3, are the AMP03 differential amplifiers that buffer the outputs of the multiplexers and provide single-ended outputs to the ADCs.
- U8, U10, and U12, at A1 → E2, are the AD7893 serial 12-bit ADCs that accomplish the analog→digital conversions.
- U6, at D2, is the AD680 precision +2.500 V reference (VREF generator). The output of U6 is buffered by U7, located at F1 → F2. U7 is an OP177 operational amplifier configured as a simple voltage follower. Its "VREF" output is directly connected to the REFIN (reference input) of all three ADCs and to a jumper switch for optional sampling as channel #24.

The discrete components on sheet 2 are:

- There are five decoupling capacitors (0.1 µF) for the analog +5 V power. C13, at A2, provides decoupling for U8. C16, at C2, provides decoupling for U10. C10, at D2, provides decoupling for U6. C19, at D2 → E2, provides decoupling for U12. C11, at E1, provides decoupling for U7.

- There are six decoupling capacitors (0.1 μF) for the analog +12 V power. C21, at A3, provides decoupling for U14. C12, at B3, provides decoupling for U9. C15, at C3, provides decoupling for U15. C24, at D3, provides decoupling for U11. C18, at D3 → E3, provides decoupling for U16. C26, at F3, provides decoupling for U13.
- There are six decoupling capacitors (0.1 μF) for the analog -12 V power. C22, at A3, provides decoupling for U14. C14, at B2 → B3, provides decoupling for U9. C17, at C3, provides decoupling for U15. C23, at D2 → D3, provides decoupling for U11. C20, at D3 → E3, provides decoupling for U16. C25, at F2 → F3, provides decoupling for U13.

In the following description, the "A-side" circuitry of the differential-analog multiplexers allows the non-inverting signals to pass, and the "B-side" allows the inverting signals to pass.

- R11, a precision resistor at B2, provides additional inverting feedback resistance in U9's circuitry, compensating the overall gain for the additional inverting input resistance that occurs due to the typical "RDSon" value through the B-side circuitry of U14.
- R14, a precision resistor at B2, provides additional non-inverting feedback resistance in U9's circuitry, compensating the overall gain for the additional non-inverting input resistance that occurs due to the typical "RDSon" value through the A-side circuitry of U14.
- R12, a precision resistor at C2, provides additional inverting feedback resistance in U11's circuitry, compensating the overall gain for the additional inverting input resistance that occurs due to the typical "RDSon" value through the B-side circuitry of U15.
- R15, a precision resistor at D2, provides additional non-inverting feedback resistance in U11's circuitry, compensating the overall gain for the additional non-inverting input resistance that occurs due to the typical "RDSon" value through the A-side circuitry of U15.
- R13, a precision resistor at E2, provides additional inverting feedback resistance in U13's circuitry, compensating the overall gain for the additional inverting input resistance that occurs due to the typical "RDSon" value through the B-side circuitry of U16.
- R16, a precision resistor at E2, provides additional non-inverting feedback resistance in U13's circuitry, compensating the overall gain for the additional non-inverting input resistance that occurs due to the typical "RDSon" value through the A-side circuitry of U16.

There are twenty-six two-pin jumper switches on the ADM1224F IPack.

- J3 → J10, located at A4 → A6, provide inverting input shorts to AREF when their respective shunts are installed for channels 1 → 8, respectively. Installing a shunt (described as H2 → H26 above in Sheet 1 components) effectively changes the input from a differential-ended input channel to a single-ended input channel.
- J11 → J18, located at C4 → C6, provide inverting input shorts to AREF when their respective shunts are installed for channels 9 → 16, respectively.
- J19 → J26, located at D4 → D6, provide inverting input shorts to AREF when their respective shunts are installed for channels 17 → 24, respectively.

Channel #24 uses the other two jumper switches to select its signal source.

- When a single shorting shunt is installed on J2, at F4, and no shunt is installed on J27, also at F4, the input to channel #24 is the buffered on-board VREF (+2.500 V).
- When a single shorting shunt is installed on J27 and J2 is left open, the signal present on pin 50 of the I/O connector, the non-inverting input for channel #24, is applied as the input to channel #24.
- As mentioned previously in the discussion of Figure 2-3, it is possible (though, not advisable) to couple VREF as an output to the I/O connector. This is accomplished by placing a shorting shunt on both J2 and J27. When this is done, VREF will be sampled as channel #24 and be exposed to the I/O connector for monitoring purposes.

NOTE: Additional jumpering information is provided in Section 3.0 of this manual.

J28, located at A6 → E6, provides all of the I/O connections to the ADM1224F IPack. Pins #25 and #26 must be connected to the analog ground reference of the signals' source. Unused channels should have their non-inverting inputs tied to these pins, while the jumper shunts should be installed on the inverting inputs for the same unused channels.

The symbol designated as H1, located at E6, is for the printed circuit board itself. This is simply used for the generation of the bill-of-materials.

2.5 SAMPLING DETAILS

The ADM1224F IPack is a fixed sequence, free-running sampling machine. As described previously, the channels are sectored into three groups of eight channels. Despite its initial appearance, the signal sampling and data conversion process is deterministic and, with the help of the appended frame count values, exact times between any samples can be calculated for samples obtained within a window of 1.12 ms. Channel→channel uncertainty is on the order of a few nanoseconds (based upon the stability of the **ICLK** supplied by the carrier).

2.5.1 SAMPLING ORDER

The channel number sampling order is: 1, 9, 17, 2, 10, 18, 3, 11, 19, 4, 12, 20, 5, 13, 21, 6, 14, 22, 7, 15, 23, 8, 16, and 24.

2.5.2 SAMPLING RATE

All channels are tightly controlled in their timings for channel selection, settling times, and when the actual conversion process starts as defined by the transition from "track" mode to "hold" mode. Each channel is repetitively sampled at a fixed cycle time of 70.000 μs, for a fixed sampling rate of 1÷70 μs = 14,285.71429 (over 14,285) samples per second per channel.

Due to the potential access contention to the CVT, the CVT controller will arbitrate the access for a no-WAIT read to the carrier while writes to the CVT of newly acquired data are delayed, as necessary. The window of opportunity for these writes to the CVT are four ICLK cycles long per sampling. This means that if the carrier starts a read of CVT

information at exactly the same time new ADC data is ready to be written into the CVT, the ADM1224F IPack can support up to a maximum of two carrier-inserted HOLD cycles and still accomplish the write to the CVT. If the carrier inserts more than two HOLD cycles, then the write to the CVT will not take place and the captured data is discarded. There are no built-in limits for the number of HOLD cycles that can be asserted by a carrier during any one transfer. This CVT write activity will be explored when the actual sequence of events is explored in greater detail in section 2.6. The "bottom line" of this immediate discussion is that while the sampling rate is fixed, the write-to-the-CVT rate is not necessarily fixed during times of contention for the usage of the CVT.

There may be applications where a sampling rate of 14,285 samples per second is insufficient for the bandwidth of the signal be captured. Supercommutation techniques solve this problem nicely. For instance, if a signal has a bandwidth of 5 KHz, then it is recommended that the signal be sampled at least at a 25 KHz rate, more if possible. Applying the same signal to both channels #1 and #5 (first and thirteenth channels to be sampled) will provide evenly spaced acquisitions 35 µs apart for an aggregate sampling rate of over 28,571 samples per second. Evenly spacing the supercommutation of multiple samplings for the same signal applied to three input channels could be accomplished by driving the signal into channels #1, #19, and #14 (first, ninth, and seventeenth channels to be sampled) for an aggregate sampling rate of over 42,857 samples per second. A four channel sampling applied to channels #1, #3, #5, and #7 (first, seventh, thirteenth, and nineteenth channels to be sampled) yields an aggregate sampling rate of over 57,142 samples per second. At the extreme, applying the same signal to all 24 channels provides an aggregate sampling rate of over 342,857 samples per second.

NOTE: The apparent input impedance drops (to a minimum of ≈ 17 KΩ) as the number of channels is increased in this scheme, thus requiring more drive capability from the signal source.

2.5.3 SAMPLING TIMING

As discussed on page 2-7 , three samplings occur per pass of the 70 states of the main GRAY CODE engine, with eight full passes required for a full frame of 24 channels of sampling. Also recall that while only 69 states were required to accomplish the necessary sampling tasks, a seventieth state was added to provide true single-bit transitions in the engine. Thus, every third sampling has an extra ICLK cycle added to its sampling time. The following is a complete list of the sampling time spacing between channels, in the order of sampling.

Using channel #1 as the start of the sampling process:

2.875 µs elapse from the sampling of channel #1 until the sampling of channel #9.
2.875 µs elapse from the sampling of channel #9 until the sampling of channel #17.
3.000 µs elapse from the sampling of channel #17 until the sampling of channel #2.
(Notice the extra 125 ns representing the seventieth state of the GRAY CODE engine.)
2.875 µs elapse from the sampling of channel #2 until the sampling of channel #10.
2.875 µs elapse from the sampling of channel #10 until the sampling of channel #18.
3.000 µs elapse from the sampling of channel #18 until the sampling of channel #3.
2.875 µs elapse from the sampling of channel #3 until the sampling of channel #11.
2.875 µs elapse from the sampling of channel #11 until the sampling of channel #19.

3.000 µs elapse from the sampling of channel #19 until the sampling of channel #4.
2.875 µs elapse from the sampling of channel #4 until the sampling of channel #12.
2.875 µs elapse from the sampling of channel #12 until the sampling of channel #20.
3.000 µs elapse from the sampling of channel #20 until the sampling of channel #5.
2.875 µs elapse from the sampling of channel #5 until the sampling of channel #13.
2.875 µs elapse from the sampling of channel #13 until the sampling of channel #21.
3.000 µs elapse from the sampling of channel #21 until the sampling of channel #6.
2.875 µs elapse from the sampling of channel #6 until the sampling of channel #14.
2.875 µs elapse from the sampling of channel #14 until the sampling of channel #22.
3.000 µs elapse from the sampling of channel #22 until the sampling of channel #7.
2.875 µs elapse from the sampling of channel #7 until the sampling of channel #15.
2.875 µs elapse from the sampling of channel #15 until the sampling of channel #23.
3.000 µs elapse from the sampling of channel #23 until the sampling of channel #8.
2.875 µs elapse from the sampling of channel #8 until the sampling of channel #16.
2.875 µs elapse from the sampling of channel #16 until the sampling of channel #24; and 3.000 µs elapse from the sampling of channel #24 until the next sampling of channel #1 again.

Summarily, MUX'A' → MUX'B' channels' samplings occur at a spacing of 2.875 µs; MUX'B' → MUX'C' take 2.875 µs; while transitions from MUX'C' → MUX'A' require 3.000 µs.

2.5.4 DETERMINISTIC SAMPLING

For any given period ≤ 1.12 ms, the exact timing relationship can be determined between any two samples to nanosecond-resolution (± ICLK uncertainty). This is accomplished by adding up the delta-time values between channel numbers as presented above in section 2.5.3, and adding to that value 70 µs per frame count difference between the two samples, as discussed in section 2.3.1.1, "4-bit Frame Counter". A few examples should help clarify any outstanding uncertainties.

Assume that channel #1 is read from the CVT and its high nibble (frame count) value = **C***hex*, and that channel #1 is subsequently read, in less than 1.12 ms, from the CVT with a new high nibble value = **E***hex*. Repeating that the frame count sequence is a true GRAY CODE sequence, which yields the path of: ..., 4, **C**, D, F, **E**, A, ..., it can be seen that the elapsed time from the first sampling to the second sampling = 70 µs × 3 = 210.000 µs.

Assume that channel #12 is read and its frame count value = **1***hex*. Channel #16 is then read and its frame count value = **3***hex*. The within-frame delta time between channel #12 and channel #16 = 35.000 µs. The frame count sequence encompassing both samples appears as: ..., 8, 0, **1**, **3**, 2, 6, ... Since the samples were in back-to-back frames, only 70.000 µs needs to be added to the value of 35.000 µs for a total time between samplings of 105.000 µs.

Assume that channel #18 is read and its frame count value = **6***hex*. Then channel #14 is read and its frame count value is **B***hex*. The within-frame delta time between channels #18 and #14 adds up to 32.125 µs. The frame count sequence that covers both of these samples is ..., 3, 2, **6**, 7, 5, 4, C, D, F, E, A, **B**, 9, ... The difference in frame count values yields an additional 70.000µS × 9 = 630µS. The total time between these two samples = 32.125 µs + 630.000 µs = 662.125 µs.

Assume that channel #8 is read and its frame count value = 7*hex*. Then channel #17 is read and its frame count value = **5***hex*. The frame count values are back-to-back as shown by the sequence of ..., 2, 6, **7**, **5**, 4, C, ... Channel #8 is the third-last sampling of frame #7 while channel #17 is the third sampling of the very next frame #5. Therefore, the total time between these two samples = 14.500 µs.

Assume that channel #19 is read and its frame count value = **8***hex*. Then channel #4 is read and its frame count value = **0***hex*. The within-frame delta time between channels #19 and #4 is only 3.000 µs since they are consecutive samples. However, the frame counts were different. The frame count sequence that includes both samples is ..., B, 9, **8**, **0**, 1, 3, ... Since the frames are consecutive, only 70.000 µs has to be added for the frame count difference. This brings the time difference between these two samples to a total of 73.000 µs.

There is a timing cross matrix, 24 channels by 24 channels, presented in section 6.0 that provides all of the different possibilities for within-frame delta timings (some of which were used as examples above), with directions on how to use it.

2.6 GRAY CODE ENGINE DETAILS

Table 2-1 provides a complete listing of all of the activities that take place for all seventy states of the primary sequence engine on the ADM1224F IPack. Every event is fully synchronous to the ICLK's 8 MHz clock; one event every 125 µs. One full sweep through this core engine takes 8.750 µs.

NOTE: States #63, 62, 42, and 40, while single-bit transitions, are not a normal GRAY CODE sequence.

Negating the most significant GRAY CODE bit from state #40 repeats the process back to state #00.

2.7 PERFORMANCE EFFICIENCY

The maximum throughput for a single ADC used on the ADM1224F is limited by the minimum specification of 8.52 µs for the conversion and fastest data retrieval rates possible. This equates to 68.16 ICLK cyles; a minimum of 69 states; or a minimum of 70 GRAY CODE states. The efficiency rating of the core engine coupled with just one of the ADC's is therefore at 97.37%. The three different ADC's were time-staggered to utilize as much common circuitry as possible for the data retrieval and CVT storage processes, and to maximize the total data acquisition rate of the entire board.

Table 2-1 GRAY CODE Sequence Engine Activities

STATE*hex*	SYNCHRONOUS EVENT:
00	idle
01	Increment 3-bit counter that drives MUX#C signal selection
03	Retrieve ADC#A's leading 0 (bit 15) & discard
02	Retrieve ADC#A's leading 0 (bit 14) & discard
06	Retrieve ADC#A's leading 0 (bit 13) & discard
07	Retrieve ADC#A's leading 0 (bit 12) & discard
05	Retrieve ADC#A's bit 11 (msb) & register
04	Retrieve ADC#A's bit 10 & register
0C	Retrieve ADC#A's bit 9 & register
0D	Retrieve ADC#A's bit 8 & register
0F	Retrieve ADC#A's bit 7 & register
0E	Retrieve ADC#A's bit 6 & register
0A	Retrieve ADC#A's bit 5 & register
0B	Retrieve ADC#A's bit 4 & register
09	Retrieve ADC#A's bit 3 & register
08	Retrieve ADC#A's bit 2 & register
18	Retrieve ADC#A's bit 1 & register
19	Retrieve ADC#A's bit 0 (lsb) & register
1B	Drive ADC#A's N_CONVST ⇓ low
1A	Write ADC#A's data to CVT if carrier not reading CVT
1E	Write ADC#A's data to CVT if carrier not reading CVT
1F	Write ADC#A's data to CVT if carrier not reading CVT
1D	Write ADC#A's data to CVT if carrier not reading CVT
1C	Drive ADC#A's N_CONVST ⇑ high (*starts actual conversion*)
14	Increment 3-bit counter that drives MUX#A signal selection
15	Retrieve ADC#B's leading 0 (bit 15) & discard
17	Retrieve ADC#B's leading 0 (bit 14) & discard
16	Retrieve ADC#B's leading 0 (bit 13) & discard
12	Retrieve ADC#B's leading 0 (bit 12) & discard
13	Retrieve ADC#B's bit 11 (msb) & register
11	Retrieve ADC#B's bit 10 & register
10	Retrieve ADC#B's bit 9 & register
30	Retrieve ADC#B's bit 8 & register
31	Retrieve ADC#B's bit 7 & register
33	Retrieve ADC#B's bit 6 & register
32	Retrieve ADC#B's bit 5 & register
36	Retrieve ADC#B's bit 4 & register
37	Retrieve ADC#B's bit 3 & register
35	Retrieve ADC#B's bit 2 & register
34	Retrieve ADC#B's bit 1 & register
3C	Retrieve ADC#B's bit 0 (lsb) & register
3D	Drive ADC#B's N_CONVST ⇓ low
3F	Write ADC#B's data to CVT if carrier not reading CVT
3E	Write ADC#B's data to CVT if carrier not reading CVT
3A	Write ADC#B's data to CVT if carrier not reading CVT
3B	Write ADC#B's data to CVT if carrier not reading CVT
39	Drive ADC#B's N_CONVST ⇑ high (*starts actual conversion*)

STATE*hex*	SYNCHRONOUS EVENT:
38	Increment 3-bit counter that drives MUX#B signal selection
28	Retrieve ADC#C's leading 0 (bit 15) & discard
29	Retrieve ADC#C's leading 0 (bit 14) & discard
2B	Retrieve ADC#C's leading 0 (bit 13) & discard
2A	Retrieve ADC#C's leading 0 (bit 12) & discard
2E	Retrieve ADC#C's bit 11 (msb) & register
2F	Retrieve ADC#C's bit 10 & register
2D	Retrieve ADC#C's bit 9 & register
2C	Retrieve ADC#C's bit 8 & register
24	Retrieve ADC#C's bit 7 & register
25	Retrieve ADC#C's bit 6 & register
27	Retrieve ADC#C's bit 5 & register
26	Retrieve ADC#C's bit 4 & register
22	Retrieve ADC#C's bit 3 & register
23	Retrieve ADC#C's bit 2 & register
21	Retrieve ADC#C's bit 1 & register
20	Retrieve ADC#C's bit 0 (lsb) & register
60	Drive ADC#C's N_CONVST ⇓ low
61	Write ADC#C's data to CVT if carrier not reading CVT
63	Write ADC#C's data to CVT if carrier not reading CVT
62	Write ADC#C's data to CVT if carrier not reading CVT
42	Write ADC#C's data to CVT if carrier not reading CVT
40	Drive ADC#C's N_CONVST ⇑ high (*starts actual conversion*)

2.8 VHDL-BASED ACTIVITY

This section concludes with, Figure 2-4, a block diagram for the VHDL model contained within the 7128 EPLD, hopefully pulling together all of the topics described above. As can be seen by the complexity of activity, this section can not be understood without first presenting section 2.6. The user will note that there are three (non GRAY CODE) binary counters contained within this model. They are the multiplexers' address counters for selecting the channels to be converted. Making these GRAY CODE sequencers, while possible and desirable from a noise-reduction viewpoint, would have caused the channel connections at the I/O Connector to appear cumbersome and confusing; hence, the binary sequencing.

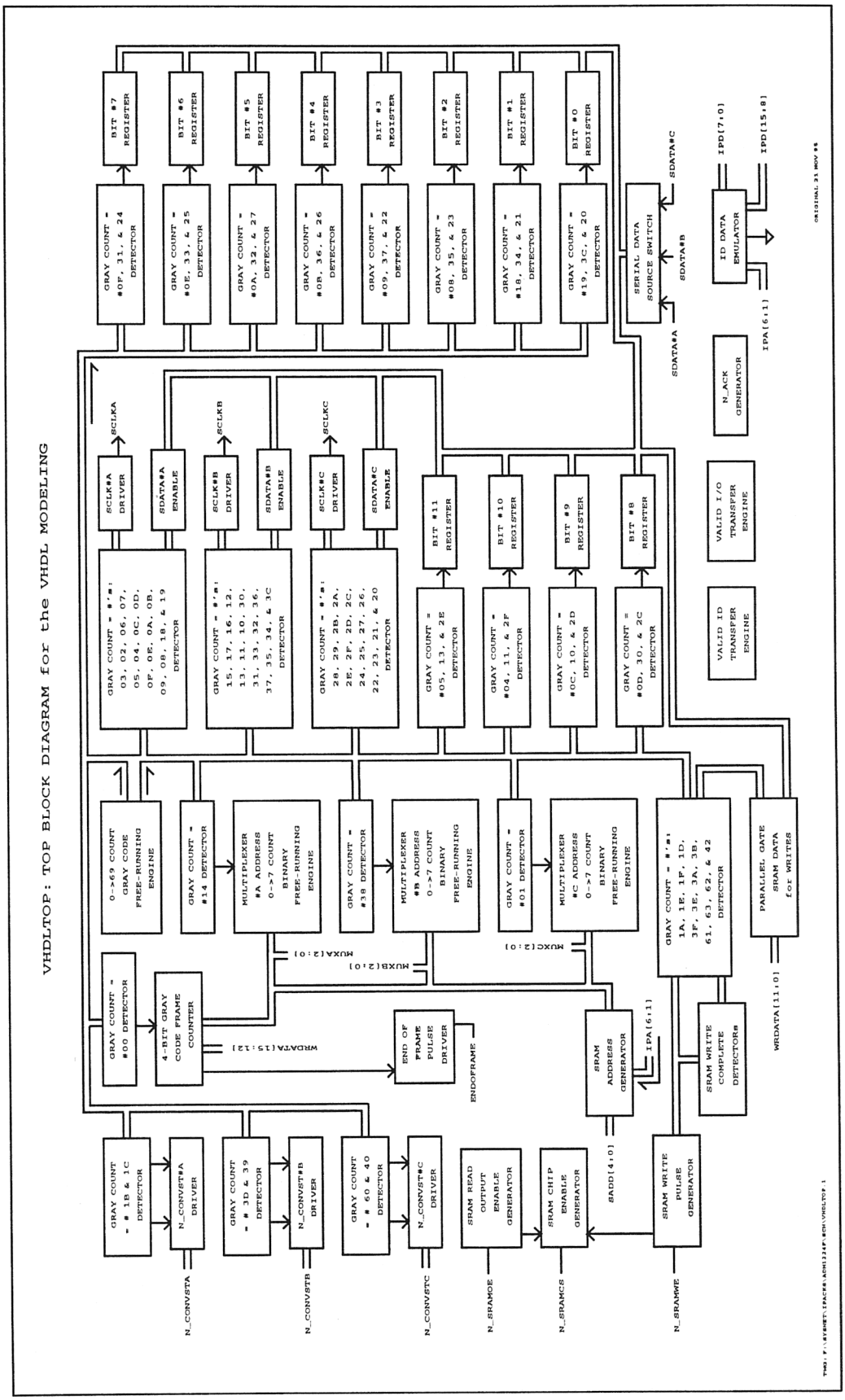


Figure 2-4 ADM1224F VHDL Model Block Diagram

3.0 HARDWARE INSTALLATION

3.1 Unpacking the ADM1224F

The contents of the ADM1224F shipping packages are listed in Table 3-1.

Table 3-1 Contents of **ADM1224F** Shipping Packages

QTY	DESCRIPTION
1	ADM1224F Printed Circuit Assembly
1	ADM1224F User Manual *

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR- ADM1224F) to obtain additional user manuals.

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

NOTE: The ADM1224F is an Electrostatic Sensitive Device (ESD). The hardware preparation and installation of the ADM1224F **MUST** be conducted on a good anti-static workbench to protect the IPack and its host carrier board. A bus-based IPack carrier board should be ("must be", if mounting hardware is being used) removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the ADM1224F can be completed.

3.2 Visual Inspection

Immediately inspect the ADM1224F to determine if any damage occurred during shipping. Do **NOT** install a board that appears to be damaged. Contact SYSTRAN immediately for return and replacement instructions.

3.3 Jumper Shunts

Reference figure 3-1, a partial (not to scale) assembly drawing, for the following discussions. Prior to the installation of the ADM1224F IPack on its carrier, the as-shipped condition may need to be modified, depending upon the application of this device. The as-shipped configuration has all 24 channels configured as single-ended inputs by the installation of shorting shunts on all 24 jumpers at J3 → J26. Additionally, channel #24 has its non-inverting input configured for a signal source to be applied from the I/O connector by the installation of a shorting shunt at J27, and with no shunt installed at J2.

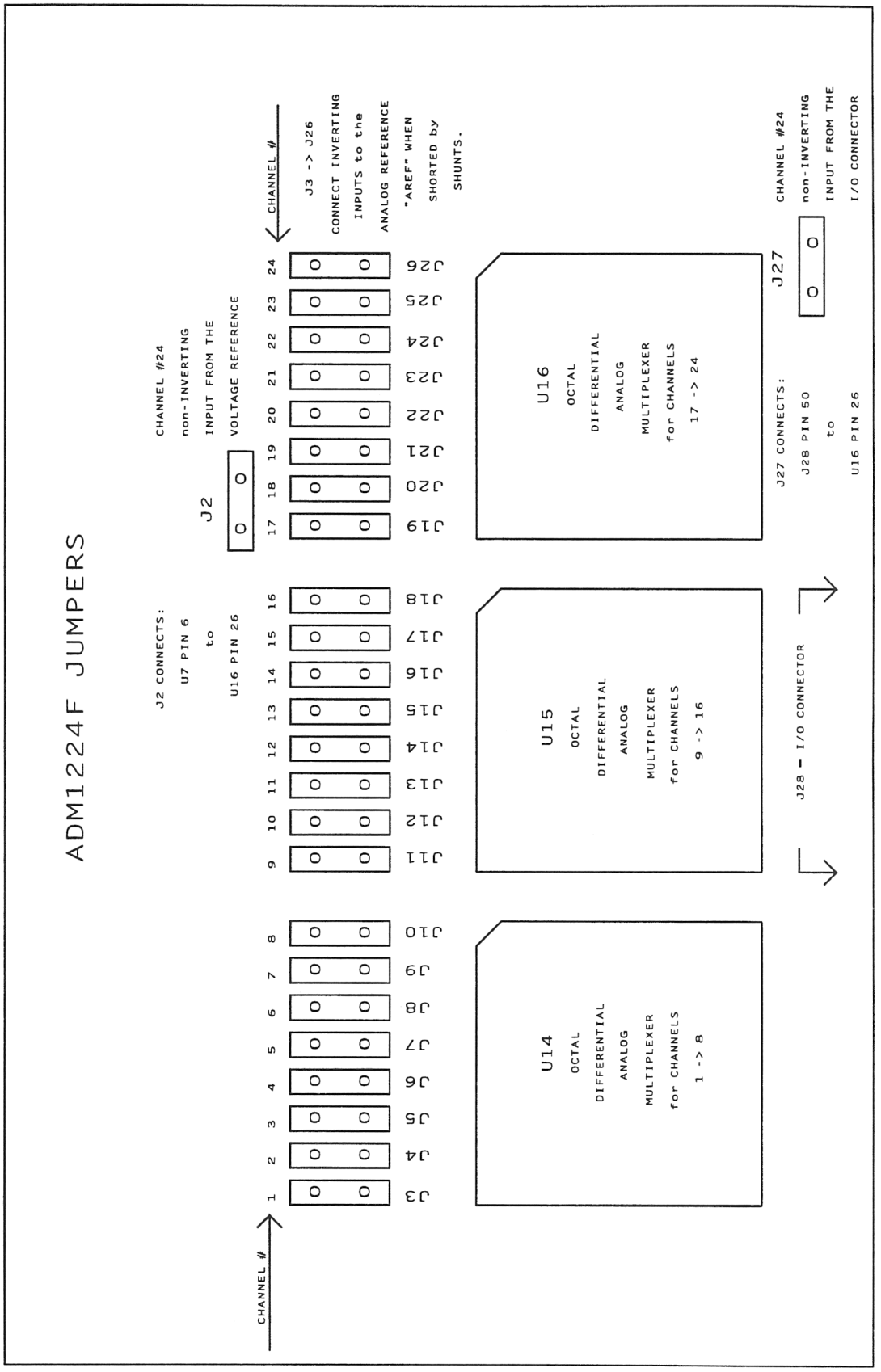


Figure 3-1 ADM1224F Jumpers

3.4 Wiring and Jumpering

The ADM1224F performs sequential (not simultaneous) sampling of channels, as described in detail in section 2.5. If there are critical timing relationships between various analog signals that need conversions, then these should be considered when assigning channel numbers and subsequently jumpering and wiring the I/O interfaces for this application. The following are a few example configurations.

3.4.1 Single-ended, Non-inverting Input Channels

Single-ended, Non-inverting Input Channels are the most commonly used configuration for analog-to-digital conversion products. Applications using the ADM1224F IPack to convert this type of signal source should:

- Apply these signals to their assigned "**VIN+#**" connections at the I/O connector.
- Leave the corresponding "**VIN-#**" inverting inputs at the I/O connector or tie them externally to pins #25 and #26, providing additional connections to "AREF".
- Install their respective jumper shunts for these channels, providing local, low-impedance connections to "AREF" to the inverting inputs.

EXAMPLE: If channels #4, #13, and #23 are to be used as single-ended, non-inverting input channels:

- Apply their input signals to I/O pins #30, #14, and #24, respectively.
- Install shorting shunts on jumpers #J6, #J15, and #J25.
- Externally connect the inverting input connections on the I/O connector at pins #29, #13, and #23 to pins #25 and #26 to provide additional external connections to the AREF (analog reference) ground plane.

3.4.2 Single-ended, Inverting Input Channels

If an application requires that a channel must have a single-ended, signal undergo, polarity inversion prior to conversion to digital format, the following technique may be used on the ADM1224F IPack.

- Apply the signal to the assigned channel's "**VIN-#**" (inverting input)
- Remove or leave off the appropriate shorting shunt for its inverting input jumper, and
- Externally connect the "AREF" to the channel's "**VIN+#**" (non-inverting input).

EXAMPLE: Assume that channel #12 needs to have its single-ended input signal inverted prior to being converted.

- Apply the inbound signal to the I/O connector pin #37 (inverting input)
- Remove the shorting shunt at J14, and
- Externally connect I/O pin #38 (non-inverting input) to both I/O pins #25 and #26.

3.4.3 Differential-ended, Non-Inverting Input Channels

Applications requiring excellent common-mode rejection capabilities can use the following configuration for converting signals using the ADM1224F IPack. It can be used regardless of whether the signal source is a single-ended driver, or a differential-ended driver. This configuration is ideal for removing deliberate offsets applied in earlier circuitry.

EXAMPLE: A full-bridge piezoresistive sensor is excited by a unipolar voltage source (e.g. +10 V referenced to ground) which generates a null-state centered at +5 V.

- The non-inverting signal source is applied to the non-inverting input of the ADM1224F
- The shorting shunt is removed from its appropriate jumper; and
- The inverting input receives either the inverting signal from a differential driver, or the remote analog ground reference point.

For best results, use tightly twisted pairs for the inverting and non-inverting signal carriers so that equal amounts of external "noise" are applied to both signal carriers for subsequent removal by the differential amplifiers on the ADM1224F. The pin-out on the I/O connector is designed to work with twisted-pair, IDC cables.

EXAMPLE: One application of this common configuration is provided for channel #2.

- Apply the non-inverting input signal to I/O pin #28
- Remove the shunt from jumper #J4, and
- Connect I/O pin #27 to the signal source's local analog ground reference (or to the inverting output of a differential driver).

3.4.4 Differential-ended, Inverting Input Channels

Applications requiring that a channel must have a differential-ended signal-pair undergo polarity inversion prior to conversion to digital format can use this technique.

A common example of this might be the need for data from an accelerometer to provide positive-going information for forward (+X-axis notation) acceleration, and the in-line gain block is presenting the negation of this goal.

- Apply the non-inverting input signal to the "**VIN-#**" (inverting input)
- Apply the inverting input signal to the "**VIN+#**" (non-inverting input), and
- Remove or leave off the appropriate shorting shunt for its inverting input jumper.

EXAMPLE: Assume that the analog signals being converted as channels #5 & #22 are differentially driven by inverting drivers, and that they need another analog inversion prior to conversion to digital format to provide analog polarity that represents valid physical events taking place.

- Connect the non-inverting signal for channel #5 to the I/O pin #5 (inverting input).
- Connect the inverting signal for channel #5 to the I/O pin #6 (non-inverting input).
- Connect the non-inverting signal for channel #22 to the I/O pin #47 (inverting input).
- Connect the inverting signal for channel #22 to the I/O pin #48 (non-inverting input).
- Leave off shorting shunts or remove them from both jumpers #J7 and #J24.

3.4.5 Unused Inputs

Ground both non-inverting and inverting inputs for all unused inputs to AREF to minimize noise in the system, since these channels will be converted anyway. This is accomplished by connecting all of the unused non-inverting inputs to the AREF signals at the I/O connector, and by installing the shorting shunts for the same channels, thereby connecting their inverting inputs to AREF.

EXAMPLE: The following demonstrates the proper wiring and jumpering scheme for all of the unused channels not cited previously in sections 3.4.1 through 3.4.4:

For channels: 1, 3, 6 → 11, 14 → 21, and 24.

- Connect I/O pins: 2, 4, 32, 8, 34, 10, 36, 12, 40, 16, 42, 18, 44, 20, 46, 22, and 50 to both I/O pins: 25 and 26 to connect all of the unused non-inverting inputs to AREF.
- Install jumpers: 3, 5, 8, 9, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 22, 23, 26, and 27 to connect all unused inverting inputs to AREF.
- Ensure that the shorting shunt is **NOT** installed at jumper #J2.
- Installing a shorting shunt at jumper #J27 connects the I/O connector's pin #50 to the non-inverting input of analog multiplexer, U16, for channel #24.

3.4.6 VREF Connections

Channel #24 can obtain its analog inputs from either the I/O connector or from the local buffered VREF signal for those applications that require continuous monitoring of the voltage reference in the data set. This is accomplished by removing the shorting shunt at jumper #J27 and installing it at jumper #J2.

As cited previously in sections 2.3.1.2 and 2.4.2, it is possible (but not recommended) to monitor VREF at pin #50 of the I/O connector. This is accomplished by installing shorting shunts at both jumpers #J2 and #J27.

In both scenarios, the inverting input to channel #24 needs to be tied to AREF. This is accomplished by installing a shorting shunt at jumper #J26.

3.4.7 High Shock/Vibration applications

For those applications where the ADM1224F will be subjected to high shock and/or vibration environments, it is recommended that the push-on shorting shunts that are supplied with the ADM1224F not be used. Instead, short together the pins of the appropriate jumpers using either wire-wrap techniques, or by soldering wires between posts normally needing the shorting shunts.

NOTE: If wires are soldered onto the jumpers, it is advised that low heat be used to prevent the melting of the jumper posts' plastic holder, and that the tip be grounded to the anti-static equipment being used to ensure safe soldering on ESD circuits.

3.5 ADM1224F Installation

The tools required for the ADM1224F installation are listed in Table 3-2.

Table 3-2 ADM1224F Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

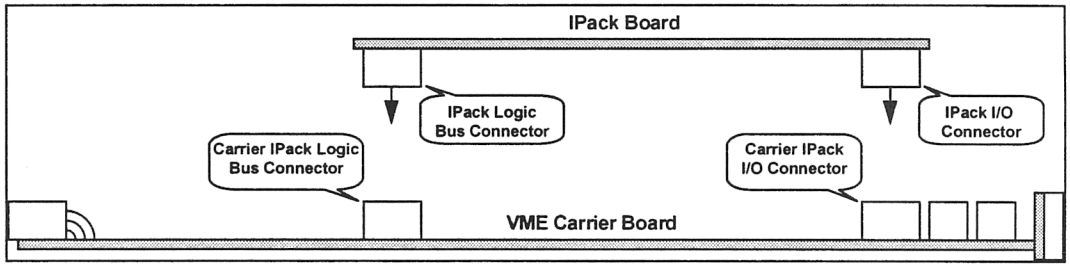


Figure 3-1 ADM1224F Installed on a VME IPack Carrier

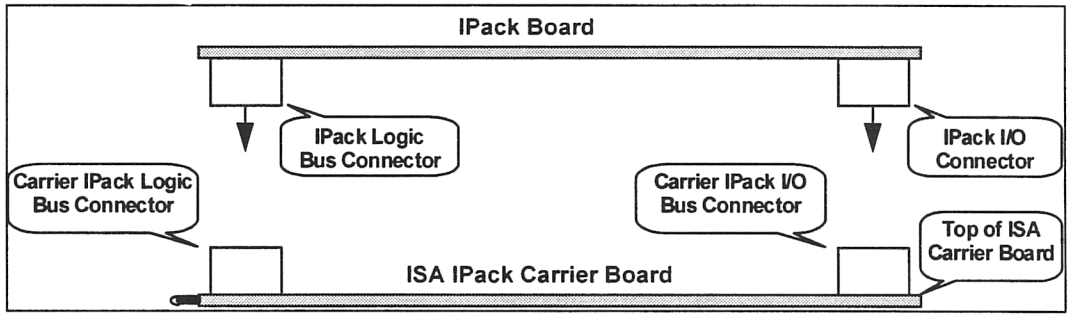


Figure 3-2 ADM1224F Installed on an ISA IPack Carrier

Figure 3-1 shows the ADM1224F installed on a VME IPack carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Refering to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the ADM1224F can be made.

3. Remove the ADM1224F from the shipping package and place it on the ESD bench.
4. Install the ADM1224F onto the carrier board by applying adequate and equal pressure to the ADM1224F board at both ends.
*5. Install four M2x5 mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the ADM1224F to the carrier board.

Table 3-3 IPack Logic Bus Pin Assignments

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
Intreq1*	44	N_INTREQ1
A4	43	IPA4
intreq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D1	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IPack I/O Connector Pin Assignments

IPack Logic Bus Pin #	Signal Names
50	VIN+#24
49	VIN-#24
48	VIN+#22
47	VIN-#22
46	VIN+#20
45	VIN-#20
44	VIN+#18
43	VIN-#18
42	VIN+#16
41	VIN-#16
40	VIN+#14
39	VIN-#14
38	VIN+#12
37	VIN-#12
36	VIN+#10
35	VIN-#10
34	VIN+#8
33	VIN-#8
32	VIN+#6
31	VIN-#6
30	VIN+#4
29	VIN-#4
28	VIN+#2
27	VIN-#2
26	GROUND
25	GROUND
24	VIN+#23
23	VIN-#23
22	VIN+#21
21	VIN-#21
20	VIN+#19
19	VIN-#19
18	VIN+#17
17	VIN-#17
16	VIN+#15
15	VIN-#15
14	VIN+#13
13	VIN-#13
12	VIN+#11
11	VIN-#11
10	VIN+#9
9	VIN-#9
8	VIN+#7
7	VIN-#7
6	VIN+#5
5	VIN-#5
4	VIN+#3
3	VIN-#3
2	VIN+#1
1	VIN-#1

4.0 PROGRAMMING GUIDE

4.1 Overview

This section of the manual describes the operation of the ADM1224 from the software perspective, detailing the ADM1224 registers and providing programming examples. A more detailed description of the hardware can be found in section 2.0 DESCRIPTION and section 6.0 TYPICAL APPLICATIONS.

4.2 Description

The ADM1224 is a simple-to-use 12 bit, 24 channel, ADC (Analog to Digital Converter) card. All channels continuously convert and place their data into a current value table. The current values are retrieved by reading the data register for the corresponding channel.

4.3 IPack ID PROM Listing

Emulating the ID PROM function is possible, due to the never-changing information it presents. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" READ accesses of this information.

NOTE: The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0C *hex*, or any attempt to WRITE to ID space (if a carrier supports such a transfer) will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) READs as all zeroes during valid ID READ-only accesses.

Table 4-1 is the ADM1224 emulated ID Address Space PROM listing.

Table 4-1 ADM1224 ID Address Space Listing

IPack Address	Description	Data Read
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 *hex*
IPA = 02 *hex*	ASCII "A"	41 *hex*
IPA = 03 *hex*	ASCII "C"	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	ADM1224's Model Number	6F *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	CD *hex*

4.4 IPack I/O Address Map

The ADM1224's I/O Address Map contains 24 registers in the IPack I/O space (IPA = 00 and IPA = 17 *hex*). The address detector circuitry is fully decoded.

NOTE: Any attempt to access I/O addresses at and above 17 *hex,* or any attempt to WRITE to any I/O space, will result in no acknowledgment and subsequent bus time-out error on the carrier upon which this IPack resides.

Table 4-2 is the ADM1224 I/O Address map and contains two data registers.

Table 4-2 ADM1224 I/O Address Space Listing

IPack Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 00 *hex*	[15:8]	[7:0]	Channel 1 Data Register 16 bits
IPA = 01 *hex*	[15:8]	[7:0]	Channel 2 Data Register 16 bits
IPA = 02 *hex*	[15:8]	[7:0]	Channel 3 Data Register 16 bits
IPA = 03 *hex*	[15:8]	[7:0]	Channel 4 Data Register 16 bits
IPA = 04 *hex*	[15:8]	[7:0]	Channel 5 Data Register 16 bits
IPA = 05 *hex*	[15:8]	[7:0]	Channel 6 Data Register 16 bits
IPA = 06 *hex*	[15:8]	[7:0]	Channel 7 Data Register 16 bits
IPA = 07 *hex*	[15:8]	[7:0]	Channel 8 Data Register 16 bits
IPA = 08 *hex*	[15:8]	[7:0]	Channel 9 Data Register 16 bits
IPA = 09 *hex*	[15:8]	[7:0]	Channel 10 Data Register 16 bits
IPA = 0A *hex*	[15:8]	[7:0]	Channel 11 Data Register 16 bits
IPA = 0B *hex*	[15:8]	[7:0]	Channel 12 Data Register 16 bits
IPA = 0C *hex*	[15:8]	[7:0]	Channel 13 Data Register 16 bits
IPA = 0D *hex*	[15:8]	[7:0]	Channel 14 Data Register 16 bits
IPA = 0E *hex*	[15:8]	[7:0]	Channel 15 Data Register 16 bits
IPA = 0F *hex*	[15:8]	[7:0]	Channel 16 Data Register 16 bits
IPA = 10 *hex*	[15:8]	[7:0]	Channel 17 Data Register 16 bits
IPA = 11 *hex*	[15:8]	[7:0]	Channel 18 Data Register 16 bits
IPA = 12 *hex*	[15:8]	[7:0]	Channel 19 Data Register 16 bits
IPA = 13 *hex*	[15:8]	[7:0]	Channel 20 Data Register 16 bits
IPA = 14 *hex*	[15:8]	[7:0]	Channel 21 Data Register 16 bits
IPA = 15 *hex*	[15:8]	[7:0]	Channel 22 Data Register 16 bits
IPA = 16 *hex*	[15:8]	[7:0]	Channel 23 Data Register 16 bits
IPA = 17 *hex*	[15:8]	[7:0]	Channel 24 Data Register 16 bits

4.5 Word Access Address Translation

Table 4-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IPack Address
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*
BASE + 18	BASE + 18	BASE + 32	IPA = 0C *hex*
BASE + 1A	BASE + 1A	BASE + 36	IPA = 0D *hex*
BASE + 1C	BASE + 1C	BASE + 3A	IPA = 0E *hex*
BASE + 1E	BASE + 1E	BASE + 3E	IPA = 0F *hex*
BASE + 20	BASE + 20	BASE + 42	IPA = 10 *hex*
BASE + 22	BASE + 22	BASE + 46	IPA = 11 *hex*
BASE + 24	BASE + 24	BASE + 4A	IPA = 12 *hex*
BASE + 26	BASE + 26	BASE + 4E	IPA = 13 *hex*
BASE + 28	BASE + 28	BASE + 52	IPA = 14 *hex*
BASE + 2A	BASE + 2A	BASE + 56	IPA = 15 *hex*
BASE + 2C	BASE + 2C	BASE + 5A	IPA = 16 *hex*
BASE + 2E	BASE + 2E	BASE + 5E	IPA = 17 *hex*

4.6 Byte Access Address Translation

Table 4-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VME BUS Address	PC-AT BUS Address	NuBus Address	IPack Address	Byte-Lane *
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1
BASE + 19	BASE + 18	BASE + 33	IPA = 0C *hex*	0
BASE + 18	BASE + 19	BASE + 32	IPA = 0C *hex*	1
BASE + 1B	BASE + 1A	BASE + 37	IPA = 0D *hex*	0
BASE + 1A	BASE + 1B	BASE + 36	IPA = 0D *hex*	1
BASE + 1D	BASE + 1C	BASE + 3B	IPA = 0E *hex*	0
BASE + 1C	BASE + 1D	BASE + 3A	IPA = 0E *hex*	1
BASE + 1F	BASE + 1E	BASE + 3F	IPA = 0F *hex*	0
BASE + 1E	BASE + 1F	BASE + 3E	IPA = 0F *hex*	1
BASE + 21	BASE + 20	BASE + 43	IPA = 10 *hex*	0
BASE + 20	BASE + 21	BASE + 42	IPA = 10 *hex*	1

VME BUS Address	PC-AT BUS Address	NuBus Address	IPack Address	Byte-Lane *
BASE + 23	BASE + 22	BASE + 47	IPA = 11 *hex*	0
BASE + 22	BASE + 23	BASE + 46	IPA = 11 *hex*	1
BASE + 25	BASE + 24	BASE + 4B	IPA = 12 *hex*	0
BASE + 24	BASE + 25	BASE + 4A	IPA = 12 *hex*	1
BASE + 27	BASE + 26	BASE + 4F	IPA = 13 *hex*	0
BASE + 26	BASE + 27	BASE + 4E	IPA = 13 *hex*	1
BASE + 29	BASE + 28	BASE + 53	IPA = 14 *hex*	0
BASE + 28	BASE + 29	BASE + 52	IPA = 14 *hex*	1
BASE + 2B	BASE + 2A	BASE + 57	IPA = 15 *hex*	0
BASE + 2A	BASE + 2B	BASE + 56	IPA = 15 *hex*	1
BASE + 2D	BASE + 2C	BASE + 5B	IPA = 16 *hex*	0
BASE + 2C	BASE + 2D	BASE + 5A	IPA = 16 *hex*	1
BASE + 2F	BASE + 2E	BASE + 5F	IPA = 17 *hex*	1
BASE + 2E	BASE + 2F	BASE + 5E	IPA = 17 *hex*	1

* Byte-lane 1 not applicable for ID Space

4.7 Data Registers Bit Description (IPA=00 → 17 hex)

The ADM1224 has 24 16-bit-wide registers, with each register corresponding to an ADC channel. The ADM1224 supports word (16-bit) READs only.

4.7.1 Data Registers 0 to 17 (IPA = 00 → 17 hex)

Table 4-5 Data Register Description

Bit#	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	FC 3	FC 2	FC 1	FC 0	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

X = Indeterminant. Real data is present in all registers 78.75 µs after negation of reset.

AD11- AD0: These bits represent the 12-bit two's complement ADC value for the corresponding channel.

FC3-FC0: These bits represent the 4 bit grey code frame count value for the corresponding channel. A detailed explaination of the frame count grey code can be found in section 2.3.1 under the heading "4-Bit Frame Counter".

4.8 Programming Example

The following example illustrates how to use the ADM1224 device from a programming perspective.

- At power-up, the ADCs begin converting and placing their data in the current value tables.
- Read ADC channel 1 by reading Data Register 0 at IPack address 0.
- The ADC value in two's complement binary is extracted by ANDING the register value with 0FFF hex.
- The frame count is extracted by shifting the register value to the right 12 bits and ANDING it with 000F hex.

All of the channels are read in the same manner as the channel 1 example above.

4.9 Integer Register Value to Floating Point Voltage Conversion

The ADM1224 uses a 12-bit two's complement binary representation of the input voltages. The following example illustrates how to convert this integer ADC value to a floating point volts representation:

CONVERTING THE REGISTER VALUE TO A VOLTAGE

Vin = SignExtendedRegVal * 0.0048828

where:
Vin is the ADC input voltage
SignExtendedRegVal is the sign extended value read from the ADC data register (see explanation below).

SIGN EXTENDING THE 12-BIT REGISTER VALUE

The following example illustrates how to sign extend the 12-bit two's complement ADC value to create a signed 16-bit ADC value:

Read the ADC data register as a 16-bit word.

Test bit 11 (bit numbering starting from 0) of the read value.

```
If bit 11 = 1,
    Then set bits 15 to 12 to 1's (OR it with F000 hex)
Else if bit 11 = 0,
    Then clear bits 15 to 12 0's (AND it with 0FFF hex)
End if
```

NOTE: In either case, the frame count in bits 15 to 12 are overwritten with 1's or 0's. The resulting 16-bit value is a two's complement signed value that can be multiplied by 0.0048828 to obtain the voltage.

5.0 PERFORMANCE

5.1 Overview

The performance of the ADM1224F can be presented as two major categories:

- internal and external digital timings, including carrier accesses to information, and
- those that directly relate to the analog circuitry and its subsequent digital representations of signals passing through this circuitry.

This latter section will be further broken up into two, major subsections:

- an analytical look at what the ADM1224F can accomplish from a worst case perspective, and
- an empirical presentation of typical accuracy and noise values.

It is important to note that most of the information provided in this section represents typical measurements, and does not supercede any related minimum and maximum specifications presented in section 1 of this document. Where possible, data is tabulated with only one response time (actual) performance figure presented to minimize the length of the presentation.

Unlike other related documents published by SYSTRAN Corp. for IPack products, there is no single-system configuration for all of its emperical data measurements. Therefore, each new set, or sets, of related data is preceded by a short description of the system configuration used to gather the information.

5.2 Internal Digital Timing

The first group of performance data to be examined includes signals that are internal to the ADM1224F; i.e. not visibile at its interface connectors. This information serves as additional descriptive material in support of section 2.0 of this document. The areas of interest include the sequencing of the Gray Code Engine, and the serial extraction of ADC data with subsequent deposition into the CVT.

5.2.1 Hardware Configuration - GRAY CODE

Individual wires ≈1″ long were connected to ADM1224F#105 for, and at:

"ICLK"	@ U1 pin 89
"GRAY0"	@ TP7
"GRAY1"	@ TP6
"GRAY2"	@ TP5
"GRAY3"	@ TP4
"GRAY4"	@ TP3
"GRAY5"	@ TP2
"GRAY6"	@ TP1.

The IPack under test was mounted on a MVME162-01 in slot A using an IPack Logic Bus Extender Board (Type 1) under the ADM1224F. No bus extension cable was used.

The board was placed on the extender to provide easier access to the connected wires. All eight signals were captured using an HP 1 GHz Timing Module, Model 1615A, in a 16500A Logic Analysis System chassis.

5.2.2 GRAY CODE ENGINE

Sections 2.3.1.1 and 2.6 presented details about the core engine of the ADM1224F, the seventy-state Gray Code Engine. Section 2.8 presented a compilation of all of the activities that take place during all of the states of this engine. Figure 5-1 presents a snapshot of slightly more than one full pass through all of the states of this engine. Note that there are only single-edge changes at any given time, the "calling card" of a Gray Code counter. Also note that the widths of both "GRAY5" and "GRAY6" are not proportional to those of the other five, lower significant bits. This phenomenon is a result of the truncated sequence (70 states instead of 128).

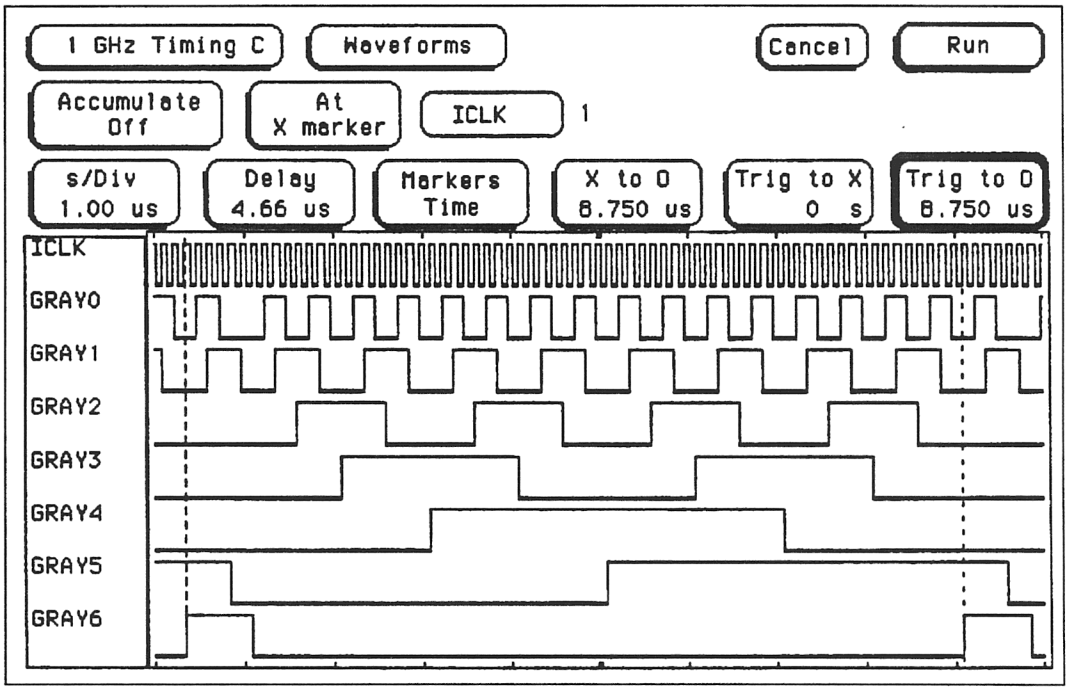


Figure 5-1 Gray Code Engine full pass

The full pass through all seventy states takes 8.750 μs, and eight passes captures all twenty-four channels in 70 μs. Captured waveforms indicate that all state transitions occurred within 5 ns→6 ns of the rising edge of ICLK. Being a fully synchronous engine, engine-state-dependent events occur at the end of a count where the system conditions, including the counter's current state, are stable and waiting for the rising edge of the ICLK to perform the next task.

5.2.3 Hardware Configuration - ADC Data

Additional 1″ wires were connected for, and at:

"CLKA"	@ U8 pin 4
"SDA"	@ U8 pin 5
"CTRLA"	@ U8 pin 7
"CLKB"	@ U10 pin 4
"SDB"	@ U10 pin 5
"CLKC"	@ U12 pin 4
"SDC"	@ U12 pin 5
"SRAMD0"	@ U4 pin 11
"SRAMD1"	@ U4 pin 12
"SRAMD2"	@ U4 pin 13
"SRAMD3"	@ U4 pin 15
"SRAMD4"	@ U4 pin 16
"SRAMD5"	@ U4 pin 17
"SRAMD6"	@ U4 pin 18
"SRAMD7"	@ U4 pin 19
"N_SRAMWE"	@ U4 pin 27.

The ADM1224F was remounted as in section 5.2.1, and the same analyzer was connected.

The "CLKA", "CLKB", and "CLKC" signals are the serial shift clocks used to extract data from the ADC's @ U8, U10, and U12, respectively. The "SDA", "SDB', and "SDC" signals are the serial data lines from the ADC's. The "CTRLA" signal is the conversion control line for ADC#A. On the third figure following, it is referred to as "N_CNVS" (N_CONVST). "SRAMD[7:0]" are the data lines that define the low byte of the parallel SRAM data bus that provide the results from the serial→parallel conversion process just prior to the writes to the CVT. The asserted low "N_SRAMWE" signal (SRAM write enable) appears on the next two figures as "SRAME".

5.2.4 ADC data movement

Sections 2.5.3 and 2.6 textually presented the activities that take place during the seventy states of the Gray Code Engine. Most of this activity involves the serial extraction of ADC data with parallel→serial conversion and subsequent deposition of data into the CVT in round-robbin fashion through all three ADC's. Figure 5-2 clearly depicts this activity.

The left portion of this diagram depicts the serial extraction of data from ADC#B with a CVT write of(F)F3 *hex*, followed by the same process for ADC#C with data = 000, and the same for ADC#A with a CVT write of (F)FB *hex*. While the leading "F" is not apparent in the parallel data being written to the CVT for ADC#B and ADC#A, they are obvious when the serial data streams are examined. The actual write of data occurs on the rising edge of "N_SRAMWE". Since all three of the writes to the CVT are uncontested, they all occur during their first-opportunity states, during Gray Code states 3F *hex*, 61 *hex*, and 1A *hex* for converters #B, #C, and #A, respectively. More details are available about these events in section 2.5.2.

Figure 5-3 presents a zoom-in view of the ADC#B's data capture activity presented in figure 5-2. Rising edges of ICLK actually capture the serial data present on SDB, with

the bit stream of 1, 1, 0, 0, 1, 1 in full view. Notice that the write to the CVT occurs 8 ns following the rising edge of its synchronous clock ICLK.

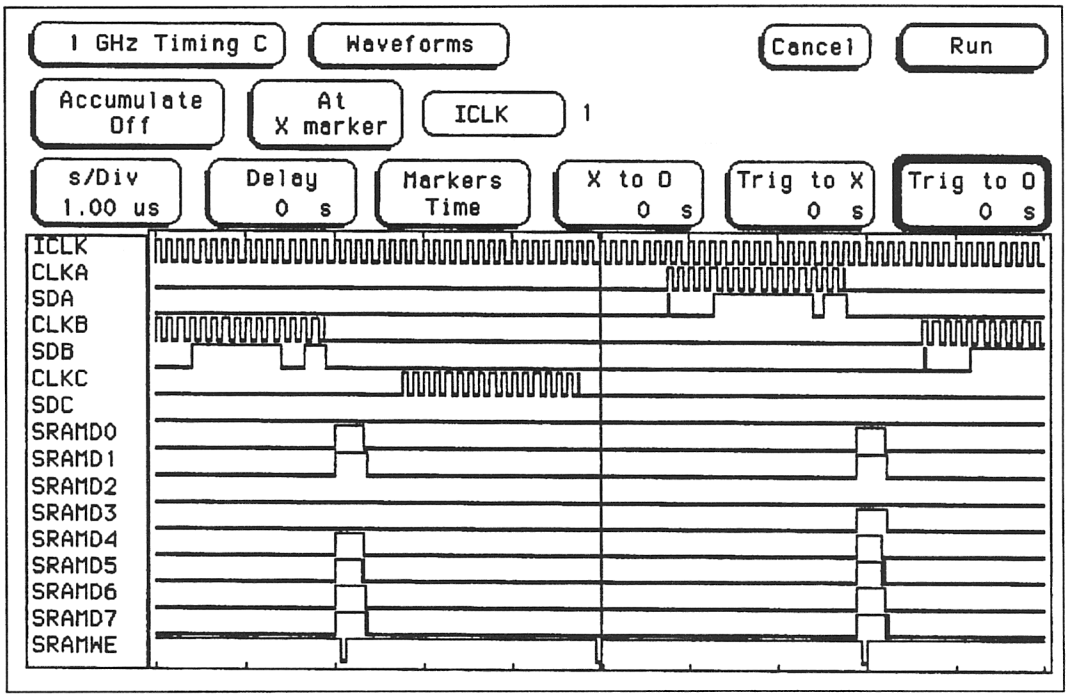


Figure 5-2 Round-robbin Overview

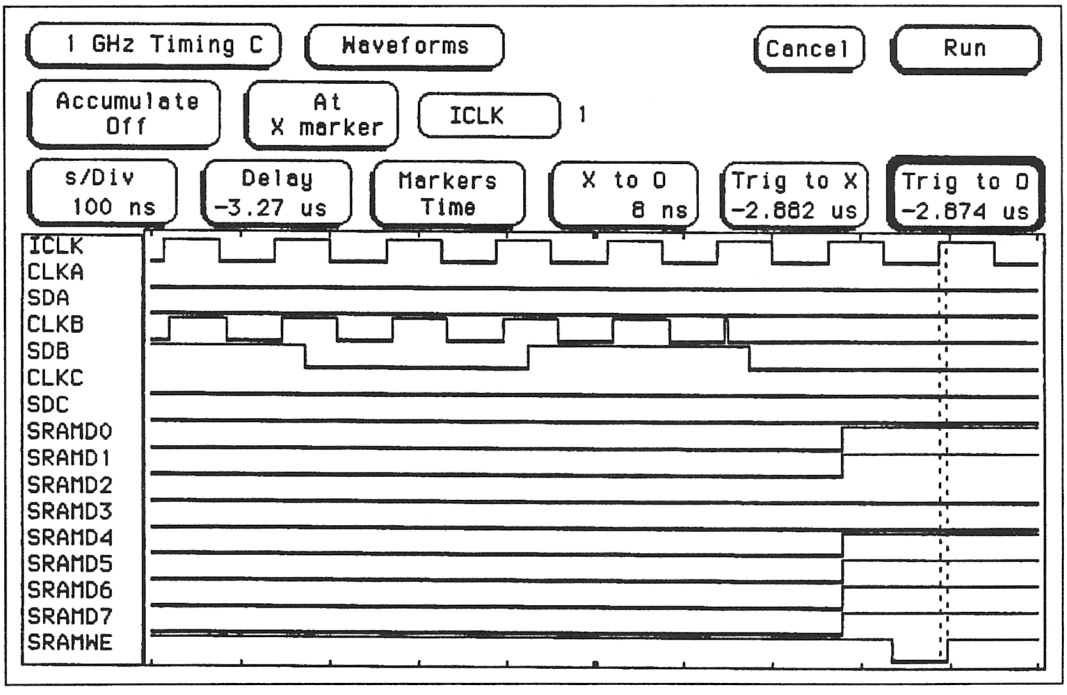


Figure 5-3 ADC Data Capture Detail

5.2.5 Converter Control

Most of the Gray Code engine generated activity has been explored to this point. One area that has not been depicted yet is the actual control signals for the ADC's. The hardware configuration was presented in section 5.2.3. Figure 5-4 presents a detailed look at the actual control of ADC#A. Note that the figure's "N_CNVS" is actually the control line "CTRLA", the asserted low conversion start signal.

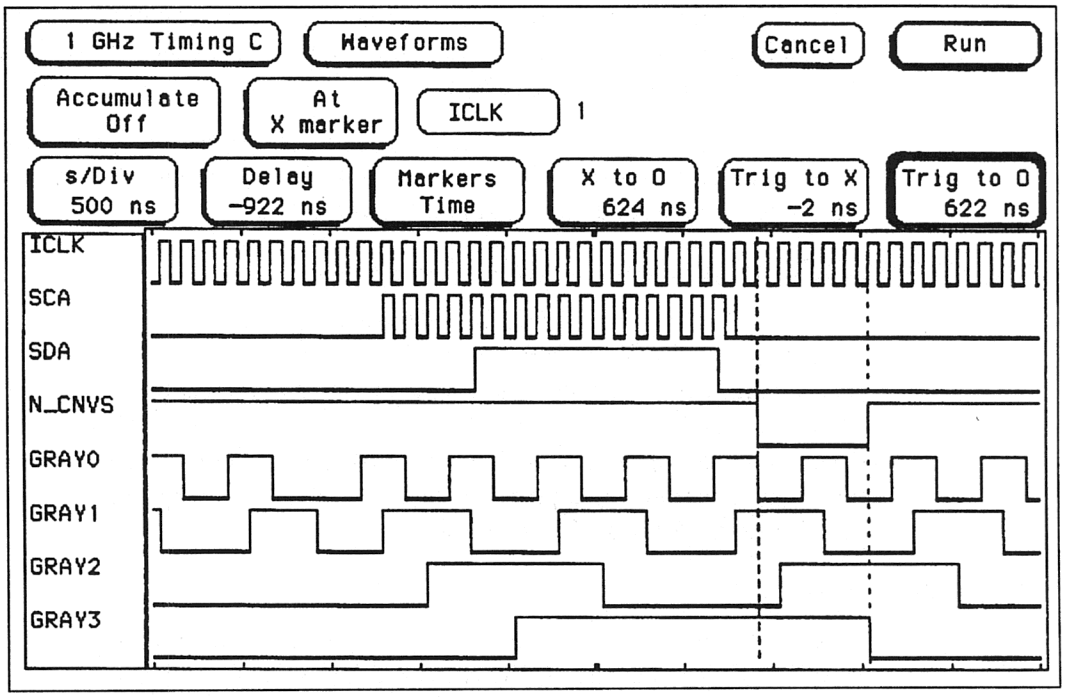


Figure 5-4 ADC Control Details

The ADC's signal acquisition and start of conversion process is controlled by the N_CONVST (CTRLA) signal. The falling edge of this signal resets the ADC's internal counters and registers, while the rising edge changes the front-end analog configuration from track to hold mode and starts the conversion process. The ADC's are self-clocked during the actual conversion process, and they go into track mode automatically following the conversion process, just prior to the first rising edge of SCA in figure 5-4.

The actual tracking time $\approx$ 2.75 µs (22 ICLK cycles preceding the rising edge of N_CONVST), while the the circuitry acquires the input signal to 12-bit accuracy in less than 1.5 µs. The aperature time (track mode $\rightarrow$ hold mode) is typically 15 ns.

The depicted width of N_CONVST is 624 ns, while the ADC's specification calls for a minimum of 600 ns. The four rising edges of ICLK between the falling and rising edges of N_CONVST is where the write to the CVT takes place. It occurs once during this window of opportunity, and on the first rising ICLK edge if no contention to the CVT resources is encountered.

The least significant four bits of the Gray Code engine count is included with this figure for comparison purposes with table 2-1. The Gray Code state just prior to the rising edge of the ICLK that causes the fall of N_CONVST is count #1B *hex*. The Gray Code state just prior to the rising edge of the ICLK that causes the rise of N_CONVST is count #1C *hex*. The four counts in between, #1A, #1E, #1F, and #1D, are states where the

N_SRAMWE pulse can occur. It was triggered to occur by state #1A in figure 5-3 since the CVT was not being read by the carrier.

5.3 Carrier Accesses

The next group of performance data to be examined includes digital-level signals that interface the ADM1224F to its carrier. This information provides the user with empirical data on how fast the carrier can retrieve I/O and ID data from the ADM1224F.

Simulations have demonstrated that a carrier that has the capability of performing back-to-back transfers with no idle cycles, if such a machine existed, could do so when retrieving data from the ADM1224F.

The following information provides typical access information for I/O reads and ID reads. Actual attempts to write to both regions resulted in the expected non-acknowledgements and their resultant bus timeouts.

5.3.1 Hardware Configuration - Carrier Accesses

ADM1224F#114 was mounted on a VMESC5 (5-slot VME-6U slave carrier) in slot A using a Type 1 IPack Logic Bus Extender Board under the ADM1224F. The carrier's base address configured the IPack's I/O addresses for a start at address FFFF2000 *hex*. A 2″ extender cable was connected between the extender and an IPack Logic Bus Breakout Board where all of the connections to signals and ground references were made. All timing information was captured using an HP 1 GHz Timing Module Model 16515A in a 16500A Logic Analysis System chassis.

5.3.2 IPack Transfers

This short section presents the typical timing data for the only two transfer types that the ADM1224F IPack supports: I/O reads and ID reads. Table 5-1 tabulates the data and figure 5-5 presents a typical I/O read (@ IPA = 00, IPD = 003). The I/O read's IPDbus data setup time ≈ 207 ns, while for the ID read it ≈ 116 ns.

Table 5-1 Carrier Accesses Typical Times

Transfer Type	↑ ICLK until:	TIME (ns)
I/O Read (IPA = 00)	↓ N_ACK	10
	↑ N_ACK	10
ID Read (IPA = 00)	↓ N_ACK	11
	↑ N_ACK	9

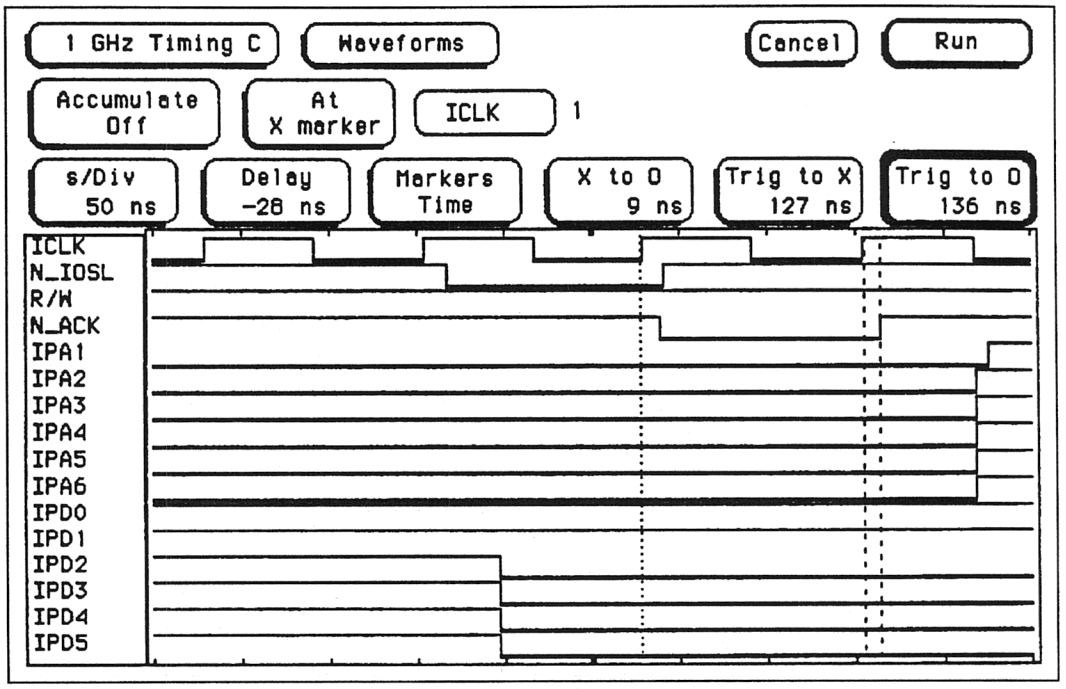


Figure 5-5 Typical I/O Read Timing

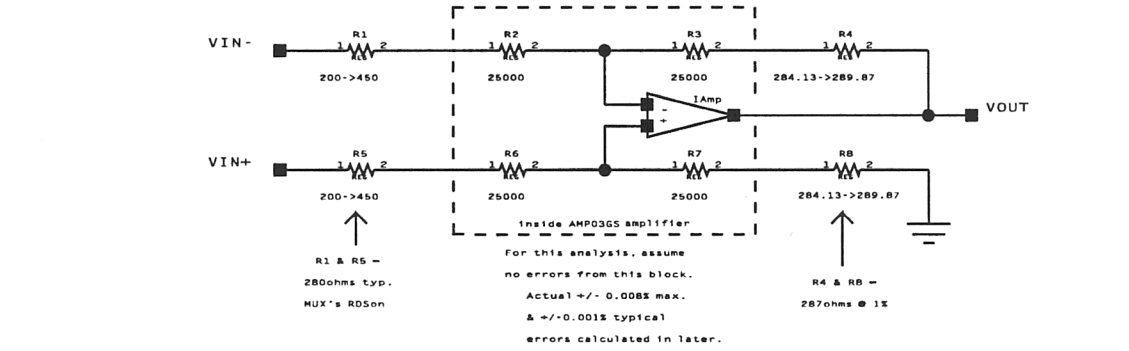
5.4 Theoretical Accuracy

This short subsection attempts to provide an analytical determination of the worst case errors that could reduce the accuracy of the ADM1224F. It uses the square-root-of-the-sum-of-the-squares technique, and covers both gain and offset contributions to overall inaccuracies. Since these include theoretical worst-case margins for most of the components used in the analog section, the statistical probability of having all components exhibiting worst-case errors is nearly nil. The bottom line is that the ADM1224F will always work better than what this analysis says.

The analysis is contained within the next three figures. Figure 5-6 and the top half of figure 5-7 attempt to determine the worst case gain errors for the analog "front-end" consisting of the analog multiplexers and their associated differential amplifiers. This is conducted in two steps:

- First, the amplifier is assumed to have no gain errors and the error contribution from the multiplexer and two "gain" resistors is determined.
- Then the worst case specification for the amplifier is factored into the analysis.

The bottom half (below the triple horizontal lines) of figure 5-7 then includes gain errors from the ADCs and their voltage reference. The result of this gain error analysis is that the worst case error = 0.769%.



$$Vout = \left(\frac{Vin+ * \left(\frac{R7 + R8}{R5 + R6 + R7 + R8} \right) - Vin- * \left(\frac{R3 + R4}{R1 + R2 + R3 + R4} \right)}{\left(\frac{R1 + R2}{R1 + R2 + R3 + R4} \right)} \right)$$

$$\text{Let "Rnum"} = \left(\frac{R7 + R8}{R5 + R6 + R7 + R8} \right) - \left(\frac{R3 + R4}{R1 + R2 + R3 + R4} \right)$$

Assumes R4 = R8, & that R1 = R5.

$$\text{Let "Rden"} = \left(\frac{R1 + R2}{R1 + R2 + R3 + R4} \right)$$

DIFFERENTIAL-MODE "GAIN"

Ideal Gain = 1

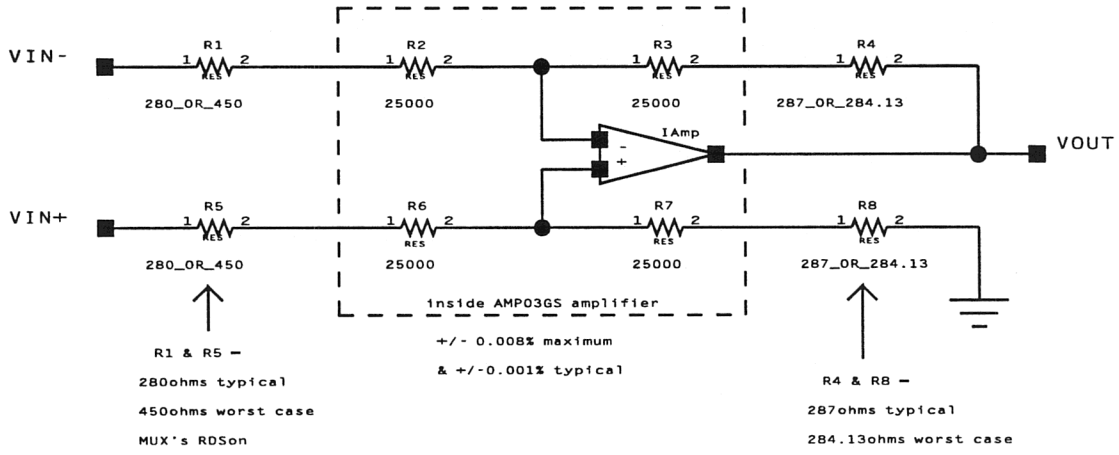
$$\text{therefore: } Vout = \left(\left(Vin+ - Vin- \right) * \left(\frac{Rnum}{Rden} \right) \right)$$

For R1 & R5, the nominal value is 280ohms, 200ohms minimum, & 450ohms maximum.

For R4 & R8, the nominal value is 287ohms, 284.13ohms minimum, & 289.87ohms maximum.

R1 = R5 =	280 ohms	450 ohms	450 ohms	200 ohms	200 ohms
R4 = R8 =	287 ohms	289.87 ohms	284.13 ohms	289.87 ohms	284.13 ohms
Rnum =	.5000692151	.4984220496	.4983653016	.5008899805	.5008332321
Rden =	.4999307849	.5015779504	.5016346984	.4991100195	.4991667679
"GAIN" =	1.000276899	.9937080551	.9934825146	1.00356627	1.003338492
% error =	+0.028%	-0.629%	-0.652%	+0.357%	+0.334%
NOTES:	TYPICAL		WORST CASE		

Figure 5-6 Front-end Gain Error Analysis



Analog Frontend Errors:

$$\sqrt{(0.652)^2 + (0.008)^2} = 0.652\% \text{ worst case}$$

$$\sqrt{(0.028)^2 + (0.001)^2} = 0.028\% \text{ typical}$$

ADM1224F "total", WORST CASE GAIN ERROR ANALYSIS

Sources of Gain Error:

"Frontend" = 0.652% (see above)

"VREF" = 2.49volts minimum = -0.4% (no "Buffer" Gain Error used)
= 2.51volts maximum = +0.398%
= 0.4%

"ADC1" = +/-3lsb maximum for +/- Full Scale Error
= 0.073%

"ADC2" = +/-1lsb maximum for Relative Accuracy
= 0.024%

Total Worst Case Gain Error =

$$\sqrt{(0.652)^2 + (0.4)^2 + (0.073)^2 + (0.024)^2}$$

Total Worst Case Gain Error = 0.769%
= 7.023 Bits Accuracy

Figure 5-7 Overall Gain Error Analysis

The top half of figure 5-8 (above the triple horizontal lines) presents a worst-case analysis of significant errors due to offsets. These do not include any offset errors that may be induced due to poor grounding techniques. The bottom half of figure 5-8 is the final combination of all worst-case gain and offset errors for this analysis. All of the margins and values used in this analysis are data sheet parameters for units operating within voltage specifications and at 25°C.

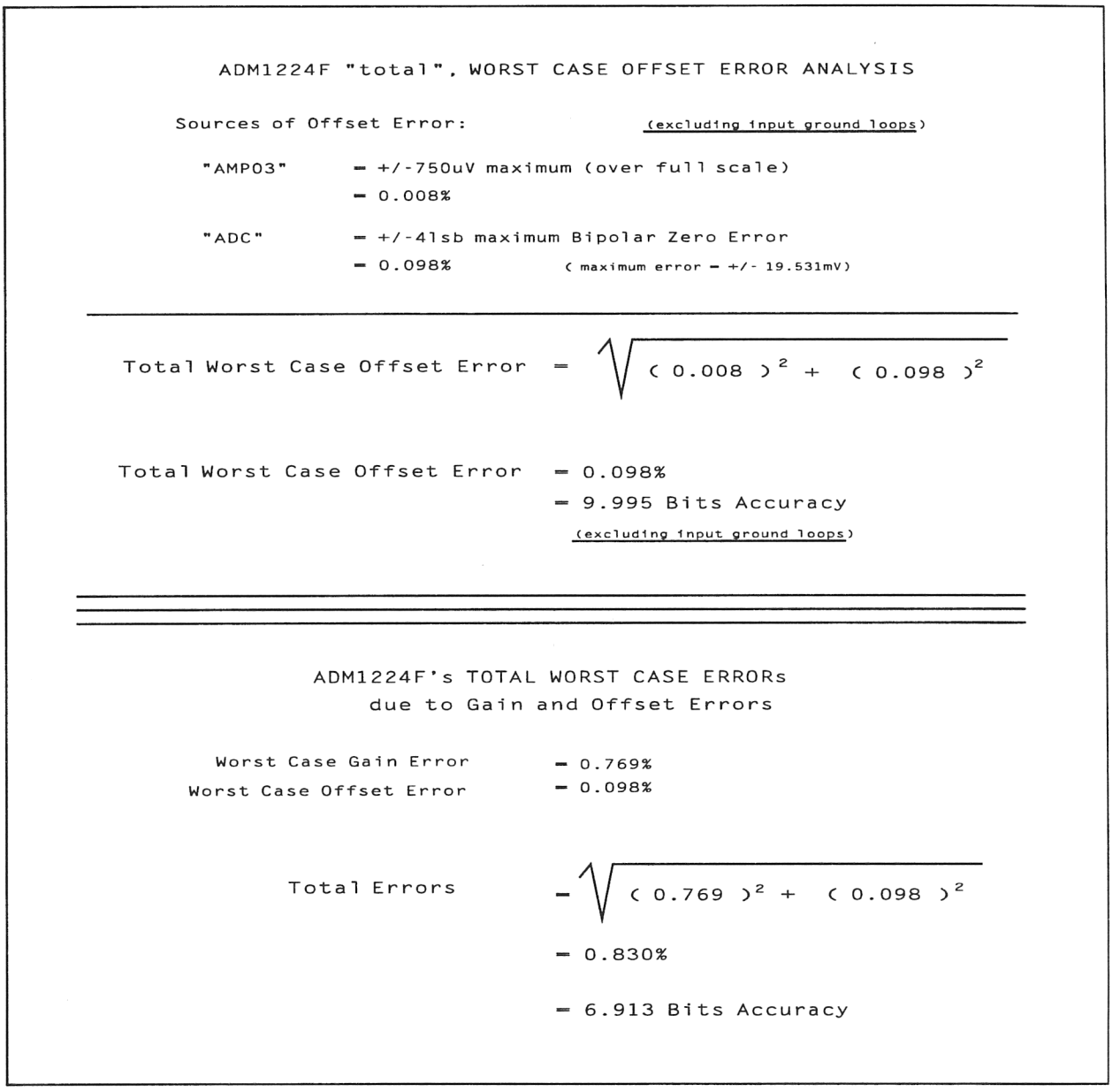


Figure 5-8 Offset and Total Error Analysis

5.5 Typical Empirical Performance

The next subsection presents a statistical analysis based on a group of samplings taken at one input voltage on one ADM1224F which provides some characteristic performance information.

5.5.1 Hardware Configuration

ADM1224F#111, with all twenty-four channels configured for single-ended inputs, was installed on slot B of a 162-01 single board computer, which was then installed in an open-frame VME-6U chassis, a 12-slot Tracewell T-FRAME. The IPack slot used provided the noisiest test environment available due to the close proximity of the 25 MHz clock generation circuitry, and the ASIC for the IPack interface logic, straddled by the XC68LC040RC25B (CPU) on one side and the VMEbus ASIC on the other.

A 3′, standard 50-pin IDC ribbon (non-twisted pair, unshielded, 26AWG) cable connected the I/O interface to a Phoneix Contact 50-pin DIN-Rail terminal block. All twenty-four noninverting inputs were tied together and all twenty-four inverting inputs were tied together and to pins #25 and #26 (AREF). A loosely twisted (≈ 1 twist per 2″) pair of 12 AWG wire, 3′ in length, attached the terminal block to a TENMA laboratory DC power supply, model #72-2005. There were four 40 watt flurescent lamps 5′ above this table-top setup, and there were three operating personal computers within 7′. No extra effort was made to protect the test configuration from noise sources to demonstrate "typical" operations.

5.6 Data Gathering

A program was written to capture a user-specified number of data points, in round-robbin fashion (channels 1 → 24 repeated the number of times specified), with the hexadecimal information being converted to volts, tabulated and stored on a hard disk. The tabulation process was done in such a manner to allow for direct insertion of the data into an EXCEL workbook for analysis.

The power supply was set to +5.000 volts. The program was run to capture 100 sample sets, which yielded 2400 samples total (100 per channel). The data was transported to a personal computer via floppy disk for analysis.

5.6.1 Data Results

A significant amount of descriptive statistical analysis was conducted on the 2400 raw samples that were acquired. One of many possible ways of summarizing the results follows.

The data was analyzed on a per-channel basis. The mean (average) was calculated for each channel (100 samples each) and the resultant scattergram was developed to plot these means by channels. Figure 5-9 is this plot. Except for channel 10, the plotted means show a distinct pattern by group of eight channels, which is expected given that there are three different analog subsystems on the ADM1224F. On similar plots for many other data samplings for many other boards, this is a common trait. Another obvious feature is that all three groupings present a negative offset from the ideal of +5.000 volts.

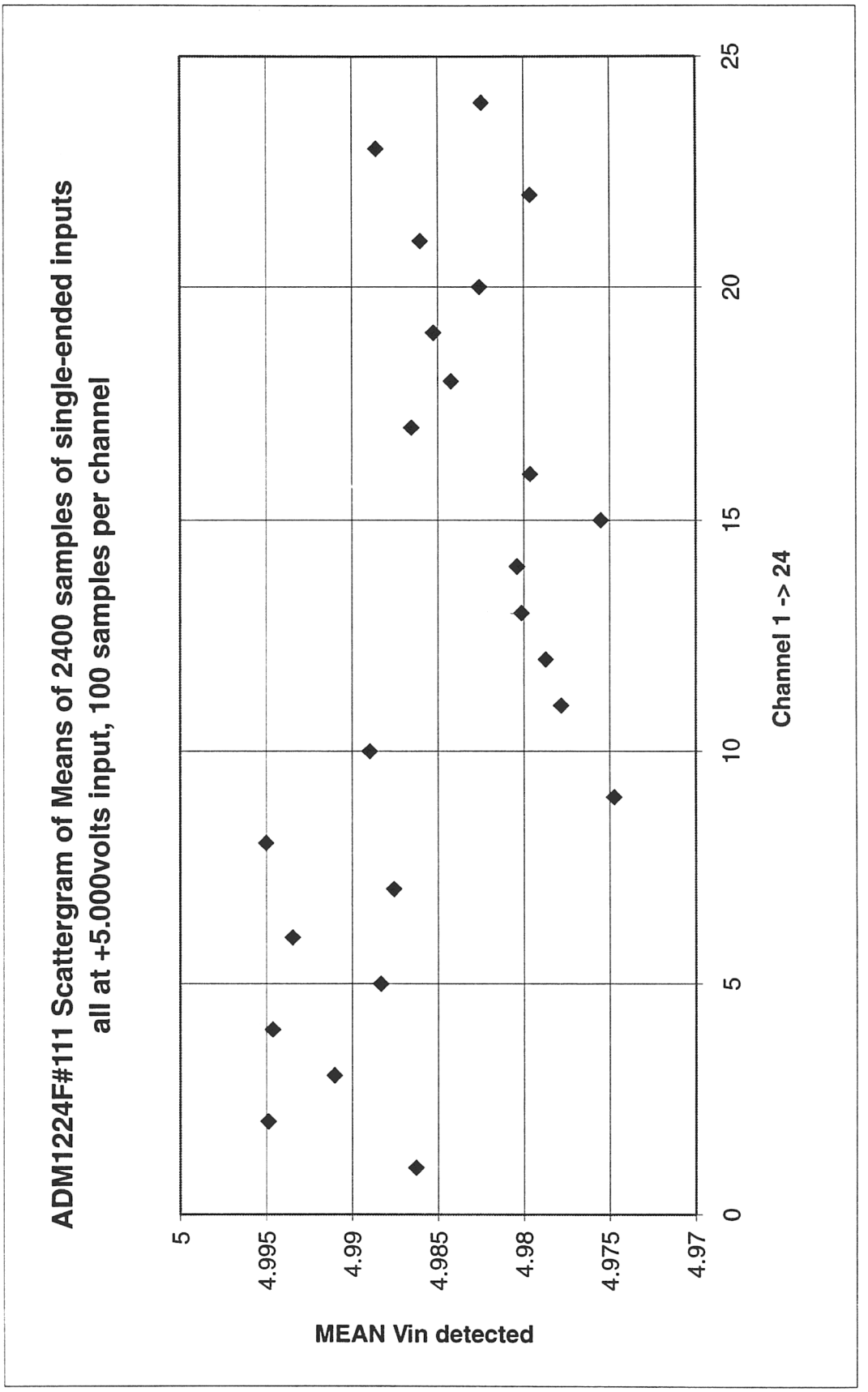


Figure 5-9 Scattergram of Means by channel

The standard deviation is often used as a definition of RMS Noise for ADCs. Figure 5-10 is a plot of the average RMS noise on a per channel basis. No per analog subsystem patterns are evident in this sampling, or any of those taken for many other boards and many different input voltages.

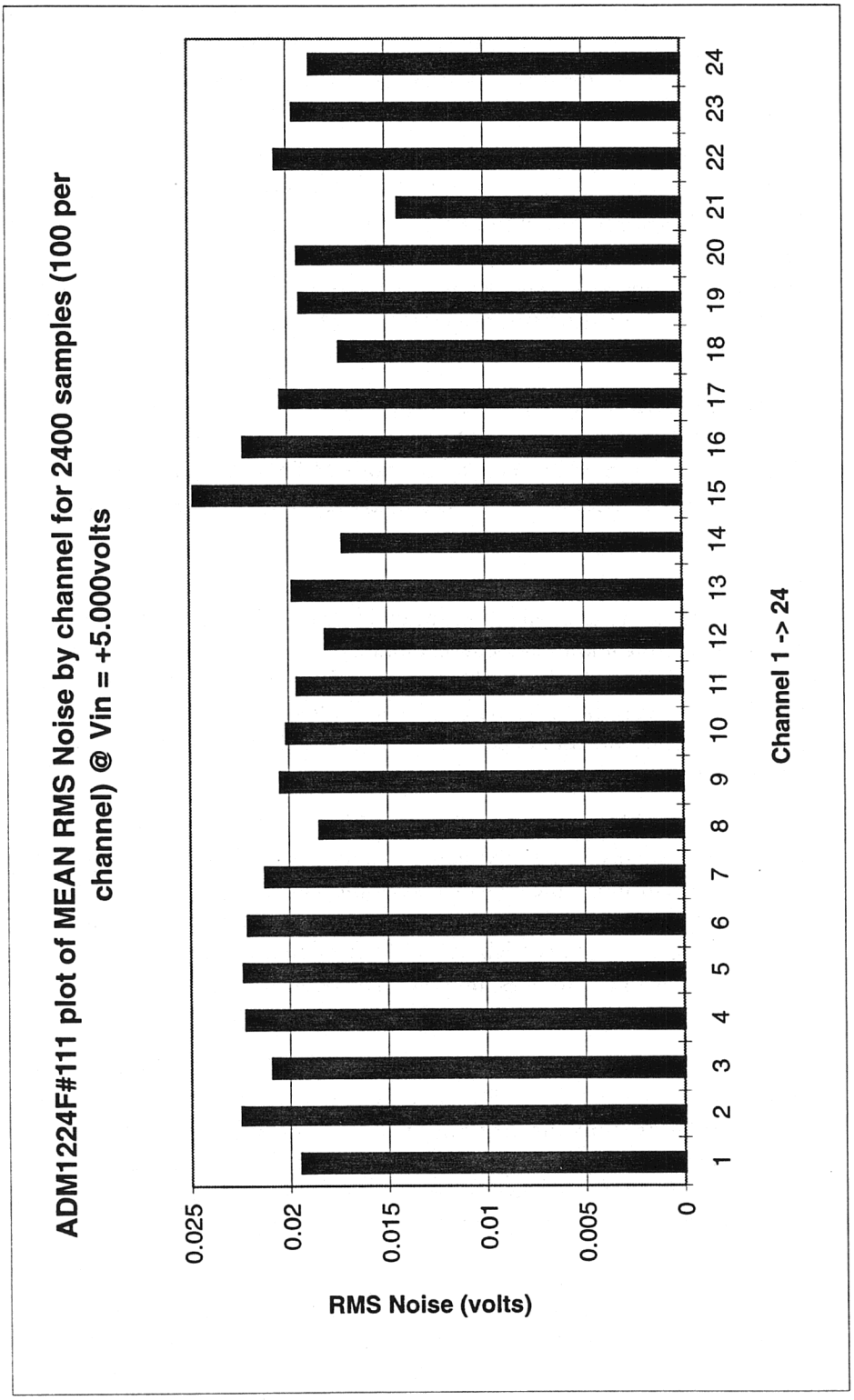


Figure 5-10 Average RMS Noise by channel

There are two more distinct viewpoints that can be used on this data. One direction includes figuring out the overall average statistics for all 2400 samples. The other is to look at non-averaged raw data distributions.

Using the descriptive statistical analysis output developed on a per channel basis, summary statistics were generated for both the mean values and the standard deviation values (RMS Noise). Remember that these calculations were performed on the 24 values of each type that were a result of the work performed above. This can be accomplished since identical numbers of samples were collected for each channel.

The overall Mean input voltage acquired is +4.985094 volts. This represents an average error of 0.014906 volts, or ≈-3.05 lsb. The minimum mean value was +4.974743 volts (*channel #9 in figure 5-9*), and the maximum mean value was +4.995055 volts (*channel #8 in figure 5-9*). These represent maximum and minimum errors (*minimum mean → maximum error and maximum mean → minimum error*) of 0.025257 volts, or ≈-5.17 lsb, and 0.004945 volts, or ≈-1.01 lsb, respectively. The median value was slightly more positive than the mean, with a value of +4.985632 volts.

The overall RMS Noise is 0.020047 volts, or ≈4.11 lsb. Channel #21 (*see figure 5-10*) presented the least amount of RMS Noise with a value of 0.014318 volts, or ≈2.93 lsb. Channel #15 presented the most amount of RMS Noise with a value of 0.024757 volts, or ≈5.07 lsb. The median value was slightly less than the mean, with a value of 0.019936 volts.

Normally, when a histogram of samples is plotted for a single ADC, the appearance of bimodal data (more than one peak) often indicates a nonlinearity error in the conversion process. Coupling additional analog circuitry to the front-end of a single ADC complicates the picture due to the addition of gain and offset errors, along with the significant increase in subsystem RMS Noise levels (as has been presented so far). When three subsystems are combined and the distribution of samples is examined, the picture becomes very complex.

Figure 5-11 is a histogram plot of just the 800 samples taken for the analog subsystem supporting channels 1 → 8. By mentally drawing a line through the columns consisting of 20 samples or more, the distribution of the samples approximates a quasi-bell-curve. The column with the most samples corresponds to the detected voltage of +4.995104 volts, which is 1 lsb below the ideal input voltage for these particular tests. The ranked percentile for this input voltage value, for channels 1 → 8, is: 44.40%, 31.30% 38.30%, 33.30% 42.40%, 30.30%, 42.40%, and 29.20%, respectively.

Figure 5-12 is a histogram plot of just the 800 samples taken for the analog subsystem supporting channels 9 → 16. By mentally drawing a line through the columns consisting of 20 samples or more, the distribution of the samples approximates a quasi-bell-curve. Again, the column with the most samples corresponds to the detected voltage of +4.995104 volts. The ranked percentile for this input voltage value, for channels 9 → 16, is: 67.60%,35.30%, 67.60%, 59.50%, 57.50%, 63.60%, and 56.50%, respectively.

Figure 5-13 is a histogram plot of just the 800 samples taken for the analog subsystem supporting channels 17 → 24. By mentally drawing a line through the columns consisting of 20 samples or more, the distribution of the samples approximates a quasi-bell-curve. This time, the column with the most samples corresponds to the detected voltage of +4.975573 volts, which is ≈5 lsb below the ideal input voltage for these particular tests. The ranked percentile for this input voltage value, for channels 17 → 24,

is: 18.10%, 15.10%, 12.10%, 14.10%, 4.00%, 18.10% 11.10%, and 21.20%, respectively. Note that the ranked percentiles for the most common value for channels 1 → 16, +4.995104 volts, had ranked percentiles for channels 17 → 24 that ranged from 49.40% → 68.6%.

Figure 5-14 presents a combined histogram for all 2400 samples. Because there are actually three different distributions overlayed with different skew and kurtosis values, it is more difficult to envision a smooth bell-curve distribution for this figure.

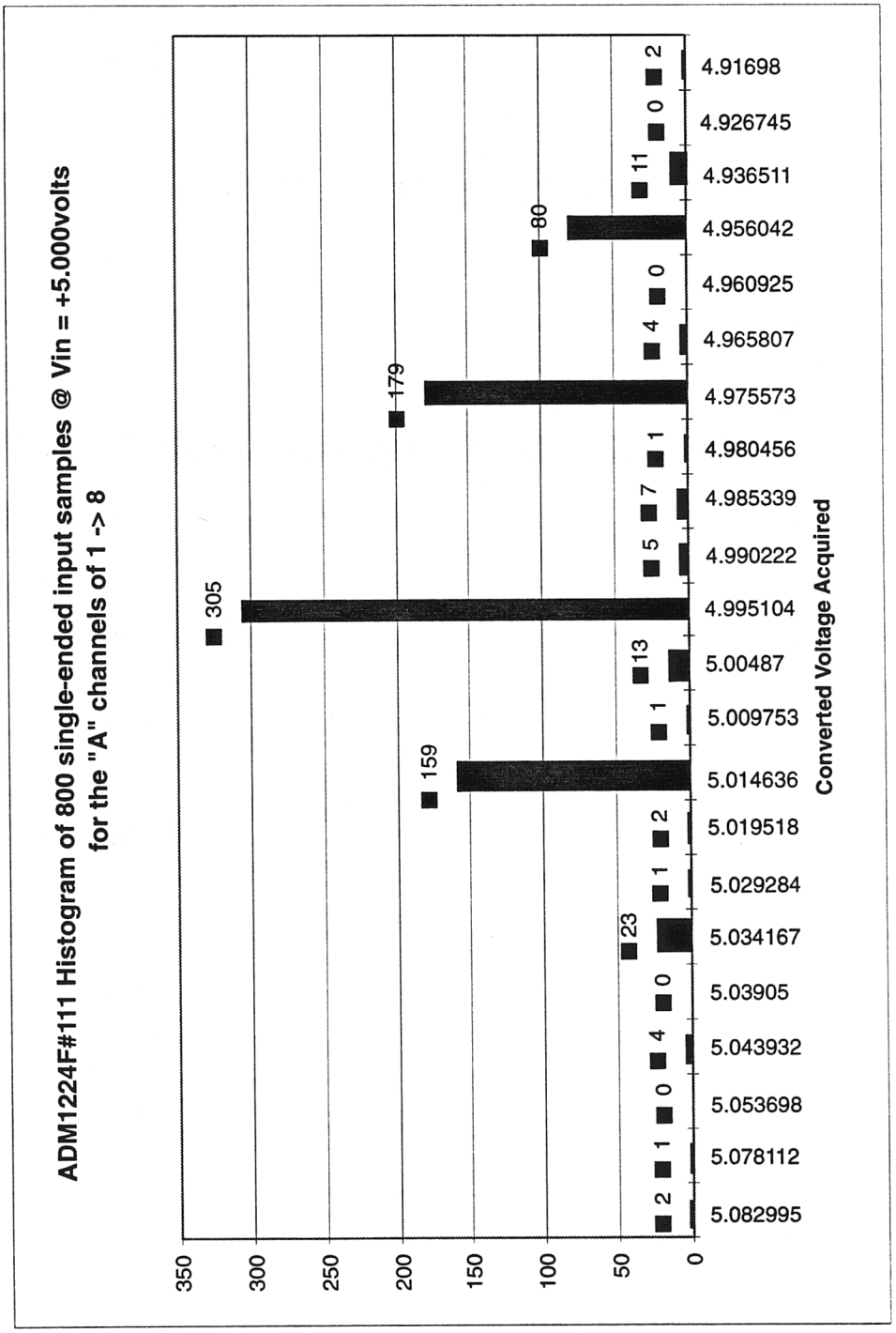


Figure 5-11 Histogram of samples for channels 1 → 8

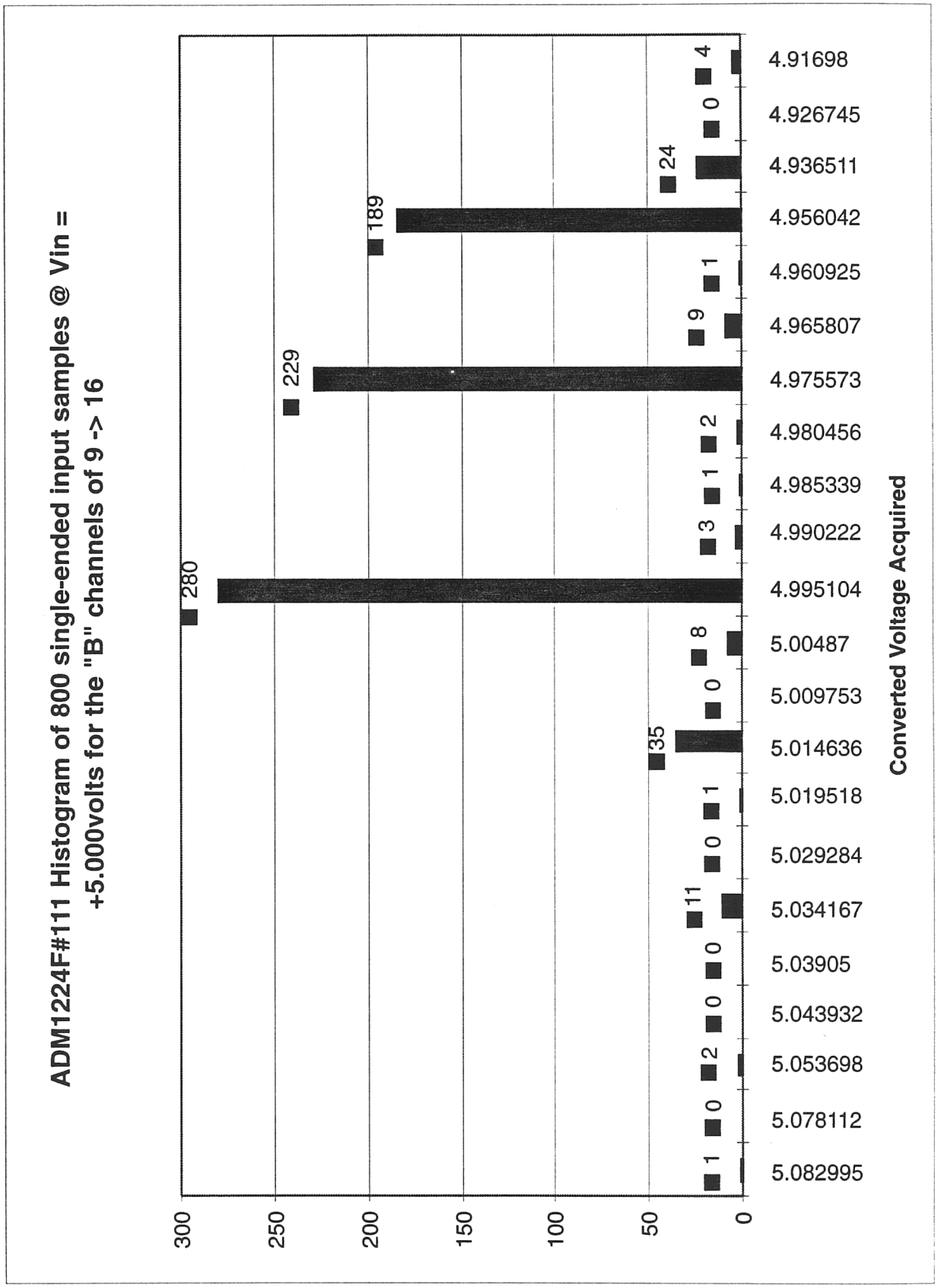


Figure 5-12 Histogram of samples for channels 9 → 16

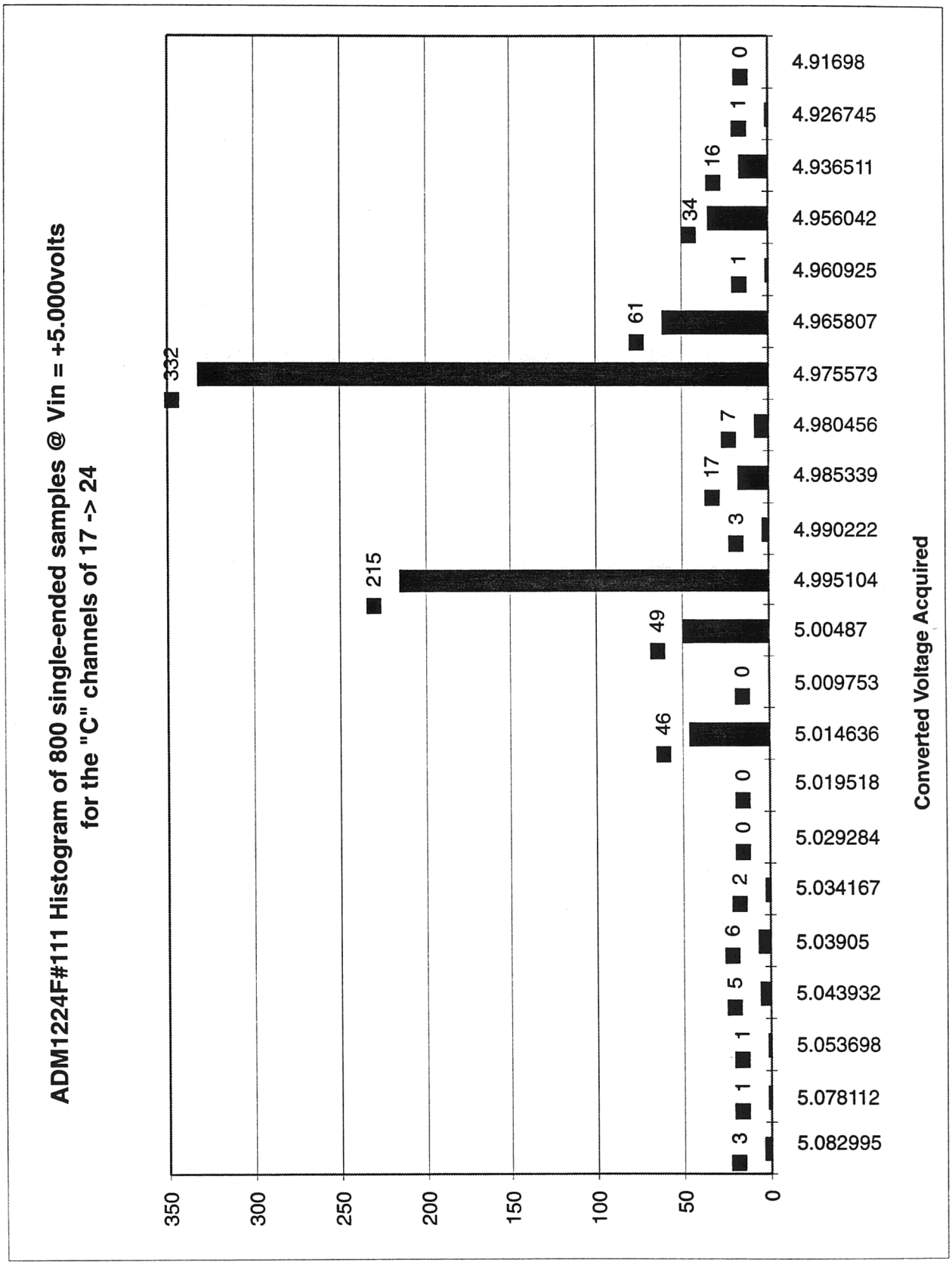


Figure 5-13 Histogram of samples for channels 17 → 24

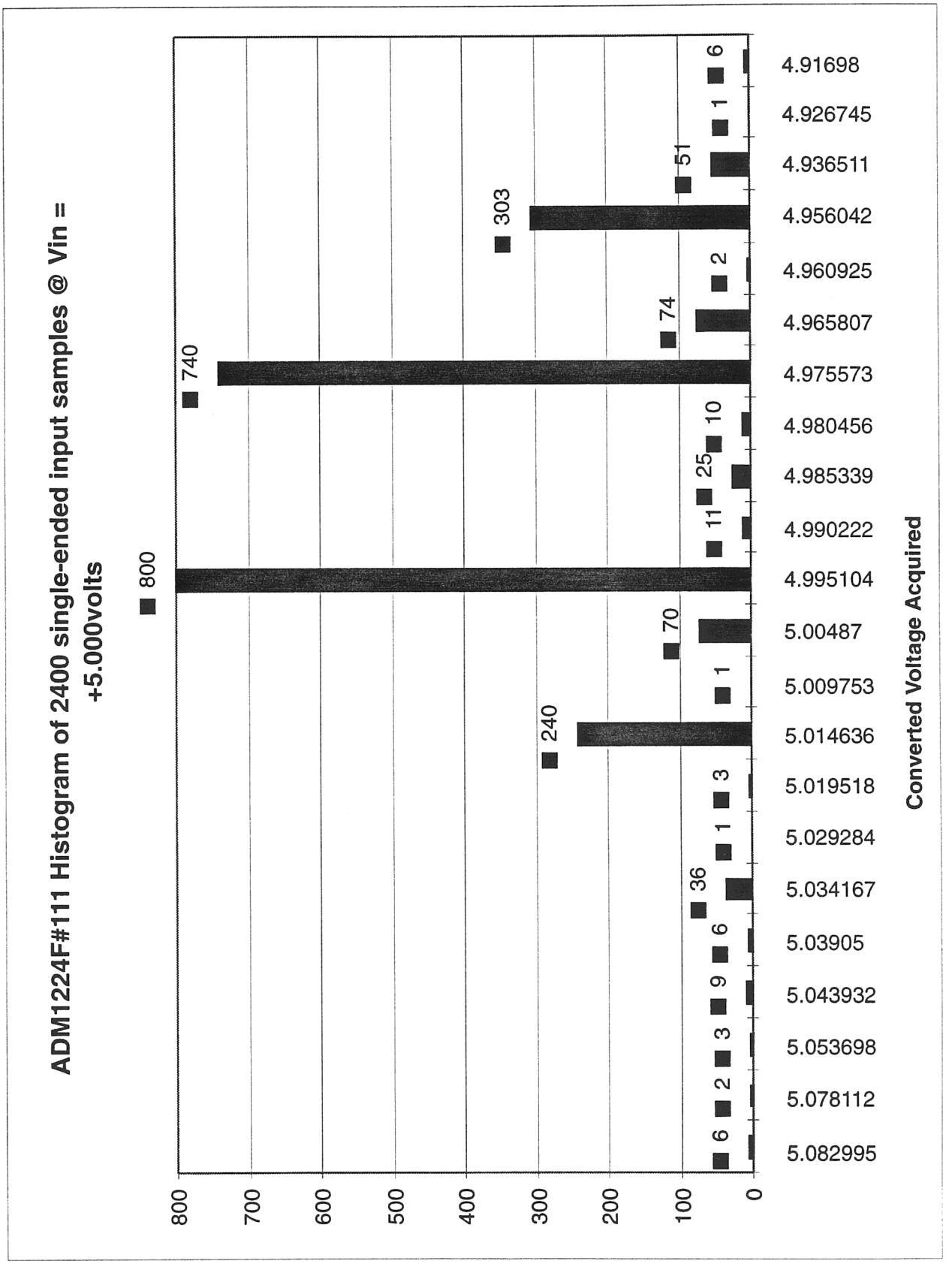


Figure 5-14 Histogram of samples for all channels

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the ADM1224F IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 Deterministic sampling Matrix

Section 2.5.3 provided detailed information about the sequential sampling timing, while section 2.5.4 provided some examples of determining the exact amount of time between any two samples given their channel numbers and the value of the samples' frame-counter nibbles. This subsection provides, in tabular/matrix format, the technical information that was consulted for the development of sections 2.5.3 and 2.5.4.

Figure 6-1 diagramatically presents the information supplied in section 2.5.3. There are eight groups of three channels separated by dashed lines. The first sample of each group is that acquired through the "A" section of circuitry for channels 1 → 8. The second sample of each group is that acquired through the "B" section of circuitry for channels 9 → 16. The third sample of each group is that acquired through the "C" section of circuitry for channels 17 → 24. The delta time between "A" channels and "B" channels is 2.875 μs. The delta time between "B" channels and "C" channels is 2.875 μs. The delta time between "C" channels and "A" channels is 3.000 μs. The extra 125ns in the latter timing is due to the addition of the seventieth Gray Code sequence state to maintain single-bit transitions through the count sequence.

The SADD# column in figure 6-1 provides the "SRAM ADDress" value of the CVT, in hexadecimal, where the ADC data is stored. These are the same addresses used by the carrier for retrieving CVT data, as driven by IPA[6:1].

The far right column of figure 6-1 provides summation aggregrate timing for all channels referenced to channel #1. For example, the elapsed time between the sampling of channel #1 until channel #6 is sampled is 43.750 μs. The time between channel #1's sampling and the capturing of channel #4 in the next frame (as defined by the frame counter values) is 26.250 μs + 70.000 μs for the additional frame. Refer to section 2.5.4 for additional examples.

While Figure 6-1 works fine for timings referenced to channel #1, this is not a complete look at all possibilities. A full matrix, of course, would be twenty-four columns wide and twenty-four rows deep. Such a matrix is presented in figures 6-2 and 6-3. The reference channel is that defined by the column, as read across the top of the matrix. The second channel's timing with respect to the reference channel is found in the left margin, read from top to bottom.

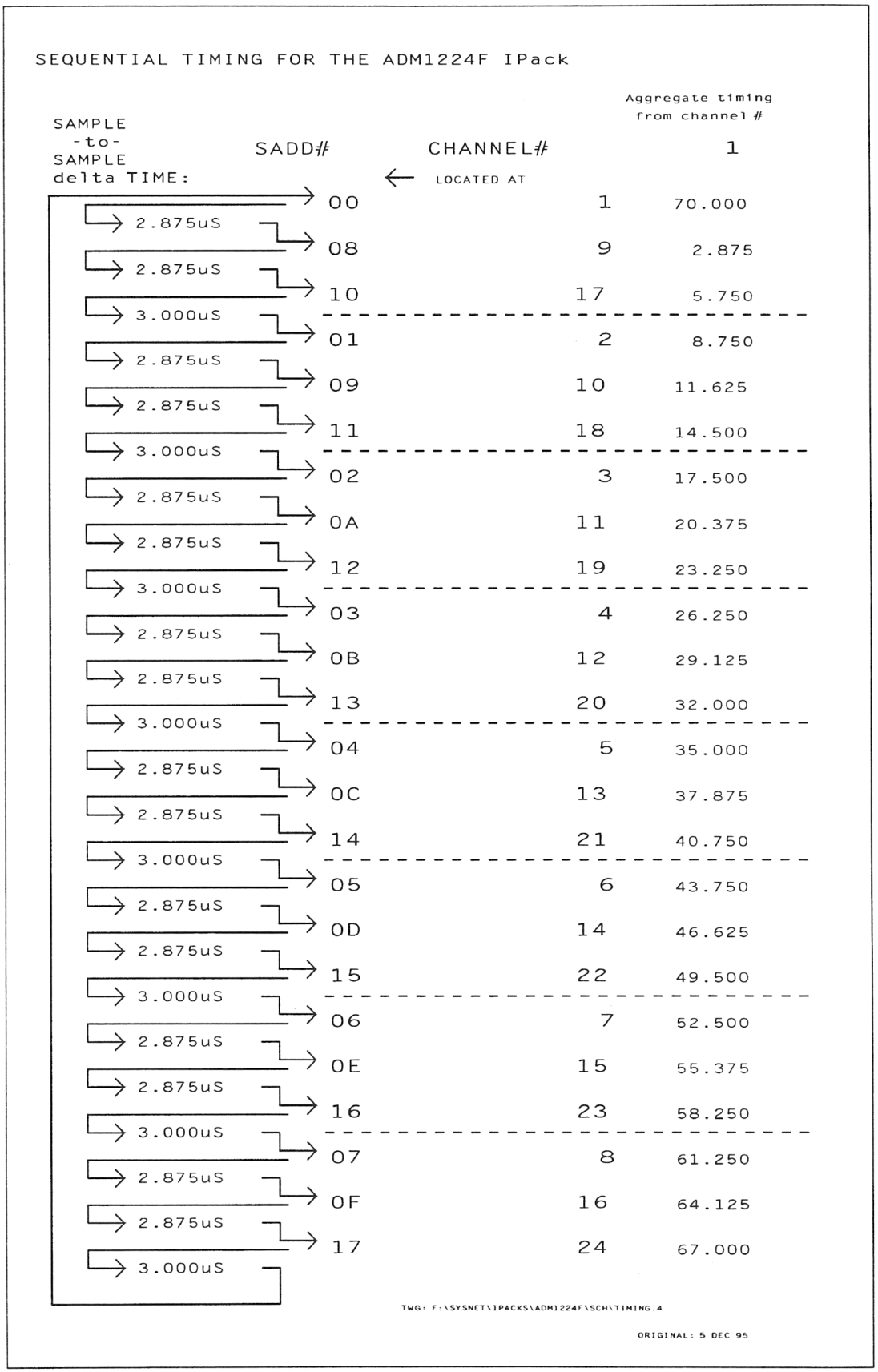


Figure 6-1 sequential sampling Timing

TIMING CROSS MATRIX FOR THE ADM1224F IPack

TO CHANNEL#: ↓ ↓ ↓ ↓ FROM CHANNEL#: →

ALL TIMES IN MICROSECONDS

SAMPLE -to- SAMPLE delta TIME:	SADD#	CHANNEL# LOCATED AT ←	1	9	17	2	10	18	3	11	19	4	12	20
→	00	1	70.000	67.125	64.250	61.250	58.375	55.500	52.500	49.625	46.750	43.750	40.875	38.000
→ 2.875uS →	08	9	2.875	70.000	67.125	64.125	61.250	58.375	55.375	52.500	49.625	46.625	43.750	40.875
→ 2.875uS →	10	17	5.750	2.875	70.000	67.000	64.125	61.250	58.250	55.375	52.500	49.500	46.625	43.750
→ 3.000uS →	01	2	8.750	5.875	3.000	70.000	67.125	64.250	61.250	58.375	55.500	52.500	49.625	46.750
→ 2.875uS →	09	10	11.625	8.750	5.875	2.875	70.000	67.125	64.125	61.250	58.375	55.375	52.500	49.625
→ 2.875uS →	11	18	14.500	11.625	8.750	5.750	2.875	70.000	67.000	64.125	61.250	58.250	55.375	52.500
→ 3.000uS →	02	3	17.500	14.625	11.750	8.750	5.875	3.000	70.000	67.125	64.250	61.250	58.375	55.500
→ 2.875uS →	0A	11	20.375	17.500	14.625	11.625	8.750	5.875	2.875	70.000	67.125	64.125	61.250	58.375
→ 2.875uS →	12	19	23.250	20.375	17.500	14.500	11.625	8.750	5.750	2.875	70.000	67.000	64.125	61.250
→ 3.000uS →	03	4	26.250	23.375	20.500	17.500	14.625	11.750	8.750	5.875	3.000	70.000	67.125	64.250
→ 2.875uS →	0B	12	29.125	26.250	23.375	20.375	17.500	14.625	11.625	8.750	5.875	2.875	70.000	67.125
→ 2.875uS →	13	20	32.000	29.125	26.250	23.250	20.375	17.500	14.500	11.625	8.750	5.750	2.875	70.000
→ 3.000uS →	04	5	35.000	32.125	29.250	26.250	23.375	20.500	17.500	14.625	11.750	8.750	5.875	3.000
→ 2.875uS →	0C	13	37.875	35.000	32.125	29.125	26.250	23.375	20.375	17.500	14.625	11.625	8.750	5.875
→ 2.875uS →	14	21	40.750	37.875	35.000	32.000	29.125	26.250	23.250	20.375	17.500	14.500	11.625	8.750
→ 3.000uS →	05	6	43.750	40.875	38.000	35.000	32.125	29.250	26.250	23.375	20.500	17.500	14.625	11.750
→ 2.875uS →	0D	14	46.625	43.750	40.875	37.875	35.000	32.125	29.125	26.250	23.375	20.375	17.500	14.625
→ 2.875uS →	15	22	49.500	46.625	43.750	40.750	37.875	35.000	32.000	29.125	26.250	23.250	20.375	17.500
→ 3.000uS →	06	7	52.500	49.625	46.750	43.750	40.875	38.000	35.000	32.125	29.250	26.250	23.375	20.500
→ 2.875uS →	0E	15	55.375	52.500	49.625	46.625	43.750	40.875	37.875	35.000	32.125	29.125	26.250	23.375
→ 2.875uS →	16	23	58.250	55.375	52.500	49.500	46.625	43.750	40.750	37.875	35.000	32.000	29.125	26.250
→ 3.000uS →	07	8	61.250	58.375	55.500	52.500	49.625	46.750	43.750	40.875	38.000	35.000	32.125	29.250
→ 2.875uS →	0F	16	64.125	61.250	58.375	55.375	52.500	49.625	46.625	43.750	40.875	37.875	35.000	32.125
→ 2.875uS →	17	24	67.000	64.125	61.250	58.250	55.375	52.500	49.500	46.625	43.750	40.750	37.875	35.000
→ 3.000uS →														

DATA TAKEN DURING FRAME COUNTS OF 0 -> 1.

TMB: F:\SYSBOT\IPACKS\ADM1224F\SCH\TIMING.X

revised: 8 DEC 95

Figure 6-2 Left half of full Timing Matrix

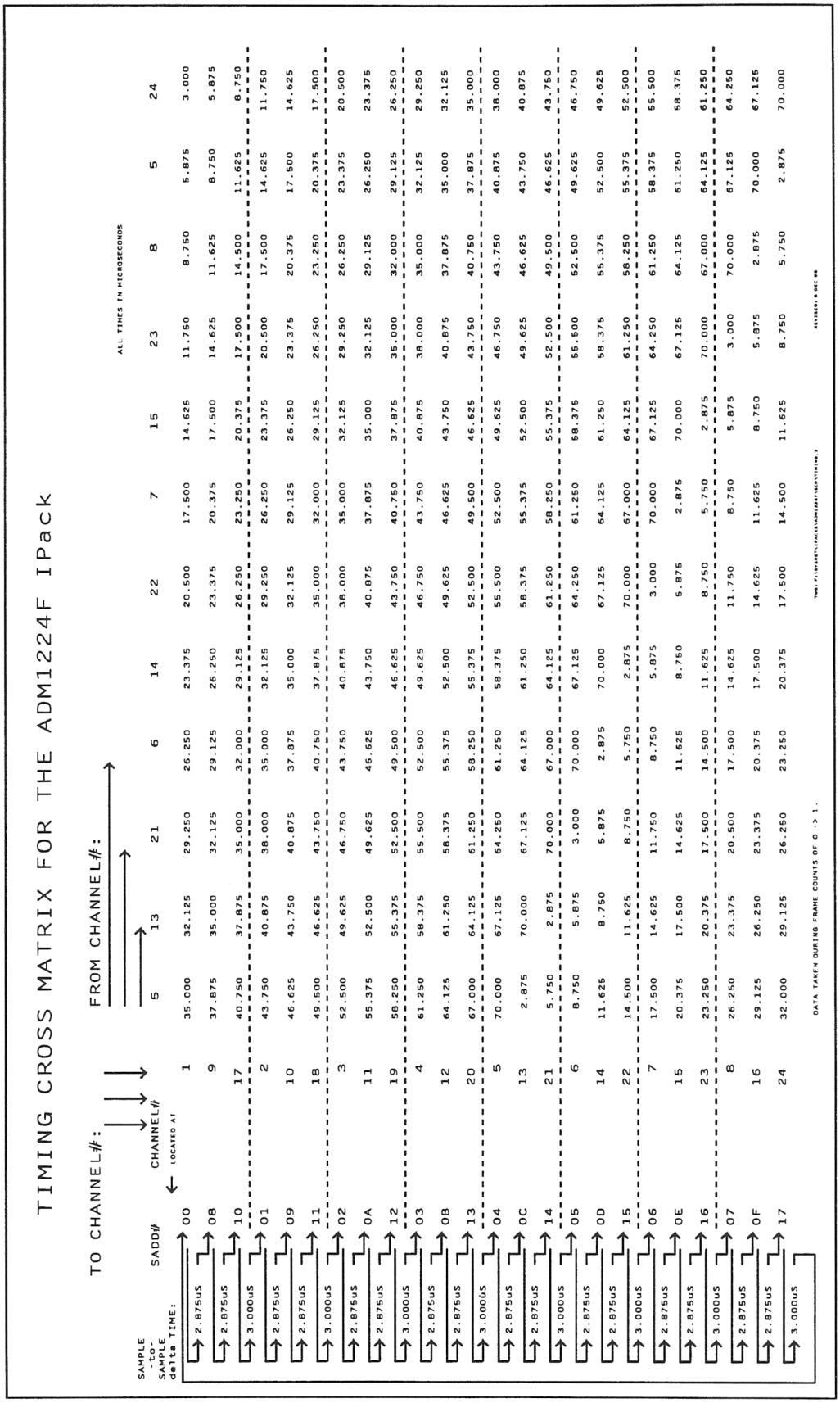


Figure 6-3 Right half of full Timing Matrix

Instead of providing detailed steps on how section 2.5.4 was developed, a couple of new examples are provided below for determining exact sampling timing relationships. At this time it is important to reiterate (from section 5.2.5) that the aperture time is typically 15ns, which is the uncertainty for these timing relationship examples.

Order of sampling is important. The time between sampling channel #18 and then sampling channel #7 is 38.000 μs, while the time between sampling channel #7 and then sampling channel #18 is 32.000 μs. Note that the summation of the two equals a full frame of 70.000 μs. Refer, first, to Figure 6-2. Across the top, moving left → right, find the column labeled as channel #18. This is the reference (first) channel. Now move down the list of "TO CHANNEL#" in the left margin until channel #7 is found (first of three channels in the second-last group). At the intersection of column #18 and row #7 is the time of 38.000 (in microseconds). Now refer to figure 6-3. Across the top find channel #7, and down the left side find channel #18. The time that elapses from the sampling of channel #7 until channel #18 is captured is 32.000 μs.

An application's engineer needs to know the timing relationships for data acquired from channels #12, #6, and #23, in that order. Reference figure 6-2 for channel #12. The elapsed time from channel #12 until channel #6 is acquired is 14.625 μs while the time from channel #12 until #23 is captured is 29.125 μs. Reference Figure 6-3 and find the column for channel #6. The time that elapses between the sampling of channel #6 and then channel #23 is 14.500 μs. This confirms the above matrix readings above (14.625 μs + 14.5000 μs = 29.125 μs). The time that elapses between the sampling of channel #6 until that of channel #12 (of the next frame) is found to be 55.375 μs. The delta times for channel #12 and #6, referenced to channel #23, are found to be 40.875 μs and 55.500 μs, respectively. Note that the dependent channels actually occur in the next frame with respect to the reference channel #23.

6.3 Supercommutation

The end of section 2.5.3 discussed briefly the concept of supercommutating channels to increase the sampling rate for higher bandwidth input signals. The three figures presented in this section, so far, make it easier to enable even distribution of samplings for a single input by spreading the number of samples out over the full frame in such a manner as to provide approximately equal delta times for the sampling process.

For instance, if a channel needs to be sampled at a rate of ≈110 Ksamples/second, then it is necessary to actually drive the input signal into eight, evenly distributed channels. A full frame time of 70 μs divided by eight yields a sample per 8.75 μs for an aggregate sampling rate of 114,286 samples/second. This can be accomplished by applying the same input signal to all eight channels of any single analog subsection; channels 1 → 8, or channels 9 → 16, or channels 17 → 24.

NOTE: The input impedance is the same as though it were a single input channel since only one analog subsection is being used; 50594 Ω for differential mode or non-inverting single-ended mode, or 25297 Ω for inverting single-ended mode with the non-inverting input grounded to AREF.

Table 6-1 presents a table of corresponding input impedances as a function of the type of input and the number of analog subsystems being used. An analog subsystem is defined as channels sharing analog circuitry, and are grouped as channels 1 → 8, 9 → 16, and 17 → 24.

Table 6-1 Input Impedances by Type & Groupings

Impedance(Ω)	Number of Groups	Type of input
50594	1	Differential & Noninverting single
25297	2	Differential & Noninverting single
16865	3	Differential & Noninverting single
25297	1	Inverting single-ended
12649	2	Inverting single-ended
8432	3	Inverting single-ended

Table 6-2 presents a cross tabulation of the number of channels supercommutated, with their corresponding "ideal" delta times for evenly distributed samplings, and their resultant aggregate sampling rates. If the minimum sampling rate is known based upon the bandwidth of the input signal, then the number of input channels needed can be found along with the preferred sampling time spacing. Use Figures 6-2 and 6-3 to assist in the distribution of the input across channel numbers. Also be alert to the decrease in input impedance as the signal is distributed across channels, as presented in Table 6-1, above.

Table 6-2 supercommutation rates/times

Number of inputs:	≈ Time between samples(μs):	≈ Aggregate sampling Rate(s/s):
1	70.000	14286
2	35.000	28571
3	23.333	42857
4	17.500	57143
5	14.000	71429
6	11.667	85714
7	10.000	100000
8	8.750	114286
9	7.778	128571
10	7.000	142857
11	6.364	157143
12	5.833	171429
13	5.385	185714
14	5.000	200000
15	4.667	214286
16	4.375	228571
17	4.118	242857
18	3.889	257143
19	3.684	271429
20	3.500	285714
21	3.333	300000
22	3.182	314286
23	3.043	328571
24	2.917	342857

Note: The 2.917 μs approximate delta time between samples for the last entry is really an average of three actual timings of 2.875 μs, 2.875 μs, and 3.000 μs.

6.4 Differencing Inputs

Perhaps the most significant technical advantage of the ADM1224F is its ability to handle differential-ended inputs. The most common purpose for this feature is that of removing common-mode signals for noise reduction purposes. There are often applications where the difference between two analog signals contains significant information. Often these applications involve comparisons between setpoints and feedback signals, like those that are encountered in servo systems, and status alarm systems.

The following table was generated by the external connection of eight channels of analog outputs from a DAC128F5 driving the differential-ended inputs of the first four channels of an ADM1224F. DAC128F5 #144 was installed on slot B of a MVME162-01, ADM1224F#100 was installed on slot A, and two 3′ ribbon cables were connected

together with a special "ATE" board. Channel #1 of the DAC128F5 was connected to the noninverting input to channel #1 of the ADM1224F (pin #2), and channel #2 of the DAC128F5 was connected to the inverting input to channel #1 of the ADM1224F (pin #1). The DAC128F5 voltages cited in the table were measured at the ATE board, while the voltages cited for the ADM1224F were calculated from the difference of the input voltages. The data tabulated is that captured by the manual control screen of the ATE software. Table 6-3 is a small subset of the data collected to present a sampling of typical acquired data results for this kind of operation of the ADM1224F.

Table 6-3 Differencing Results

Noninverting Voltage:	Inverting Voltage:	ADM1224F's Acquisition Results: DATA(*hex*):	≡Volts:
+4.99	-4.98	7E7	+9.98
+2.500	-4.98	5EB	+7.49
-0.018	-4.98	3F7	+5.01
-2.492	-4.98	1F7	+2.495
+4.99	+4.99	FFF	0.000
-4.98	-4.98	FFF	0.000
-4.98	-2.491	E07	-2.496
-4.98	+0.004	C0B	-4.99
-4.98	+2.500	A13	-7.48
-4.99	+4.99	81A	-9.98

6.5 DAC Monitors

For those systems that require built-in self-testing capability, the ADM1224F is an ideal candidate for providing real-time monitoring of analog outputs in a system. This is true due to the high-density, and ability to configure each input in any of several configurations. The only down-side for this application is when a DAC is providing smaller incremental steps than that which can be detected by the ADM1224F. This will occur, for instance, when a 12-bit DAC has a smaller full-scale range than that of ±10 volts, or when a DAC can provide full ±10 volt outputs but has a higher resolution, like for 14 and 16-bit DACs.

As with any measurement system, probing a signal modifies it, sometimes significantly. The impact of monitoring DACs with the ADM1224F is that it provides a slightly lower load impedance, requiring a little more drive capability from the DACs.

6.6 ENDOFRAME strobe

The Carrier's strobe connection, for the slot on which an ADM1224F resides, provides an output signal that contains significant timing information about the current state of the IPack in its continuous sequencing through all twenty-four channels. Section 2.3.1.1 discussed this briefly. A short, ½-ICLK-cycle-width pulse, ≈62 ns in duration, occurs every time the frame counter is incremented at the end of every 70 µs period defining a full sweep of all twenty-four channels.

ADM1224F #119 was loaded onto slot B of a VME3SC2 carrier. The "A1" probe of an HP DSO-monitored ICLK on the back of the logic connector at pin #2, while the "A2" probe was attached to J5 pin B on the MVE3sC2's strobe connector. Figure 6-4 presents

the resultant DSO snapshot. The ENDOFRAME pulse (lower trace) is ≈62 ns in width, lagging the ICLK low state by ≈9.6 ns, with a repetition rate of one pulse per 70 µs.

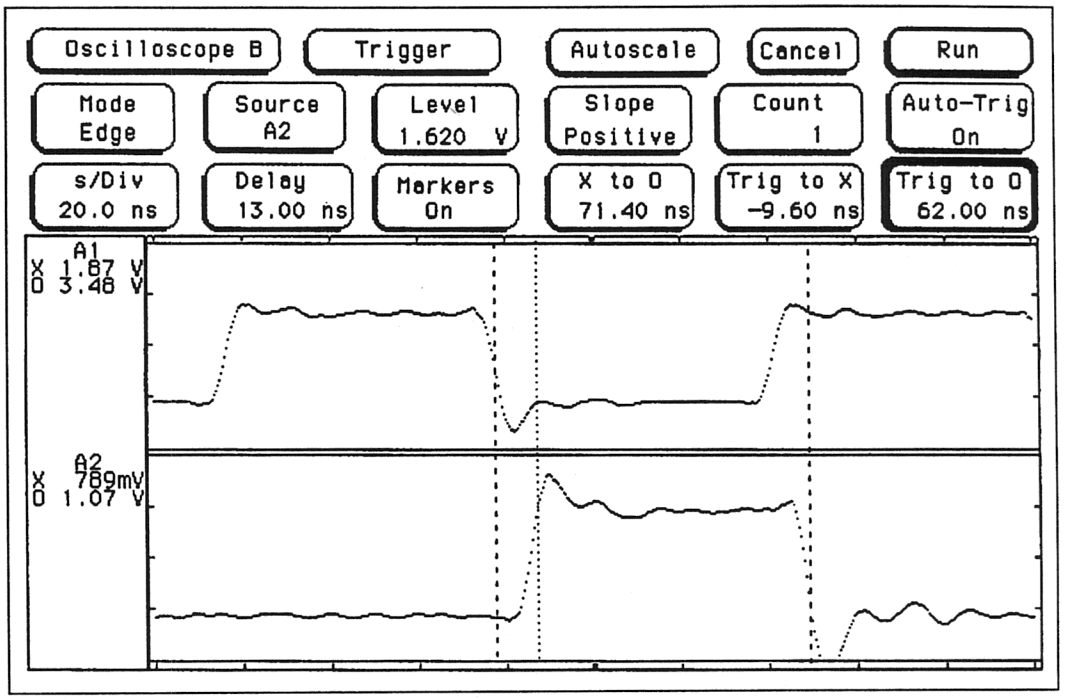


Figure 6-4 ENDOFRAME "strobe" Pulse

This pulse is driven directly, through an 18 Ω series termination resistor, by the ALTERA EPLD with no buffer. Minimize the loading on this strobe connection, especially the capacitive loading.

This pulse is ideal for triggering an interrupt to the system, signalling a processor to execute an Interrupt service Routine to read all of the data from the ADM1224F. Be aware that channel#1's data will be overwritten soon after the ENDOFRAME strobe pulse occurs so that its data should be retrieved early in the ISR.

Connecting this strobe signal to a DIO316I is the preferred way of generating an interrupt. It is recommended that the DID48 not be used for this purpose since the DID48 will probably interpret this 62 ns pulse as nothing more than noise, and ignore it as a valid input.

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.1.1 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.1.2 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.1.3 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

7.7 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.
- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling **(513) 252-5601**, or by sending an E-mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:
This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general-purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high-speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system-level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:
The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK
This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)
These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)
These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier-driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:

+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:

There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:

There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:

Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:

The outside dimensions of a "singlewide" IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a "doublewide" IP are 3.600″ by 3.900″, +.000/-.020″. There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a "singlewide" IP, and 3.6″ by 3.188″ for a "doublewide" IP. The maximum height of components on the IP is 0.315″, with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:

The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

MEMORY TRANSFERS CYCLE TABLES

CYCLE	MEM WRITE NO HOLDS NO WAITS				MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS							MEM WRITE 1 HOLD 3 WAITS								DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15:0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH @ END OF:			◇					◇			◇											◇					

CYCLE	MEM READ NO HOLDS NO WAITS				MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS					MEM READ 1 HOLD 3 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND:

* IPD[15:0] = IPA[22:7] during during the SELECT cycle, and is used for data for all other cycles.

X — DON'T CARE

Z — HIGH IMPEDANCE

1 — HIGH STATE, +5v

0 — LOW STATE, GND

→ — DRIVEN INTO IPack

← — DRIVEN OUT OF IPack

◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS CYCLE TABLES

CYCLE	ID READ NO HOLDS NO WAITS				ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS						ID READ 2 HOLDS 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7:0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND:

X — DON'T CARE

Z — HIGH IMPEDANCE

1 — HIGH STATE, +5v

0 — LOW STATE, GND

→ — DRIVEN INTO IPack

← — DRIVEN OUT OF IPac

INT TRANSFERS CYCLE TABLES

CYCLE	INT READ NO HOLDS NO WAITS				INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
PD[7:0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS· CYCLE TABLES

CYCLE·	I/O WRITE NO HOLDS NO WAITS				I/O WRITE NO HOLDS 3 WAITS						I/O WRITE 2 HOLDS NO WAITS							I/O WRITE 3 HOLDS 1 WAIT						DRIVEN BY·	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPD[15·0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH @ END OF·			◇						◇			◇										◇					

CYCLE·	I/O READ NO HOLDS NO WAITS				I/O READ NO HOLDS 2 WAITS					I/O READ 3 HOLDS NO WAITS					I/O READ 2 HOLDS 3 WAITS					I/O READ 3 HOLDS 2 WAITS					DRIVEN BY·	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15·0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND·

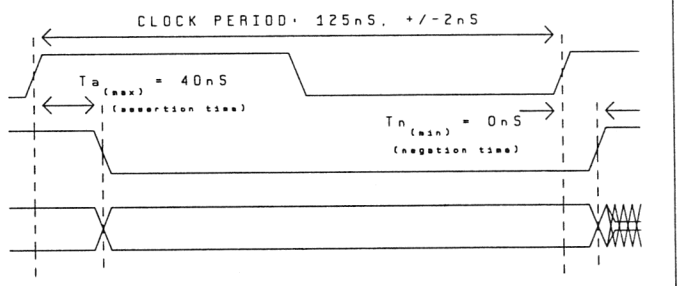
- X DON'T CARE
- Z HIGH IMPEDANCE
- 1 HIGH STATE· +5v
- 0 LOW STATE· GND
- → DRIVEN INTO IPack
- ← DRIVEN OUT OF IPack
- ◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED· IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE·	DOUBLEWIDE								SINGLEWIDE				
SIDE·													
ASSERTED LOW·	N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IOSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IOSEL	N_MEMSEL	N_IOSEL	N_INTSEL	N_IOSEL	VALID TRANSFER(s)·
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY· A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY· B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY· BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O· A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O· B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O· BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT· A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT· B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	ID· A-SIDE ONLY

B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B
SCHEMATICS

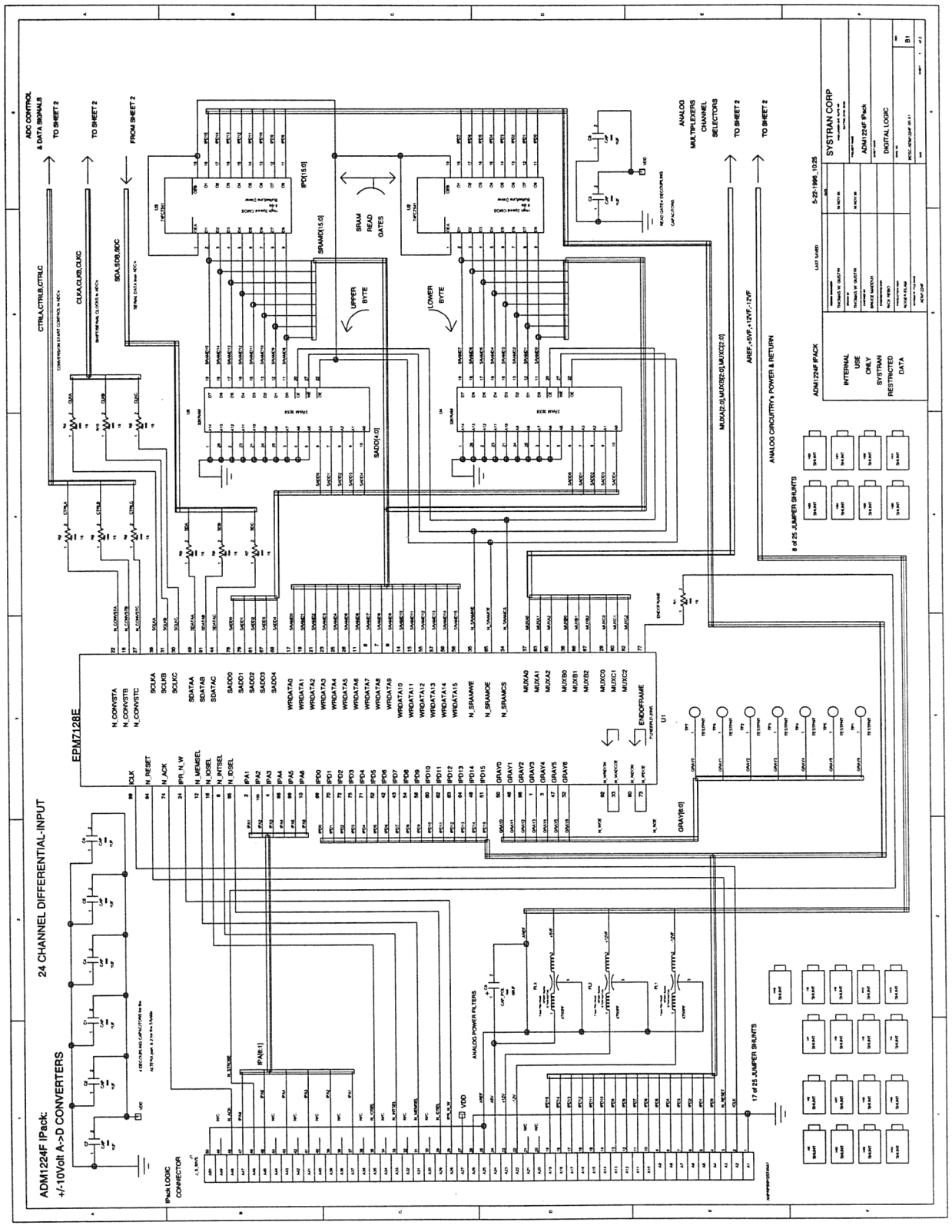


Figure B-1 Schematic #1

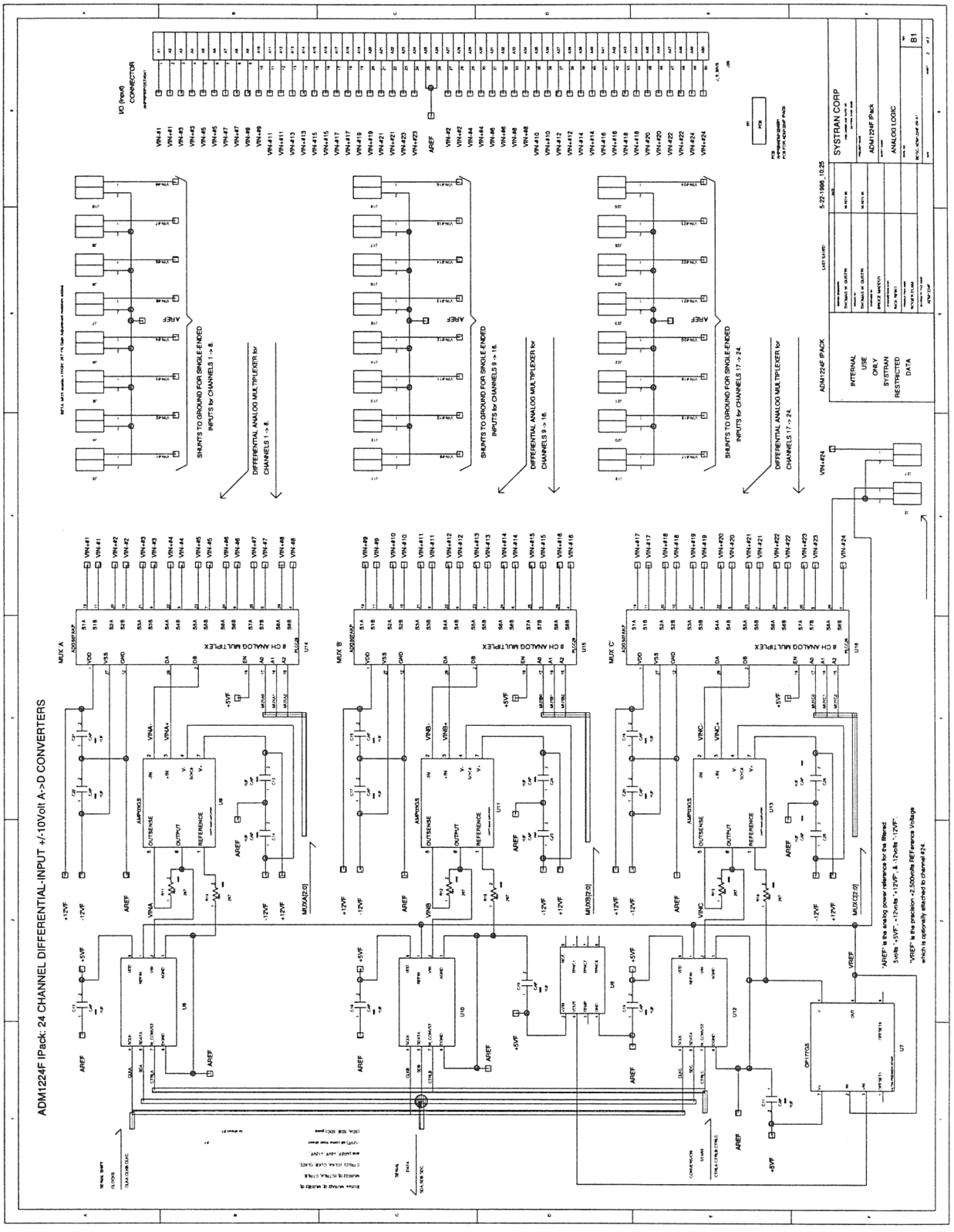


Figure B-2 Schematic #2