DAC128V

8 Channel, 12-bit, 8-range
±V Digital to Analog Board
USER MANUAL

Document No. B-T-MU-DAC128V#-A-0-A2

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane. 8-bits of a data bus on octal boundaries.

CAE. Computer Aided Engineering.

DAC. Digital-to-Analog Converter.

doublewide. An IPack module that is twice the size of the singlewide board.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IndustryPack. Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O. Input/Output.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 8 MB/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6-bit wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IPack module.

IPDbus. IPack Data Bus.

LRU. Line-replaceable units.

MTBF. Mean Time Between Failures.

ns, µs, ms. Nanoseconds, Microseconds, and Milliseconds, respectively.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for Systran's 8-channel, 12-bit, 8-range ±V Digital to Analog Converter (DAC) IndustryPack (also called IPack) board, referred to in this manual as the DAC128V (part number BHAS-DAC128V).

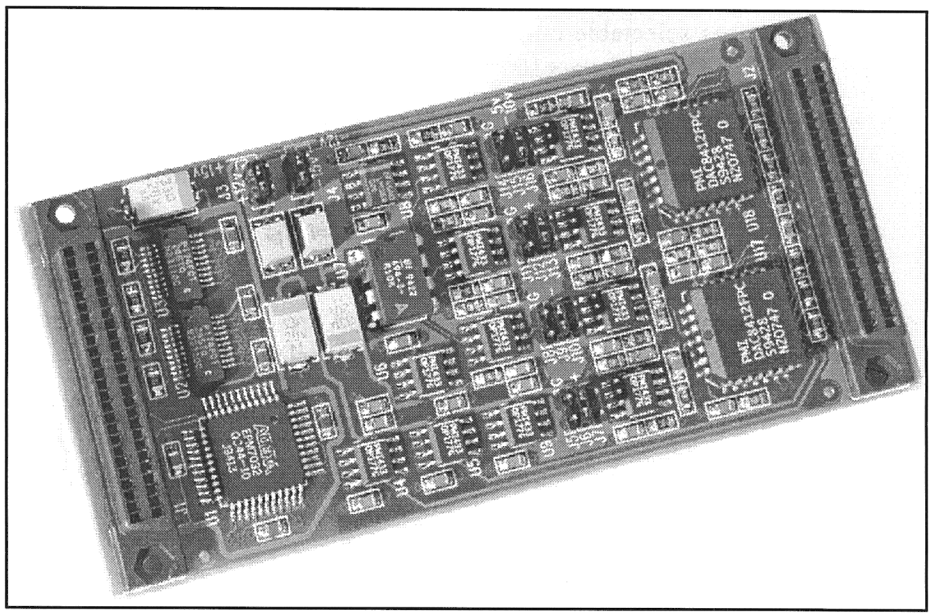

Figure 1-1 DAC128V Board

1.2 Scope

This reference manual covers the physical and operational description of the DAC128V, both from hardware and software perspectives. This manual also contains detailed technical information about the DAC128V's performance characteristics, and some typical applications. It is assumed that the reader has general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The DAC128V is a singlewide IPack board, conforming both mechanically and electrically to the IndustryPack specification, revision 0.7.1. For a typical IPack carrier that holds four IPacks, it can provide up to 32 channels of DACs for a single slot on a

computer bus backplane, or be mixed with other IPacks for a more customized, modular I/O system solution.

The DAC128V is designed to maintain the highest possible accuracy by minimizing the accumulative errors in the design by using the best (yet, reasonably affordable) parts for the tasks to be accomplished.

1.3.1 Features

- Eight independent channels of 12-bit resolution DACs in two groups of four outputs scaled to one of eight possible voltage ranges between ±10 V, with no-wait write and read-back accesses
- Jumper selectable output voltage ranges: 0 ⇒ +5 V, 0 ⇒ +10 V, -5 ⇒ 0 V, -5 ⇒ +5 V, -5 ⇒ +10 V, -10 ⇒ 0 V, -10 ⇒ +5 V, -10 ⇒ +10 V
- Output current is ±20 mA (Max.) for ±10 V output (running on ±15 V power)
- Buffered reference outputs: -10 V, -5 V, +5 V, and +10 V
- Jumper selectable analog power sources: ±12 V from carrier, or ±15 V from I/O connector (recommended for 10 V ranges)
- Integral and differential nonlinearities are ±1 LSB (Max.); settling time is 6 µs (Typical); Slew rate of 2.2 V/µs (Typical)
- $Vout = Vref + \frac{(Vref_{high} - Vref_{low}) * N}{4096}$ (Where N = decimal digital code)

  Straight binary coding; DAC output at Mid-scale on power-up.

1.4 Specifications

MECHANICAL: Singlewide IPack

- Measurements: 1.800″ x 3.900″ x 0.303″ (above board), 4.572 x 9.906 x 0.770 cm
- Weight: 1.056 oz., 29.93 grams
- Board thickness: 0.062″, 0.157 cm, nominally, (4 layer)

PROTOCOL: Singlewide IPack Transfers

- 8 MHz clock rate
- No wait cycles on any transfer types
- Hold cycles supported on all valid transfer types
- Complete (no partial) address decoding
- I/O transfers: 16-bit writes, 16-bit reads
- Eight, 16-bit I/O locations:

- 8 for ports
- Maximum read/write rate: 4 MTransfers/second, sustained

- ID transfers: 8-bit read (only)
  - Zero-fill on upper byte
  - Twelve bytes, including CRC
  - Systran's manufacturer's ID = 45 *hex*, = E *ASCII*
  - DAC128V's model number = 69 *hex*, = i *ASCII*
  - Cyclic Redundancy Check value = E8 *hex*
  - Maximum read rate: 4 MTransfers/second, sustained
- Memory transfers: not supported
- Interrupt Vector transfers: not supported
- Interrupt requests: none generated
- DMA activity: none supported
- No acknowledgement on unsupported transfer attempts:
  - Memory read and write, Interrupt read, ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- All data registers power up at mid-scale (I/O read of '0800' *hex*)
- No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

- Power: +5 Vdc @ 24 mA (typical no load)
  +12 Vdc @ 24 mA (typical no load)
  -12 Vdc @ 22 mA (typical no load)

PERFORMANCE CHARACTERISTICS

- Electrical Characteristics: Refer to Section 5.0 on Performance

ABSOLUTE MAXIMUM RATINGS

- Supply voltage with respect to ground:
  - −0.5 V minimum, +7.0 V maximum for digital
  - ±15.45 V maximum for analog

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RECOMMENDED OPERATING CONDITIONS:

- Supply voltage: +4.75 V → +5.25 V for digital
  - ±11.5 V → ±15.0 V for ±5 V range analog
  - ±12.5 V → ±15.0 V for ±10 V range analog
- Logic Interface: IndustryPack specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

- Temperature (Operating): 0°C to +70°C
- Temperature (no bias, storage): −40°C to +85°C
- Humidity (Non-condensing): 5% to 95%
- Vibration (Operating): 10 G's RMS (10→55 Hz)
- Shock (Operating): 50 G's maximum
- Altitude (Operating): 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

- 2,683,123 hours per MIL-HDBK-217F

1.5 Related Products

- Software: 'C' library and OS-9 device driver routines with documentation.
- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.6 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This Synopsis is included in this document as Appendix A).
- SYSTRAN I/O Products Technical Note #2001 titled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by Greenspring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.7 Ordering Process

To order SYSTRAN products, call (513) 252-5601. For additional product information you may call the above number, or send an E-Mail message to **info@systran.com**.

1.8 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any and all technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help you solve your problem.

Refer to Section 7.0 for warranty and repair information.

1.9 Reliability

SYSTRAN Corporate policy is to provide the highest-quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.

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- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

2.0 DESCRIPTION

NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the "IndustryPack Logic Interface Specification Synopsis" included as Appendix A.

2.1 Block Diagram Description

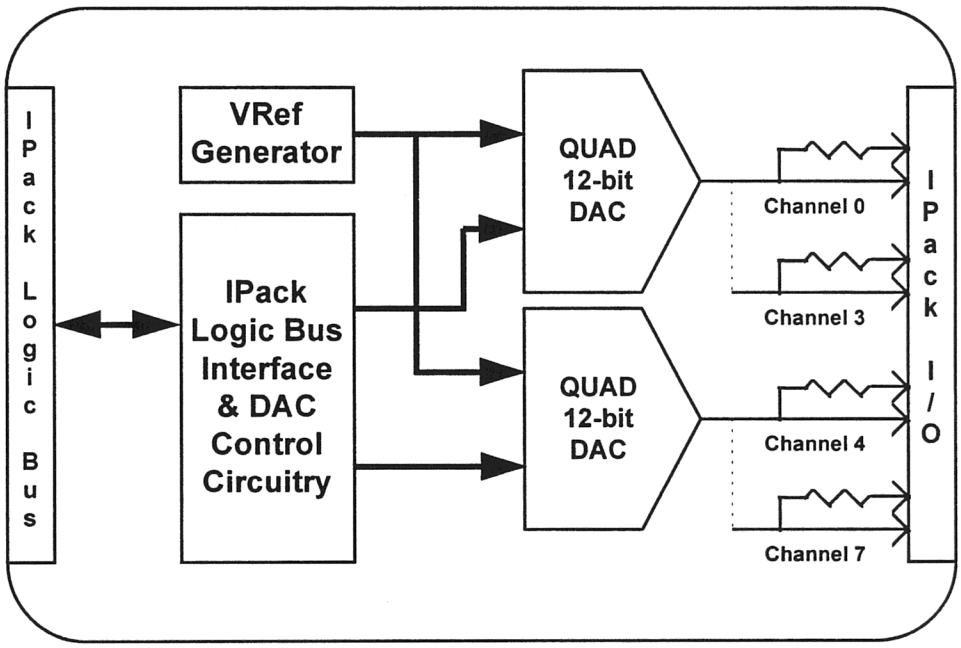

Figure 2-1 DAC128V Simplified Block Diagram.

Figure 2-1 presents a simplified block diagram of the DAC128V. On the left side is the IPack's Logic Bus connector through which all transfers between the IPack carrier and the DAC128V's registers and data sources are conducted. The block labeled "IPack Logic Bus Interface and DAC Control Circuitry" contains the ID "PROM" data, the DACs' access detection and control logic, the IPack transfer sequence/control logic, and the data path gate control signals. All of this circuitry is implemented in one small EPLD. The block labeled "VRef Generator" consists of a precision (+10.000) voltage reference, a quad voltage (±10 volt, ±5 volt) derivation circuit with buffers, two sets of high and low reference voltage selection blocks with buffers (one set per quad DAC), and four reference voltage buffers with connections to the I/O connector (not shown in this block diagram).

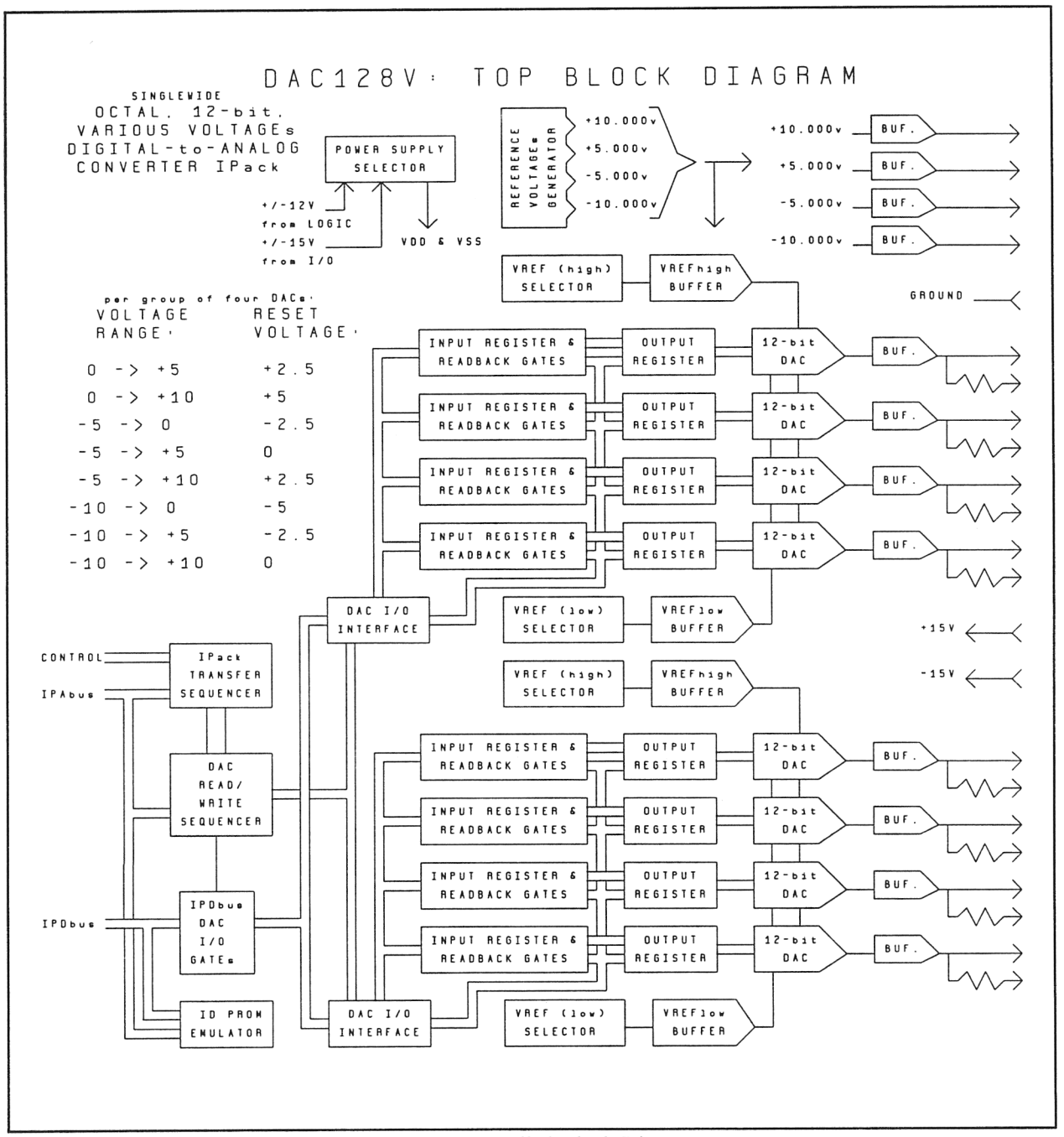

Figure 2-2 Detailed Block Diagram

Each of the elements labeled "QUAD 12-bit DAC" consists of four 12-bit digital-to-analog converters with output voltage buffers, individual high and low reference inputs shared by all four DACs, double-buffered write registers, and read-back gating. As depicted in Figure 2-1, all eight DAC outputs have both direct connections, and series-resistance connections (for applications with highly capacitive loads) to the I/O

connector. On the right side is the DAC128V's I/O connector, providing sixteen DAC analog outputs, four buffered reference outputs, two external power supply inputs, and 28 connections to the ground plane.

Figure 2-2 presents a detailed block diagram of the DAC128V. Again, on the left side is carrier ↔ IPack interface via the IPDbus, the IPAbus, and the access Control signals. The block labeled "IPDbus DAC I/O GATEs" consists of a pair of bi-directional bus transceivers for buffering the writes and quickly terminating read operations.
This second level "top" block diagram provides more detail to better understand the inner functional elements of each of the quad DAC units, including the digital registration and read-back capabilities, the buffered high and low voltage references, and the buffered outputs to the I/O connector. Also provided in more detail (at the top of Figure 2-2) is the ability to run this board using external (clean) power supplies, and the quad-reference voltage generator, with individual buffers for the reference outputs to the I/O connector.

The table on the (upper half) left side of Figure 2-2 provides all of the eight valid voltage ranges that can be selected per quad DAC unit, and their respective (centered) power-up default voltage outputs.

2.2 Detailed Description

NOTE: Refer to the DAC128V schematics located in Appendix B while reading this material since individual components are referred to by functional name, schematic reference designator, or industry-standard device part number.

The DAC128V was developed using VHDL and synthesis, targeted to an ALTERA EPLD, schematic captured and integrated to standard integrated circuits, connectors, and discrete components using VIEWLogic's Viewdraw and associated packages. This top-down design approach is evident in the schematics in appendix B.

2.3 DAC128V Schematics

For those readers not familiar with the top-down design methodology used, the following is a short travel-map through the schematics of the DAC128V. There are four pages that comprise the schematic set.

The first one, labeled BDSC-IDAC128V-69-A1 (sheet 1 of 3) is about one-third of the top level drawing, composed of the IPack Logic connector, the access controller EPLD (labeled S_DA128V), a pair of 74FCT245SC bus transceivers, a symbol for the printed circuit board itself, four pull-down resistors and six de-coupling capacitors for the three digital logic devices depicted on this sheet.

The next sheet (2 of 3) presents (from left → right) four sets of voltage selection (pins and shunt style) jumper blocks for selection of the high and low voltage references for each of the quad DACs, four reference buffer amplifiers, the two quad DACs, the

user's I/O connector interface, eight resistors for series terminated DAC outputs, and thirty-six other discrete components, most of which are used for filtering purposes.

Sheet (3 of 3) presents all of the remaining board level schematic composed of the analog circuitry's voltage source selection and filtering circuitry (top left quarter), the precision voltage reference and quad reference voltage generator with buffers (right side), and four separate buffer amplifiers for providing all four reference voltages to the I/O connector.

If you were to "push-down" into the controller block "S_DA128V" on the first sheet of the schematics, you would then arrive at the fourth sheet of the schematics in appendix B, the netlisted EPLD that controls the operations of the IPack, including the emulation of the ID "PROM". If you were to "push-down" into the EPM7032 symbol on this fourth sheet of the schematics, then the underlying schematic of the controller itself would be revealed.

2.4 Digital Components and their Functions

All IPack Logic Bus transfers take place across J1, the IPack Logic Connector, located on the left side of all block and schematic diagrams. Refer to Appendix A for details about the signals on this connector. Generally speaking, this IPack does not support DMA or Interrupts, and has no memory accesses.

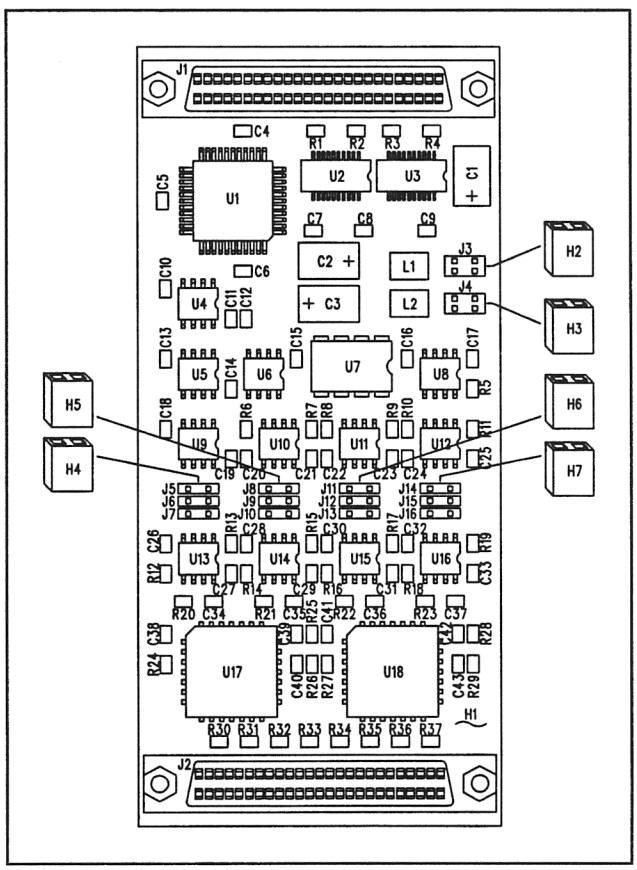

Figure 2-3 DAC128V Physical Assembly

It performs no-wait ID reads, and no-wait reads from and writes to a short, eight location, I/O map. Figure 2-3 presents the physical assembly drawing for the DAC128V. Connector J1 is located at the top of this drawing.

The DAC128V's primary activity controller "S_DA128V" is housed within the EPM7032LC44-10 EPLD located at U1 (just below J1 in figure 2-3, on sheet 1 of the schematics). It serves as the IPack transfer engine, whose responsibilities include:

- Detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier.
- ID PROM emulation data pattern generation for ID read transfers.
- DAC chip select and read/write control signal generation for I/O reads and (16-bit only) writes where QDAC#1 at U17 is enabled for the first four I/O locations and QDAC#2 at U18 is enabled for the last four I/O locations.
- Direction with output enable control signals for the data bus coupling (IPDbus ↔ DACDbus) transceivers.

The data bus transceivers are implemented using a pair of 74FCT245SC devices, and are designated U2 and U3 (just below J1 to the right of U1 in Figure 2-3, on sheet 1 of the schematics). Normally an IPack does not require data bus transceivers. However, since the DACs' specified time for release of the data bus during read operations (low impedance → high impedance state change time) exceeds the maximum time allowed by the IndustryPack specification, these transceivers are employed to quickly decouple the data buses.

2.5 DAC's Voltage Ranges

The following description provides the user with the information necessary to properly set the voltage output ranges for the DACs on the DAC128V. In general, there are three high-side reference voltage levels and three low-side reference voltage levels per group of four DAC outputs. There is one combination that is not logical for normal operations, and this is the default shipment state of the DAC128V.

CAUTION: The DACs will not provide a valid output if both high and low references are set to ground; the voltage outputs remain at 0.000 V (±1.0 mV) regardless of the binary code written to their respective registers.

This "shipped-state" configuration requires the user carefully ascertain and set the output voltage ranges prior to using the DAC128V. The intent in shipping the DAC128V in this benign state is to attempt to minimize the potential impact on the user's external circuitry to which the DAC128V is attached if it is simply installed upon arrival without properly configuring the voltage range selections. The assembly drawing presented in Figure 2-3 and the second sheet of the schematics should be referenced for the following four topic areas.

2.5.1 High Reference For QDAC#1

The high-side reference for the first four DAC outputs generated by QDAC#1 at U17 is selected by placing the jumper shunt designated as H4 onto one pair of three jumper pads designated as J5 (ground or 0.000 volts), J6 (+5.000 volts), or J7 (+10.000 volts). The selection is buffered by the Operational Amplifier at U13 (called "VREFH1" on the schematics) which, in turn, provides the high-side reference voltage for QDAC#1. Using J6 or J7 is valid for any configuration. Use of J5 should occur if, and only if, J8 is not used for the low reference for QDAC#1 (see 2.5.2 below).

2.5.2 Low Reference For QDAC#1

The low-side reference for the first four DAC outputs generated by QDAC#1 at U17 is selected by placing the jumper shunt designated as H5 onto one pair of the three jumper pads designated as J8 (ground or 0.000volts), J9 (−5.000 volts), or J10 (−10.000 volts). The selection is buffered by the Operational Amplifier at U14 (called "VREFL1" on the schematics) which, in turn, provides the low-side reference voltage for QDAC#1. Using J9 or J10 is valid for any configuration. Use of J8 should occur if, and only if, J5 is not used for the high reference for QDAC#1 (see 2.5.1 above).

2.5.3 High Reference For QDAC#2

The high-side reference for the last four DAC outputs generated by QDAC#2 at U18 is selected by placing the jumper shunt designated as H6 onto one pair of three jumper pads designated as J11 (ground or 0.000 volts), J12 (+5.000 volts), or J13 (+10.000 volts). The selection is buffered by the Operational Amplifier at U15 (called "VREFH2" on the schematics) which, in turn, provides the high-side reference voltage for QDAC#2. Using J12 or J13 is valid for any configuration. Use of J11 should occur if, and only if, J14 is not used for the low reference for QDAC#2 (see 2.5.4, below).

2.5.4 Low Reference For QDAC#2

The low-side reference for the last four DAC outputs generated by QDAC#2 at U18 is selected by placing the jumper shunt designated as H7 onto one pair of the three jumper pads designated as J14 (ground or 0.000 volts), J15 (−5.000 volts), or J16 (−10.000 volts). The selection is buffered by the Operational Amplifier at U16 (called "VREFL2" on the schematics) which, in turn, provides the low-side reference voltage for QDAC#2. Using J15 or J16 is valid for any configuration. Use of J14 should occur if, and only if, J11 is not used for the high reference for QDAC#2 (see 2.5.3, above).

2.6 Reference Voltage Generation

The right half of the third sheet of the schematics presents the primary circuitry involved with the generation of the various reference voltages used by the voltage range selectors discussed in paragraph 2.5.

The principle voltage reference is the LM369DM device at U8, and is based upon a buried zener reference technology. Its nominal output voltage is +10.000 volts, with a

typical error of ±70 ppm or ±700 μvolts. Its temperature coefficient over the product's specified operating range is typically 5 ppm/°C. The multi-reference generator's architecture is such that there is a constant load on this voltage reference, regardless of the demands of the DACs or the user's loads for the reference voltages supplied to the I/O connector. That load is a constant 500 μA. The 0.1 μF capacitor at C16 provides additional noise filtering such that the noise voltage is reduced to a typical value of 4 μVrms for the spectrum of 10 Hz through 10 KHz.

This reference has a relatively low drop-out voltage ceiling which enables proper operation even when running the DAC128V from a carrier-sourced ±12 volt supply. At 25°C, the minimum supply voltage is about 11 volts, with it increasing to about 11.5 volts for the low temperature operations of the DAC128V, and down to about 10.5 volts for the high temperature end. The reference generator's power supply connections are identical to those of the remaining analog circuitry, and are switched to the externally supplied power sources when jumpered to do so (see paragraph 2.7, below).

The resistor divider network located at U7, in conjunction with the three Operational Amplifiers at U10, U11, and U12 derive the remaining three reference voltages (not supplied by U8): +5.000 volts, −5.000 volts, and −10.000 volts. U7 contains four 10 KΩ resistors that have an absolute tolerance (not very important for this application) of ±0.1%, and a ratiometric tolerance of ±0.05% (very important) that track at 5 ppm/°C, in the worst case.

All four reference voltages are buffered by the four Operational Amplifiers at U4, U5, U6, and U9 to provide the user with outputs at the I/O connector for the voltages of +10.00 volts, −5.00 volts, +5.00 volts, and −10.00 volts, respectively.

2.7 External Analog Supply

The DAC128V has provisions for running all of its analog circuitry off of an external power source. There are at least two reasons for taking this action. First, some applications may require "quieter" performance than is possible using the carrier's power sources. These are usually developed using noisier "switcher" technology than the older "linear" techniques.

Second, and more importantly, the external power source provides greater accuracy. While the reference circuitry is capable of running well from the +12 volts provided by a carrier, the DAC128V will not be able to maintain accuracy specifications when using either of the 10 volt rails to drive loads.

The DAC128V is shipped with the analog power selections configured for running from the carrier's ±12 volt supplies. This is implemented by the placement of the shunt H2 at the two-by-two jumper block designated J3, and the shunt H3 at the jumper block J4 at the top (towards the logic connector J1, away from the I/O connector J2) pair of jumper pins. The printed circuit board's silkscreen has these positions labeled as "+12v" and "−12v", respectively.

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To operate the DAC128V from external (±12 →) ±15 volt supplies:

- First ensure that the +15 volts is wired to pin 48 of the I/O connector, and that −15 volts is wired to pin 45 of the I/O connector
- Ensure its power supply ground is well connected to the DAC128V's ground connections at J2
- Then, move jumper H2 to the bottom connections of J3, and move jumper H3 to the bottom connections of J4 (bottom ≡ away from the logic connector J1, towards the I/O connector J2).

These positions are silkscreen labeled on the printed circuit board as "+15v" and "−15v", respectively.

2.8 The Buffers

There are eleven analog buffers used on the DAC128V, located at U4, U5, U6, U9, U10, U11, U12, U13, U14, U15, and U16. They are all configured as unity-gain (non-inverting) voltage followers, all using the ultra-precision Operational Amplifier #OP177GS. This device was selected because it provides performance characteristics that approach those typically only possible with chopper-stabilized amplifiers, without the usual "chopper" problems of noise and spikes, large size with mandatory external storage capacitors, limited common-mode input ranges, and high expense.

The 60 µV maximum input offset voltage (over temperature) is so small that offset voltage reduction circuitry implemented with trim-potentiometers would fail to provide significant accuracy improvements over temperature due to the tracking problems of dissimilar temperature coefficients between the Operational Amplifiers and the potentiometers. Therefore, all buffers are untrimmed, which also increases reliability and reduces costs.

2.9 The DACs

Most of the functional and architectural topics concerning the DACs used have been covered. For the sake of completeness, both DACs are supplied by Analog Devices, #DAC-8412FPC. Note that this technology was obtained from the former company "PMI" and that these two devices, designated as U17 and U18, may be marked as PMI instead of AD or ADI.

The technical specifications in Section 1: INTRODUCTION, and the performance data presented in Section 5 of this document completely cover the remaining text concerning the DACs. Comparison of the specifications published as tables by Analog Devices and to those presented in this document will reveal certain anomalies. The specifications presented in Section I include (beyond those of ADI) empirical data as well as information obtained from characteristic curves, and not just those tabulated by ADI.

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2.10 DAC128V Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol. Do NOT use gasoline or thinner type solvents on this product.

3.0 HARDWARE INSTALLATION

3.1 Unpacking the DAC128V

The contents of the DAC128V shipping package is listed in Table 3-1:

Table 3-1 Contents of DAC128V Shipping Package

QTY	DESCRIPTION
1	DAC128V Printed Circuit Assembly
1	DAC128V User Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-DAC128V).

3.2 Visual Inspection of the DAC128V

Examine the DAC128V to determine if any damage occurred during shipping.

3.3 DAC128V Installation

NOTE: The DAC128V is an Electrostatic Sensitive Device (ESD), the hardware installation of the DAC128V must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the DAC128V can be completed.

The DAC128V installation requires the following tools:

Table 3-2 DAC128V Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

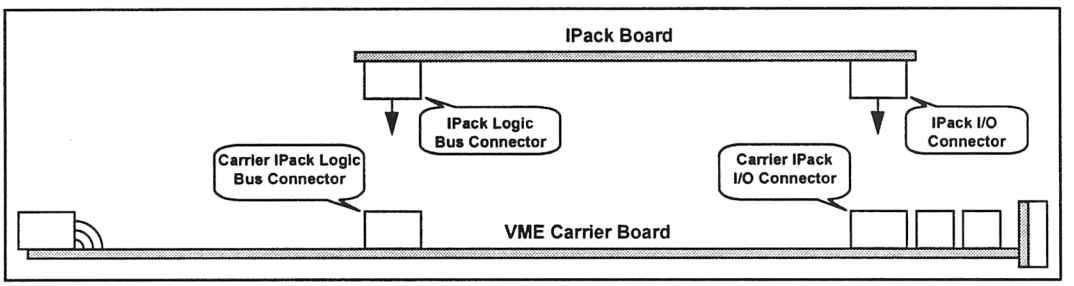

Figure 3-1 Installation of the DAC128V on a VME IPack carrier board.

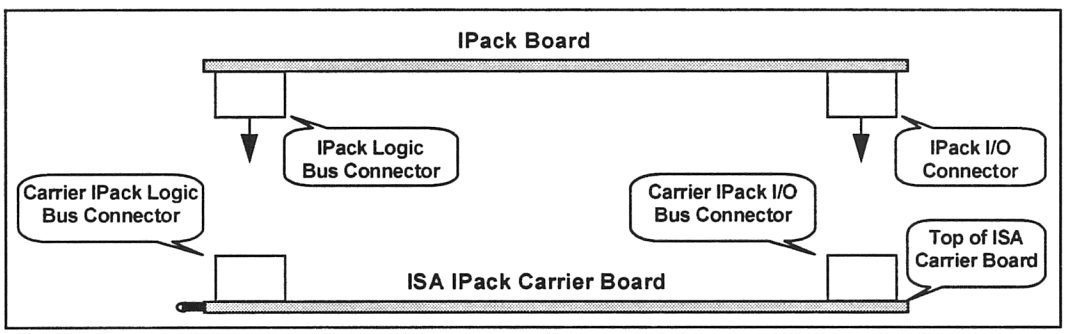

Figure 3-2 Installation of the DAC128V on a ISA IPack carrier board.

Reference Figure 3-1 for the diagram of how the DAC128V is installed on a VME IPack carrier, and Figure 3-2 for installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Referring to the appropriate figures and tables described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the DAC128V can be made.
3. Remove the DAC128V from the shipping package and place it on the ESD bench.
4. Install the DAC128V onto the carrier board by applying adequate and equal pressure to the DAC128V board at both ends.

* 5. Install four M2x5 mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the DAC128V to the carrier board.

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Table 3-3 IPack Logic Bus Pin Assignments

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IPack I/O Connector Pin Assignments

IPack I/O Pin #	Signal Name
50	GND
49	GND
48	+15VIN
47	GND
46	GND
45	-15VIN
44	GND
43	GND
42	-10VOUT
41	GND
40	GND
39	-5VOUT
38	GND
37	GND
36	+5VOUT
35	GND
34	GND
33	+10VOUT
32	GND
31	GND
30	GND
29	GND
28	GND
27	GND
26	GND
25	2DAC08R
24	DAC08
23	GND
22	2DAC07R
21	DAC07
20	GND
19	2DAC06R
18	DAC06
17	GND
16	2DAC05R
15	DAC05
14	GND
13	2DAC04R
12	DAC04
11	GND
10	2DAC03R
9	DAC03
8	GND
7	2DAC02R
6	DAC02
5	GND
4	2DAC01R
3	DAC01
2	GND
1	GND

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4.0 PROGRAMMING GUIDE

This section of the manual describes the operation of the DAC128V from the software perspective, detailing the DAC128V registers and providing programming examples. A more detailed description of the hardware can be found in section 2.0: DESCRIPTION, and in the application examples sections of this manual.

4.1 Description

The DAC128V is a simple to use IPack card with 8 channels of 12-bit digital to analog convertors. The output ranges can be selected via a jumper for each group of four channels. Eight data registers, one per channel, set the output voltage for the channel. On power-up all data registers are set to '0800' *hex* (all channels at mid-range).

4.2 IPack ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information it presents. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" read accesses of this information.

Table 4-1 DAC128V ID Address Space Listing

IPack ADDRESS	DESCRIPTION	DATA READ
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 *hex*
IPA = 02 *hex*	ASCII "A"	41 *hex*
IPA = 03 *hex*	ASCII "C"	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	DAC128V's Model Number	69 *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	E8 *hex*

The ID address space is fully decoded.

NOTE: Any attempt to access IPA addresses at and above IPA = 0C *hex*, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement, and its subsequent bus timeout error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane #0 (IPD[7:0]). The upper byte-lane #1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.
Table 4-1 is the DAC128V emulated ID Address Space PROM listing.

4.3 IPack I/O Address Map

The DAC128V's I/O Address Map is designed with efficiently located data registers in the IPack I/O space (IPA = 00 ⇒ 07 *hex*). The address detector circuitry is fully decoded.

NOTE: Any attempt to access IPA addresses at and above IPA = 08 *hex* will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IPack resides.

The first location (IPA = 00 *hex*) is the write-and-read-back Data Register 0 for the DAC output channel #1. Valid accesses to and from this location include: 16-bit writes, and 16-bit reads. All of the subsequent locations (IPA = 01 ⇒ 07 *hex*) correspond to the DAC channels #1 through #8 respectively (where IPA = 01 is channel #2 - IPA = 07 for channel #8).

Table 4-2 is the DAC128V I/O Address Map and contains the data register:

Table 4-2 DAC128V I/O Address Map

IPack ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 00 *hex*	[XXXX] [11:8]	[7:0]	Data Register 0, Channel 1, 12-bits
IPA = 01 *hex*	[XXXX] [11:8]	[7:0]	Data Register 1, Channel 2, 12-bits
IPA = 02 *hex*	[XXXX] [11:8]	[7:0]	Data Register 2, Channel 3, 12-bits
IPA = 03 *hex*	[XXXX] [11:8]	[7:0]	Data Register 3, Channel 4, 12-bits
IPA = 04 *hex*	[XXXX] [11:8]	[7:0]	Data Register 4, Channel 5, 12-bits
IPA = 05 *hex*	[XXXX] [11:8]	[7:0]	Data Register 5, Channel 6, 12-bits
IPA = 06 *hex*	[XXXX] [11:8]	[7:0]	Data Register 6, Channel 7, 12-bits
IPA = 07 *hex*	[XXXX] [11:8]	[7:0]	Data Register 7, Channel 8, 12-bits

4.4 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NUBUS ADDRESS	IPack ADDRESS
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 1A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*

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4.5 Byte Access Address Translation

Table 4-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS	BYTE-LANE*
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1

* Byte-lane 1 not applicable for ID Space

4.6 Data Registers 0-7 Bit Description (IPA = 00 ⇒ 07 *hex*)

The DAC128V has eight 16-bit wide registers, each corresponding to a DAC channel. The DAC128V supports word (16-bit) reads and writes. The upper 4 bits are discarded during writes and are read back as zeros. The eight 16-bit read/write data registers are used to set the output voltage of the eight DAC channels. Data register 0 corresponds to DAC channel 1, register 1 to channel 2, ... register 7 to channel 8. On power-up all data registers are set to '0800' *hex* (all channels at mid-range).

Table 4-5 Data Registers Bit Descriptions

Bit #	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	Not used	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	Read as 0's, Writes discarded.	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up state	N/A	1	0	0	0	0	0	0	0	0	0	0	0

D11 - D0 : These bits comprise the 12-bit DAC value.

4.7 Programming Example

The following example illustrates how to program the DAC128V device. The power up state is that all of the channels are set to their mid range. This example assumes that the output range is set to -5 V to +5 V. This example only interacts with channel 1, however, all of the channels work the same way.

- At power-up all the data registers values are '0800' *hex* corresponding to 0 volts.
- Write '0000' *hex* to data register 0, DAC channel 1's data register.
- The DAC channel 1 voltage output should now be -5.0 volts.
- Write '0FFF' *hex* to data register 0.
- The DAC channel 1 voltage output should now be +5.0 volts.
- Write '0800' *hex* to data register 0.
- The DAC channel 1 voltage output should now be 0.0 volts.

5.0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in section 1.0: INTRODUCTION. Where possible, data is tabulated with only one response time (actual) performance figure presented in order to minimize the length of the presentation.

5.2 Timing measurements

Timing measurements were conducted on the DAC128V using an HP model 16500A Logic Analyzer with a 400 megasamples per second Digitizing Oscilloscope Module, model 16531A, plugged into slot E, and a 1 GHz Timing Master Module, model 16515A in slot C. The DAC128V was installed in the IPack slot 'A' of a Motorola MVME-162-01 VME processor IPack carrier board. Figure 5-1 shows the test configuration for the oscilloscope and state timing measurements.

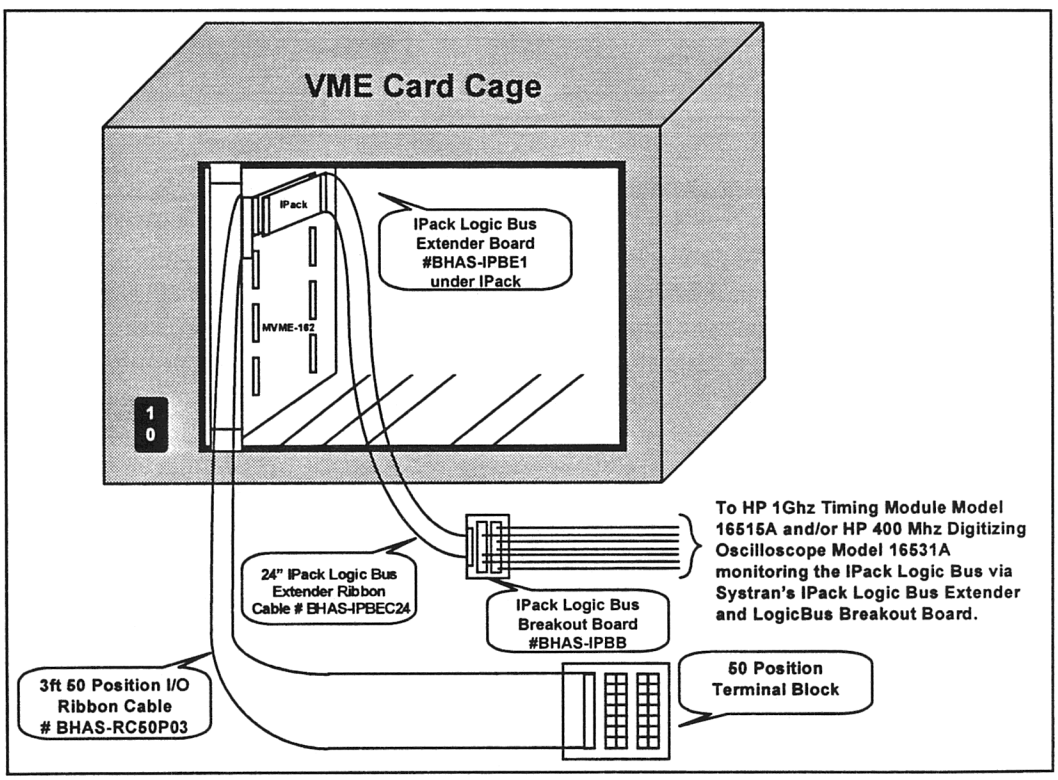

Figure 5-1 IPack Test Configuration for Oscilloscope and State Timing Measurements

5.3 IPack Accesses

There are some parameters that are important when evaluating an IPack's performance on a specific carrier board. These involve the assertion and negation, or driving to logic state versus high impedance states, of signals from the IPack to the carrier, with reference to the rising edge of ICLK. According to specification, these state changes must occur within 40 ns. Figure 5-2 presents just one of the logic state analysis figures captured for the development of the data in Table 5-1. Figure 5-2 depicts an I/O write to the first I/O location (IPA = 00 *hex*) of data whose least significant nibble is zero (IPD[3:0] = 0). The important parameter here is that it typically takes 10 ns to negate N_ACK.

Table 5-1 IPack Typical Access Time

FUNCTION/OPERATION	↓ ICLK UNTIL	TIME
I/O READ @ IPA = 00	↓ N_ACK	10 ns
I/O READ @ IPA = 00	↓ N_ACK	11 ns
I/O READ @ IPA = 00	IPDbus' HIGH to LOW Impedance	22 ns
I/O WRITE @ IPA = 00	↓ N_ACK	09 ns
I/O WRITE @ IPA = 00	↓ N_ACK	10 ns
ID READ @ IPA = 00	IPDbus' HIGH to LOW Impedance	06 ns
ID READ @ IPA = 00	↓ N_ACK	10 ns
ID READ @ IPA = 00	↓ N_ACK	11 ns

There is one additional note to add concerning DAC128V IPack operations. Normally, an IPack does not drive the IPDbus to a low impedance state until (and during) its assertion of N_ACK during HOLD and termination cycles. To date, this policy has been faithfully followed in the design of all Systran's IPacks. The best practical reason for this is to avoid data bus contention with a carrier or other IPack that is slow to release the IPDbus following a preceding transfer without an idle cycle. The specification requires the release within 40 ns. There is no restriction against an IPack driving the IPDbus during the select cycle.

The DAC's read-back registers have a very long data valid delay time, potentially approaching 160 ns following the assertion of their appropriate chip-select signal. For this reason, the IPDbus is coupled to the DAC's read buffers as soon as possible in the read transfer to provide the maximum amount of time for data line stabilization and carrier data setup time for capturing the data with the rising edge of the ICLK signal at the termination of the transfer. This phenomenon is depicted in Figure 5-3. Figure 5-3 also shows why read gates were installed, as described in Section 2: DESCRIPTION.

5.4 Wrong Supply Impact

It is important to use the provisions of external analog power source when attempting to use any of the eight analog voltage ranges that include either or both +10.0 volt and -10.0 volt outputs. By specification, the supply voltage must be a minimum of 12.5 volts, with 15 volts recommended; especially for heavy loads. When this rule is violated, voltage outputs will not meet specifications.

Table 5-2 presents some data that is typical of the problem that may result. If you are not getting smooth changes in output for even code changes, this could be the reason.

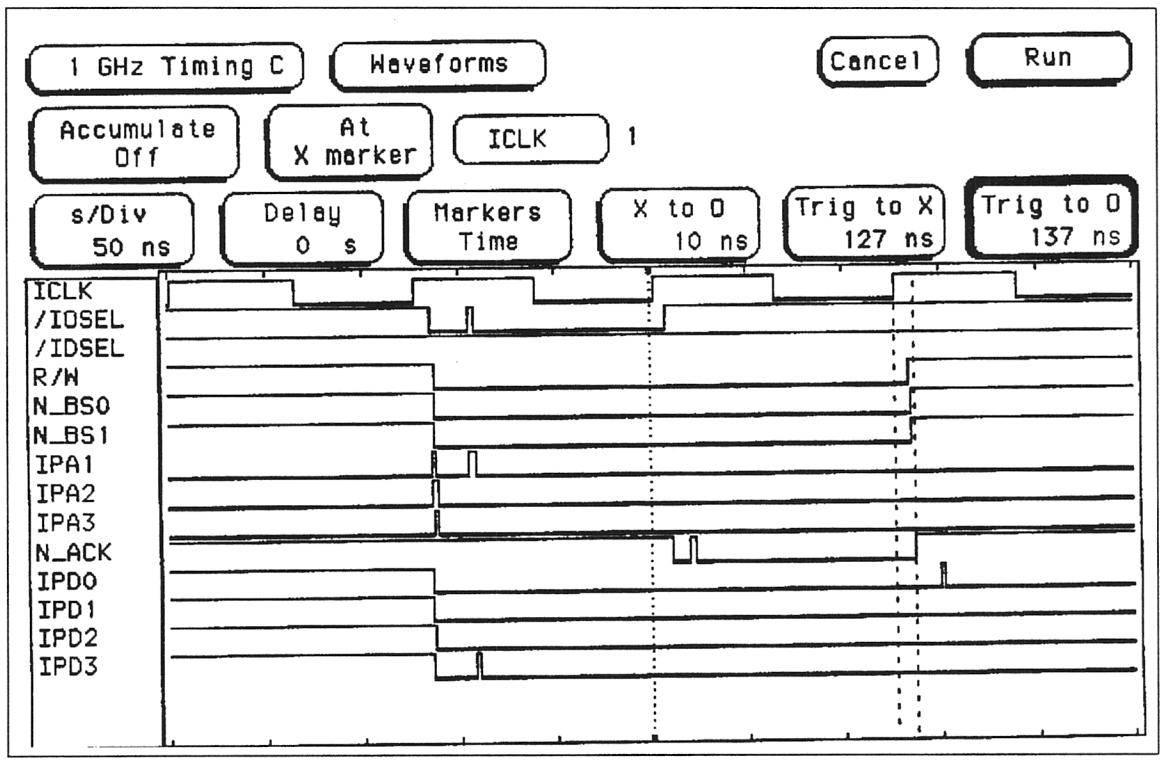

Figure 5-2 I/O Write at IPA = 00

Table 5-2 Wrong Power Supplies

CODE Hex	VOLTAGE OUTPUT (mV)	ΔV (mV)	CODE Hex	VOLTAGE OUTPUT (mV)	ΔV (mV)
800	00.2	6.9	812	43.0	0.3
801	07.1	4.6	813	43.4	0.4
802	11.7	6.1	814	43.6	0.2
803	17.8	2.2	815	44.4	0.8
804	20.0	10.0	816	44.6	0.2
805	30.0	3.1	817	44.9	0.3
806	33.1	3.4	818	45.2	0.3
807	36.5	0.9	819	46.7	1.5
808	37.4	1.8	81A	47.3	0.6
809	39.2	0.5	81B	48.4	1.1
80A	39.7	0.8	81C	49.1	0.7
80B	40.5	0.2	81D	51.0	0.9
80C	40.7	0.8	81E	51.7	0.7
80D	41.5	0.3	81F	52.6	0.9
80E	41.8	0.2	820	158.5	105.9
80F	42.0	0.1	821	166.5	8.0
810	42.1	0.1	822	171.8	5.3
811	42.7	0.6	823	179.0	7.2

NOTE: 4.8828 mV/bit is the theoretical ΔV

Similar mid-scale anomalies were noticed for 0 → +10, 0 → -10, -5 → +10, and +5 → -10 volt ranges. However, quarter scale and full scale codes yielded the expected outputs.

For the 10 volt range example, hex codes of 000, 400. 800, C00, and FFF yielded the expected results: -10.0, -5.00, 0.00, +5.00, and +10.0 volts output, respectively.

NOTE: Use external ±15 volt supplies for any 10 volt range usage.

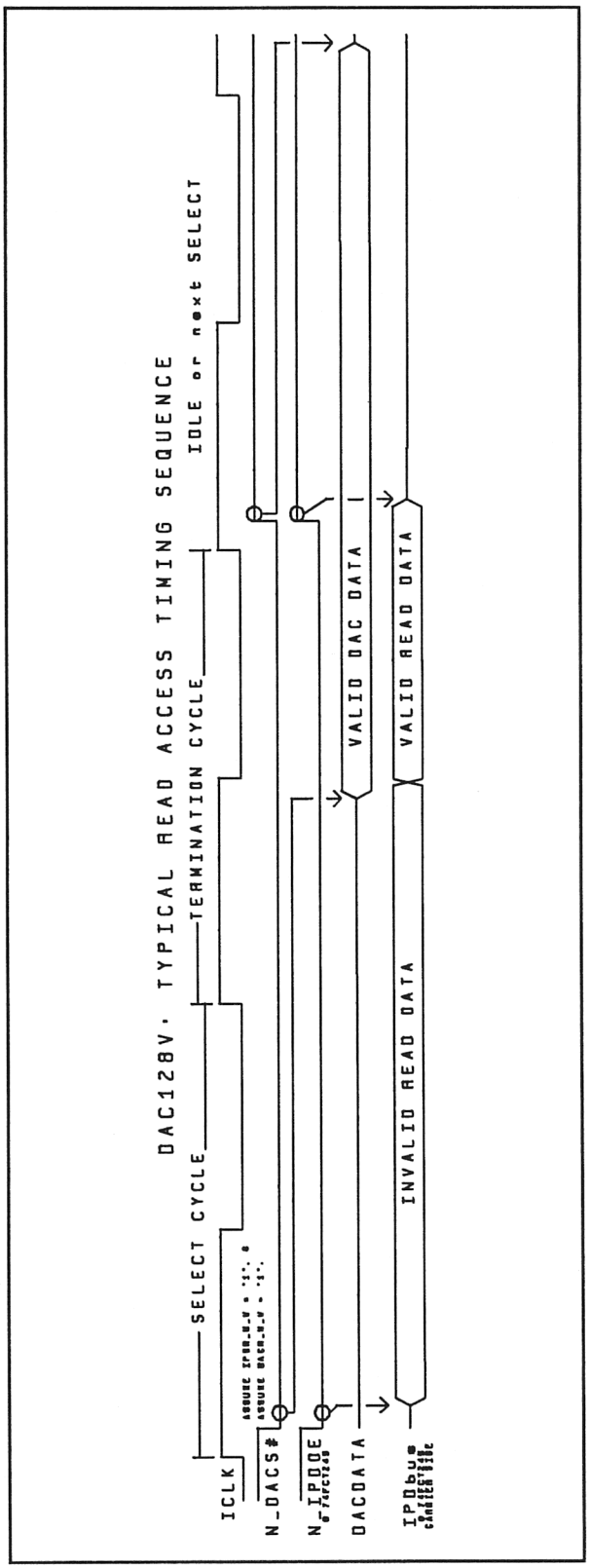

Figure 5-3 Typical Read Access Timing Sequence

5.5 Maximum Loads

The specification sheet for the DACs used on the DAC128V cite that the maximum current output for all analog channels is 5 mA. However, a curve near the end of the data sheet presents information that indicates that the maximum capacity should be slightly over 20 mA per channel. Two separate experiments were conducted to clarify the apparent discrepancy. To be safe, use 5 mA as the typical peak loads, with confidence in knowing that you can get almost 20 mA out if required.

The system configuration used to develop Table 5-3 is the same as that depicted in Figure 5-1. A 200.7 Ω resistor was placed, as a load to DAC01, across pins 2 and 3. DAC02 was left unloaded and was monitored at pin 6 of the I/O termination block. The DACs were run from 15 volt external supplies with their ranges set to 10 volt full scale.

Table 5-3 Fixed Overloads

CODE Hex	DAC02 Vout	DAC01 Vout	DAC01 Iout	COMMENTS
000	-10.00 V	-4.15 V	20.7 mA	Flatlined overcurrent condition
200	-7.50 V	-4.15 V	20.7 mA	
400	-5.00 V	-4.15 V	20.7 mA	
480	-4.37 V	-4.14 V	20.6 mA	
4C0	-4.06 V	-4.05 V	20.2 mA	
500	-3.74 V	-3.73 V	18.6 mA	
600	-2.50 V	-2.494 V	12.4 mA	
700	-1.25 V	-1.247 V	6.2 mA	
FFF	+9.99 V	+4.26 V	21.2 mA	Flatlined overcurrent condition
F00	+8.75 V	+4.25 V	21.2 mA	
E00	+7.50 V	+4.25 V	21.2 mA	
D00	+6.25 V	+4.25 V	21.2 mA	
C00	+5.00 V	+4.25 V	21.2 mA	
B40	+4.06 V	+4.05 V	20.2 mA	
B00	+3.75 V	+3.74 V	18.6 mA	
A00	+2.50 V	+2.493 V	12.4 mA	
900	+1.25 V	+1.246 V	6.2 mA	
880	+0.624 V	+0.623 V	3.1 mA	
800	-0.30 mV	0.00 V	—	

Table 5-3 clearly illustrates that there is a finite power limit for the DACs' buffered outputs and what happens to the voltage output when more current is requested than is deliverable. It does not give a clear picture as to what level of loading will deliver the proper voltage output for given code inputs at maximum, non-overcurrent loading conditions.

Table 5-4 was developed by decreasing the load resistance to that value, lower than which the voltage output begins to droop.

The mean for the last 14 samples is 20.97857 mA with a standard deviation of 0.38946 mA. Note that this last test shows some droop near the positive rail. Therefore the caution: use the DAC128V with loads exceeding 5 mA carefully, after your own capacity testing.

Table 5-4 Maximum Currents

CODE Hex	DAC01 Vout	LOAD RESISTANCE (Ω)	LOAD CURRENT (mA)
FFF	+9.99 V	592	16.9
F00	+8.74 V	456	19.2
E00	+7.49 V	362	20.7
D00	+6.24 V	295.1	21.1
C00	+4.99 V	231.4	21.6
B00	+3.74 V	174.9	21.4
A00	+2.497 V	115.6	21.6
900	+1.247 V	58.3	21.4
800	0.00 V	N/A	N/A
700	-1.245 V	60.4	20.6
600	-2.494 V	121.6	20.5
500	-3.74 V	179.4	20.8
400	-4.98 V	237.1	21.0
300	-6.23 V	300.1	20.8
200	-7.48 V	356	21.0
100	-8.73 V	418	20.9
000	-10.00 V	493	20.3

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5.6 Beyond Temperature

Table 5-5 presents a brief summary of a subset of data taken during product design verification temperature testing on four DAC128V boards loaded onto a Motorola MVME162-01 and put into a temperature chamber.

Table 5-5 Extreme Temperature Performance

I/O PIN	FUNCTION	VOLTAGE @ +25°C	VOLTAGE @ -15°C	VOLTAGE @ +85°C
For DAC128V #104 and DAC's CODE = 000:				
3	DAC01	-4.99	-4.99	-4.99
6	DAC02	-5.00	-4.99	-4.99
9	DAC03	-5.00	-4.99	-5.00
12	DAC04	-4.99	-5.00	-5.00
15	DAC05	-4.99	-4.99	-4.99
18	DAC06	-4.99	-4.99	-4.99
21	DAC07	-4.99	-4.99	-4.99
24	DAC08	-4.99	-4.99	-4.99
33	+10 Vout	+10.00	+10.00	+10.00
36	+5 Vout	+5.00	+5.00	+5.00
39	-5 Vout	-4.99	-4.99	-4.99
42	-10 Vout	-10.00	-10.00	-10.00
For CODE = FFF				
3	DAC01	+4.99	+4.99	+4.99
6	DAC02	+4.99	+4.99	+4.99
9	DAC03	+4.99	+4.99	+4.99
12	DAC04	+4.99	+4.99	+5.00
15	DAC05	+4.99	+4.99	+4.99
18	DAC06	+4.99	+4.99	+4.99
21	DAC07	+4.99	+4.99	+4.99
24	DAC08	+5.00	+5.00	+4.99

For each of five temperature points, 64 DAC voltage output readings and 16 reference voltage outputs were recorded with no load applied. The shortened table is presented to provide the user assurance that the DAC128V can handle wide temperature extremes while maintaining a high degree of accuracy.

Table 5-5 was developed using the carrier's 12 volt supplies and the DACs were set up for 5 volt full scale range operations.

5.7 Slew Time Tests

While the specification sheet indicates that the DAC128V outputs typically settle within 6 µs, and ramp at a rate of 2.2 V/µs, the parameters are not always representative of those that may be encountered in practical applications.

Figure 5-4 presents one of 66 DSO diagrams that were captured for the generation of Table 5-6. The top trace ("D1") is the N_ACK logic signal where the trigger was set up for the falling edge. The bottom trace presents the DAC's voltage output.

NOTE: The plateau that exists where the voltage is passing through 0 volts was found to be typical for many large "step" changes, especially when heavily loaded.

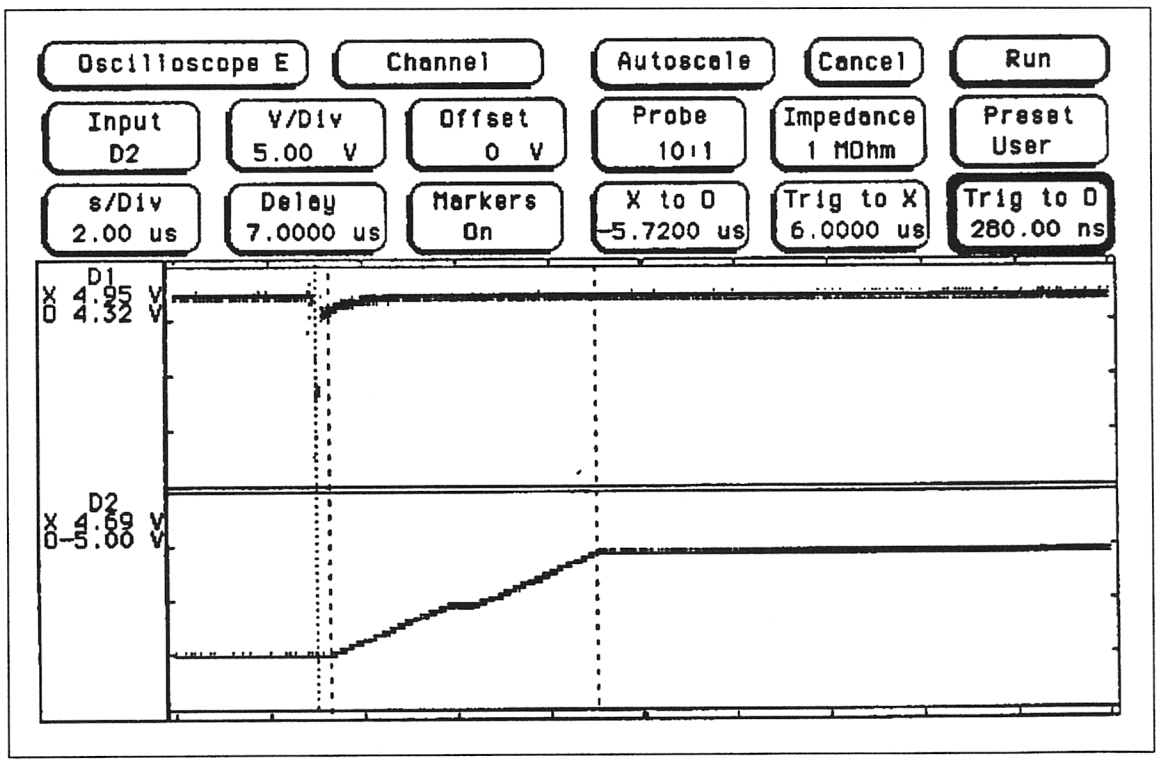

Figure 5-4 Typical Slew Time Waveform

Table 5-6 Slew Time Tests

LOAD:			269 Ω *	677 Ω	5.54 KΩ	NO LOAD
CHANGE	CODE	VOLTAGE	TIME (μs)			
FULL SCALE	000→FFF	-9.99→+9.99	—	11.48	9.96	9.08
	FFF→000	+9.99→-9.99	—	10.24	9.12	9.04
¾ SCALE	000→C00	-9.99→+4.99	—	8.88	7.60	6.92
	C00→000	+4.99→-9.99	—	8.16	7.00	7.08
	400→FFF	-4.99→+9.99	—	8.00	7.60	6.92
	FFF→400	+9.99→-4.99	—	7.32	6.92	6.92
½ SCALE	000→800	-9.99→0.00	—	5.68	5.20	4.68
	800→000	0.00→-9.99	—	5.24	4.72	4.96
	800→FFF	0.00→+9.99	—	5.00	4.72	4.72
	FFF→800	+9.99→000	—	4.68	4.40	4.92
	400→C00	-4.99→+4.99	6.88	5.72	5.28	4.60
	C00→400	+4.99→-4.99	6.00	5.20	4.76	4.88
¼ SCALE	000→400	-9.99→-4.99	—	3.16	2.40	2.36
	400→000	-4.99→-9.99	—	2.72	2.08	2.84
	400→800	-4.99→0.00	3.36	3.84	3.24	2.56
	800→400	0.00→-4.99	4.52	4.04	4.12	4.28
	800→C00	0.00→+4.99	2.64	2.36	2.40	2.24
	C00→800	+4.99→0.00	2.32	2.16	2.24	2.96
	C00→FFF	+4.99→+9.99	—	2.40	2.36	2.36
	FFF→C00	-9.99→+4.99	—	2.04	2.24	2.80

* The 269 Ω load, the codes were limited for ±5 volt outputs maximum to avoid overcurrent conditions; hence the 14 non-applicable table positions with the "—" entries.

For a small change under no-load conditions, code 800 → 820, the corresponding voltage change of 0.00 V → 0.156 V occurred in about 500 ns.

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the DAC128V IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 A Short Glossary Of Analog Signal Applications

The following typical applications were developed by using one or more channels on the DAC128V IPack. Most of the analog output voltage reference configuration operations can be performed (within limits) by proper connections and software manipulations.

NOTE: If the DAC128V is to be used with the voltage range at +10 V and/or -10 V, the user must supply the ±15 V power source to the I/O connector and make the appropriate jumper selections. This is necessary due to the onboard DAC's requiring the reference voltage be at least 2.5 volts below the power source. For example the +10 V range is only 2 volts under the carrier's +12 V source and will cause possible errors in the DACs operation. Therefore an external power source of ± 15 V is required to ensure proper operation.

6.2.1 Avionics Signal Simulations

This application example provides the user with one of many possible configurations for using the DAC128V as an analog output reference. Flight Simulators and Automated-Test-Equipment (ATE) systems require the need for simulation of many analog signals generated from the line-replaceable-units (LRUs) contained in most avionics navigation suites. Most avionics signals are directly proportional to a unit of measure (i.e. nautical miles per hour, feet per second squared, inches of mercury, etc) via an analog voltage representation.

One example would be a barametric altitude signal from an LRU that would be represented by a 12-bit DAC with 10 feet of altitude per bit resolution. This would be represented as 2 raised to the 12th power which equals 4096, for a total of 40,960 feet of absolute altitude. If the DAC128V were configured for 0 to +10 V outputs, the altitudes between 0 and 40,960 feet would equate linearly to the range of 0 to +10 volts (in 0.000244 volt increments).

Another example would be a range or distance-to-go signal that would be represented by a 12-bit DAC with 1 nautical mile per bit resolution. This would be represented as 2 raised to the 12th power which equals to 4096, for a total of 4096 nautical miles of absolute distance. Again with the DAC128V configured for 0 to +10 V outputs the distance between 0 and 4096 nautical miles would equate linearly to 0 to +10 volts (in 0.00244 volt increments). Similarly with the DAC128V configured for 0 to +5 V, a velocity or true-air-speed signal could have a resolution of 0.1 miles-per-hour (mph) per bit (which equals 0.00122 volt increments), yielding 0 to 409.6 mph true-air-speed.

6.2.2 Automatic Test Equipment Applications

The DAC128V can be used as one element of the "Self Test" portion of an ATE system that requires the use of analog-to-digital conversion. The DAC128V can exercise ADCs in the ATE systems for system integrity or confidence tests. Figure 6-1 shows the DAC128V connected to one of Systran's ADCs (BHAS-ADC128F1) in a VME based test system.

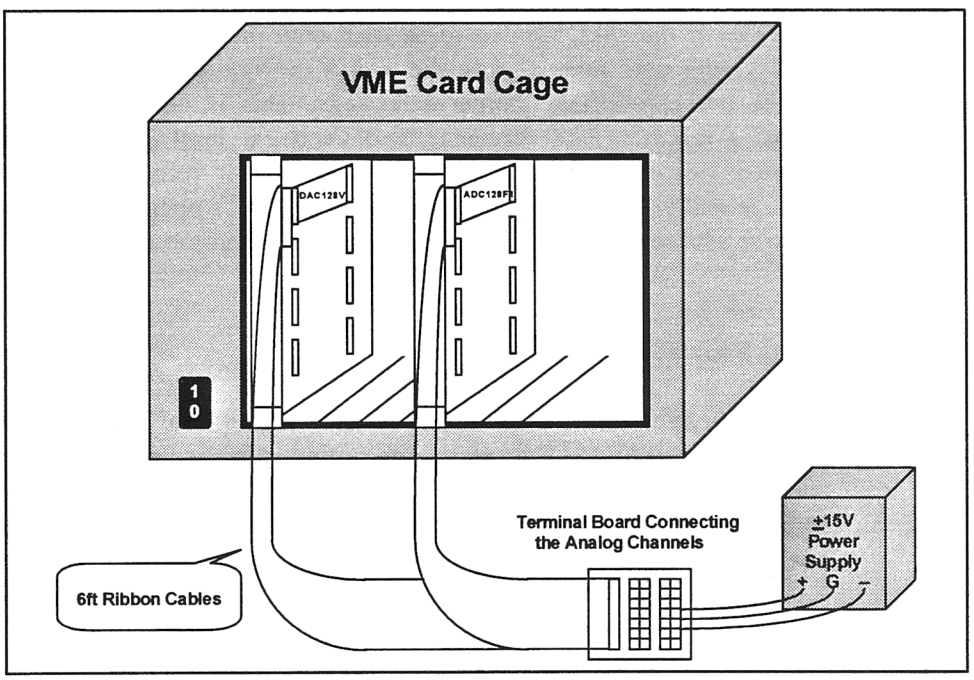

Figure 6-1 DAC128V ATE application.

Figure 6-2 shows the DAC128V connected to the ADC128F1 channel for channel which then can be exercised across its ±10 V input voltage range. An external power supply is required for this application because the +10 V range, are used on the DAC128V.

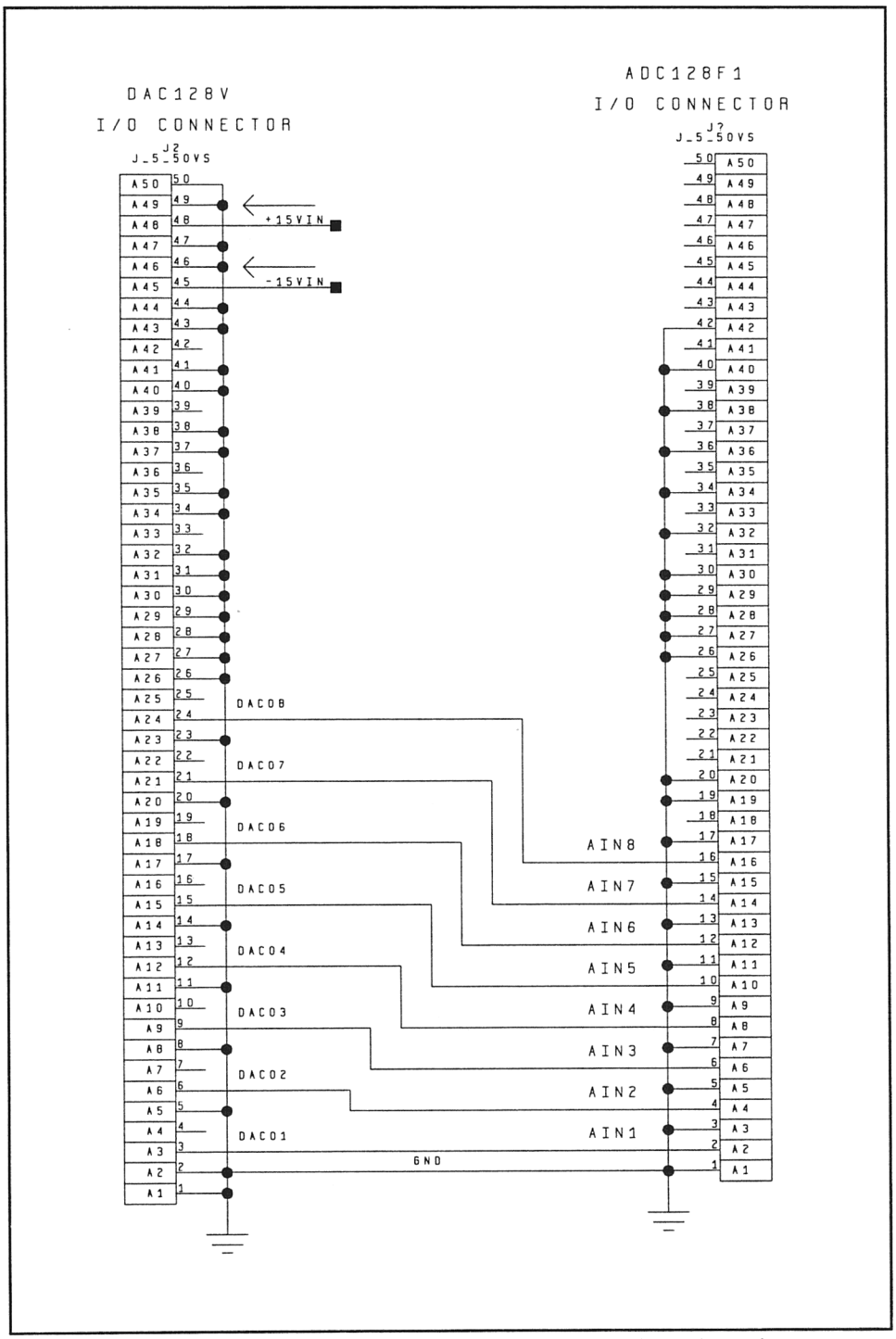

Figure 6-2 DAC128V ATE terminal block connection schematic.

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.1.1 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.1.2 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.1.3 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

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7.7 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.
- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:
This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:
The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK
This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)
These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)
These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "double-wide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:
+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a "singlewide" IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a "doublewide" IP are 3.600″ by 3.900″, +.000/-.020″. There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a "singlewide" IP, and 3.6″ by 3.188″ for a "doublewide" IP. The maximum height of components on the IP is 0.315″, with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

IndustryPack is a registered trademark of GreenSpring Computers, Inc.

MEMORY TRANSFERS: CYCLE TABLES

CYCLE:	MEM WRITE NO HOLDS NO WAITS				MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS								MEM WRITE 1 HOLD 3 WAITS								DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15:0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH * END OF:			◇					◇			◇											◇					

CYCLE:	MEM READ NO HOLDS NO WAITS				MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS					MEM READ 1 HOLD 3 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND:

* IPD[15:0] = IPA[22:7] during during the SELECT cycle, and is used for data for all other cycles.

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE: +5v
- 0 — LOW STATE: GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS: CYCLE TABLES

CYCLE:	ID READ NO HOLDS NO WAITS				ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS						ID READ 2 HOLDS 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7:0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND:

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE: +5v
- 0 — LOW STATE: GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPac

INT TRANSFERS: CYCLE TABLES

CYCLE:	INT READ NO HOLDS NO WAITS				INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
PD[7:0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS - CYCLE TABLES

CYCLE -	I/O WRITE NO HOLDS NO WAITS				I/O WRITE NO HOLDS 3 WAITS						I/O WRITE 2 HOLDS NO WAITS								I/O WRITE 3 HOLDS 1 WAIT						DRIVEN BY - IPack	DRIVEN BY - CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE		
IPA[6-1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPD[15-0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH * END OF -			◇						◇			◇									◇					

CYCLE -	I/O READ NO HOLDS NO WAITS				I/O READ NO HOLDS 2 WAITS						I/O READ 3 HOLDS NO WAITS						I/O READ 2 HOLDS 3 WAITS								I/O READ 3 HOLDS 2 WAITS								DRIVEN BY - IPack	DRIVEN BY - CARRIER
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE		
IPA[6-1]	X	→	→	X	→	→	→	→	X	X	→	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	→		✓
IPD[15-0]	X	Z	←	X	Z	Z	Z	←	X	X	Z	←	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	X	1	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND -

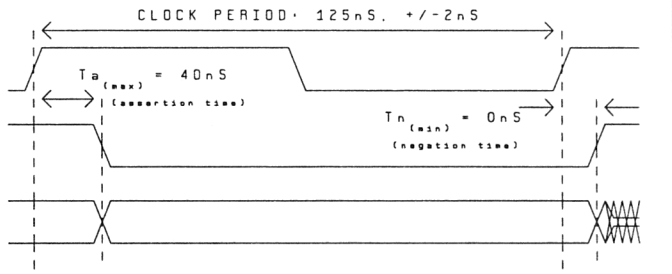
- X DON'T CARE
- Z HIGH IMPEDANCE
- 1 HIGH STATE - +5v
- 0 LOW STATE - GND
- → DRIVEN INTO IPack
- ← DRIVEN OUT OF IPack
- ◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED; IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE -	DOUBLE-WIDE								SINGLE-WIDE				
SIDE -													
ASSERTED LOW -	N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IOSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IOSEL	N_MEMSEL	N_IOSEL	N_INTSEL	N_IOSEL	VALID TRANSFER(s) -
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY - A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY - B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY - BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O - A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O - B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O - BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT - A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT - B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	ID - A-SIDE ONLY

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B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B

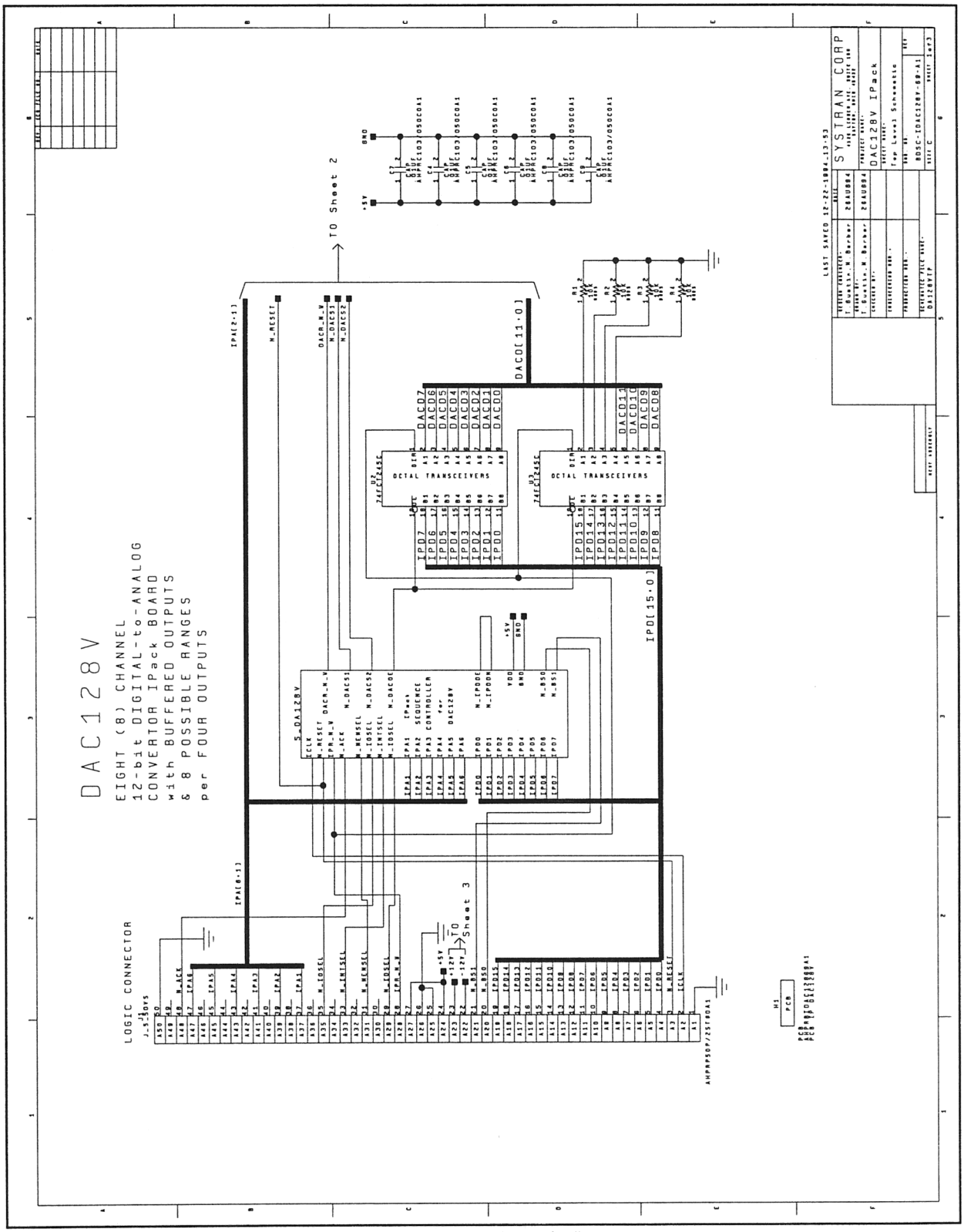

Figure B-1 Schematic #1

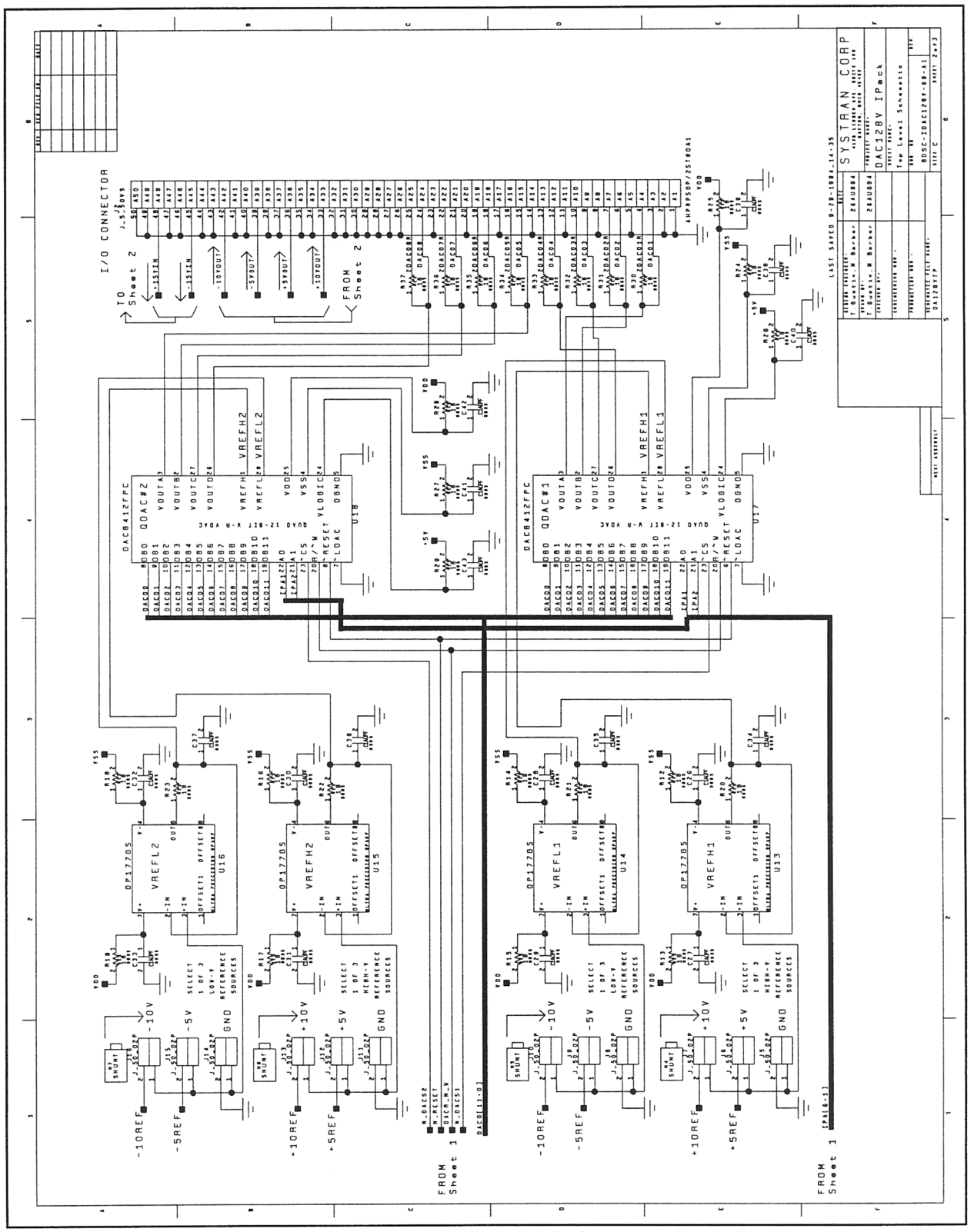

Figure B-2 Schematic #2

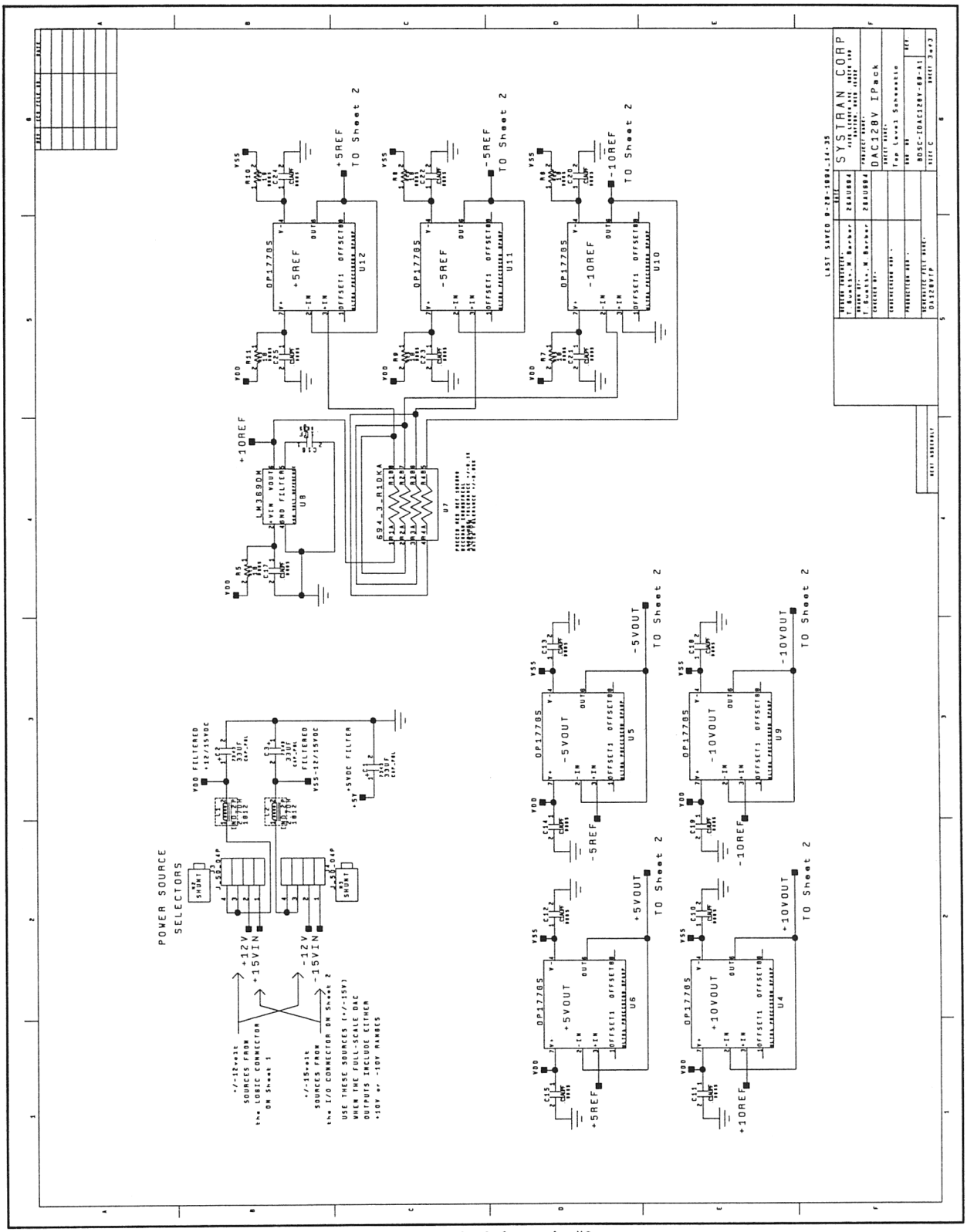

Figure B-3 Schematic #3

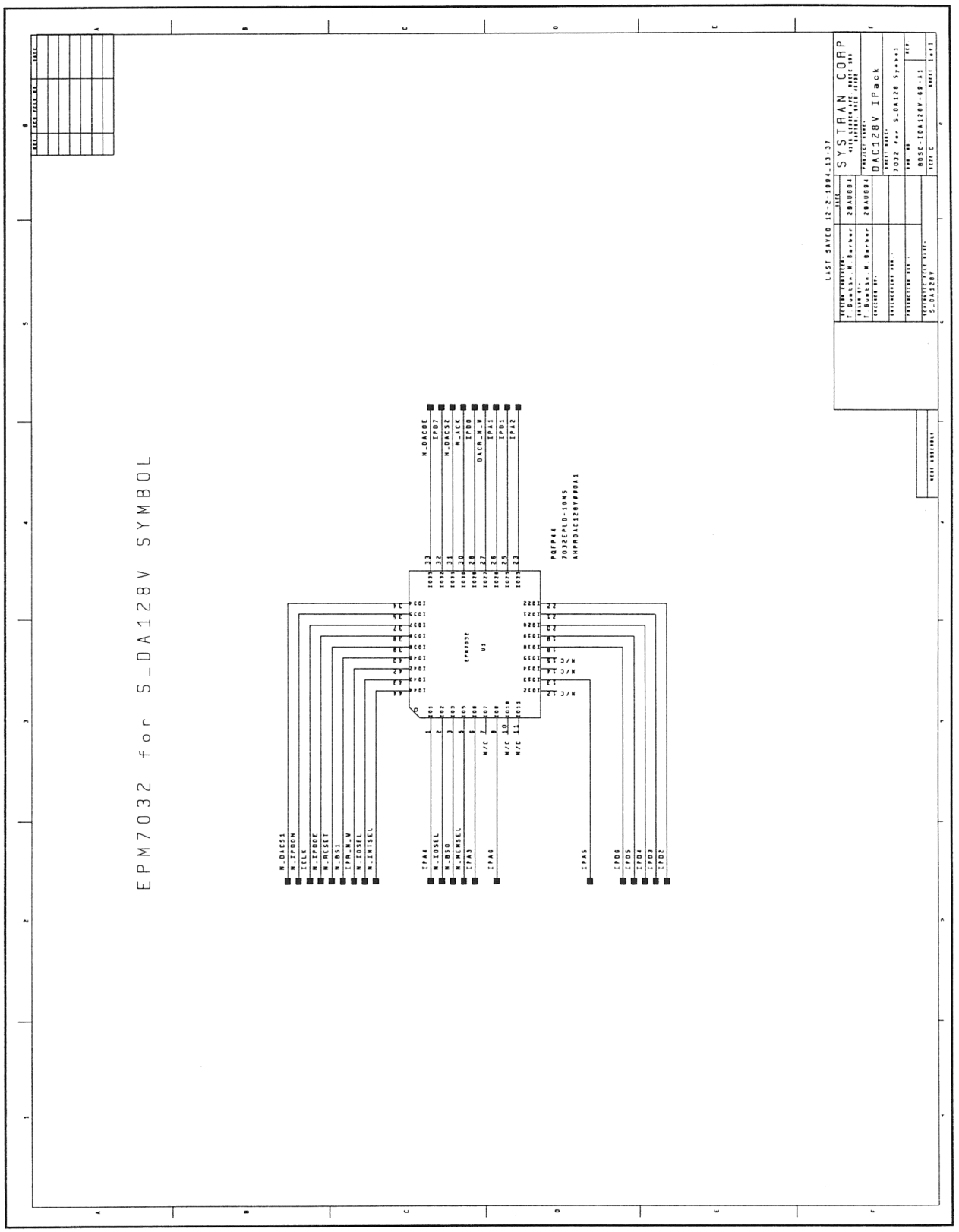

Figure B-4 Schematic #4