DID48

48 Channel Debounced Discrete Input Board User Manual

Document No. B-T-MU-DID48###-A-0-A2

FOREWORD

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane. 8-bits of a data bus on octal boundaries.

doublewide. An IPack module that is twice the size of the singlewide board.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data pattens to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IndustryPack. Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 8 Mbytes/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is a 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4Mwords of memory space per IPack module.

IPDbus. IPack Data Bus.

ISR. Interrupt Service Routine

MTBF. Mean Time Between Failures.

ns, µs, ms Nanoseconds, microseconds, and milliseconds respectively.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for the SYSTRAN Debounced, 48 Channel Discrete Input (DID48) board, part number BHAS-DID48.

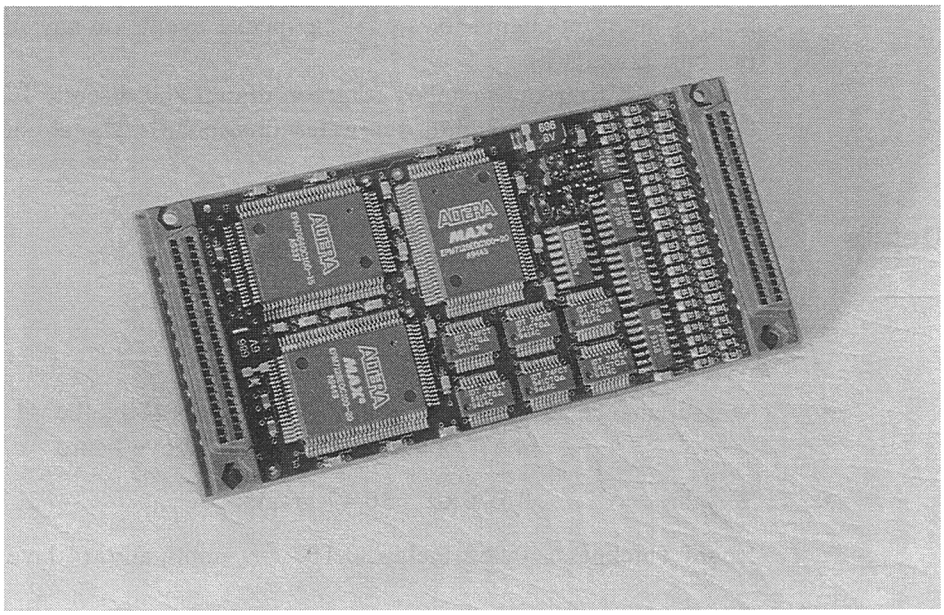


Figure 1-1 DID48 Board

1.2 Scope

This reference manual covers the physical and operational description of the DID48, both from hardware and software perspectives. This manual also contains detailed technical information about the DID48's performance characteristics, and some typical applications. It is assumed that the reader has a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on their carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The SYSTRAN 48 Channel Debounced Discrete Input board implements a general purpose discrete input interface, featuring per-channel overvoltage-protected, bounce/noise elimination circuitry with interrupt-on-change support. The DID48 is a singlewide IPack designed in accordance with the *IndustryPack Logic Interface Specification Revision 0.7.1*.

1.3.1 Features

- 48 channels of hardware debouncing to one of four sampling window time periods: (256 µs, 1.024 ms, 4.096 ms, 16.384 ms).
- Eliminates need for software "debounce" algorithms.
- Software controlled per-byte-lane debounce disabling for direct drive inputs.
- All channels define a logic '1' or 'high' as any input voltage between +2.0 to +32.0 Vdc, and incorporate current-limited high clamps to +5 volts.
- All channels define a logic '0' or 'low' as any input voltage between -32.0 to +0.8 Vdc, and incorporate current-limited low clamps to ground.
- Simple Interrupt engine for signaling special events on any input logic change per-port granularity.
- The DID48's pin-out matches common digital and discrete I/O cards for peripheral compatibility, including screw terminal boards, signal conditioning boards, etc.

1.3.2 Details

MECHANICAL

- Measurements: 1.800 x 3.900 x 0.303 inches above board
  4.572 x 9.906 x 0.770 cm above board
- Weight: 1.076 oz 30.49 grams
- Board Thickness: 0.062 inches, 0.157 cm, nominally, (4 layers)

ELECTRICAL

- 8 MHz clock rate.
- No wait cycles on any transfer types.
- Hold cycles supported on all valid transfer types.
- Complete (no partial) address decoding.
- I/O transfers:
  - 8-, and 16-bit writes,
  - 16-bit reads
  - Seven 16-bit locations:
    three for data ports
    one for control
    three for interrrupt control/status
  - Maximum read/write rate: 4 MTransfers/second, sustained

- ID transfers:
  - 8-bit read (only)
  - Zero-fill on upper byte
  - Twelve bytes, including CRC
  - SYSTRAN's manufacturer's ID = **45** *hex*, **E** *ASCII*
  - DID48's model number = **68** *hex*, **h** *ASCII*
  - Cyclic Redundance Check value = **89** *hex*
  - Maximum read rate: 4 MTransfers/second, sustained
- Memory transfers:
  Not Supported.
- Interrupt Vector transfers:
  - 8-bit read (only)
  - Zero-fill on upper byte
  - Maximum read rate: 4 MTransfers/second, sustained
- Interrupt requests:
  - IPack signal **INTREQ0** is driven on programmed event.
  - IPack signal **INTREQ1** is not used.
- DMA activity: None supported.
- No Acknowledgement on unsupported transfer attempts:
  - Memory read and write,
  - ID write, and addresses beyond those needed for valid transfers.

POWER REQUIREMENTS

- Power: +5 Vdc @ 310 mA (typ., no load)
- Electrical Characteristics: Refer to Section 5.0 on Performance

ABSOLUTE MAXIMUM RATINGS

- Supply voltage with respect to ground: -0.5 V min. and +7.0 V max
- I/O port signals' voltage: -32.3 V min. and +32.3 max. (100% duty cycle)

RECOMMENDED OPERATION CONDITIONS

- Supply voltage: +4.75 V to +5.25 V
- I/O port signals' specifications:
  - Input voltage range: -32 V to +32 V
  - Input rise/fall times: No limit, as long as the input signal is continually rising or falling through the logic transition area (0 - 5 V) with less than 200 mV of hysterisis.

ENVIROMENTAL SPECIFICATIONS

- Temperature
  - (Operating): 0 C to +70 C
  - (Storage): -40 C to +85 C
- Humidity (Noncondensing): 5% to 95%
- Vibration (Operating): 10 G's RMS, 20-2000 Hz, random
- Shock (Operating): 50 G's Max.
- Altitude (Operating): 10,000 feet

MEAN TIME BETWEEN FAILURE (MTBF):

- 3,748,126 hours per MIL-HDBK-217F

1.4 Related Products

- Software: 'C' library and OS-9® device driver routines with documentation.
- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.5 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This Synopsis is included in this document as Appendix A)
- SYSTRAN I/O Products Technical Note #2001 titled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by Greenspring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.6 Ordering Process

To order SYSTRAN products, call (513) 252-5601. For additional product information you may call the above number, or send an E-Mail message to **info@systran.com** to place an order.

2.0 DESCRIPTION

NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the *IndustryPack Logic Interface Specification Synopsis* included as Appendix A.

2.1 Block Diagram Description

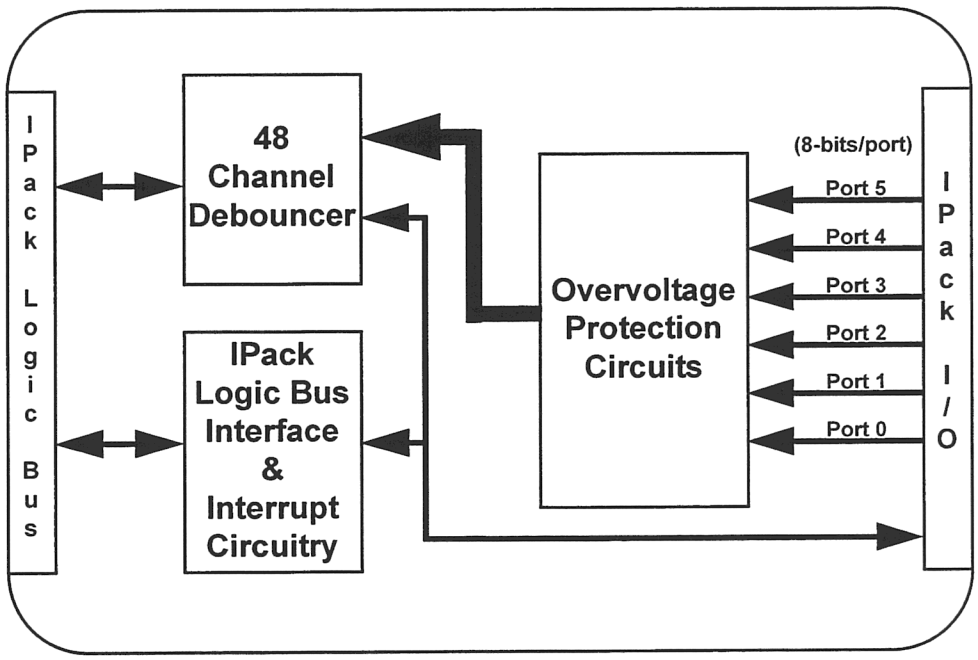


Figure 2-1 DID48 Block Diagram

Figure 2-1 is a simplified block diagram of the DID48 representing the signal flow between the IPack Logic Bus and I/O connectors. On the left side of the diagram is the IPack's Logic Bus connector through which all transfers between the IPack carrier and the DID48's registers and data sources are conducted. The block labeled "IPack Logic Bus Interface and Interrupt Circuitry" contains all of the read data ports, ID "PROM" data, control register, interrupt vector, interrupt control/status registers and interrupt engine, and IPack sequence/control and data bus interface logic.

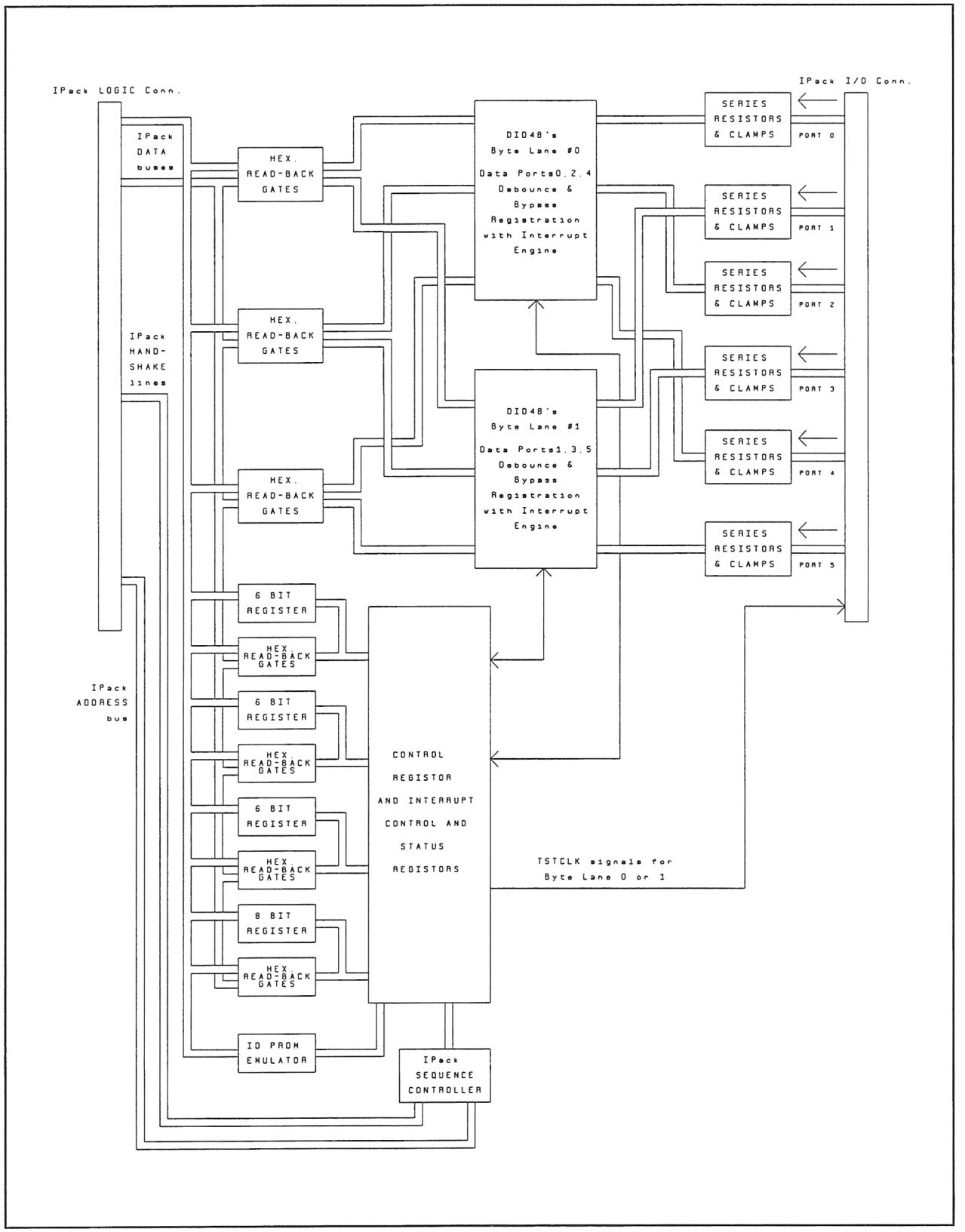


Figure 2-2 DID48 IPack Board Detailed Block Diagram

The block labeled "48 Channel Debouncer" contains the per bit debouncing circuitry, implemented by byte-lane with two Altera EPLD devices. The block labeled "Overvolage Protection Circuits" provides the per input channel current limited high and low clamps, implemented with individual SOIC-packaged logic and series current-limiting resistors. On the right side of the block diagram is the DID48's I/O connector where the six 8-bit data ports (48 discrete lines) are brought on-board, and a ground reference. Also, a debouncing sampling signal is provided on the DID48's I/O connector for external synchronization.

Figure 2-2 presents a detailed block diagram of the DID48. As in the previous figure, on the left side is the IPack's Logic Bus connector through which all host carrier transfers take place. The six 8-bit input data ports are paired into three 16-bit "words". Each "word" contains a 16-bit tristateable gate for driving the IPack Data bus (IPDbus) during I/O reads. All I/O data port reads are performed at the "word" width of 16-bits only.

The block labled "Control Register and Interrupt Control/Status Registers" has a similar IPack carrier interface. This block's function is maintenance of the debounce enable/disabling for both byte-lanes. The interrupt control/status register's primary functions are maintenance of the interrupt engine.

These registers are for enabling, showing the status of the on-change port data and for registering and driving the interrupt vector.

The ID "PROM" Emulator is the circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers. Emulating the (never-changing) ID information in this way reduces parts count and costs, and increases system reliability with its associated Mean Time Between Failures (MTBF) value.

The blocks labeled "IPack Sequence Controller" contain all of the control logic for performing orderly transfers between the DID48 and its carrier. The power-up default logic for this board is included in this section.

The blocks labeled "DID48's byte-lane 0 and 1 Data Ports 0, 2, 4 and 1, 3, 5 Debounce and Bypass Registration with Interrupt Engine" contain the debounce enabling (resolved independently for 256 µs, 1.024 ms, 4.096 ms, and 16.384 ms input sampling periods) or disabling of each byte-lane (three 8-bit data input port for direct drive inputs). For IPack interrupts the N_INTREQ0 signal is driven if the Interrupt-Enable bit is set for any or all input data ports, and any signal changes within each data port asserting the port interrupt status bit.

The blocks labeled "Series Resistors and Clamps" contain 10 KΩ series resistors and high/low clamps on each input channel from the IPack I/O connector.

2.2 Theory of Operation

NOTE: Refer to the DID48 schematics located in Appendix B while reading this material since individual components are referenced by functional name, schematic reference designator, or industry-standard device part number.

The DID48 was developed using VHDL and Synthesis, targeted to Altera EPLDs, schematic captured and integrated to standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the schematics and product design material presented in this document.

2.2.1 DID48 Schematics

The following is a short travel-map through the schematics of the DID48 which incorporate the top-down design methodology. There are six pages of the schematic set in Appendix B.

SCHEMATIC #1

The first page, labeled "Top Level Schematic" (sheet 1 of 3), is the first third of the top-level drawing for the DID48 composed of the IPack Logic connector, three large generic blocks of circuitry (one labeled S_DIDCTL, and the other two labeled S_DIDBT1 and S_DIDBT0), and a 14-stage binary ripple counter providing the jumper selectable debounce sampling periods for each byte-lane with reference designator U10.

SCHEMATIC #2

The second page, labeled "Top Level Schematic" (sheet 2 of 3), is the second third of the top-level drawing of the DID48 composed of six 74FCT541 buffers with reference designators U3, 4, 6, 7, 8, and 9.

SCHEMATIC #3

The third page, labeled "Top Level Schematic" (sheet 2 of 3), is the third part of the top-level drawing for the DID48 composed of the (user's) I/O connector, 48 series resistors, SP720AB/SP721AB high/low clamp electronic protection arrays for ESD and overvoltage protection, a shunt for connecting one of the TSTCLK signals to the I/O connector, and power filter/by-pass capcitors. All 48 input channels are interfaced from the I/O connector via series 10 KΩ resistors, and have reference designators R1 through R48. In parallel with each input channel is SP720AB/ SP721AB high/low clamp electronic protection arrays for ESD and overvoltage protection, and have reference desinators U11, 12, 13, and 14.

SCHEMATIC #4

Pushing-down into the block labeled "S_DIDCTL" brings us to the fourth page of the DID48 schematics. This block is the first of three Altera EPLD's where the IPack interface logic is implemented. The S_DIDCTL is an Altera EPM7064QC100, and is referred to as the DID48 controller module. It has reference designator U2.

SCHEMATIC #5

Pushing-down into the block labeled "S_DIDBT1" brings us to the fifth page of the DID48 schematics. This is the second Altera EPM7128EQC100 EPLD, and is referred to as the byte-lane 1 controller module, and has reference designator U5.

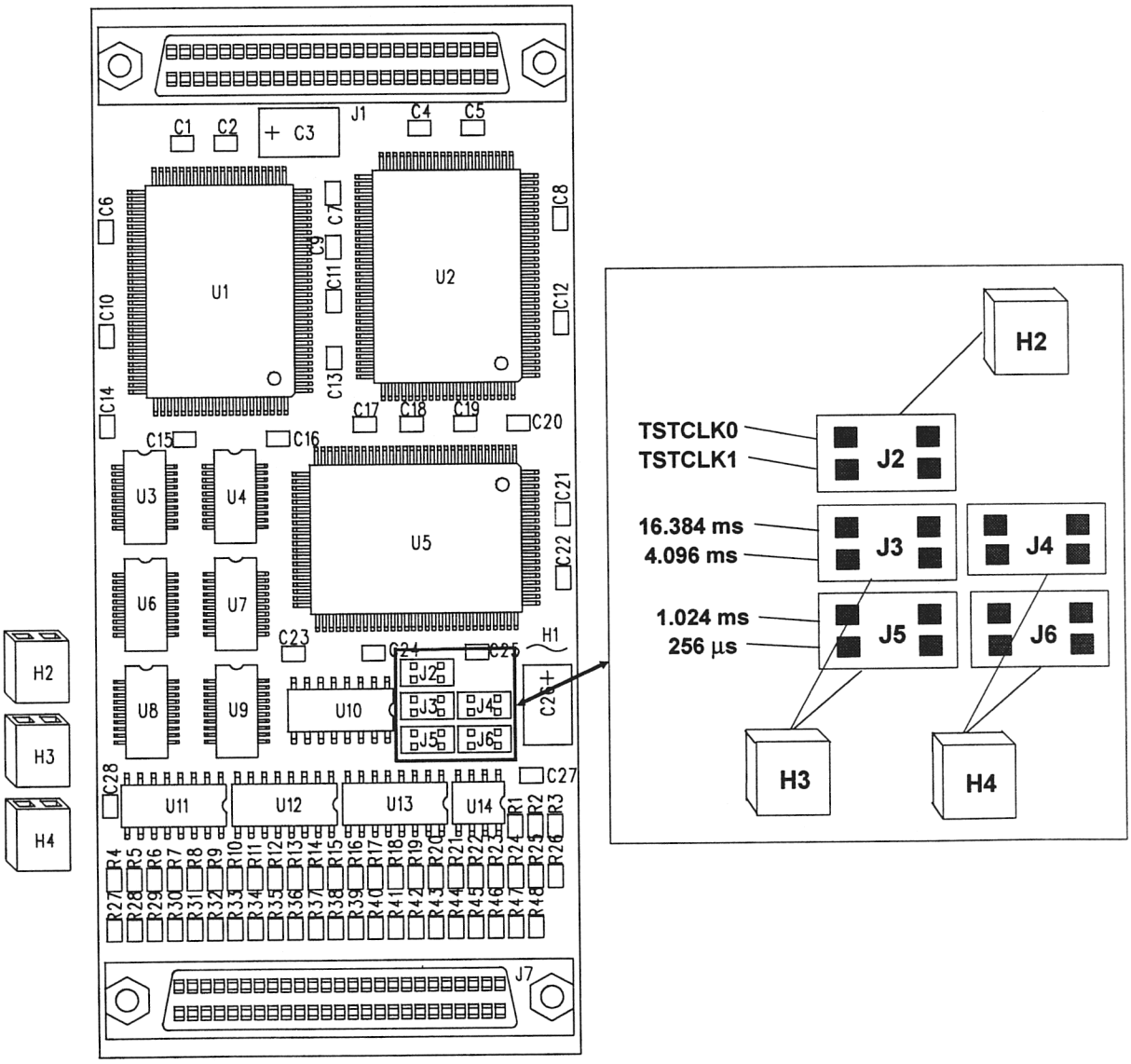


Figure 2-3 DID48 Jumper and shunt Positions

SCHEMATIC #6

Pushing-down into the block labeled "S_DIDBT0" brings us to the sixth page of the DID48 schematics. This third Altera is also an EPM7096QC100, and is referred to as the byte-lane 0 controller module, and has reference designator U1.

2.2.2 DID48 Components and Functions

Figure 2-3 shows the physical positions of the shunts and jumpers on the DID48 IPack. Shunt H3 determines the debounce period for byte-lane 0, and if placed on J3 in the position closest to the IPack Logic connector configures byte-lane 0 for a sampling period of 16.384 ms. H3 placed on J3 in the position closest to the I/O connector configures byte-lane 0 for 4.096 ms sampling period (factory default). Placing H3 on J5 in the position closest to the IPack Logic connector configures the DID48 for 1.024 ms sampling period, and placing H3 in the position closest to the I/O connector on J5 configures byte-lane 0 for 256 µs sampling period.

For byte-lane 1, shunt H4 determines the debounce period, and if placed on J4 in the position closest to the IPack Logic connector configures byte-lane 1 for a sampling period of 16.384 ms. H4 placed on J4 in the position closest to the I/O connector configures byte-lane 1 for 4.096 ms sampling period (factory default). Placing H4 on J6 in the position closest to the IPack Logic connector configures byte-lane 1 for 1.024 ms sampling period, and placing H4 in the position closest to the I/O connector on J6 configures the DID48 for 256 us sampling period.

Shunt H2 on J2 connects the TSTCLK0 or TSTCLK1 signal to pin 49 of the I/O connector. If H2 is placed in the position closest to IPack Logic Connector then the TSTCLK0 signal for port 0 is connected to the I/O connector. Consequently, if H2 is placed in the other postion it connects TSTCLK1 to the I/O connector for port1.

The TSTCLK0 and TSTCLK1 signals (one for each byte-lane) pulse to a logic low for 125 ns once every debounce sample period. If debouncing is disabled, then the TSTCLK signals will pulse low once every 500 ns which is a 2 Mhz sampling rate. This signal was provided on the I/O connector for external synchronization.

DID48 CONTROLLER RESPONSIBILITIES

The DID48 Contoller's primary responsibilities are registering the Control register (debounce enable/disable) and Interrupt control/status/vector registers, emulation of the ID PROM data fields, for handshake control of the IPack I/O space driving of the data ports, and for generation of the sampling period signal to each byte-lane controller. Figure 2-4 shows the inputs block diagram and debounce model contained in the byte-lane 0 and 1 controllers.

BYTE-LANE 0 RESPONSIBILITIES

The byte-lane 0 controller's primary responsibilities are for providing the IPack interface operations for the data ports 0, 2, and 4 which are the lower 8-bits ([7:0]) of the 16 IPack Data Bus bits (IPD[15:0]). The byte-lane 0 controller contains the debouncing logic programmable to one of four sampling periods determined by shunt

H3 and jumpers J3 and J5, and contains the on-change logic (per-port-granularity) used by the DID48 Controller to generate interrupts.

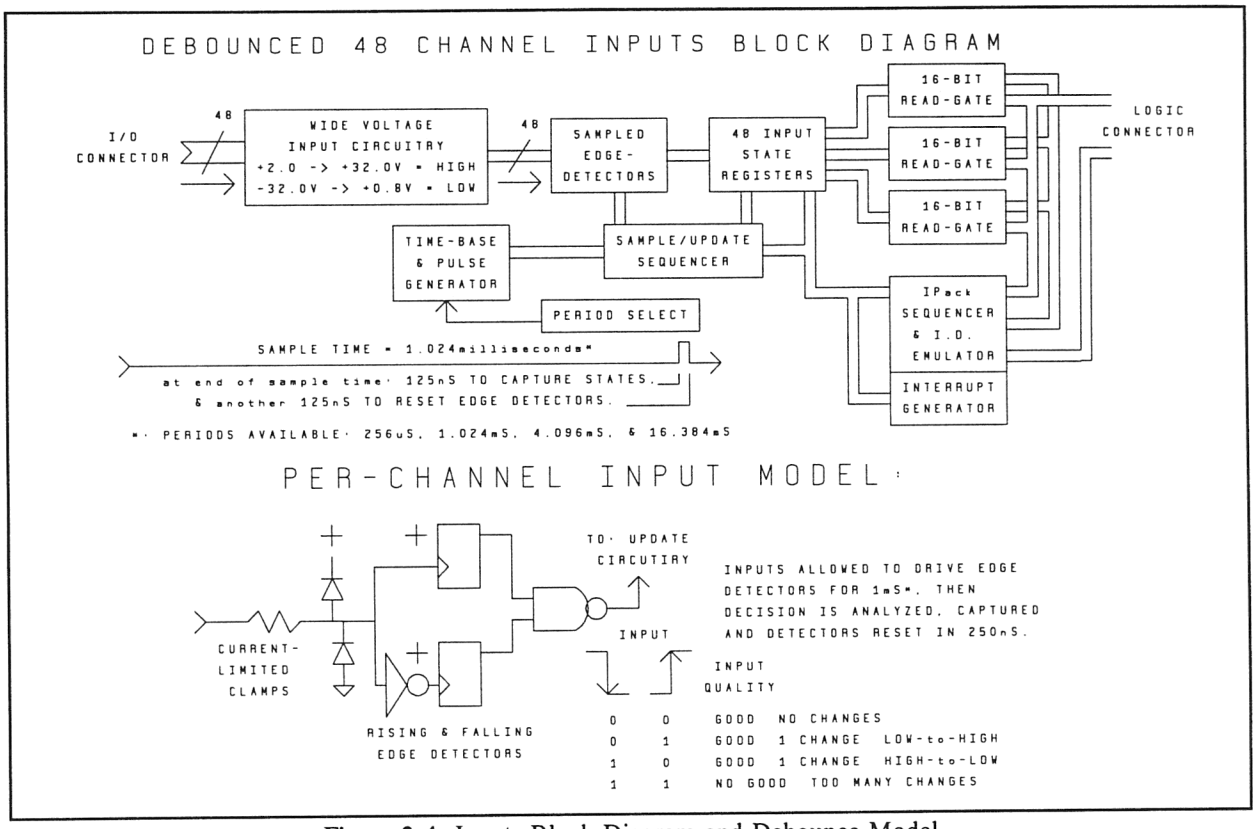


Figure 2-4 Inputs Block Diagram and Debounce Model

BYTE-LANE 1 RESPONSIBILITIES

The byte-lane 1 controller's primary responsibilities are exactlly the same as byte-lane 0's except for providing the IPack interface operations for the data ports 1, 3, and 5 which are the high 8-bits ([15:8]) of the 16 IPack Data Bus bits (IPD[15:0]). The byte-lane 1's debounce logic is determined by shunt H4 and jumpers J4 and J6, and contains the on-change logic for data ports 1, 3, and 5. Also, the byte-lane 1 drives zeros onto IPD[15:8] bits during ID reads and I/O accesses to the control/interrupt registers.

CURRENT-LIMITED CLAMPS

The 10 KΩ series resistors (R1-R48) on each input channel provide extra current limiting protection against electrostatic discharge/over voltage conditions beyond what is already in the Altera devices's input circuitry. The SP720AB/SP721ABs are arrays of SCR/Diode bipolar structures for the high/low discrete input clamps. They provide a logic '1' or 'high' clamping of any input voltage between +2.0 to +32.0 Vdc to a current-limited +5 Vdc. Correspondingly a logic '0' or 'low' of each input channel voltage between -32.0 to +0.8 Vdc is current-limited clamped to ground.

NOTE: If using interrupts, ground or pull up the unused inputs to prevent spurious interrupts. Also, for any pulse wider than the sampling period, two interrupts will be generated; one for the rising edge and one for the falling edge.

RELIABILITY

All of the components on the DID48 were carefully selected to ensure satisfactory operation and to provide the optimum features necessary to create a highly reliable (high MTBF numbers) and economical general purpose digital I/O board.

3.0 HARDWARE INSTALLATION

3.1 Unpacking the DID48

The contents of the DID48 shipping packages are listed in Table 3-1:

Table 3-1 Contents of DID48 Shipping Packages

QTY	DESCRIPTION
1	DID48 Printed Circuit Assembly
1	DID48 User Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-DID48).

3.2 Visual Inspection of the DID48

Examine the DID48 to determine if any damage occurred during shipping.

3.3 DID48 Installation

NOTE: The DID48 is an Electrostatic Sensitive Device (ESD), the hardware installation of the DID48 must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the DID48 can be completed.

The DID48 installation requires the following tools:

Table 3-2 DID48 Installation Tools

QTY	DESCRIPTION
1	ESD STATIC CONTROL KIT/GROUND STRAP/ETC.
1	STANDARD FLAT HEAD SCREWDRIVER (OPTIONAL)

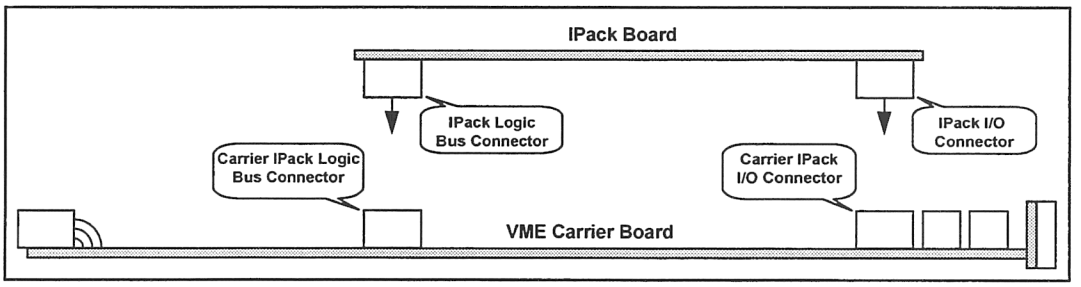


Figure 3-1 Installation of the DID48 on a VME IPack carrier board.

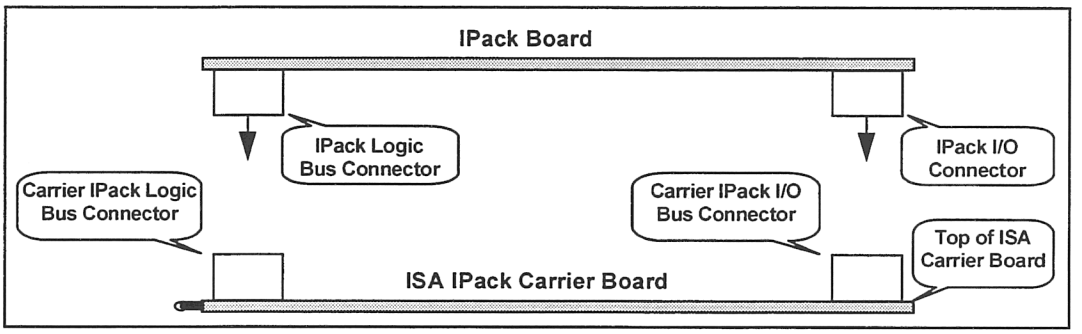


Figure 3-2 Installation of the DID48 on a ISA IPack carrier board.

Figure 3-1 shows how the DID48 is installed on a VME IPack carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Refering to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the DID48 can be made.
3. Remove the DID48 from the shipping package and place it on the ESD bench.
4. Install the DID48 onto the carrier board by applying adequate and equal pressure to the DID48 board at both ends.

* 5. Install four M2x5mm flat head machine screws onto the IPack carrier's IPack connectors.

NOTE: If using interrupts, ground or pull up the unused inputs to prevent spurious interrupts. Also, for any pulse wider than the sampling period, two interrupts will be generated; one for the rising edge and one for the falling edge.

This completes the installation of the DID48 to the carrier board.

Table 3-4 IPack Logic Bus Pin Assignments

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 DID48 IPack I/O Connector Pin Assignments

IPack I/O Pin #	Signal Name
50	GND
49	TSTCLK (jumper select)
48	Port 5 Bit 0
47	Port 5 Bit 1
46	Port 5 Bit 2
45	Port 5 Bit 3
44	Port 5 Bit 4
43	Port 5 Bit 5
42	Port 5 Bit 6
41	Port 5 Bit 7
40	Port 4 Bit 0
39	Port 4 Bit 1
38	Port 4 Bit 2
37	Port 4 Bit 3
36	Port 4 Bit 4
35	Port 4 Bit 5
34	Port 4 Bit 6
33	Port 4 Bit 7
32	Port 3 Bit 0
31	Port 3 Bit 1
30	Port 3 Bit 2
29	Port 3 Bit 3
28	Port 3 Bit 4
27	Port 3 Bit 5
26	Port 3 Bit 6
25	Port 3 Bit 7
24	Port 2 Bit 0
23	Port 2 Bit 1
22	Port 2 Bit 2
21	Port 2 Bit 3
20	Port 2 Bit 4
19	Port 2 Bit 5
18	Port 2 Bit 6
17	Port 2 Bit 7
16	Port 1 Bit 0
15	Port 1 Bit 1
14	Port 1 Bit 2
13	Port 1 Bit 3
12	Port 1 Bit 4
11	Port 1 Bit 5
10	Port 1 Bit 6
9	Port 1 Bit 7
8	Port 0 Bit 0
7	Port 0 Bit 1
6	Port 0 Bit 2
5	Port 0 Bit 3
4	Port 0 Bit 4
3	Port 0 Bit 5
2	Port 0 Bit 6
1	Port 0 Bit 7

4.0 PROGRAMMING GUIDE

This section of the manual describes the operation of the DID48 from the software perspective, detailing the DID48 registers and providing programming examples. A more detailed description of the hardware can be found in section "2.0 DESCRIPTION" and the application examples sections of this manual.

4.1 Description

The DID48 has seven 16-bit wide registers: three data, one general control, and three interrupt related. The data registers may be viewed as either three 16-bit registers or six 8-bit ports. The general control register allows user selection of hardware debounce enable/disable. The interrupt related registers allow the enabling/disabling of interrupts, provide status of the interrupt-capable ports, and programming of the interrupt vector. Byte writes to any of these registers are non-destructive to adjacent bytes.

4.2 IPack ID PROM Listing

Emulating the ID PROM function is possible due to the never changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" read accesses of this information. The ID address space is fully decoded. Therefore, attempted accesses to IPA addresses at and above 0C *hex*, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table 4-1 is the DID48 emulated ID Address Space PROM listing:

Table 4-1 DID48 ID Address Space Listing

IPack ADDRESS	DESCRIPTION	DATA READ
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 *hex*
IPA = 02 *hex*	ASCII "A"	41 *hex*
IPA = 03 *hex*	ASCII "C"	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	DID48's Model Number	68 *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	89 *hex*

4.3 IPack I/O Address Map

The DID48's I/O Address Map was designed with efficiently located data and control/status registers in the IPack I/O space (IPA = 00 ⇒ 06 *hex*). The address detector circuitry is fully decoded.

NOTE: Any attempt to access IPA addresses at and above 07 *hex* will result in no acknowledgment and its subsequent bus timeout error on the carrier upon which this IPack resides.

The first location (IPA = 00 *hex*) is the read data register 0 for the input ports 0 and 1. Port 0 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 1 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The second location (IPA = 01 *hex*) is the read data register 1 for the input ports 2 and 3. Port 2 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 3 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The third location (IPA = 02 *hex*) is the read data register 2 for the intput ports 4 and 5. Port 4 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 5 resides on byte-lane 1 such that accesses occur on IPD[15:8]. A valid access from this location is a 16-bit read of both bytes simultaneously.

The fourth location (IPA = 03 *hex*) is the write and read-back control register 0 for the debounce-control register bits. There are two bits used in this register to enable/disable the debounce function on a per-byte-lane basis with bit 1 for byte-lane 1 down to bit 0 for byte-lane 0.

The next three addresses (IPA= 04⇒06 *hex*) are the interrupt control/status registers and are located in byte-lane 0. Interrupt Register 0 (IR0) is the "Interrupt Status" register, IR1 is the "Interrupt Enable" register, and they use bits [5:0] the same as CR0, with bit 5 to control port 5 down to bit 0 for port 0. IR2 is the "Interrupt Vector" register and uses bits [7:0] and is placed on the IPD[7:0] data lines during an IPack Interrupt cycle.

Table 4-2 is the DID48 I/O Address Map and contains the data ports, control registers and interrupt registers:

Table 4-2 DID48 I/O Address Map

IPack ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 00 *hex*	Data Port 1	Data Port 0	Data Register 0 = Ports 1&0, 8-bits each
IPA = 01 *hex*	Data Port 3	Data Port 2	Data Register 1 = Ports 3&2, 8-bits each
IPA = 02 *hex*	Data Port 5	Data Port 4	Data Register 2 = Ports 5&4, 8-bits each
IPA = 03 *hex*	[XXXX,XXXX]	[XXXX,XX] [1:0]	Control Register 0, Debounce Enable, 2-bits, 0=Debounce, 1=No Debounce
IPA = 04 *hex*	[XXXX,XXXX]	[XX] [5:0]	Interrupt Register 0, Interrupt Status register, 6-bits, 0=No Interrupt, 1=On Change bit set for that port
IPA = 05 *hex*	[XXXX,XXXX]	[XX] [5:0]	Interrupt Register 1, Interrupt Enable register, 6-bits, 0=Disabled, 1=Enabled
IPA = 06 *hex*	[XXXX,XXXX]	[7:0]	Interrupt Register 2, Interrupt Vector Register, 8-bits

NOTE: [X] means not used and are read as zeros

On power-up, all forty-eight (48) data bits defined above are set to the state of the input pins.

4.4 Word Access Address Translation

Table 4-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*

4.5 Byte Access Address Translation

Table 4-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS	BYTE-LANE*
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1

* Byte-lane 1 not applicable for ID Space

4.6 Register Definitions

The DID48 has seven 16 bit-wide registers: three data, one control, and three interrupt. The data registers may be viewed as either three 16-bit registers (two data ports each) or six 8-bit ports. Byte writes to any of these registers are non-destructive to adjacent bytes. The registers are described in detail in the following sections.

The values in the Read/Write (R/W) row of the register bit description indicate: Read Only (R), Write Only (W), or Read/Write (RW).

4.6.1 Data Register 0 Description (IPA = 00 *hex*)

This 16-bit read-only register is the data register consisting of the 8-bit wide input ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up all bits are set to the state of the input pins.

Table 4-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P1 7	P1 6	P1 5	P1 4	P1 3	P1 2	P1 1	P1 0	P0 7	P0 6	P0 5	P0 4	P0 3	P0 2	P0 1	P0 0
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	Din 1 B7	Din 1 B6	Din 1 B5	Din 1 B4	Din 1 B3	Din 1 B2	Din 1 B1	Din 1 B0	Din 0 B7	Din 0 B6	Din 0 B5	Din 0 B4	Din 0 B3	Din 0 B2	Din 0 B1	Din 0 B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din1B7 - Din1B0 : Bits 7 to 0 of the input data for port 1.
Din0B7 - Din0B0 : Bits 7 to 0 of the input data for port 0.

4.6.2 Data Register 1 Description (IPA = 01 *hex*)

This 16-bit read/write register consists of the 8-bit wide input ports 2 and 3. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up all bits are set to the state of the input pins.

Table 4-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power-Up State	Din3B7	Din3B6	Din3B5	Din3B4	Din3B3	Din3B2	Din3B1	Din3B0	Din2B7	Din2B6	Din2B5	Din2B4	Din2B3	Din2B2	Din2B1	Din2B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din3B7 - Din3B0 : Bits 7 to 0 of the input data for port 3.
Din2B7 - Din2B0 : Bits 7 to 0 of the input data for port 2.

4.6.3 Data Register 2 Description (IPA = 02 *hex*)

This 16-bit read only register consists of the 8-bit wide input ports 4 and 5. These two 8-bit ports can also be viewed as a single 16-bit register. Any write to this register is ignored. When read, it returns the state of the input pins. On power-up all bits are set to the state of the input pins.

Table 4-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Power Up State	Din5 B7	Din5 B6	Din5 B5	Din5 B4	Din5 B3	Din5 B2	Din5 B1	Din5 B0	Din4 B7	Din4 B6	Din4 B5	Din4 B4	Din4 B3	Din4 B2	Din4 B1	Din4 B0

Pn7 - Pn0 : Port n data bits 7 through 0. Bit 0 is the least significant bit.
Din5B7 - Din50 : Bits 7 to 0 of the input data for port 5.
Din4B7 - Din40 : Bits 7 to 0 of the input data for port 4.

4.6.4 CR0 - Debounce Control Register 0 (IPA = 03 *hex*)

This 16-bit wide read/write register enables/disables the debounce circuitry for the six input ports on a per byte-lane basis. Bits[1:0] enable/disable debouncing for byte-lanes 1 and 0, respectively.

Table 4-8 Debounce Control Register Bit Descriptions

Bit #	Bits 15 to 2	1	0
Bit Name	Not Used Read as 0's	BL1 DBD	BL0 DBD
R/W	Reads 0s / Writes Disregarded	RW	RW
Power-Up State		0	0

BL1DBD-BL0DBD: Debounce Disable bits [1:0]

Table 4-9 Output Enable Control Bit

DBD Value	OUTPUT ENABLE SELECTION PER PORT
0	Debounce Enabled for byte-lane n
1	Debounce Disabled for byte-lane n

4.6.5 IR0 - Interrupt Status Register (IPA = 04 *hex*)

This 16-bit wide read/write register provides the status for the input ports. A bit is set in this register if there is a state change in the corresponding input port. If a bit is set in this register, it is cleared by writing a '1' to that bit position. Clearing this bit does not affect any other status bits. The status indication is valid whether the interrupt is enabled or disabled for the bit.

Table 4-10 Interrupt Status Register Bit Descriptions

Bit #	Bits 15 to 6	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	P5 IS	P4 IS	P3 IS	P2 IS	P1 IS	P0 IS
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW
Power-Up State		0	0	0	0	0	0

Table 4-11 Interrupt Status Per Bit

IS Value	INTERRUPT ENABLE SELECTION PER BIT
0	Input condition not detected for bit
1	Input condition detected for bit

4.6.6 IR1 - Interrupt Enable Control Register (IPA = 05 *hex*)

This 16-bit wide read/write register enable/disables the interrupt for each port. Interrupts can be enabled/disabled on a per-port basis with bit 5 controlling port 5 down to bit 0 for port 0.

Table 4-12 Interrupt Enable Control Register Bit Descriptions

Bit #	Bits 15 to 2	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	P5 IE	P4 IE	P3 IE	P2 IE	P1 IE	P0 IE
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW
Power-Up State		0	0	0	0	0	0

4.6.7 IR2 - Interrupt Vector Register (IPA = 06 *hex*)

This 16-bit wide read/write register contains the interrupt vector. Only the lower 8 bits are used. The upper 8 bits are read as zeros. This vector will be presented on the IPack data bus during an interrupt-request transfer.

Table 4-13 Interrupt Vector Register Bit Descriptions

Bit #	Bits 15 to 8	7	6	5	4	3	2	1	0
Bit Name	Not Used Read as 0's	IV B7	IV B6	IV B5	IV B4	IV B3	IV B2	IV B1	IV B0
R/W	Reads 0s / Writes Disregarded	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State		0	0	0	0	0	0	0	0

IVB7-IVB0: The 8-bit interrupt vector

4.7 Programming Examples

The following examples show how to control and operate the DID48. The two examples demonstrate how to: enable and disable hardware debouncing, and how to use the interrupts.

4.7.1 Debounce Enable Example

This example illustrates debounce enable and disable control for the DID48. Only port 0 is used in this example; however, ports 2 and 4 are simultaneously enabled/disabled with port 0 because they are all in byte-lane 0.

- At power-up, the data registers are all cleared (value of '0000').
- At power-up, the Debounce Disable register is cleared (value of '0000' which equals debounce enabled).
- At this point, the inputs are in the debounce mode, and any change on the input signals will be required to be outside of the jumper selectable debounce sampling period to see the new input data.
- Read values from data port 0 for debounced input data.
- Write '0001' *hex* to the CR0 (Debounce Disable register). This disables the debouncing for byte-lane 0.
- Read data value from data port 0 for non-debounced input data.
- Write '0000' *hex* to the CR0. This enables the debouncing for byte-lane 0 again.

4.7.2 Interrupt Example

This example illustrates how to configure the DID48 for interrupts. Only port 0 is used in this example; however, the programming concept is the same for the other ports.

NOTE: The detection of the selected input condition is independent of whether the interrupt is enabled or disabled. This allows polling of the interrupt-status register to determine if the selected input condition was detected. For example, the status register will indicate detection of a rising or falling edge within data port 0 regardless of whether the bit 0 interrupt is enabled.

NOTE: This example assumes a suitable ISR (Interrupt Service Routine) exists. An example ISR is shown on page 4-13.

- Write a '0000' *hex* to the Interrupt Enable register. This disables all interrupts.
- At this point, the input condition required to set the status bit (and generate an interrupt if the interrupt is enabled) is a change (rising or falling edge) on any signal in data port 0.
- Write a '0001' *hex* to the Interrupt-Enable register. This enables the interrupt for bit 0.
- Applying a rising or falling edge to any bit in data port 0 that will now generate an interrupt.
- Write a '0000' *hex* to the Interrupt-Enable register. This disables all interrupts.

4.7.3 Interrupt Service Routine Example

If the interrupt capability of the DID48 is used, a suitable ISR must exist. This example describes some steps that the ISR should perform. The host dependent details are left out since they will vary.

ISR entry point:

- Read the Interrupt Status register. Test the bits to determine which interrupt(s) has(have) occurred.
- The event (interrupt) usually indicates that some event driven action is to be taken. If this is the case, take the action associated with the detected interrupt(s). If the action taken must not be interrupted, disable interrupts while taking the action then re-enable them.
- Remove the condition that caused the interrupt. If this is not practical to do from the ISR, disable the interrupt by clearing the enable bit for the interrupt in the interrupt enable register, and set a flag indicating that some other process should clear the condition. If the condition is cleared outside the ISR, then the clearing process must also re-enable the interrupt.
- Clear the interrupt status register by writing a 1 to the bit(s) that is(are) set in the status register. This can effectively be accomplished by writing back the same value read from the status register.
- Return from exception

5.0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration citied, and do not supplant the maximum and minimum envelopes presented in section 1: INTRODUCTION.

5.2 State Timing Diagrams

The state waveforms for Figures 5-2 through 5-9 were made using the HP 1 GHz Timing Master Module and the Systran IPack Logic Bus Extender (IPLBE) with the IPack Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer's screen are active-low, and are represented by a '/' as the first character as opposed to the 'N_' used elsewhere, due to the limited amount of character spacing.

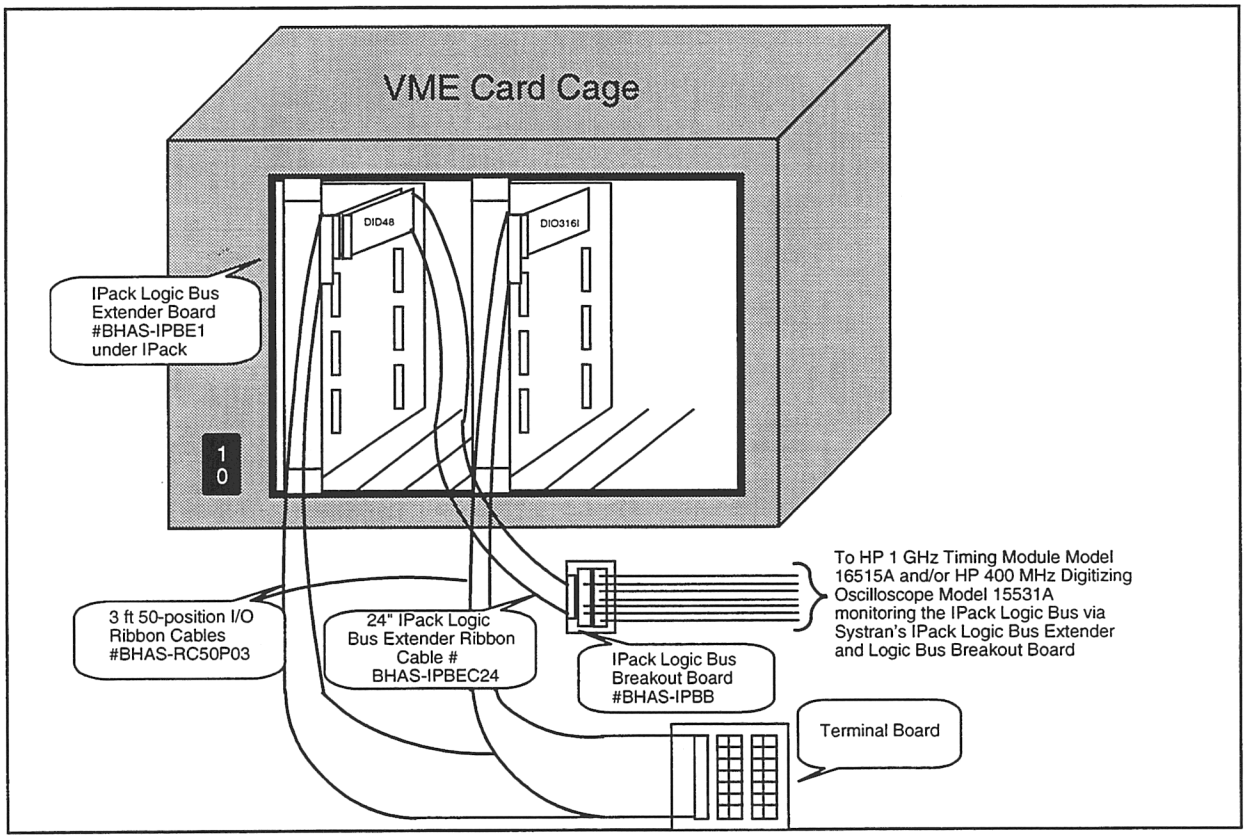


Figure 5-1 IPack Test Configuration for State Timing Measurements

5.2.1 ID Read Cycle

Figure 5-2 is a complete DID48 ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals.

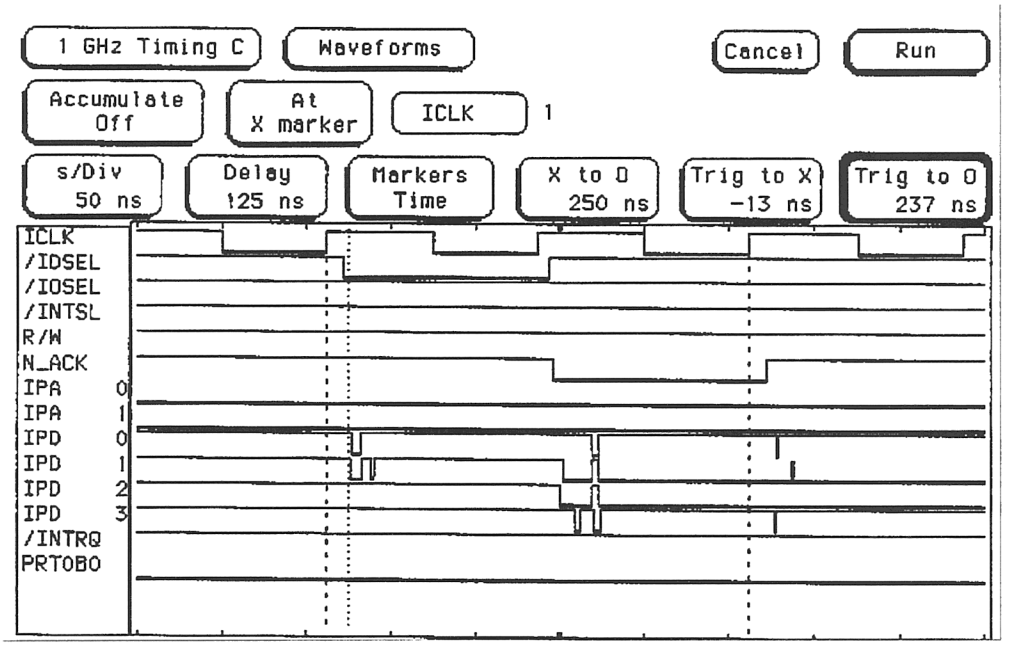


Figure 5-2 Complete DID48 ID Read Cycle

Figure 5-3 is a zoomed-in view of the DID48 ID cycle driving the N_ACK and IPD0-3 signals; showing a typical response time of about 15 nanoseconds for driving these signals. The IPack Logic I/F Specification (Rev. 0.7.1, page 35) requires these signals be driven within 40 nanoseconds.

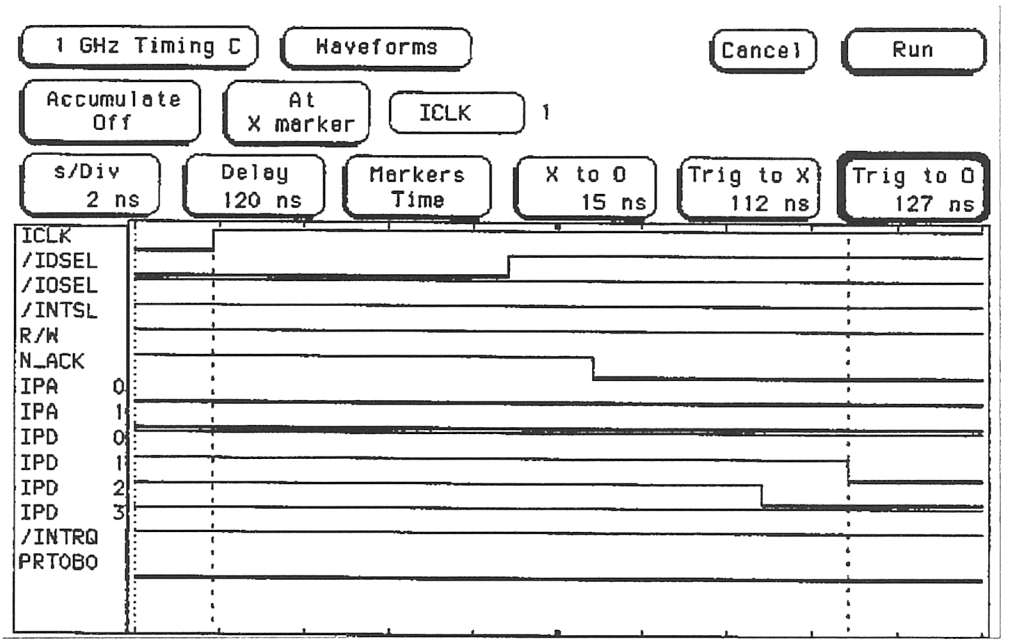


Figure 5-3 Zoomed-in Version of DID48 ID Cycle Driving N_ACK and IPD0-3

5.2.2 I/O Read Cycle

Figure 5-4 is a complete DID48 I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals.

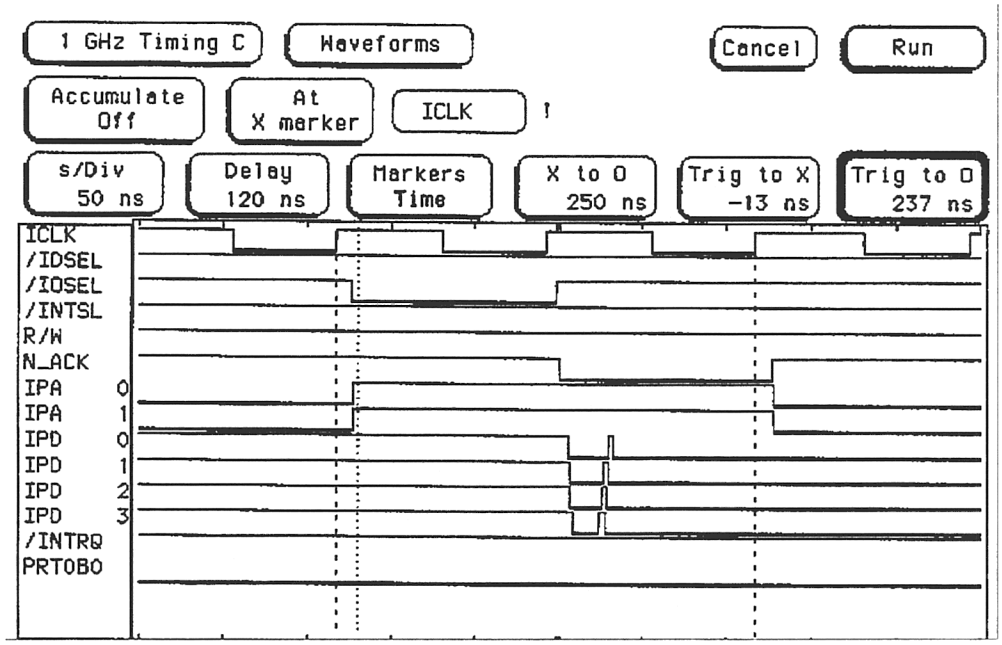


Figure 5-4 Complete DID48 I/O Read Cycle

Figure 5-5 is a zoomed-in view of the DID48 IO read cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 16 nanoseconds for driving these signals.

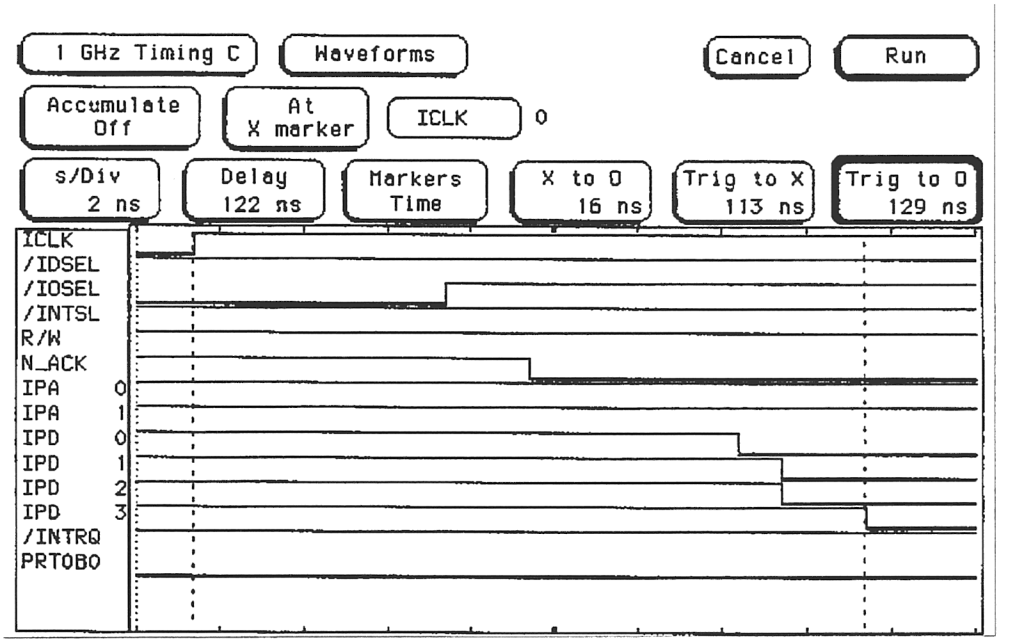


Figure 5-5 Zoomed-in View of DID48 I/O Read Cycle Driving N_ACK and IPD0-3

5.2.3 Interrupt Request With "Debouncing Disabled"

Figure 5-6 shows an Interrupt Request with "Debouncing Disabled" and a few microseconds later an IPack Interrupt Select Cycle.

NOTE: Figure 5-6 is very important information for users concerned about system response time with debouncing disabled. The Interrupt Request signal is asserted by the DID48 in less than 1 microsecond. This means that the host IPack carrier board will receive the interrupt request signal as fast as possible to begin its interrupt service routine.

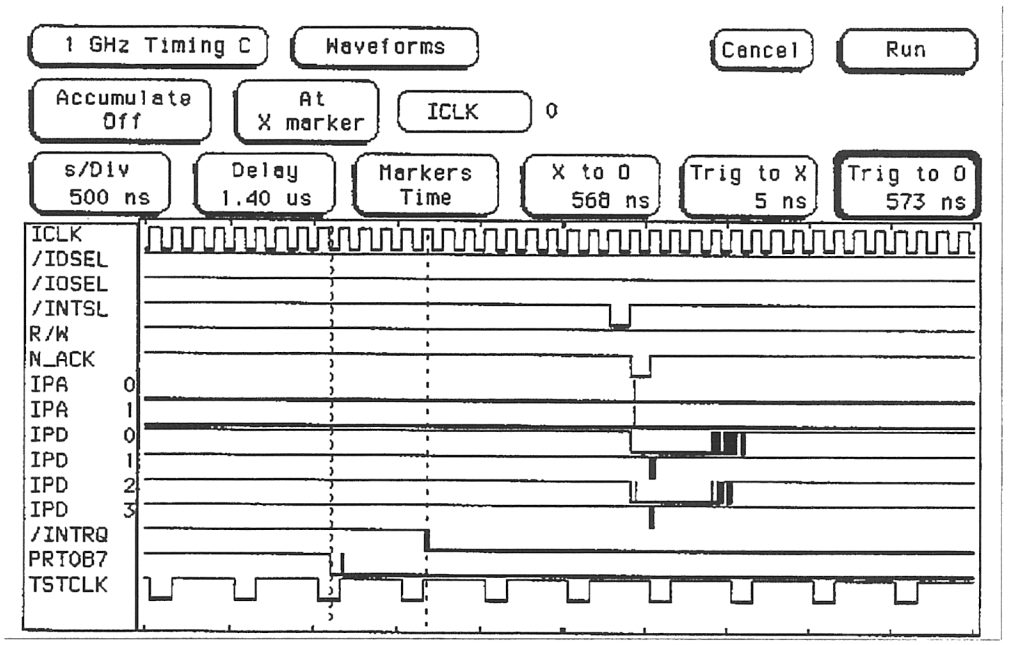


Figure 5-6 DID48 Interrupt Request and Select Cycle (Debounce Disabled)

Figure 5-7 is a view of the DID48's Interrupt Request signal (/INTRQ) being asserted 571 nanoseconds after the programmed event "Interrupt on a change of port 0, bit 7 with debouncing disabled", which is the 'PRT0B7' signal label on the waveform diagram.

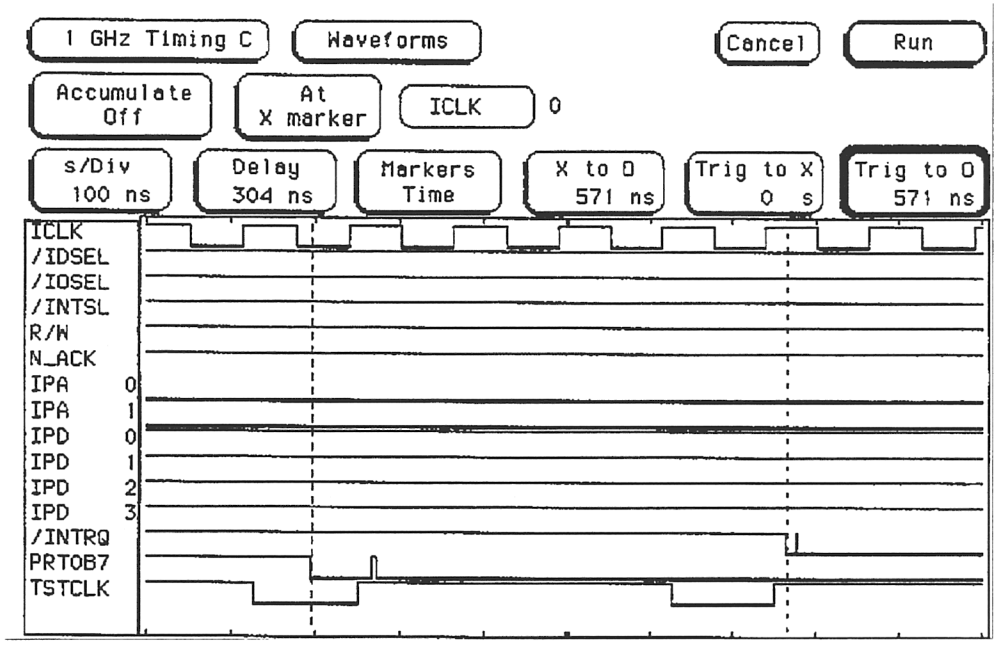


Figure 5-7 DID48 Driving N_INTREQ0 (Debounce Disabled)

5.2.4 Interrupt Request With "Debouncing Enabled"

Figure 5-8 shows an Interrupt Request with "Debouncing Enabled" and a few microseconds later an IPack Interrupt Select Cycle.

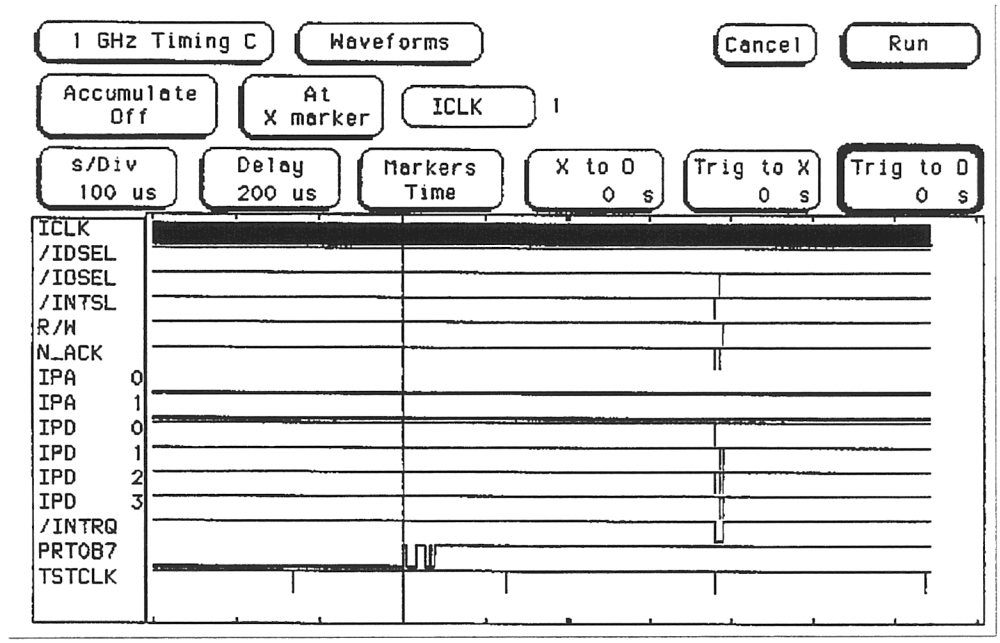


Figure 5-8 DID48 Interrupt Request and Service Routine (Debounce Enabled)

Figure 5-9 is a view of the DID48's Interrupt Request signal (/INTRQ) being asserted a few nanoseconds after the second debounce sample period after the programmed event "Interrupt on a change of port 0, bit 7 with debouncing", which is the 'PRT0B7' signal label on the waveform diagram. This figure also shows N_ACK and IPD0-3.

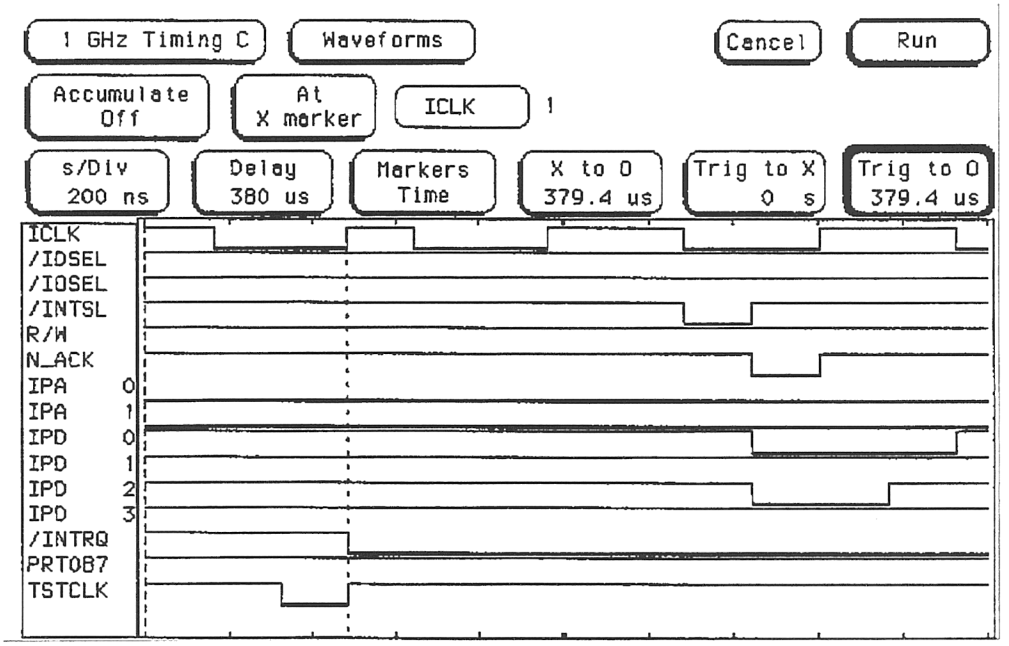


Figure 5-9 DID48 Interrupt Request and Select Cycle (Debounce Enabled)

NOTE: Figures 5-8 and 5-9 are very important for users concerned about system response time with debouncing enabled. The Interrupt Request signal is asserted by the DID48 a few nanoseconds after the second debounce sample period. This means that the host IPack carrier board will receive the interrupt request signal as fast as possible after the signal is debounced to begin its interrupt service routine. For example; if the debounce sample period is set to 16.384 ms (worst case), it may take as long as just under 32.768 ms to drive the IPack N_INTREQ0 signal.

6.0 Typical Applications

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the DID48 IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 A Short Glossary Of DID48 Applications

The following typical applications were developed using one or more channels on the DID48 IPack.

- Monitoring of switched signals
- Relays and positive discrete voltages
- Relays and negative discrete voltages

Most common discrete signal monitoring configuration operations may be performed (within limits) by proper connections and software manipulations.

6.2.1 Monitoring Of Switched Signals

Figure 6-1 is an application example that provides the user with one of many possible configurations for using the DID48 as a monitor of common single-pole double-throw switches. The common of up to 48 individual switches may be connected directly to each DID48 input. The switches are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). In this application the discrete signals being monitored are connected to the normally-open contact of the switches. Switches S1 through S4 have the +2.0 to +32.0 voltage range connected to the normally-open contacts, and the -32.0 to GND voltage range connected to the switch common via a resistor. Switches S45 through S48 have the -32.0 to GND voltage range connected to the normally-open contacts, and the +2.0 to +32.0 voltage range connected to the switch common via a resistor.

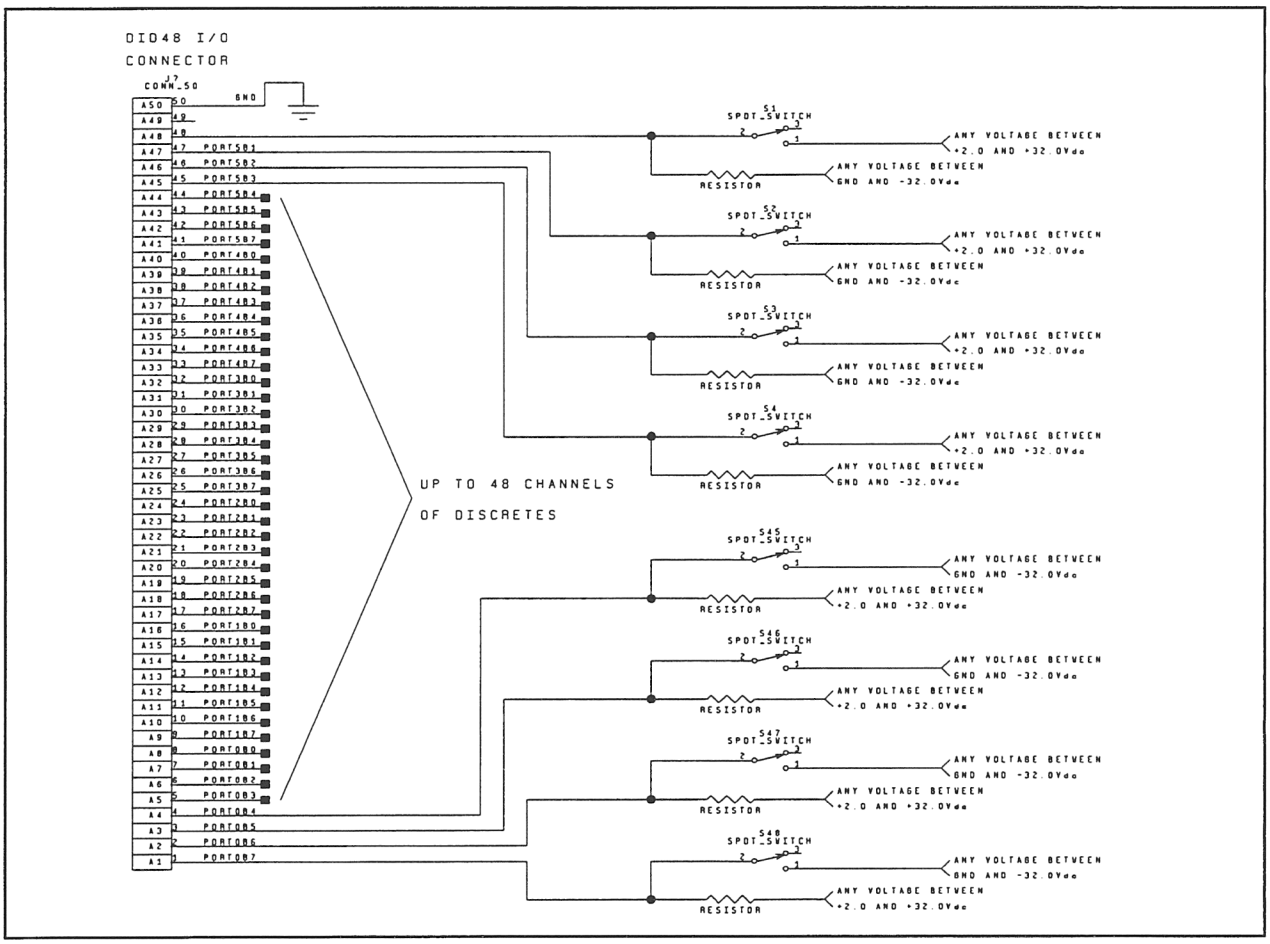


Figure 6-1 Monitoring Switched Signals

6.2.2 Relays and Positive Discrete Voltages

Figure 6-2 is a combination application example of connecting the DID48 to double-pole double-throw relays, and monitoring positive discrete voltages (like +28 Vdc aircraft discretes). The common of up to 48 individual relays can be connected directly to each DID48 input. The relays are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). The discrete signals connected to the normally-open and normally-closed contacts of the relays can be interchanged for make-or-break monitoring.

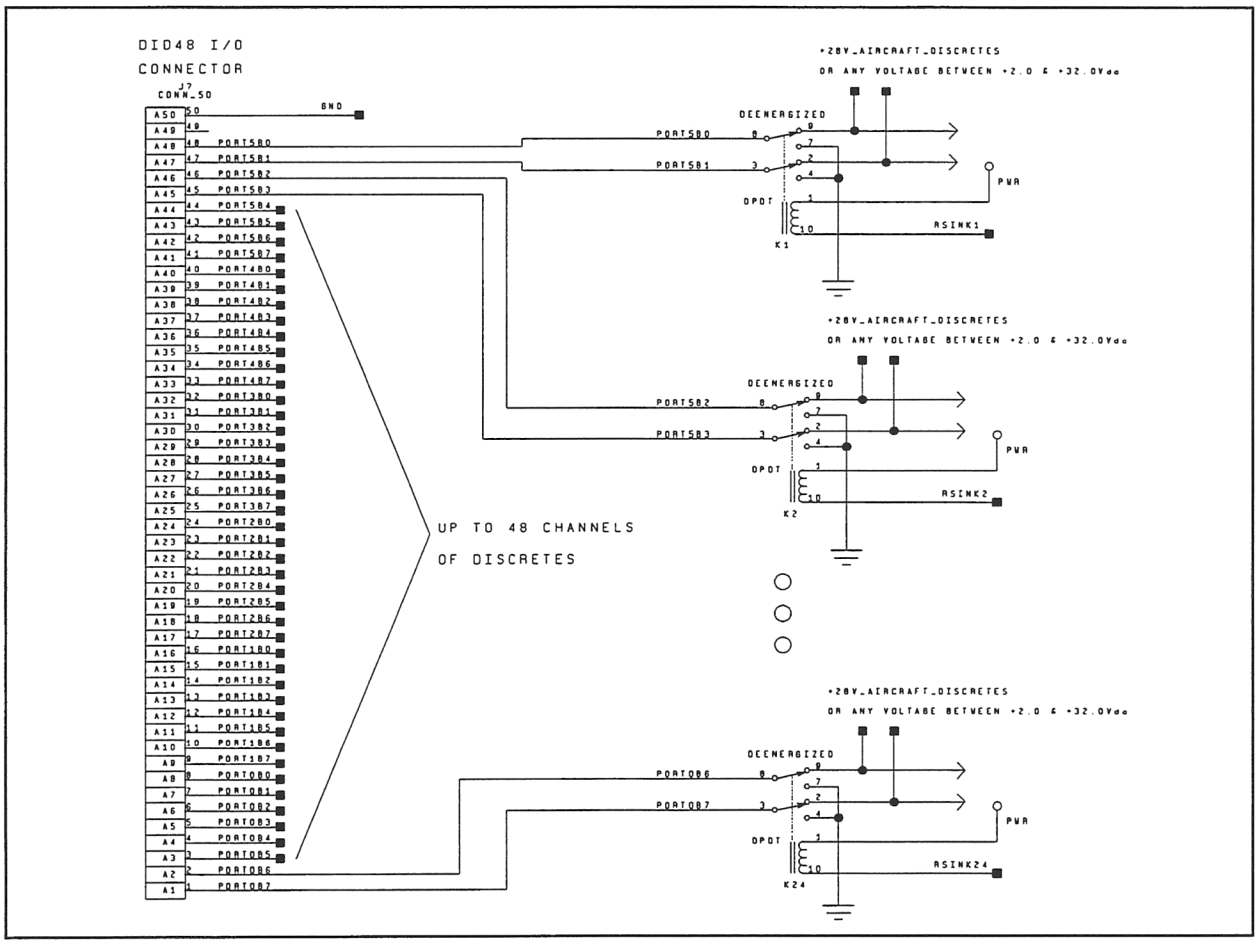


Figure 6-2 Relays and Positive Discrete Voltages

6.2.3 Relays and Negative Discrete Voltages

Figure 6-3 is a combination application example like Figure 6-2 except that the DID48 is connected to double-pole double-throw relays, and uses negative discrete voltages. The common of up to 48 individual relays may be connected directly to each DID48 input. Again the relays are debounced and interrupts can be enabled in groups of eight (per 8-bit input port). The discrete signals connected to the normally-open and normally-closed contacts of the relays can be interchanged for make-or-break monitoring.

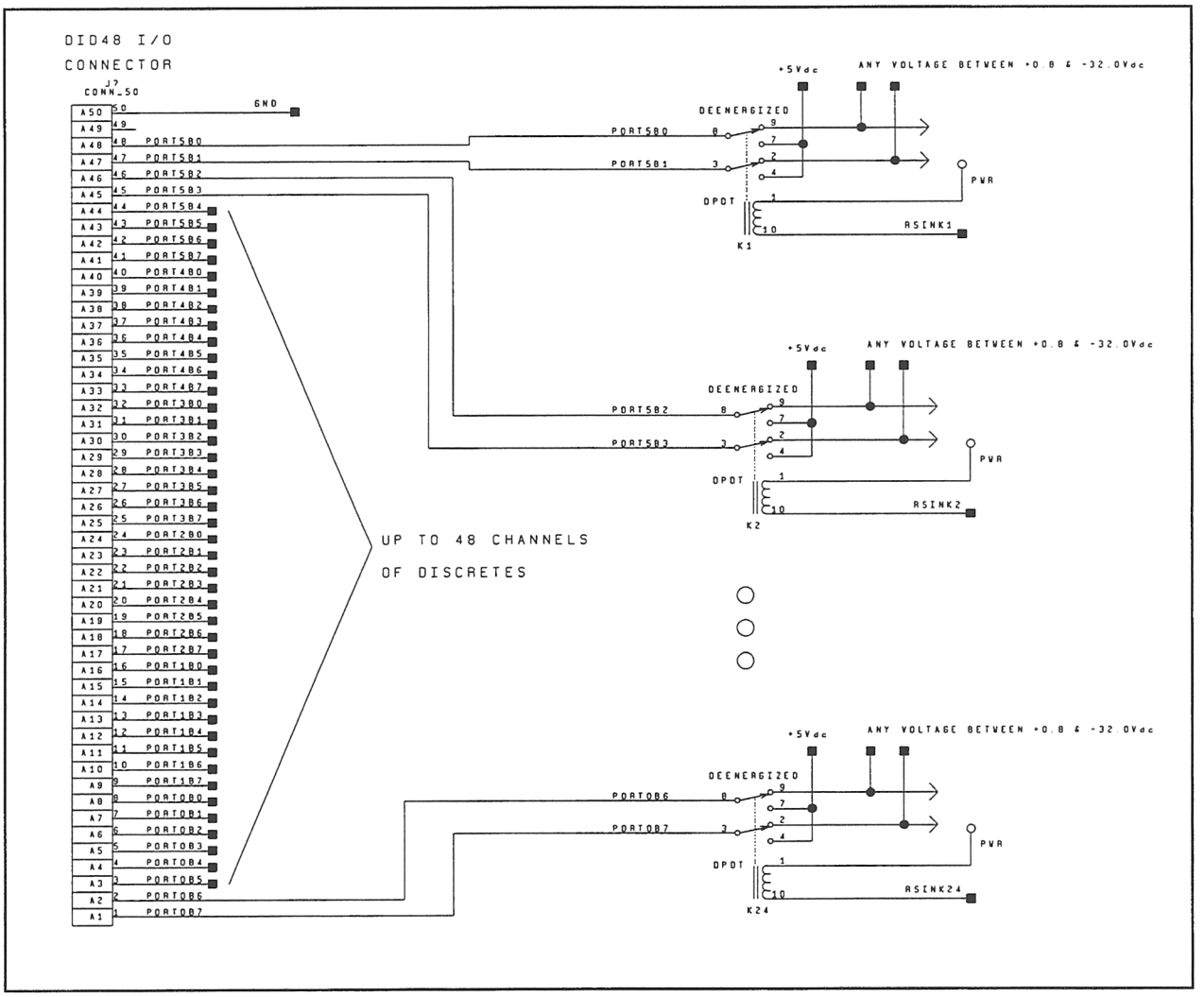


Figure 6-3 Relays and Negative and Discrete Voltages

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.1.1 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.1.2 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.1.3 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

7.7 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.
- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:

This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high speed (32MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:

The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0mA (logic low) in parallel with 30ρF. All signals have a 10KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK

This signal, ≡ CLK in the specification, is an 8MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)

These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)

These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200mS following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "double-wide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:
+5volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50. +12volts is sourced via pin 23. And, -12volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a "singlewide" IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a "doublewide" IP are 3.600″ by 3.900″, +.000/-.020″. There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a "singlewide" IP, and 3.6″ by 3.188″ for a "doublewide" IP. The maximum height of components on the IP is 0.315″, with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

MEMORY TRANSFERS' CYCLE TABLES

CYCLE'	MEM WRITE NO HOLDS NO WAITS			MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS								MEM WRITE 1 HOLD 3 WAITS								DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15'0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH * END OF'			◇					◇			◇											◇					

CYCLE'	MEM READ NO HOLDS NO WAITS			MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS					MEM READ 1 HOLD 3 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15'0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND'

* IPD[15'0] = IPA[22'7] during during the SELECT cycle, and is used for data for all other cycles.

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE' +5v

0 LOW STATE' GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS' CYCLE TABLES

CYCLE'	ID READ NO HOLDS NO WAITS			ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS						ID READ 2 HOLDS 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7'0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND'

X DON'T CARE

Z HIGH IMPEDANCE

1 HIGH STATE' +5v

0 LOW STATE' GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPac

INT TRANSFERS' CYCLE TABLES

CYCLE'	INT READ NO HOLDS NO WAITS			INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
PD[7'0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS' CYCLE TABLES

CYCLE'	I/O WRITE NO HOLDS NO WAITS IDLE	SELECT	TERM	IDLE	I/O WRITE NO HOLDS 3 WAITS SELECT	WAIT	WAIT	WAIT	TERM	IDLE	I/O WRITE 2 HOLDS NO WAITS SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	IDLE	I/O WRITE 3 HOLDS 1 WAIT SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	DRIVEN BY' IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPD[15'0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH (◇ END OF')			◇						◇			◇										◇					

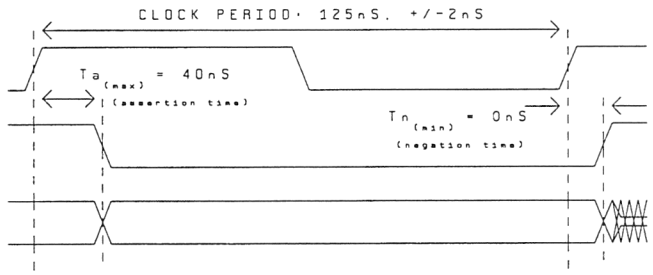
CYCLE'	I/O READ NO HOLDS NO WAITS IDLE	SELECT	TERM	IDLE	I/O READ NO HOLDS 2 WAITS SELECT	WAIT	WAIT	TERM	IDLE	I/O READ 3 HOLDS NO WAITS SELECT	HOLD	HOLD	HOLD	TERM	I/O READ 2 HOLDS 3 WAITS SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	I/O READ 3 HOLDS 2 WAITS SELECT	WT&HLD	WT&HLD	HOLD	TERM	DRIVEN BY' IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15'0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND'

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE' +5v
- 0 — LOW STATE' GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE' / SIDE' / ASSERTED LOW'	DOUBLE-WIDE N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IOSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IOSEL	SINGLE-WIDE N_MEMSEL	N_IOSEL	N_INTSEL	N_IOSEL	VALID TRANSFER(s)'
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY' A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY' B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY' BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O' A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O' B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O' BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT' A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT' B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	ID' A-SIDE ONLY

Product specifications subject to change without notice
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B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B

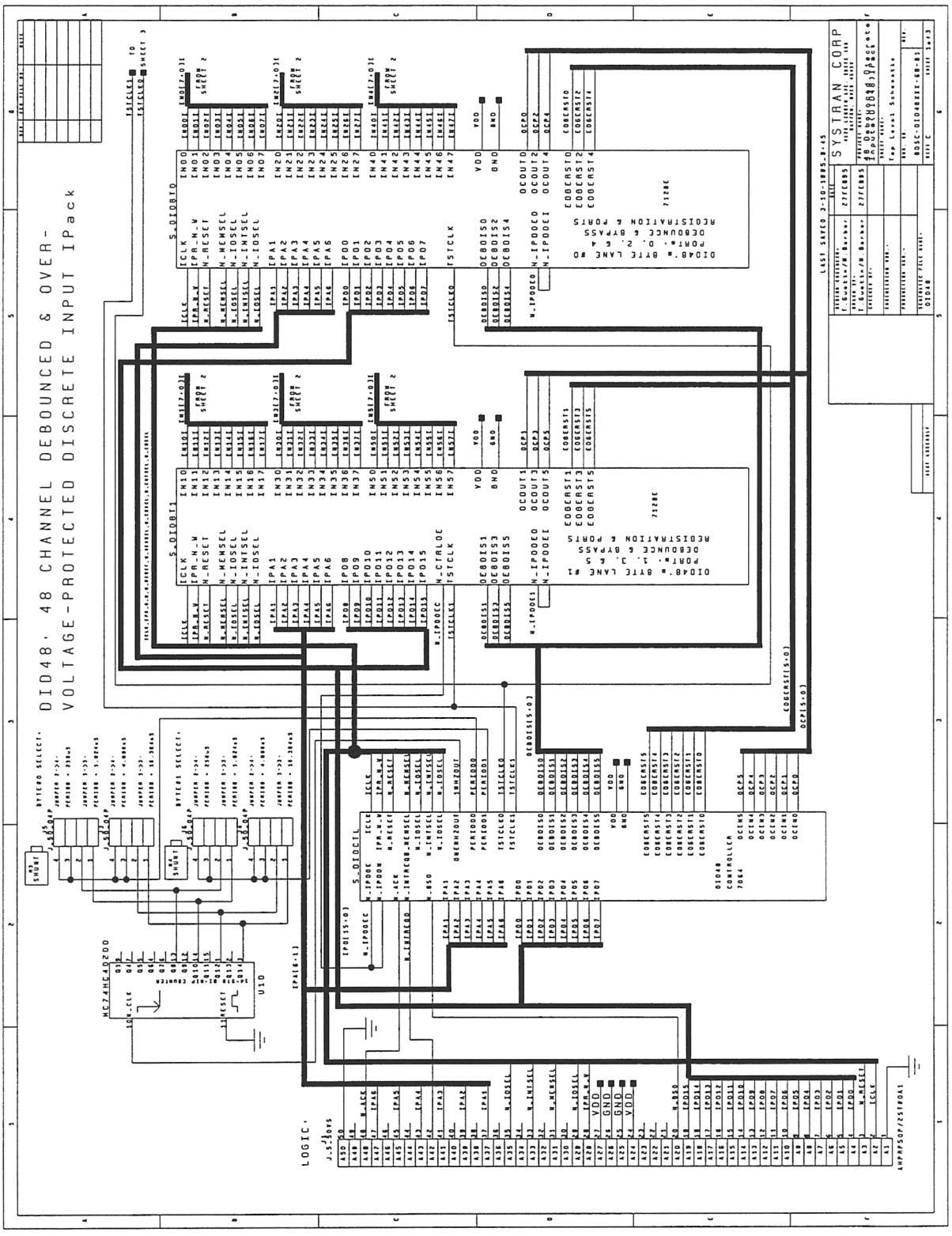

Figure B-1 Schematic #1

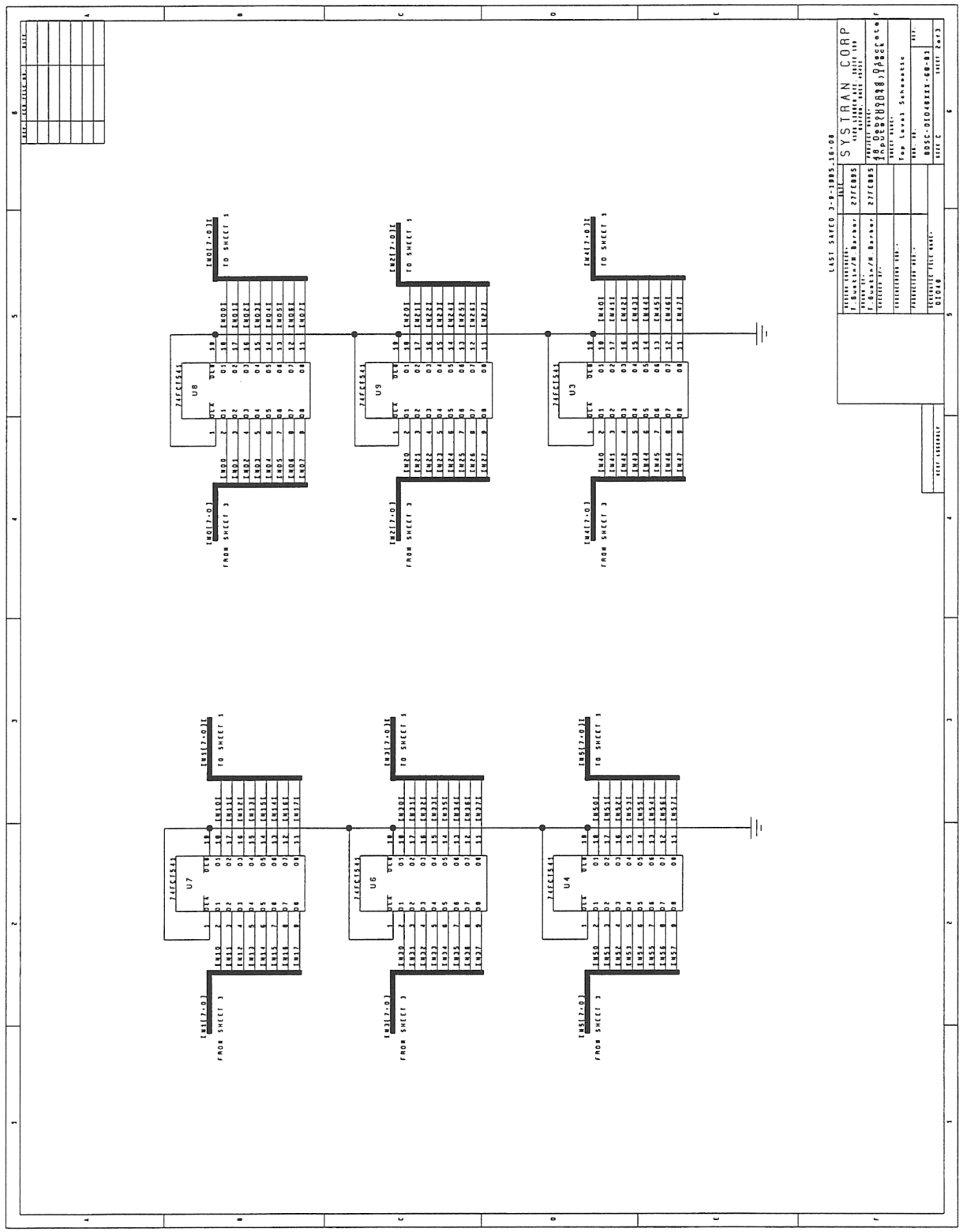

Figure B-2 Schematic #2

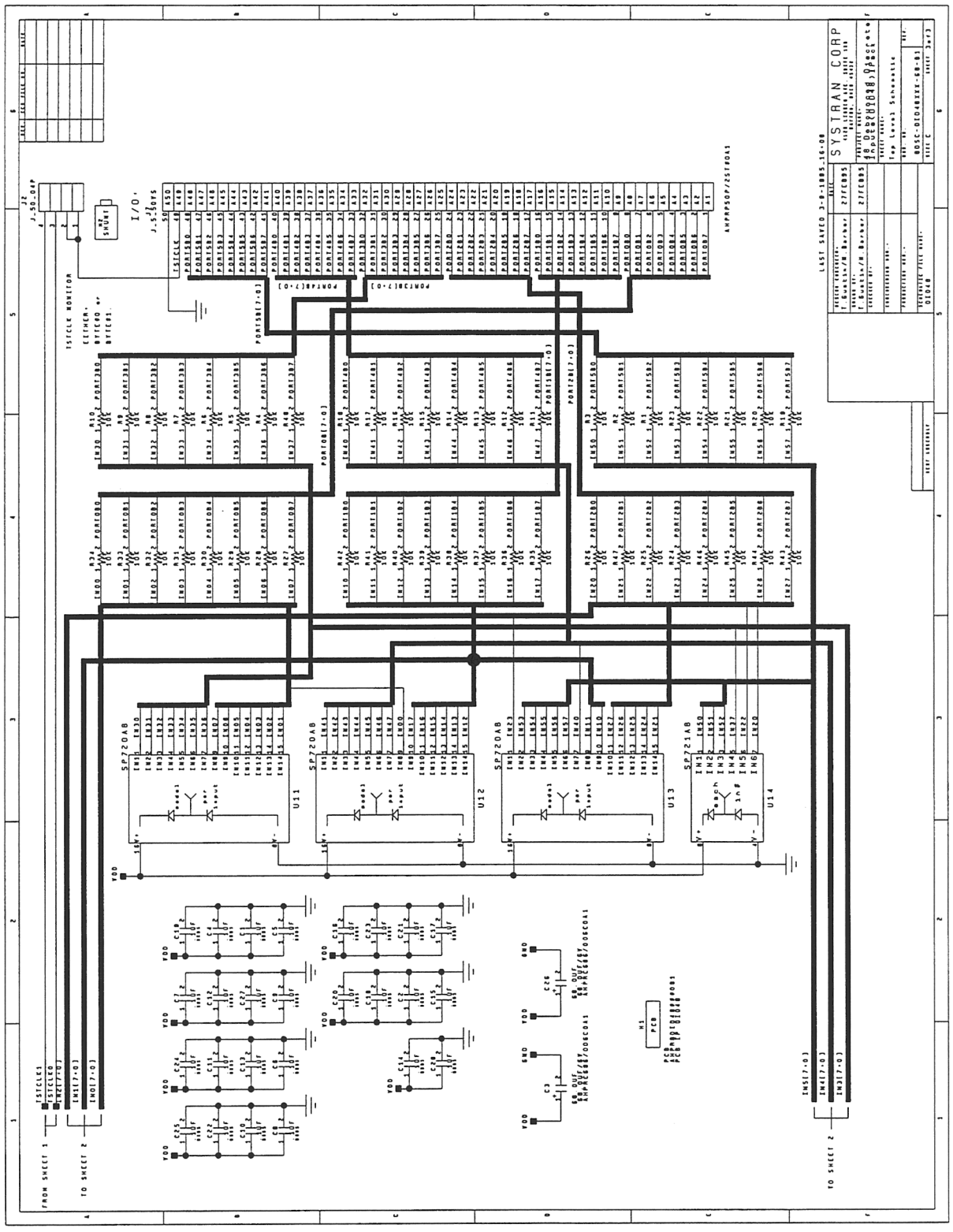

Figure B-3 Schematic #3

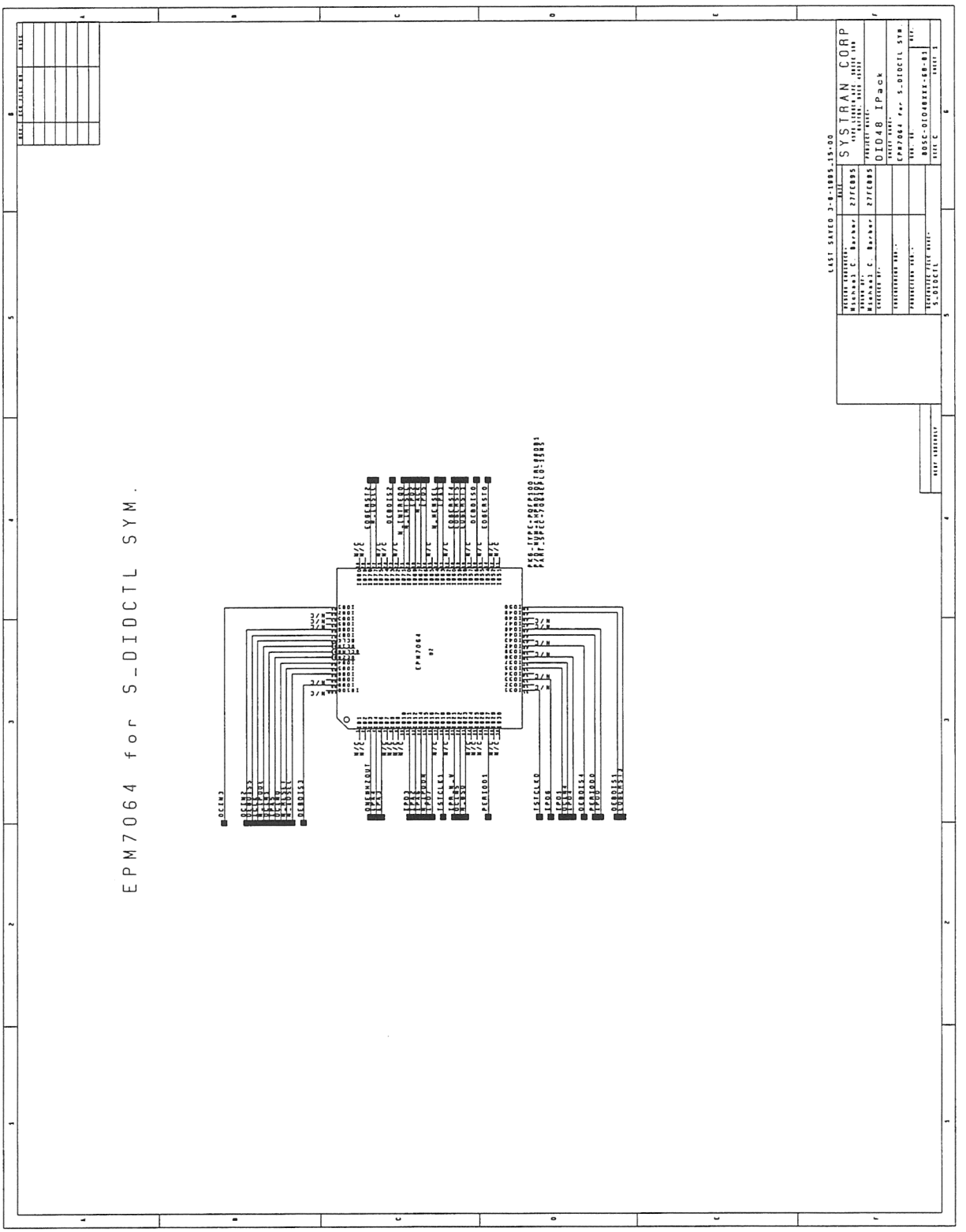

Figure B-4 Schematic #4

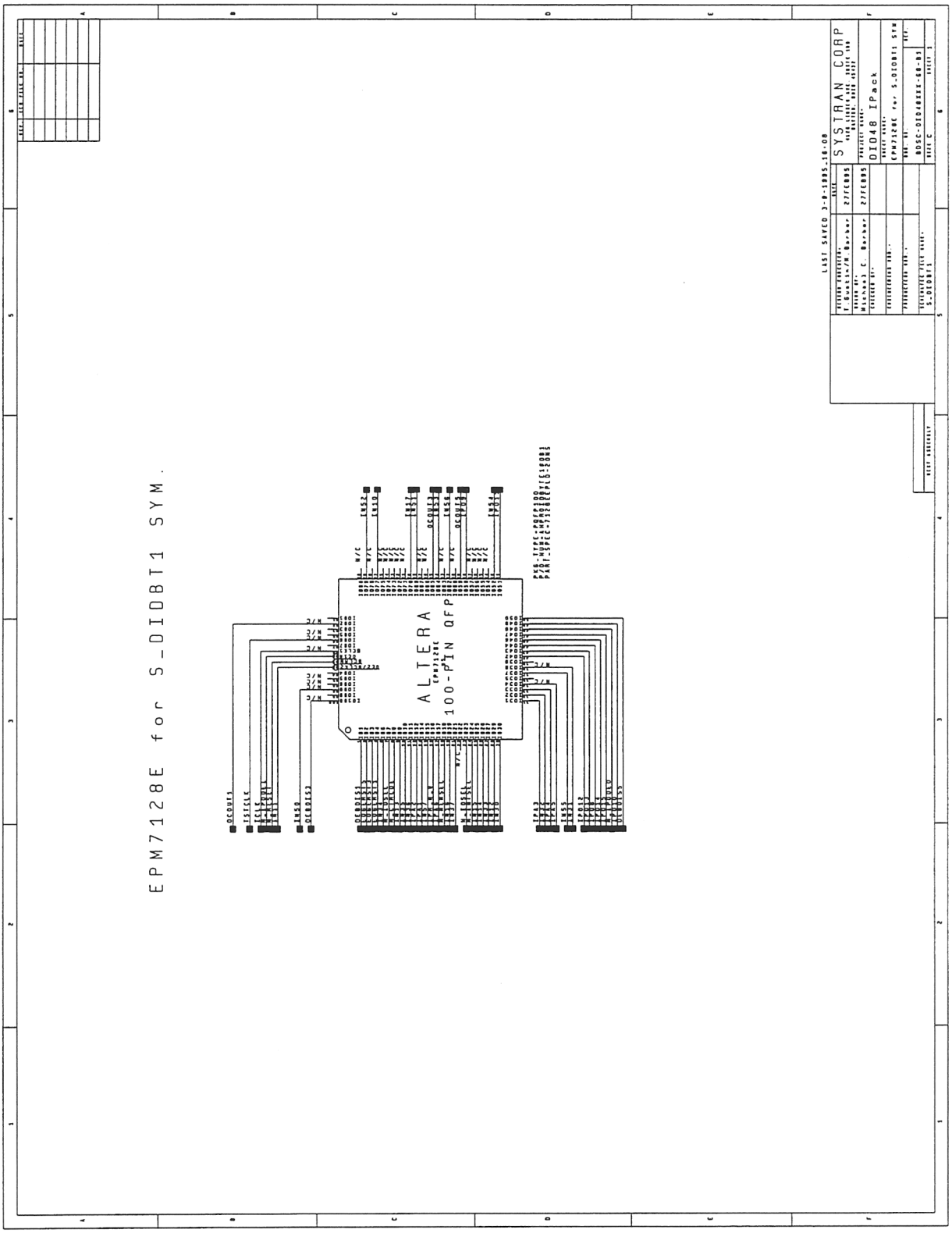

Figure B-5 Schematic #5

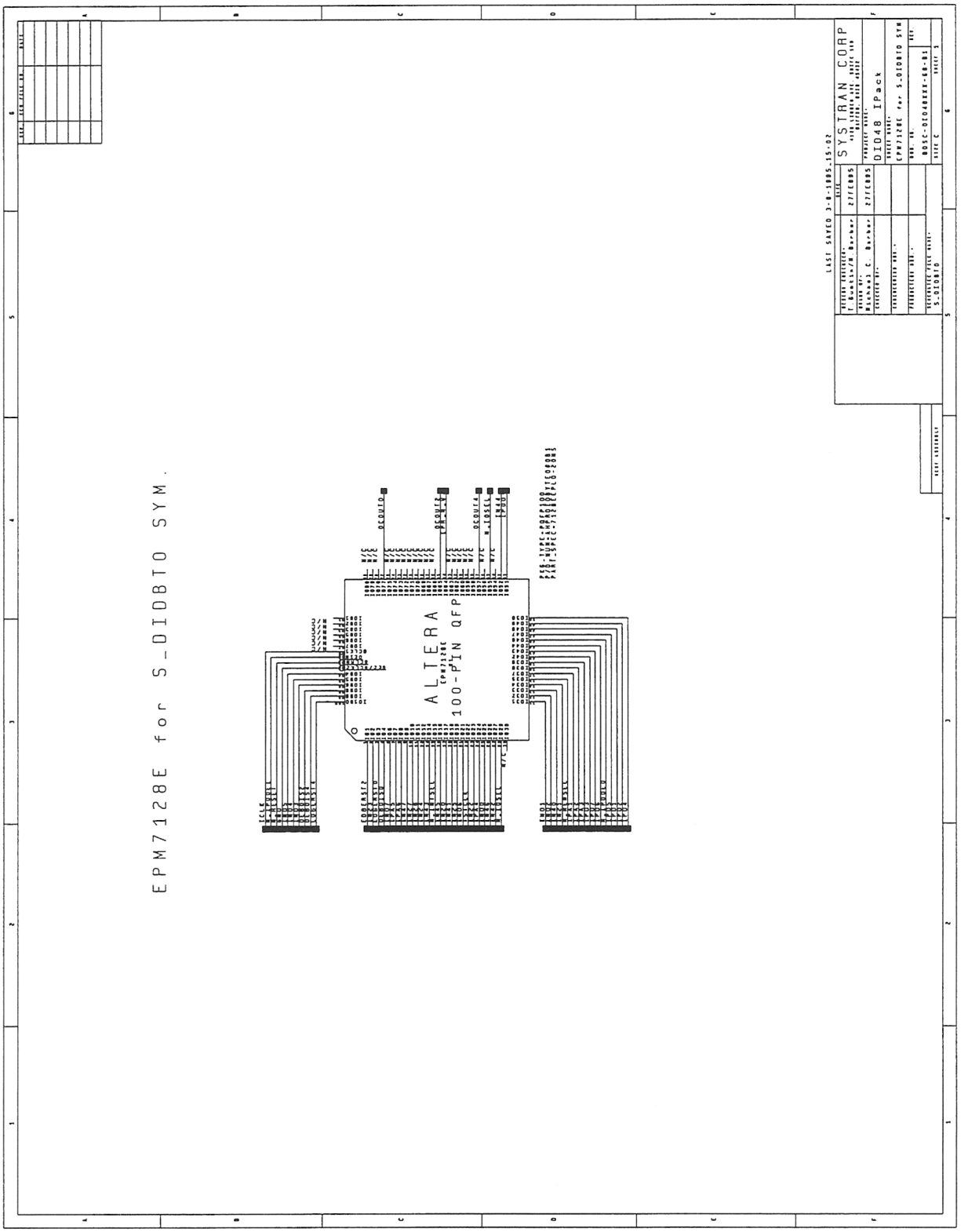

Figure B-6 Schematic #6