IPLBB

IP Module Logic Bus Breakout Board User Manual

Document No. B-T-MU-IPLBB###-A-0-A2

FOREWORD

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FCC

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CE

Please note: As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for the SYSTRAN ANSI/VITA 4-compatible Logic Bus Breakout Board (IPLBB), part number BHAS-IPBB.

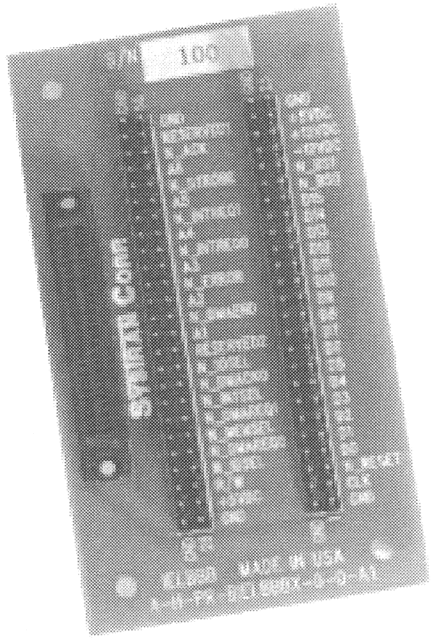

Figure 1-1 IPLBB

1.2 Scope

This reference manual covers the physical and operational description of the IPLBB designed to provide physical access to singlewide IP Module Logic Bus Signals. The reader should have a systems level understanding of general computer processing, memory and hardware operation, and a systems understanding of the IP Module Logic Bus Interface.

1.3 Overview

The SYSTRAN IP Module Logic Bus Breakout Board (IPLBB) provides physical access to singlewide IP Module Logic Bus signals. The IPLBB is used in conjunction with other SYSTRAN IP Module products like the IP Module Logic Bus Extender Boards, via a 50-position ribbon cable, to form a user friendly IP Module system integration package.

IP Modules manufacturers or system integrators using IP Modules in their systems can use the IPLBB to monitor all IP Module Logic Bus transfer types for system integrity, IP Module board response, and carrier board performance. The IP Module Logic Bus signals are accessed on the J2 and J3 header connectors extended from the J1 connector. By using a logic analyzer or oscilloscope, any of the IP Module Logic Bus signals can easily be accessed.

Using the IPLBB will significantly shorten the design to production cycle for companies developing or upgrading new IP Module products. The IPLBMHP was designed in accordance with ANSI/VITA 4-1995 American National Standard for IP Modules, but the IPLBMHP itself, is not an IP Module..

1.4 IPLBB Details:

- Mechanical Interface: Singlewide IP Module Connector and two 50-position Header Connectors
- Electrical Interface: Singlewide IP Module Logic Bus Extension
- IP Module Transfer Types: Access to Memory, I/O, ID, and Interrupt

1.5 IPLBB Specifications:

- Board size: 3.50 x 2.00 x 0.303 inches

1.6 IPLBE Accessories:

- 50-position Ribbon Cable
  - 3-foot length (BHAS-50PRC3)*
  - 6-foot length (BHAS-50PRC6)*
- IP Module Bus Extender Cable
  - 18-inch length (BHAS-IPBEC18)*
  - 24-inch length (BHAS-IPBEC24)*
- IP Module Logic Bus Extender Board
  - Type I (BHAS-IPBE1)*
  - Type II (BHAS-IPBE2)*
- IP Module Bus Monitor Board (HPLA) (BHAS-IPBMHP)*
- Logic Analyzer Configuration Software (BSUT-IPBMHP)*

* SYSTRAN part/order numbers

1.7 Related Publications

IP Module Logic Bus Extender Board User Manual published by SYSTRAN Corp.
(Doc number: B-T-MR-IPLBE)

IP Module Logic Bus Monitor Board User Manual (for HP 1650/16500 series)
(Doc number: B-T-MU-IPBMHP)

1.8 Reliability

SYSTRAN Corporate policy is to provide the highest quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

SYSTRAN has developed a Quality System which conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard is the most comprehensive of the conformance standards, in that it addresses all 20 clauses of the ISO quality system requirements.

SYSTRAN's Quality System addresses the following basic quality objectives:

- Achieve, maintain and continually improve the quality of SYSTRAN products
- Improve the quality of its own operations to meet the needs of SYSTRAN customers and stakeholders
- Provide confidence internally that quality is being fulfilled, maintained and improved
- Provide confidence to the customer and other stakeholders that requirements for quality will be achieved in the delivered product.

SYSTRAN's Quality System was assessed by BSI QA, which is the certification division of British Standards Institution, the largest and most respected standardization authority in the world. SYSTRAN's Quality System was found to meet or exceed the international

standards in all areas, and Certificate of Registration number FM 31468 was issued to SYSTRAN on May 16, 1995.

The scope of SYSTRAN's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's program of continuing assessment, under which an audit of the quality system is performed by BSI QA every six months.

An integral part of meeting SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems using SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

1.9 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct questions not satisfactorily answered by this document, or concerns about the functional-fit of this product for your particular application, or programming questions, to the factory at **(937)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

1.10 Ordering Process

If you wish to learn more about SYSTRAN products or to place an order, the following contacts are available:

Phone: **(937) 252-5601**
E-mail address: **info@systran.com**
World Wide Web address: **http://www.systran.com**

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2.0 HARDWARE INSTALLATION

2.1 Unpack the IPLBB

The IPLBB shipping package will contain the following:

Table 2-2-1 IPLBB Shipping Package Contents

Qty	Description
1	IPLBB Printed Circuit Assembly

2.2 Visually Inspect the IPLBB

Examine the IPLBB to determine if any damage occurred during shipping.

2.3 IPLBB Installation

NOTE: Although the IPLBB is not an ESD sensitive product, acceptable ESD practices should be used during the assembly and installation to protect the IP Module boards and carrier boards.

The IPLBB installation requires the following tools:

Table 2-2-2 IPLBB Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.

The IPLBB is used in conjunction with other SYSTRAN IP Module products like the IP Module Logic Bus Extender Boards, via a 50-position ribbon cable, to form a user friendly IP Module system integration package.

Figure 2-1 shows the connections for installing the IPLBB with an IPLBE on a VME IP Module carrier. Figure 2-2 shows the connections for installing the IPLBB with an IPLBE on an ISA IP Module carrier. Table 2-3 reflects the IPLBB pin assignments, Table 2-4 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Refer to the IP Module Carrier board user's manual for more information.

Refer to Figures 2-1 and 2-2, and Tables 2-3 and 2-4 as appropriate to perform the following steps. The steps with an asterisk (*) are optional.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the IPLBB can be made.
3. Remove the IPLBE and IPLBB from the shipping packages and place them on the ESD bench.

3a.*Install the four hex standoffs onto the IPLBE IP Module connectors with four M2x5mm flat head machine screws.

4. Install the target IP Module board on the IPLBE by applying adequate and equal pressure to the IP Module board at both ends.

4a. *Install four M2x5mm flat head machine screws onto the IP Module's IP Module connectors.

5. Install the 50-position ribbon cable to J1 of the IPLBE.
6. Install the IPLBE with the IP Module board and 50-position cable onto the carrier board by applying adequate and equal pressure to the IPLBE board at both ends.

6a. *Install four M2x5mm flat head machine screws onto the IP Module carrier's IP Module connectors.

7. Install the 50-position ribbon cable to J1 of the IPLBB.
8. Connect Logic Analyzer Pod connections or oscilloscope probes to the desired signals to be monitored on the IPLBB J2 and J3 connectors.

This completes the installation of the IPLBB to the carrier board.

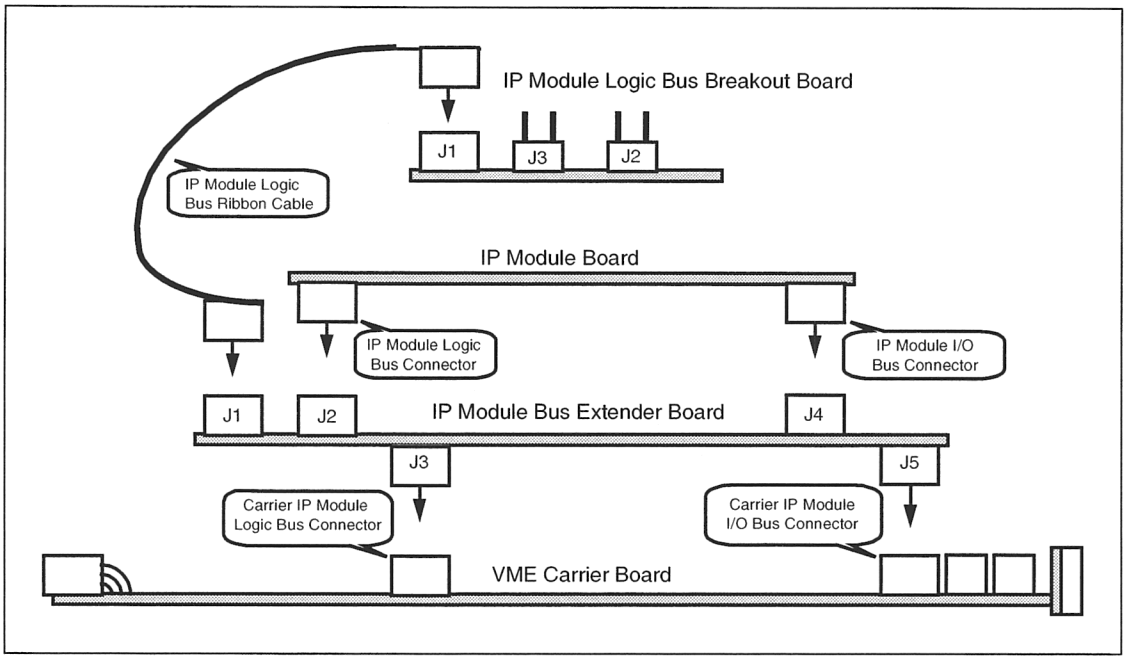

Figure 2-1 IPLBB/IPLBE Assembly Diagram for a VME Carrier Board

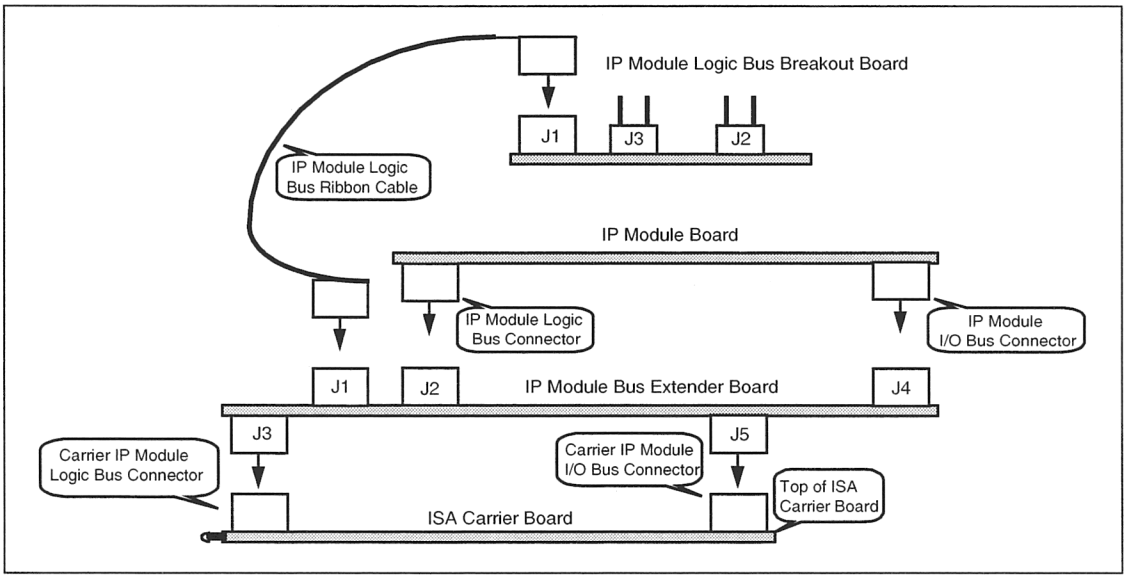

Figure 2-2 IPLBB/IPLBE Assembly Diagram for an ISA Carrier Board

Table 2-2-3 IPLBB Pin Assignments

J3			J2		
GND	**PIN #**	**IP Module Signal**	**GND**	**PIN #**	**IP Module Signal**
Gnd	50	GND	Gnd	25	GND
Gnd	49	RESERVED	Gnd	24	+5VDC
Gnd	48	N_ACK	Gnd	23	+12VDC
Gnd	47	A6	Gnd	22	-12VDC
Gnd	46	N_STROBE	Gnd	21	N_BS1
Gnd	45	A5	Gnd	20	N_BS0
Gnd	44	N_INTREQ1	Gnd	19	D15
Gnd	43	A4	Gnd	18	D14
Gnd	42	N_INTREQ0	Gnd	17	D13
Gnd	41	A3	Gnd	16	D12
Gnd	40	N_ERROR	Gnd	15	D11
Gnd	39	A2	Gnd	14	D10
Gnd	38	N_DMAEND	Gnd	13	D9
Gnd	37	A1	Gnd	12	D8
Gnd	36	RESERVED	Gnd	11	D7
Gnd	35	N_IOSEL	Gnd	10	D6
Gnd	34	N_DMACK0	Gnd	9	D5
Gnd	33	N_INTSEL	Gnd	8	D4
Gnd	32	N_DMAREQ1	Gnd	7	D3
Gnd	31	N_MEMSEL	Gnd	6	D2
Gnd	30	N_DMAREQ0	Gnd	5	D1
Gnd	29	N_IDSEL	Gnd	4	D0
Gnd	28	R/W	Gnd	3	N_RESET
Gnd	27	+5VDC	Gnd	2	CLK
Gnd	26	GND	Gnd	1	GND
J3 Signals			**J2 Signals**		

Table 2-4 IP Module Logic Bus Pin Assignments

Original IP Module Signal Names	IP Module Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

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3.0 USING THE IPLBB

3.1 Purpose

This section describes the use of the IPLBB in a debugging/troubleshooting or systems integration environment.

3.2 How To Use The IPLBB

IP Module manufacturers or companies using IP Modules in their systems can use the IPLBB with an IPLBE via the 50-position ribbon cable to monitor the IP Module signals for system integrity of all the IP Module Logic Bus transfer types. Figure 3-1 describes logic analyzer or oscilloscope probe connections for monitoring any of the IP Module Logic Bus signals via the header connectors on the IPLBB (Also refer to Figure 2-3 for the IPLBB pin assignments).

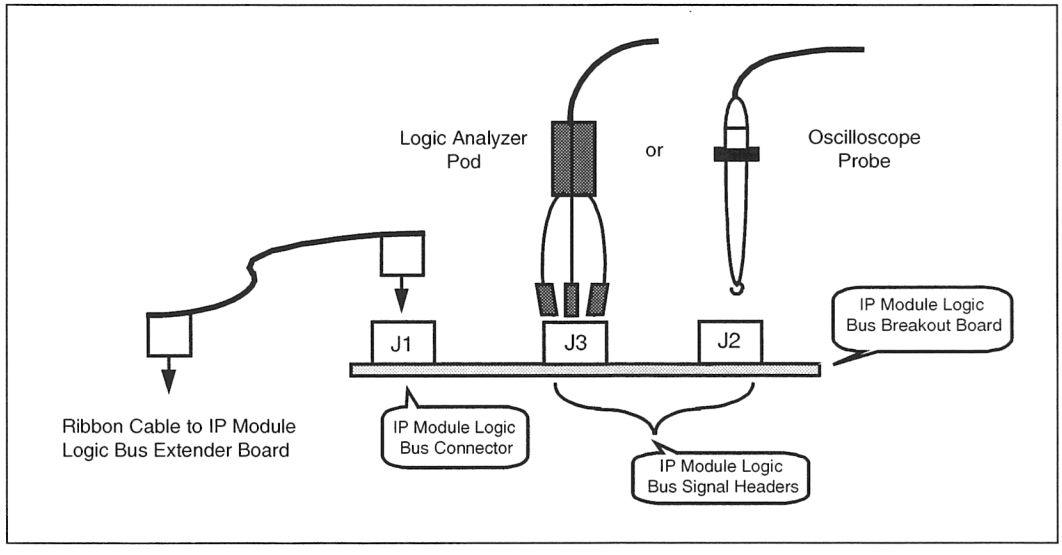

Figure 3-1 IP Module Logic Analyzer or Oscilloscope Probe Connections

The IPLBB gives IP Module users the ability to quickly and easily monitor specific IP Module transfer cycles for IP Module board prototyping through alpha and beta board testing. Using the IPLBB will significantly shorten the design to production cycle for companies developing or upgrading new IP Module products.

For systems integration companies using IP Modules, the IPLBB is a usefull tool for providing information like IP Module board response or carrier board performance. This type of IP Module logic bus monitoring is made much easier by using the IPLBE.

3.3 IPLBB IP Module Signal Specifications

Timing measurements were conducted using the HP model 16500A Logic Analyzer with a 400 megasamples per second Digitizing Oscilloscope Module, model 16530A, plugged into slot E. Figures 3-2 through 3-7 show the IPLBB's negligible affect on the IP Module Logic Bus signals making the IPLBB a very effective and non-intrusive troubleshooting aid in IP Module integration.

Figures 3-3 and 3-4 shows typical rising and falling edges of the IP Module 8MHz Clock measured on the SYSTRAN TRIDO48 IP Module board (BHAS-TRIDO48) mounted on a Motorola MVME-162-23 IP Module Carrier board without the IPLBE and IPLBB. Figures 3-5 and 3-6 shows the same IP Module Clock edges with the Type 1 version of the IPLBE and IPLBB installed on the MVME-162-23. Figures 3-7 and 3-8 show typical IP Module Data Bit 0 signal drive without and with the IPLBE and IPLBB installed, respectively. The following summary is derived from this data:

Table 3-1 IPLBE Timing Measurements

Signal/Edge	Without	With	IPLBB & IPLBE Installed Differences
8 MHz ICLK/Rising	6.80 ns	12.80 ns	+6.00 ns
8 MHz ICLK/Falling	8.00 ns	11.80 ns	+3.80 ns
IPD0/Falling	11.00 ns	17.60 ns	+6.60 ns

NOTE: All of the above measurements were made on the IP Module Logic Bus connector Pin #2 for the 8 MHz Clock and Pin #4 for IPD0.

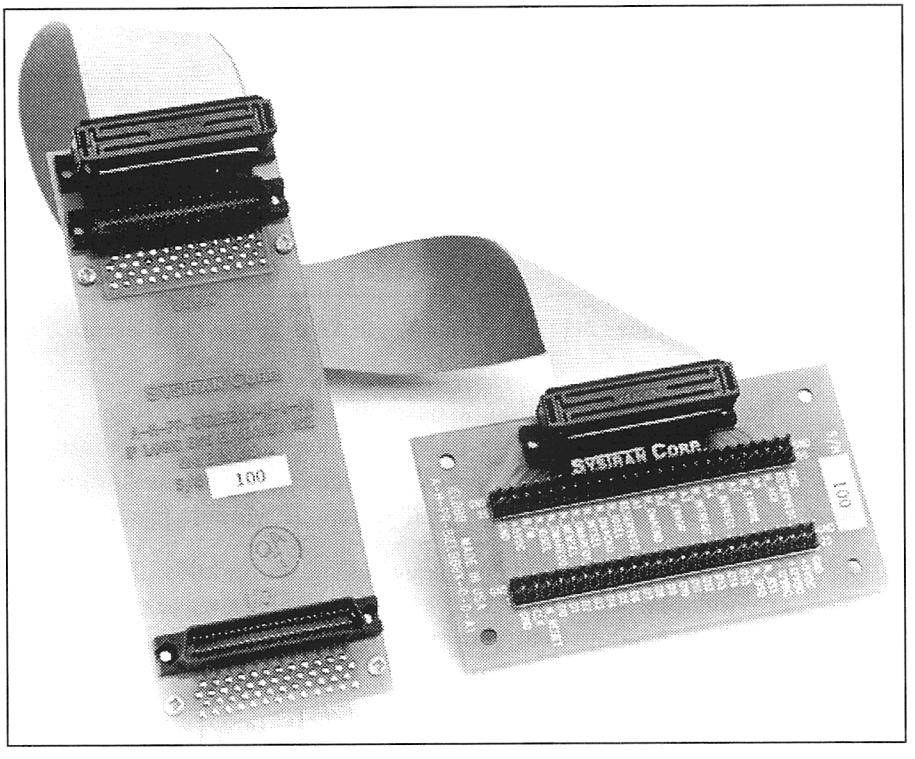

Figure 3-2 IPLBE, Type 1 and IPLBB on 18" Bus Extender Cable

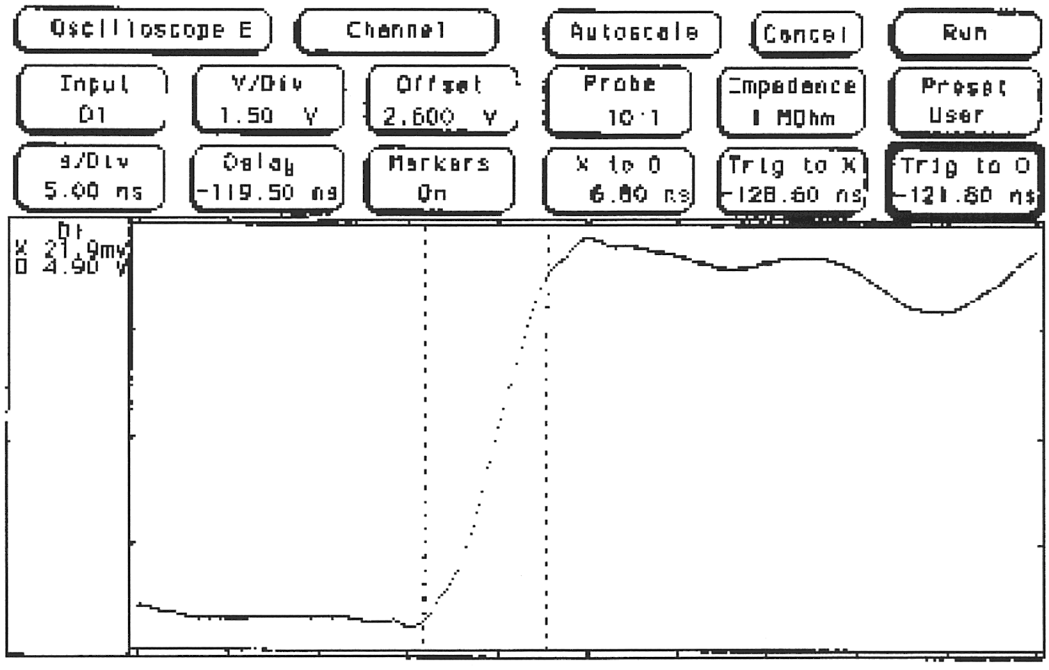

Figure 3-3 IP Module 8 MHz Clock (Rising Edge) Without IPLBB Installed

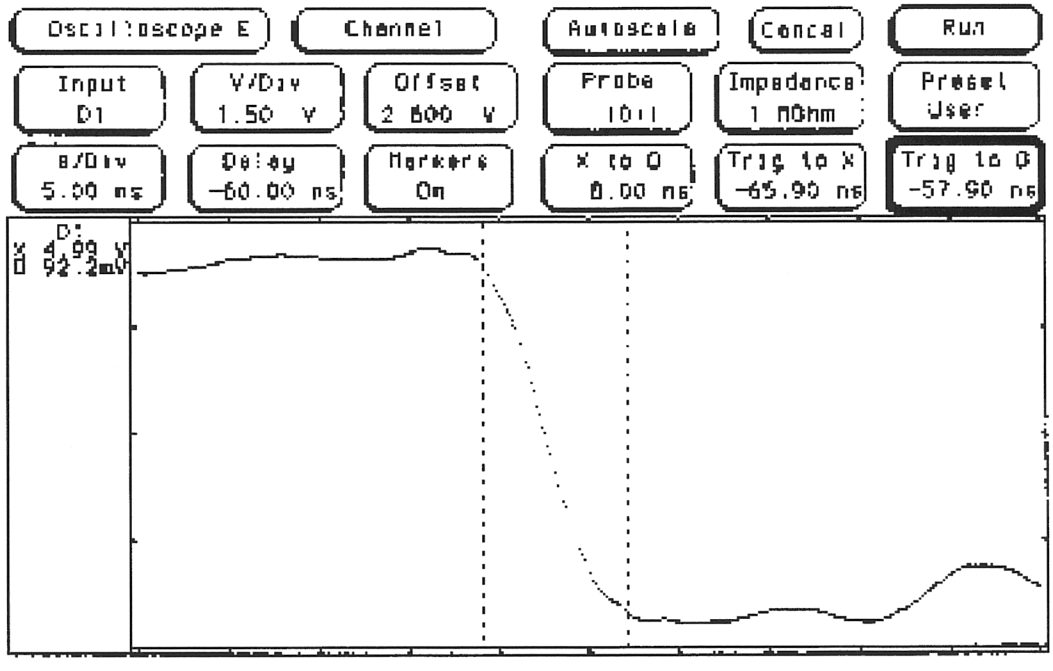

Figure 3-4 IP Module 8 MHz Clock (Falling Edge) Without IPLBB Installed

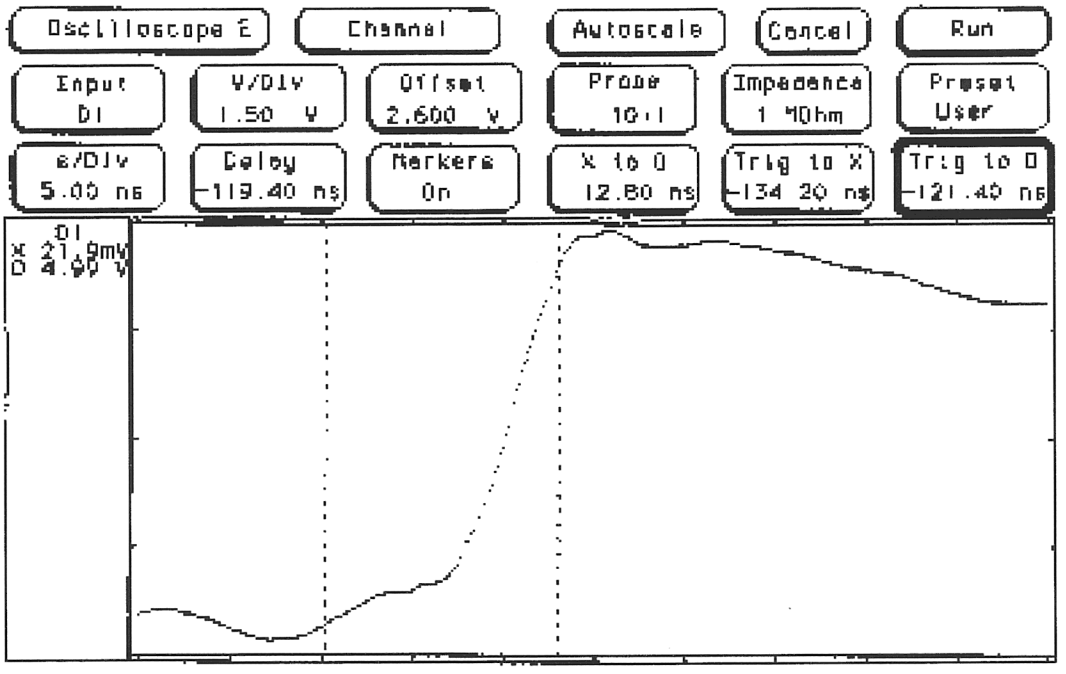

Figure 3-5 IP Module 8 MHz Clock (Rising Edge) With IPLBB and IPLBE, Type 1

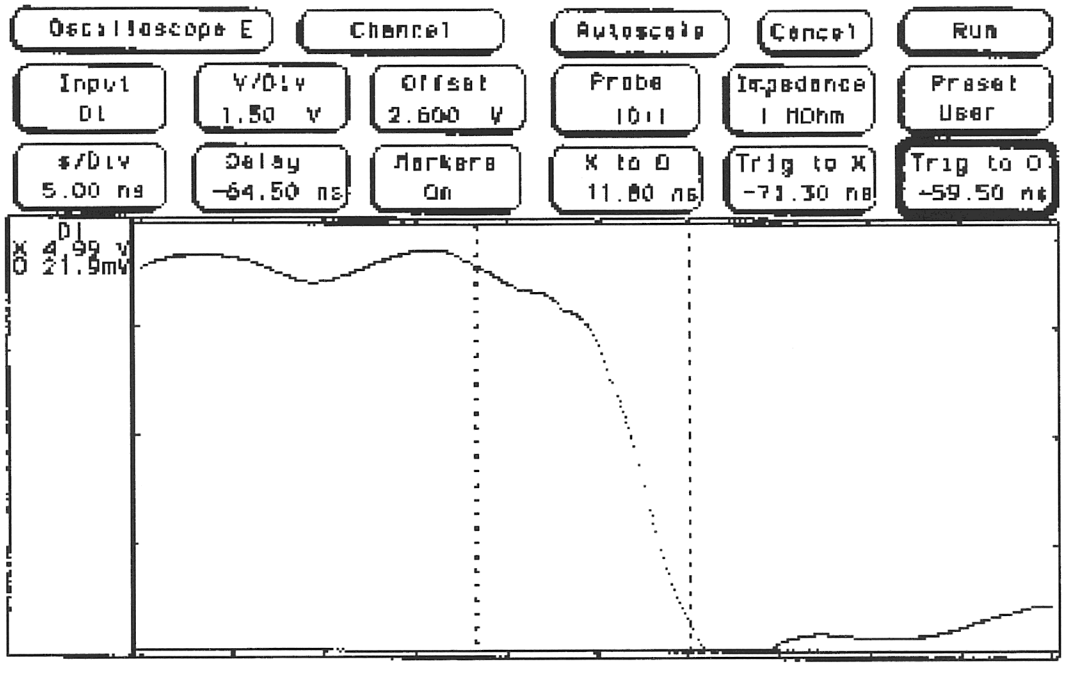

Figure 3-6 IP Module 8 MHz Clock (Falling Edge) With IPLBB and IPLBE, Type 1

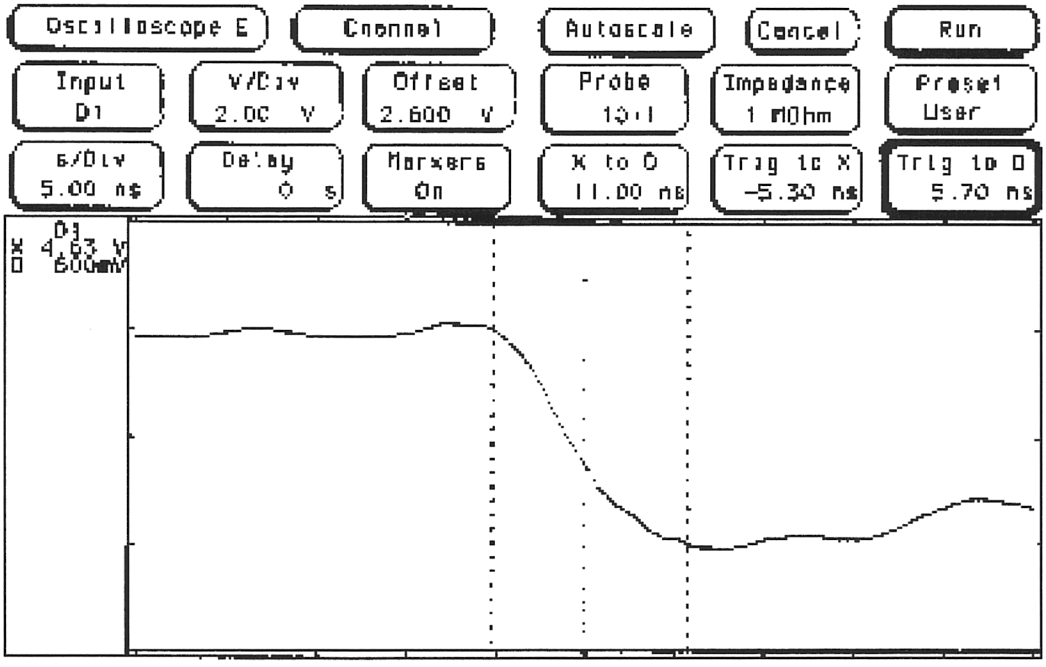

Figure 3-7 IP Module Data Bit 0 Without IPLBB

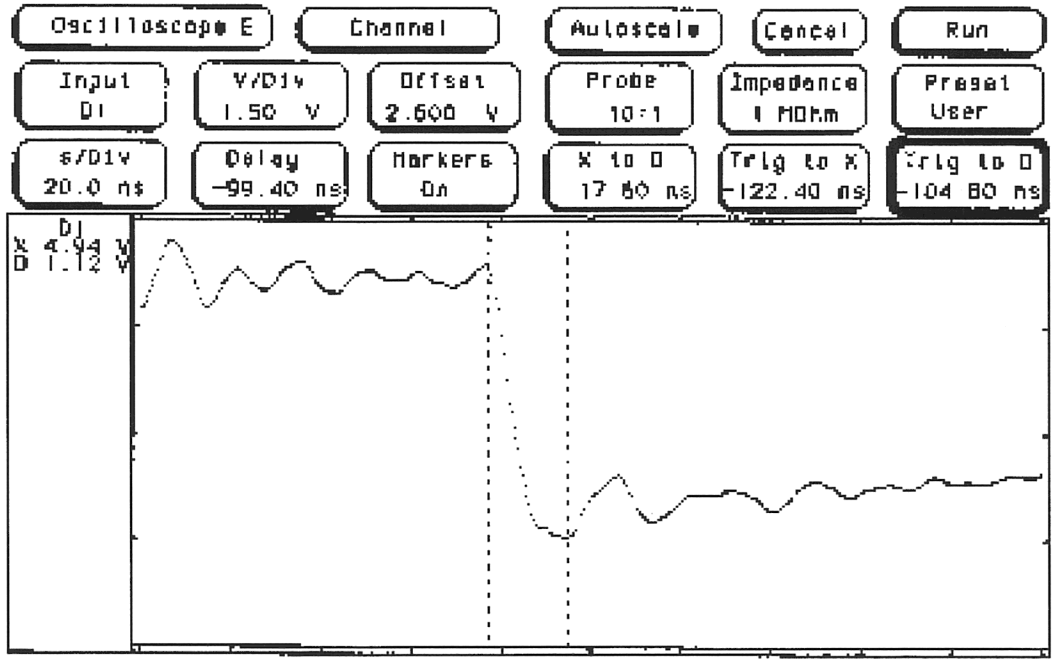

Figure 3-8 IP Module Data Bit 0 With IPLBB and IPLBE, Type 1

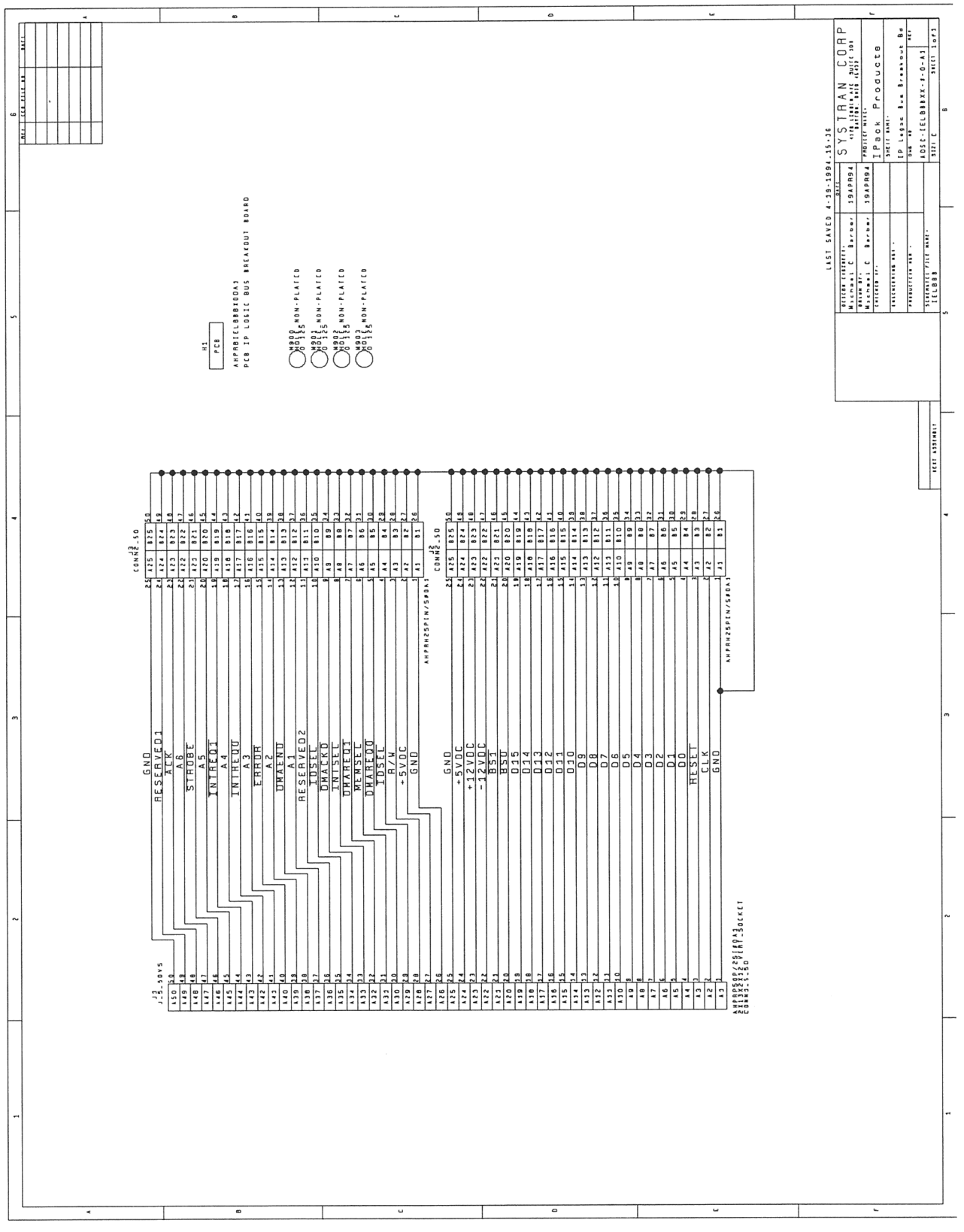

Figure 3-9 IPLBB Schematic Sheet