LOW40 - 40 Channel High Power Low-Side Driver Board

USER MANUAL

Document No. B-T-MU-LOW40###-A-0-A1

FOREWORD

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SYSTRAN makes no warranty of any kind with regard to this printed material including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose.

The schematic diagrams contained in this publication are included for reference only. The information was current at the time the printed circuit board was last revised. This information is not necessarily current or complete manufacturing data, nor is it part of the product specification. Schematics may not be reproduced without the express permission of SYSTRAN Corp.

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane. 8-bits of a data bus on octal boundaries.

CAE. Computer Aided Engineering.

doublewide. An IPack module that is twice the size of the singlewide board.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IndustryPack. Credit-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O. Input/Output.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 8 Mbytes/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6-bit wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IPack module.

IPDbus. IPack Data Bus.

MTBF. Mean Time Between Failures.

ns, µs, ms. Nanoseconds, Microseconds, and Milliseconds respectively.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for Systran's 40 channel high power low-side driver IndustryPack (also called IPack) board, herein referred to as the LOW40 (part number BHAS-LOW40).

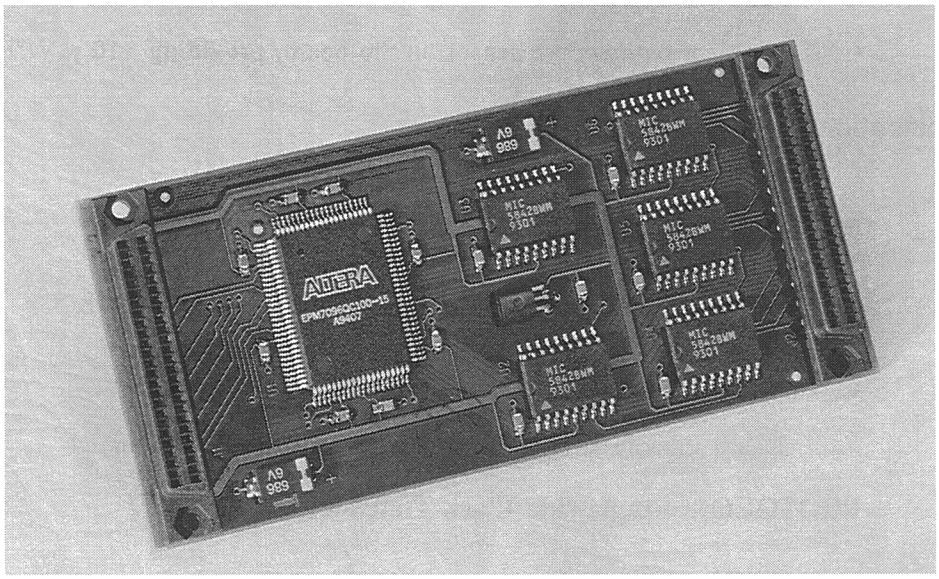


Figure 1-1 LOW40 Board

1.2 Scope

This reference manual covers the physical and operational description of the LOW40, both from hardware and software perspectives. This reference manual also contains detailed technical information about the LOW40's performance characteristics, and a few typical applications. It is assumed that the reader has a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks on a carrier(s) of choice. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The LOW40 is a singlewide IPack board, conforming both mechanically and electrically to the *IndustryPack Logic Interface Specification, Revision 0.7.1.* For a typical IPack carrier that holds four IPacks , it can provide up to 160 channels of low-side drivers for a single slot on a computer bus backplane, or be mixed with other IPacks for a more customized, modular I/O system solution.

1.3.1 Features

- Per byte-lane 8 channels of low-side (open-collector) drivers
- Minimum breakdown voltage ratings of 80 V (50 V sustaining) @ up to 500 mA per channel (See Table 2-2)
- Board-level emitter commons all brought out to 8 pins of the I/O connector
- Per-channel transient diode cathode commons brought out to the I/O connector
- Per byte-lane output enabling via host software
- Ambient temperature sensor on the board, providing +10 mV/°F output

1.4 Specifications

MECHANICAL: Singlewide IPack

- Measurements: 1.8000″ x 3.900″ x 0.303″ (above board), 4.572 x 9.906 x 0.770 cm
- Weight: 0.976 oz., 27.67 grams
- Board thickness: 0.062″, 0.157 cm, nominally, (4 layer)

PROTOCOL: Singlewide IPack Transfers

- 8 MHz clock rate
- No wait cycles on any transfer types
- Hold cycles supported on all valid transfer types
- Complete (no partial) address decoding
- I/O transfers: 8-, 16-bit writes, 16-bit reads
- Four, 16-bit I/O locations:
  - 3 for ports
  - 1 for control
  - Maximum read/write rate: 4 MTransfers/second, sustained
- ID transfers: 8-bit read (only)
  - Zero-fill on upper byte
  - Twelve bytes, including CRC
  - Systran's manufacturer's ID = 45 *hex*, = E *ASCII*
  - LOW40's model number = 67 *hex*, = g *ASCII*
  - Cyclic Redundancy Check value = 60 *hex*

  - Maximum read rate: 4 MTransfers/second, sustained
- Memory transfers: not supported
- Interrupt Vector transfers: not supported
- Interrupt requests: none generated
- DMA activity: none supported
- No acknowledgement on unsupported transfer attempts:
  - Memory read and write, Interrupt read, ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

- All registers power up as all 0's (I/O read of all 0's — '0000' *hex*)
- No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

- Power: +5 Vdc @ 87 mA (typical no load)

PERFORMANCE CHARACTERISTICS

- Electrical Characteristics: Refer to Section 5.0: PERFORMANCE

ABSOLUTE MAXIMUM RATINGS

- Supply voltage with respect to ground: −0.3 V minimum, +5.55 V maximum

RECOMMENDED OPERATING CONDITIONS

- Supply voltage: +4.75 V → +5.25 V
- Logic Interface: IndustryPack specification compliant carrier
- Environmental: see below

ENVIRONMENTAL SPECIFICATIONS

- Temperature (Operating): 0°C to +70°C
- Temperature (no bias, storage): −65°C to +150°C
- Humidity (Non-condensing): 5% to 95%
- Vibration (Operating): 15 G's RMS (10→55 Hz)
- Shock (Operating): 50 G's maximum
- Altitude (Operating): 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

- 1,702,417 hours per MIL-HDBK-217F

1.5 Related Products

- Software: 'C' library and OS-9® device driver routines with documentation.
- ATE: Automatic Test Equipment Software/Hardware Package, with CASE based design/analysis.

1.6 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This Synopsis is included in this document as Appendix A).
- SYSTRAN I/O Products Technical Note #2001 titled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1).
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by Greenspring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.7 Ordering Process

To order SYSTRAN products, call (513) 252-5601. For additional product information you may call the above number, or send an E-Mail message to **info@systran.com** to place an order.

1.8 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct any programming questions, any concerns about the functional-fit of this product for your particular application, or any questions not answered satisfactorily by this document, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance.

Refer to Section 7.0 for warranty and repair information.

1.9 Reliability

SYSTRAN Corporate policy is to provide the highest-quality products in support of customer's needs. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. The SYSTRAN commitment to quality begins with product concept, and continues after receipt of the purchased product.

An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

2.0 DESCRIPTION

NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in the "IndustryPack Logic Interface Specification Synopsis" included as Appendix A.

2.1 Block Diagram Description

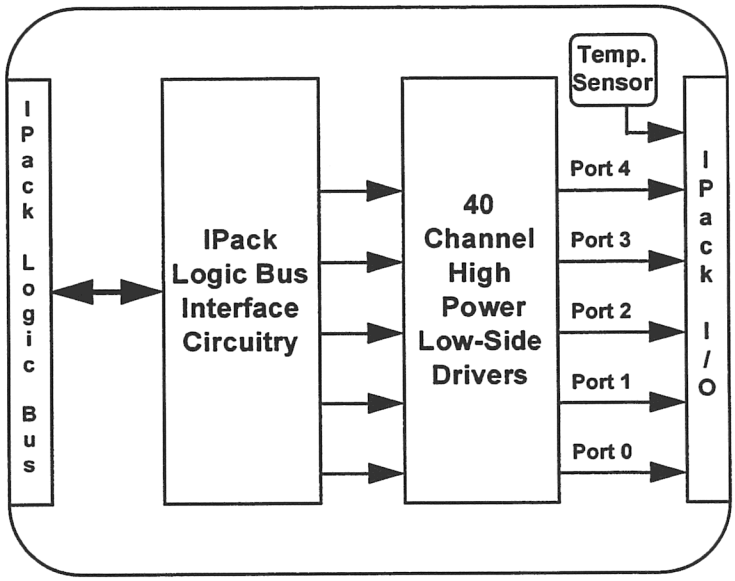


Figure 2-1 LOW40 Simplified Block Diagram

Figure 2-1 is a simplified block diagram of the LOW40. On the left side is the IPack's Logic Bus connector through which all transfers between the IPack carrier and the LOW40's registers and data sources are conducted. The block labeled "IPack Logic Bus Interface Circuitry" contains all of the write/read-back data registers, the ID "PROM" data, control (output enable) register, serial data stream engine for driver inputs, and IPack transfer sequence/control and data bus interface logic. All of this logic is implemented in one EPLD. The block labeled "40 Channel High Power Low-Side Drivers" contains the five 8-bit serial latched drivers, implemented with individual logic devices, housed in wide small outline integrated circuit packages (SOIC). The block labeled "Temp. Sensor" is the precision ambient fahrenheit temperature sensor. On the right side is the LOW40's I/O connector, providing sink currents for all 40 discrete lines, ground and cathode references, and the single-temperature sensor signal line.

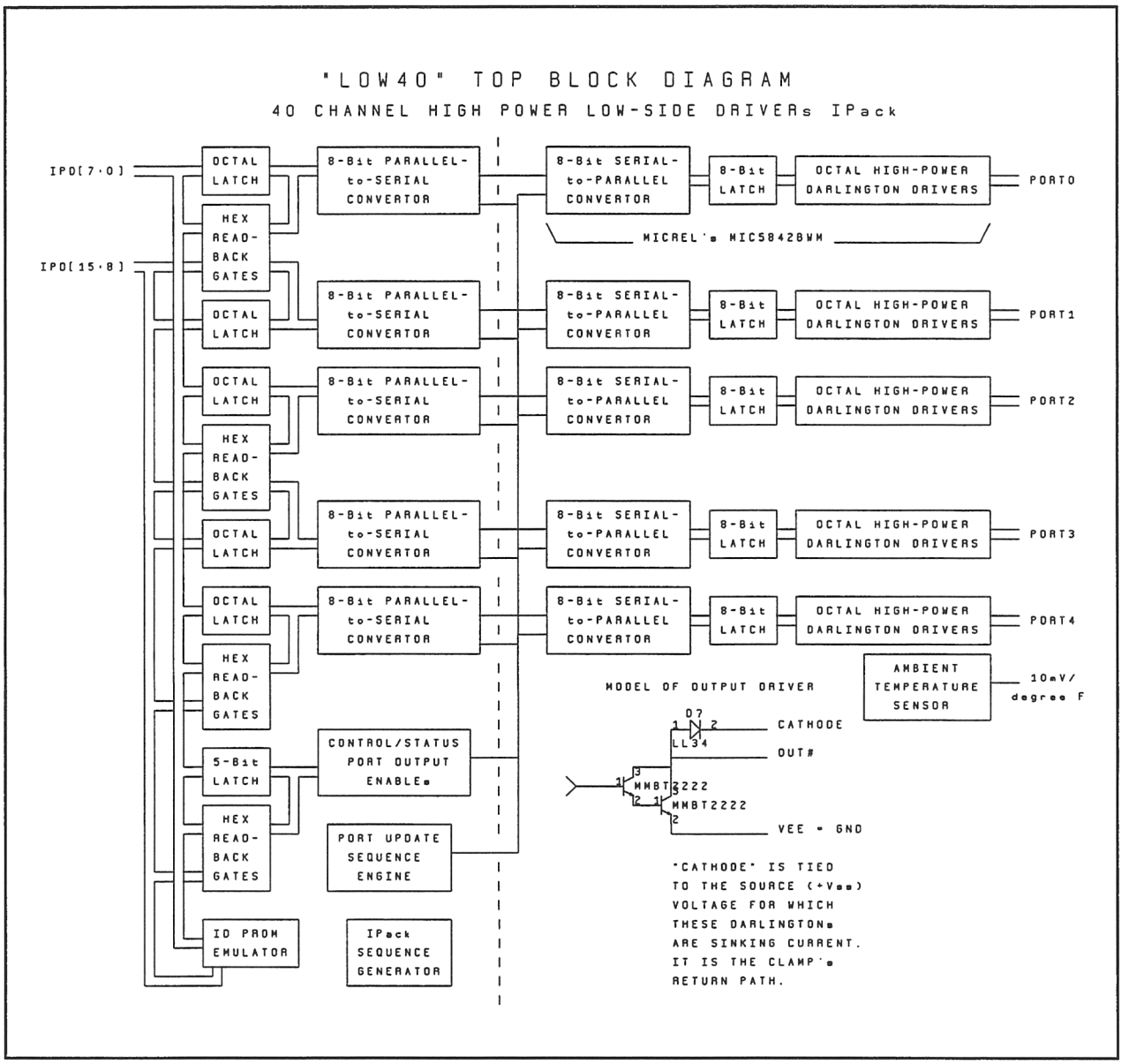


Figure 2-2 LOW40 Detailed Block Diagram

Figure 2-2 presents a detailed block diagram of the LOW40. Again, on the left side of the vertical dotted line is the IPack's Logic Bus interface through which all host carrier transfers take place. The five 8-bit ports are paired-off into three 16-bit "words". Each "word" contains two 8-bit registers, a 16-bit tristateable gate for driving the IPDbus during I/O reads. Also in the Logic bus interface there is an 8-bit serial driver port that directly feeds each of the low-side output driver MIC5842BWM's. The architecture supports byte-writes to either octal register, or to both as 16-bit writes. All I/O register reads are performed at the "word" width of 16-bits, only.

The control register has a similar IPack carrier interface, lacking the octal tristate gate interface. Its function is to register the output enable control signals for each port.

The ID PROM Emulator is the circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero-fills, during the ID (read) transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability and its associated Mean Time Between Failures (MTBF) value.

The sequence control logic performs orderly IPack logic bus transfers between the LOW40 and its carrier, and the power-up state logic for this board.

On the right side of the vertical dotted line are the five octal low-side port drivers that receive the 8-bit serial data from the IPack logic bus interface. The ambient fahrenheit temperature sensor is shown with it's voltage output corresponding to 10 mV/°F. Also a model of the low-side driver outputs (which is a Darlington pair) is shown.

2.2 Detailed Description

NOTE: Refer to the LOW40 schematics located in Appendix B while reading this material since individual components are referenced by functional name, schematic reference designator, or industry-standard device part number.

The LOW40 was developed using VHDL and synthesis, targeted to an Altera EPLD, schematic captured and integrated into standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the schematics and product design material presented in this document.

2.2.1 LOW40 Schematics

For those readers not familiar with the top-down design methodology used, the following is a short travel-map through the schematics of the LOW40. There are three pages that comprise the schematic set.

The first schematic sheet, labeled ADSC-IDLS40T0-67-A1 (sheet 1 of 2) is the top level drawing, composed of the IPack Logic connector (J1), and one large generic block labeled "S_LOW40". The symbol labeled S_LOW40 is the LOW40's Controller module. It is an ALTERA EPLD of the type EPM7096 in a 100-pin plastic quad flat pack with a reference designation of U1.

The second schematic page (sheet 2 of 2) is the top-level drawing of the user's IPack I/O connector (J2), the five 8-bit serial input latched drivers labeled "MIC5842BWM" and have reference designators of U2 - U6, and the ambient temperature sensor labeled "LM34D2" which is U7.

"Pushing-down" into the underlying detailed schematic sheet for the symbol "S_LOW40" is the third sheet of the LOW40 schematic set

2.2.2 LOW40 Components

All IPack Logic Bus transfers take place across J1, the IPack Logic Connector, located on the left side of all block and schematic diagrams. Refer to Appendix A for details about the signals on this connector. Generally speaking, this IPack does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to a short, four location, I/O map.

LOW40 Controller

The LOW40's primary activity "CONTROLLER" is housed within the EPM7096QC100 EPLD located at U1 on the schematics. It serves as the primary IPack transfer sequence engine, whose responsibilities include: detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier; ID PROM emulation data pattern generation for ID read transfers; port output enable control circuitry with power-up default initialization circuits; encoding of registration (for I/O writes) and IPDbus output enable (for I/O reads), and parallel-to-serial conversion of the registered data for each port with strobe, clock, and enable signals.

The Controller's "Parallel-to-Serial" data-handling function consists of five 8-bit write-read-back registers, that converts 8-bit parallel data for each port to serial data. The low-side driver's data update is initiated by an I/O write to any of the five data ports and then updates all five ports simultaneously. The I/O write transfers, after being detected as being valid, consist of any one of four individual byte-wide writes to the first two I/O locations (IPA = 00 and 01 *hex*) or individual byte-wide writes in byte-lane 0 to the next two locations (IPA = 02 and 03 *hex*), or as any one of four double-byte (word, 16-bit) writes, while the read operations are always as full-word accesses.

LOW40 Low-side Drivers

The five byte-wide low-side drivers consist of MIC5842BWM devices in wide SOIC packages, located at (U2-U6) on the schematics. Each port driver contains eight bipolar current-sink Darlington output drivers with a minimum breakdown voltage rating of 80 V (50 V sustaining) at up to 500 mA per channel (1 Amp per 8-bit port). The LOW40's outputs (with integral transient-suppression diodes per channel) are suitable for use with lamps, relays, solenoids, and other inductive loads. The low-side driver outputs and per channel diode cathode and emitter commons connect directly to the I/O connector.

Per byte-lane output enabling is conducted via host software. After power-up or a system reset the output-enable bits default to "disabled", which is a logic '0'. A driver is turned on (output near ground) when both its data bit and control register output-enable bits are logic '1's. Otherwise, the output is off (floating, not sinking current).

2.2.3 MIC5842BWM Low-Side Driver Details

The purpose of this short subsection is to provide some additional background material relating to proper use of this product.

At normal operating conditions of free-air temperature equal 25°C , V_{DD} = 5 V and V_{SS} = V_{EE} = 0 V the maximum collector-emitter saturation voltage V_{CE} (sat) = 1.1 V @ 100 mA I_{OUT} current per channel, and V_{CE} (sat) = 1.3 V @ 200 mA I_{OUT} current.

The following list contains the absolute maximum ratings for the MIC5842BWM low-side drivers at 25°C free-air temperature and Vss=0 V (ground):

Output voltage, V_{CE}	80 V
Output voltage sustained, V_{CE}	50 V
Continuous output current, I_{OUT}	500 mA
Package power dissipation	1.82 W

Table 2-2 shows the maximum allowable duty cycle for the MIC5842BWM low-side drivers.

Table 2-1 Maximum Allowable Duty Cycle

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 5.0 V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	100%	100%
4	100%	100%	100%	100%	100%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

2.2.4 Temperature Sensor Details

The ambient temperature sensor (U7) labeled "LM34DZ" is a precision integrated-circuit temperature sensor, whose output voltage is linearly proportional to the Fahrenheit temperature. This has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from it's output to obtain convenient Fahrenheit scaling. The LM34DZ has ±½°F accuracy (at 77°F) with a linear +10 mV/°F scale factor.

CAUTION: All 40 drivers'cathodes are combined onto a single I/O connector pin. Consequently, all the loads for which the LOW40 is providing sink switching must be powered from the same power source to provide adequate functionality from the diode clamping circuits.

2.2.5 LOW40 Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents that are based on: Fluorine, Chlorine, Aqueous, and Alcohol are safe to use. Do NOT use gasoline or thinner type solvents on this product.

3.0 HARDWARE INSTALLATION

3.1 Unpacking the LOW40

The contents of the LOW40 shipping packages are listed in Table 3-1:

Table 3-1 Contents of LOW40 Shipping Packages

QTY	DESCRIPTION
1	LOW40 Printed Circuit Assembly
1	LOW40 User Manual *

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals up to one per board are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR-LOW40).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visual Inspection of the LOW40

Examine the LOW40 to determine if any damage occurred during shipping.

3.3 LOW40 Installation

NOTE: The LOW40 is an Electrostatic Sensitive Device (ESD), the hardware installation of the LOW40 must be conducted on a good anti-static workbench to protect the IPack and carrier boards. The IPack carrier board must be removed from the host system using good ESD practices and moved to an ESD controlled area where the installation of the LOW40 can be completed.

The LOW40 installation requires the following tools:

Table 3-2 LOW40 Installation Tools

QTY	DESCRIPTION
1	ESD STATIC CONTROL KIT/GROUND STRAP/ETC.
1	STANDARD FLAT HEAD SCREWDRIVER (OPTIONAL)

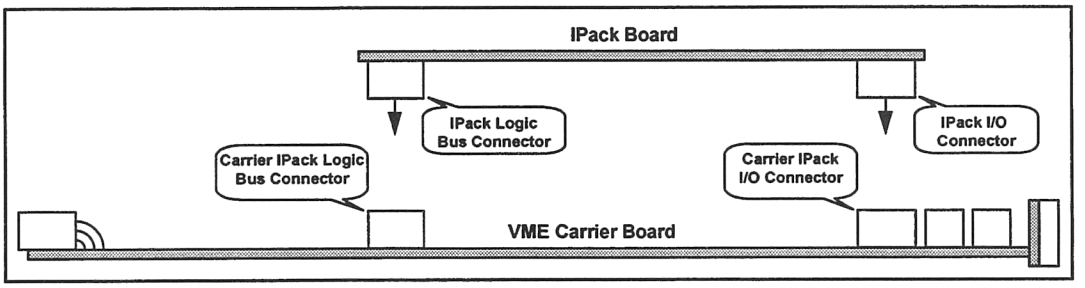


Figure 3-1 Installation of the LOW40 on a VME IPack carrier board.

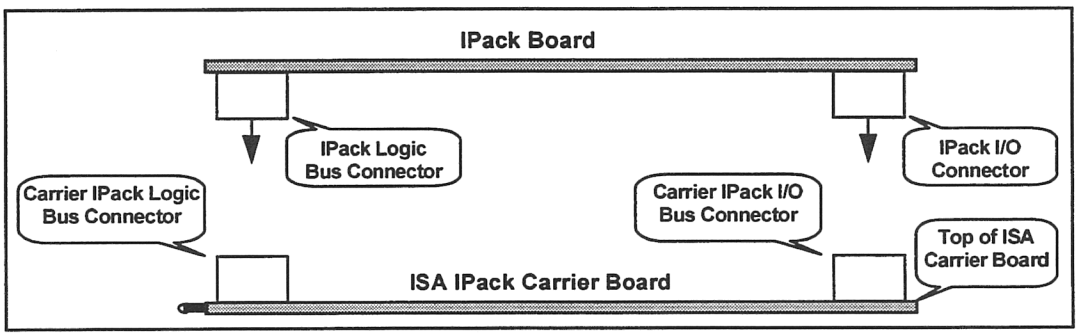


Figure 3-2 Installation of the LOW40 on a ISA IPack carrier board.

Reference Figure 3-1 for the diagram of how the LOW40 is installed on a VME IPack carrier, and Figure 3-2 for installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IPack Carrier board user's manual for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IPack carrier and move it to the ESD controlled area where the installation of the LOW40 can be made.
3. Remove the LOW40 from the shipping package and place it on the ESD bench.
4. Install the LOW40 onto the carrier board by applying adequate and equal pressure to the LOW40 board at both ends.

* 5. Install four M2x5mm flat head machine screws onto the IPack carrier's IPack connectors.

This completes the installation of the LOW40 to the carrier board.

Table 3-3 IPack Logic Bus Pin Assignments

Original IPack Signals Names	IPack Logic Bus Pin #	SYSTRAN Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IPack I/O Connector Pin Assignments

IPack I/O Pin #	Signal Name
50	GND
49	Temperature
48	GND
47	P4B7
46	P4B6
45	P4B5
44	P4B4
43	P4B3
42	P4B2
41	P4B1
40	P4B0
39	GND
38	GND
37	P3B7
36	P3B6
35	P3B5
34	P3B4
33	P3B3
32	P3B2
31	P3B1
30	P3B0
29	GND
28	CATHODE
27	GND
26	P2B7
25	P2B6
24	P2B5
23	P2B4
22	P2B3
21	P2B2
20	P2B1
19	P2B0
18	GND
17	P1B7
16	P1B6
15	P1B5
14	P1B4
13	P1B3
12	P1B2
11	P1B1
10	P1B0
9	GND
8	P0B7
7	P0B6
6	P0B5
5	P0B4
4	P0B3
3	P0B2
2	P0B1
1	P0B0

4.0 PROGRAMMING GUIDE

This section of the manual describes the operation of the LOW40 from the software perspective, detailing the LOW40 registers and providing programming examples. A more detailed description of the hardware can be found in section "2.0 DESCRIPTION" and the application examples sections of this manual.

4.1 Description

The LOW40 is a simple to use 40 channel low-side driver card. The outputs can be software enabled/disabled on byte boundaries. The LOW40 has four 16-bit-wide registers: three data and one control. The data registers may be viewed as either three 16-bit registers or five 8-bit ports (IPA= 02 *hex* has port 4 data in byte-lane 0 and the upper byte-lane 1 (IPD[15:8]) reads as all zeroes). The single control register allows user control of output enable on byte boundaries. Byte writes to any of these registers are non-destructive to adjacent bytes.

4.2 IPack ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IPack to provide "no-wait" read accesses of this information.

NOTE: The ID address space is fully decoded. Therefore, any attempt to access IPA addresses at and above IPA = 0C *hex*, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IPack resides.

The IPack ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table 3-31 is the LOW40 emulated ID Address Space PROM listing:

Table 4-1 LOW40 ID Address Space Listing

IPack ADDRESS	DESCRIPTION	DATA READ
IPA = 00 *hex*	ASCII "I"	49 *hex*
IPA = 01 *hex*	ASCII "P"	50 *hex*
IPA = 02 *hex*	ASCII "A"	41 *hex*
IPA = 03 *hex*	ASCII "C"	43 *hex*
IPA = 04 *hex*	SYSTRAN's ID	45 *hex*
IPA = 05 *hex*	LOW40's Model Number	67 *hex*
IPA = 06 *hex*	Revision Level	30 *hex*
IPA = 07 *hex*	Reserved	00 *hex*
IPA = 08 *hex*	Low Byte Driver ID	00 *hex*
IPA = 09 *hex*	High Byte Driver ID	00 *hex*
IPA = 0A *hex*	Number of Bytes Used	0C *hex*
IPA = 0B *hex*	CRC	60 *hex*

4.3 IPack I/O Address Map

The LOW40's I/O Address Map was designed with efficiently located data and control/status registers in the IPack I/O space (IPA = 00 ⇒ 03 *hex*).

NOTE: The address detector circuitry is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 04 *hex* will result in no acknowledgement and its subsequent bus timeout error on the carrier upon which this IPack resides.

On power-up, all forty (40) data and 5 control bits defined below are cleared to a zero-state. This equates to the outputs being disabled and are a logic-high (near cathode potential) on the I/O connector's port lines.

The first location (IPA = 00 *hex*) is the write-and-read-back Data Register 0 for the output ports 0 and 1. Port 0 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 1 resides on byte lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte lanes simultaneously, and 16-bit reads of both bytes simultaneously.

The second location (IPA = 01 *hex*) is the write-and-read-back Data Register 1 for the output ports 2 and 3. Port 2 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 3 resides on byte lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte-lanes simultaneously, and 16-bit reads of both bytes simultaneously.

The third location (IPA = 02 *hex*) is the write-and-read-back Data Register 2 for the output port 4. Port 4 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 16-bit writes to both byte-lanes simultaneously (with byte-lane 1 data ignored), and 16-bit reads of both bytes simultaneously with the upper byte-lane 1 (IPD[15:8]) read as all zeroes. An 8-bit write to byte lane 1 is not supported, and will result in no acknowledgement and its subsequent bus timeout error.

The fourth location (IPA = 03 *hex*) is the write-and-read-back Control Register for the control and status of the output-enable bits (referred to as CR, and CR bits as CR or CR[:]). There are five (5) functional bits in this CR which are defined as follows. Bits [4:0] are the output enable bits with bit 4 to control Port 4 down to bit 0 for Port 0. When a bit is set to a '1' (logic high) the corresponding output port is enabled, and when it is set to a '0' (logic low) the corresponding output port is disabled. In the CR, bits [15:5] are not used and are read as zeros.

The following table is the LOW40 I/O Address Map and contains the data register:

Table 4-2 LOW40 I/O Address Map

IPack ADDRESS	BYTE-LANE 1	BYTE-LANE 0	DESCRIPTION
IPA = 00 *hex*	Data Port 1	Data Port 0	Data Register 0 = Ports 1 and 0, 8 bits each
IPA = 01 *hex*	Data Port 3	Data Port 2	Data Register 1 = Ports 3 and 2, 8 bits each
IPA = 02 *hex*	[XXXX,XXXX]	Data Port 4	Data Register 2 = Port 4, 8 bits
IPA = 03 *hex*	[XXXX,XXXX]	[XXX] [4:0]	Control Register 0, (CR0) output enables for ports 4 to 0, 0=Disabled, 1=Enabled

X = Not used/don't care

4.4 Word Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table 4-3 Word Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS
BASE + 0	BASE + 0	BASE + 2	IPA = 00 *hex*
BASE + 2	BASE + 2	BASE + 6	IPA = 01 *hex*
BASE + 4	BASE + 4	BASE + A	IPA = 02 *hex*
BASE + 6	BASE + 6	BASE + E	IPA = 03 *hex*
BASE + 8	BASE + 8	BASE + 12	IPA = 04 *hex*
BASE + A	BASE + A	BASE + 16	IPA = 05 *hex*
BASE + C	BASE + C	BASE + 1A	IPA = 06 *hex*
BASE + E	BASE + E	BASE + 1E	IPA = 07 *hex*
BASE + 10	BASE + 10	BASE + 22	IPA = 08 *hex*
BASE + 12	BASE + 12	BASE + 26	IPA = 09 *hex*
BASE + 14	BASE + 14	BASE + 2A	IPA = 0A *hex*
BASE + 16	BASE + 16	BASE + 2E	IPA = 0B *hex*

4.5 Byte Access Address Translation

The following table shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IPack address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table 4-4 Byte Access Address Translation Table

VME BUS ADDRESS	PC-AT BUS ADDRESS	NuBus ADDRESS	IPack ADDRESS	BYTE-LANE*
BASE + 1	BASE + 0	BASE + 3	IPA = 00 *hex*	0
BASE + 0	BASE + 1	BASE + 2	IPA = 00 *hex*	1
BASE + 3	BASE + 2	BASE + 7	IPA = 01 *hex*	0
BASE + 2	BASE + 3	BASE + 6	IPA = 01 *hex*	1
BASE + 5	BASE + 4	BASE + B	IPA = 02 *hex*	0
BASE + 4	BASE + 5	BASE + A	IPA = 02 *hex*	1
BASE + 7	BASE + 6	BASE + F	IPA = 03 *hex*	0
BASE + 6	BASE + 7	BASE + E	IPA = 03 *hex*	1
BASE + 9	BASE + 8	BASE + 13	IPA = 04 *hex*	0
BASE + 8	BASE + 9	BASE + 12	IPA = 04 *hex*	1
BASE + B	BASE + A	BASE + 17	IPA = 05 *hex*	0
BASE + A	BASE + B	BASE + 16	IPA = 05 *hex*	1
BASE + D	BASE + C	BASE + 1B	IPA = 06 *hex*	0
BASE + C	BASE + D	BASE + 1A	IPA = 06 *hex*	1
BASE + F	BASE + E	BASE + 1F	IPA = 07 *hex*	0
BASE + E	BASE + F	BASE + 1E	IPA = 07 *hex*	1
BASE + 11	BASE + 10	BASE + 23	IPA = 08 *hex*	0
BASE + 10	BASE + 11	BASE + 22	IPA = 08 *hex*	1
BASE + 13	BASE + 12	BASE + 27	IPA = 09 *hex*	0
BASE + 12	BASE + 13	BASE + 26	IPA = 09 *hex*	1
BASE + 15	BASE + 14	BASE + 2B	IPA = 0A *hex*	0
BASE + 14	BASE + 15	BASE + 2A	IPA = 0A *hex*	1
BASE + 17	BASE + 16	BASE + 2F	IPA = 0B *hex*	0
BASE + 16	BASE + 17	BASE + 2E	IPA = 0B *hex*	1

*Byte-lane 1 is not applicable for ID space

4.6 Data Register 0 (IPA = 00 *hex*)

This 16-bit read/write register is the data register consisting of the 8-bit-wide ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of '1', and turned off with a bit value of '0'. On power-up, all bits are set to '0'.

Table 4-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pn7 - Pn0 : Port n data bits 7 through 0.
Bit 0 is the least significant bit.

4.7 Data Register 1 (IPA = 01 *hex*)

This 16-bit read/write register is the data register consisting of the 8-bit-wide ports 2 and 3. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of '1', and turned off with a bit value of '0'. On power-up, all bits are set to '0'.

Table 4-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

4.8 Data Register 2 (IPA = 02 *hex*)

This 16-bit read/write register is the data register for the 8-bit-wide port 4. This 8-bit port can also be accessed as a 16-bit register with bits 15 through 8 set as "don't care". When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of '1', and turned off with a bit value of '0'. On power-up, all bits are set to '0'.

Table 4-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	X	P47	P46	P45	P44	P43	P42	P41	P40
R/W	Read as 0's, Writes discarded								RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0

X = Don't care

4.9 Control Register (IPA = 03 *hex*)

This 16-bit-wide read/write register selects the output-enable control. The output-enable control can be selected on 8-bit port boundaries. A bit value of '0' disables the corresponding port's output, and a bit value of '1' enables the port's output.

Table 4-8 Control Register Bit Descriptions

Bit #	Bits 15 to 5	4	3	2	1	0
Bit Name	Not used	P4 0E	P3 0E	P2 0E	P1 0E	P0 0E
R/W	Read as 0's Writes discarded	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0

Table 4-9 OE: Output Enable Control Bits

OE Bit Value	OUTPUT ENABLE SELECTION PER PORT
0	Port outputs disabled
1	Port outputs enabled

4.10 Programming Example

This example illustrates output enable control of the LOW40. Only port 0 is controlled in this example, however, the mechanism is the same for all the ports.

- At power up, the data registers are all cleared (value of '0000').
- At power up, the control register is cleared (value of '0000'). At this point, the outputs are disabled.
- Write 'FF' *hex* to the port 0 data register.
- At this point the outputs are still disabled (drivers off) because the output enable control bit for this port is 0 (disabled).
- Write '0001' to the control register enabling port 0's outputs. At this point the outputs are enabled (drivers on, outputs near ground).
- Write '00' the port 0 data register.
- At this point the outputs are disabled (drivers off) because the data register value of '00' turns off the drivers.
- Write '0000' to the control register to return to the power up state.

5.0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration citied, and do not supplant the maximum and minimum envelopes presented in section 1.0: INTRODUCTION.

5.2 State Timing Diagrams

The state waveforms for Figures 5-2 through 5-6 were made using the HP 1 GHz Timing Master Module and the Systran IPack Logic Bus Extender (IPLBE) with the IPack Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer's screen are active-low, and are represented by a '/' as the first character as opposed to the 'N_' used elsewhere, due to the limited amount of character spacing.

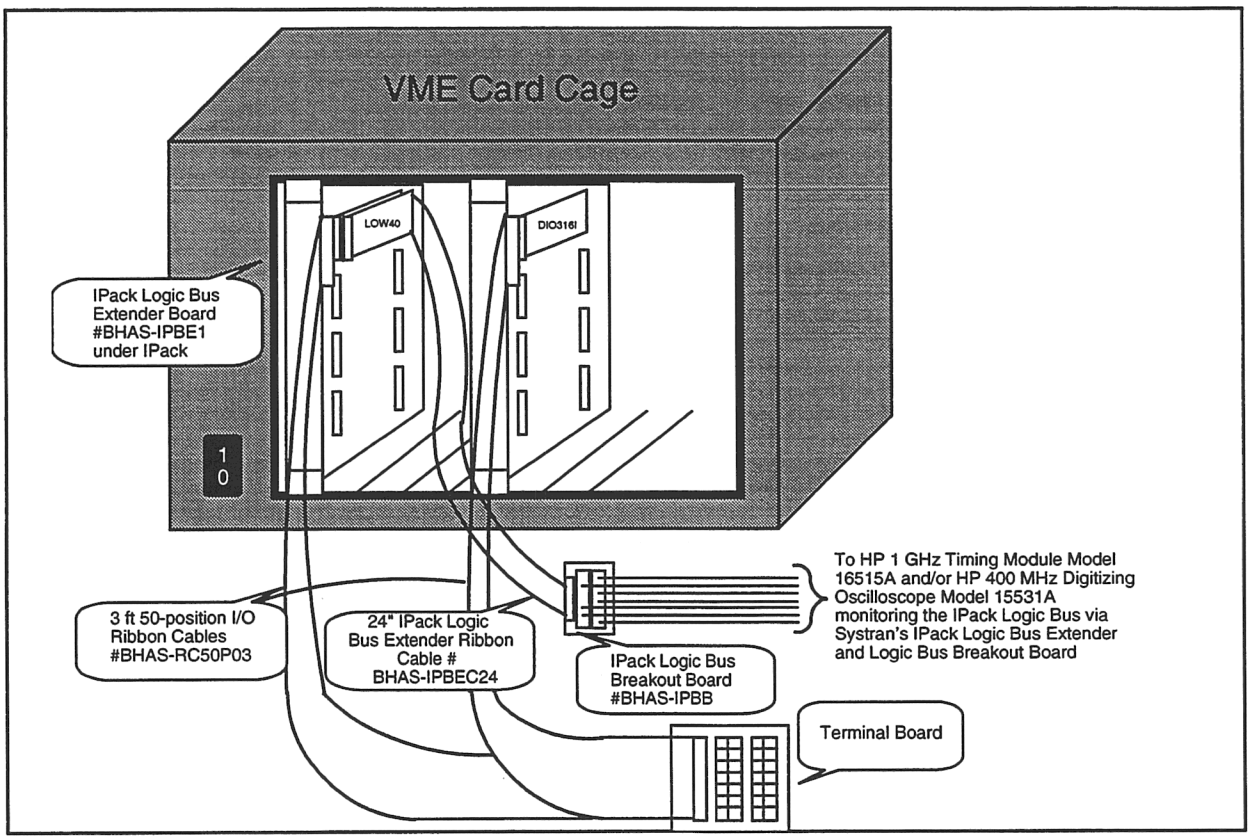


Figure 5-1 IPack Test Configuration for State Timing Measurements

5.2.1 ID Read Cycle

Figure 5-2 is a complete LOW40 ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals.

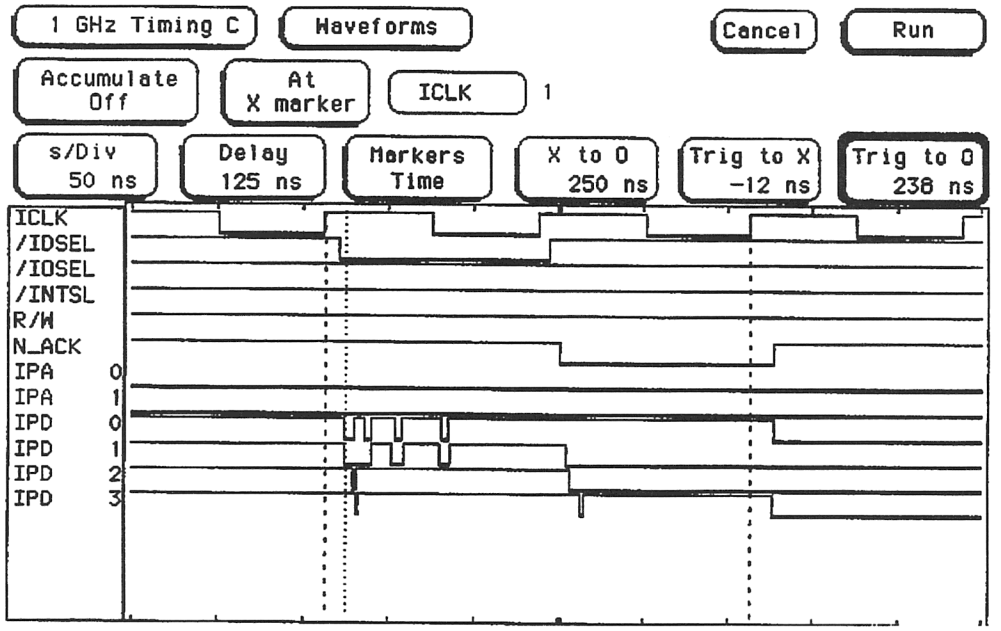


Figure 5-2 Complete LOW40 ID Read Cycle

Figure 5-3 is a zoomed-in view of the LOW40 ID cycle driving the N_ACK and IPD0-3 signals; showing a typical response time of about 18 nanoseconds for driving these signals. The IPack Logic I/F Specification (Rev. 0.7.1, page 35) requires these signals be driven within 40 nanoseconds.

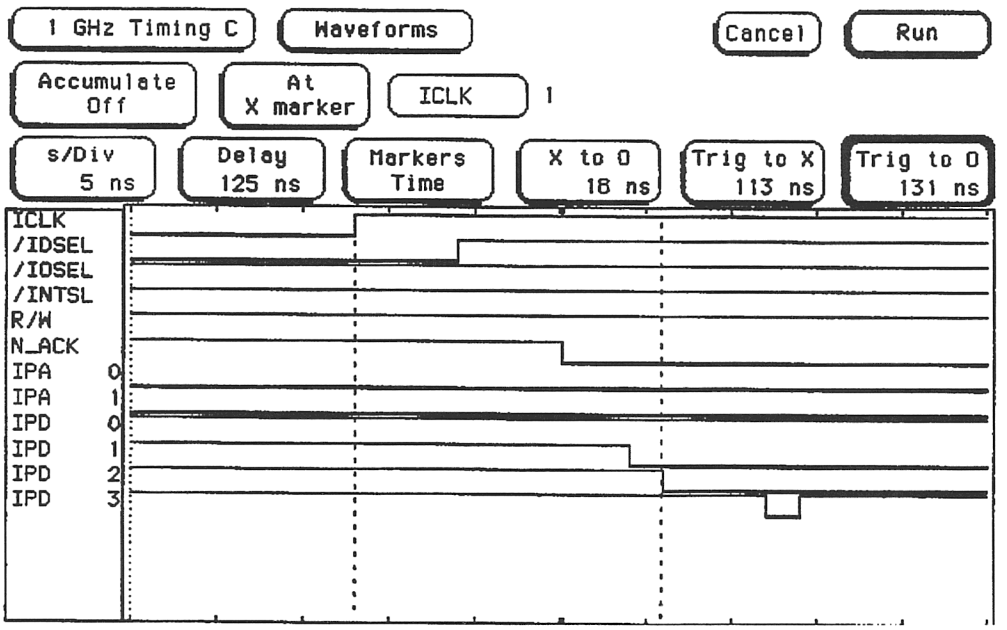


Figure 5-3 Zoomed-in Version of ID Cycle Driving N_ACK and IPD0-3

5.2.2 I/O Read Cycle

Figure 5-4 is a complete LOW40 I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals.

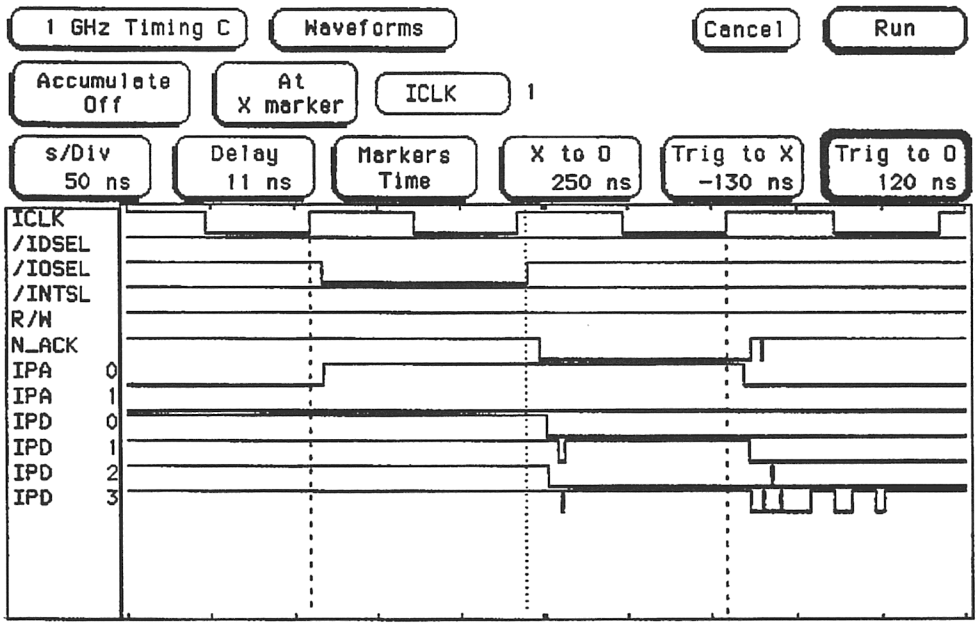


Figure 5-4 Complete LOW40 I/O Read Cycle

Figure 5-5 is a zoomed-in view of the LOW40 I/O read cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 18 nanoseconds for driving these signals.

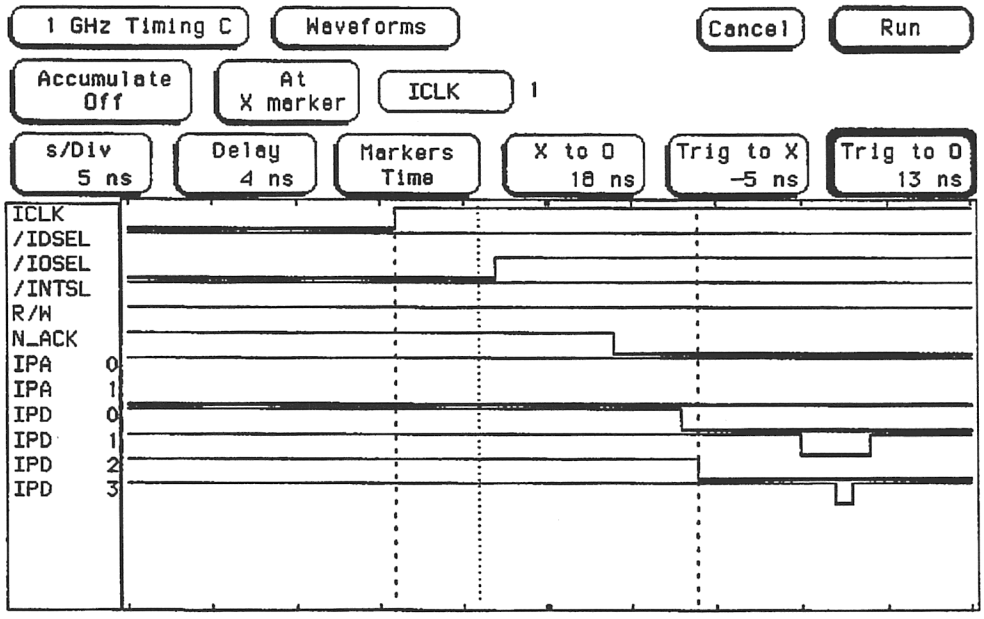


Figure 5-5 Zoomed-in View of I/O Read Cycle Driving N_ACK and IPD0-3

5.2.3 Typical Output Response Time

Figure 5-6 shows a typical board response time of an output being asserted after an I/O write. In this figure the signal of interest is the Port0 Bit0 (which is the 'PRT0B0' signal label on the waveform diagram) being asserted 4.698 µs after the end of the termination cycle of the I/O write to this data port. This delay, which is measured in microseconds rather than nanoseconds, is due to the parallel-to-serial conversion in the LOW40 "Controller" module then the serial-to-parallel conversion in the MIC5842BWM low-side drivers.

NOTE: Figure 5-6 is very important information for users concerned about system response time. An I/O write to any data port will result in approximately a 4.7 µs delay until the output bit or bits are asserted.

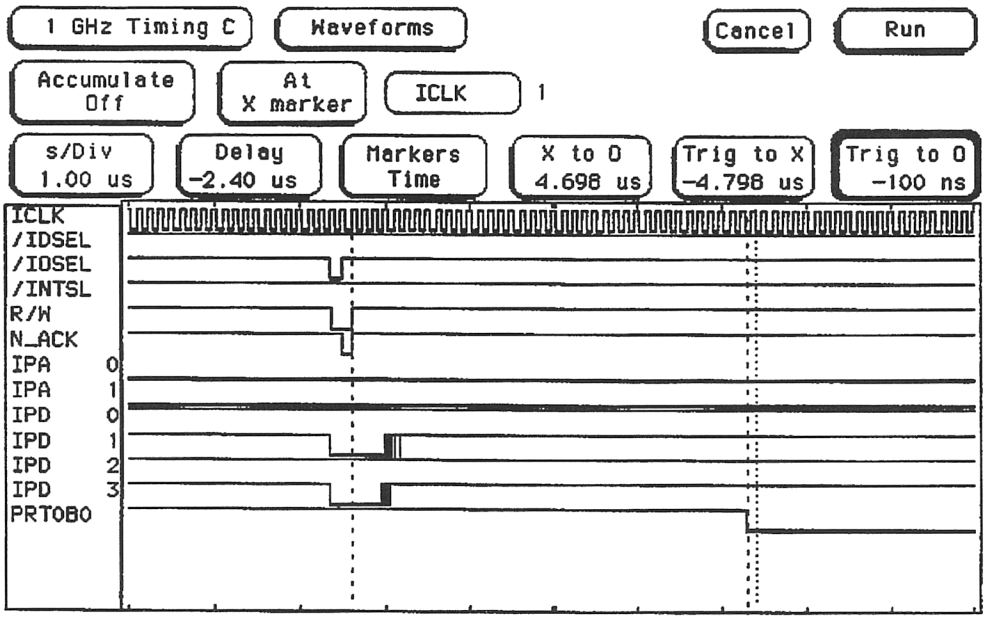


Figure 5-6 LOW40 Typical Output Response Time

NOTE: For back-to-back writes to the LOW40, the serial transmission process to the drivers is terminated mid-stream without affecting the port outputs, and is restarted including the data from the latest write. All outputs are modified with the current data register information simultaneously within 4.7 µs of the last data register write transfer from the carrier.

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the LOW40 IPack to solve a problem. This section of the manual will be revised periodically to include new application ideas for all subsequent readers to consider. Help advance the level of technology by participating with our team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and the author reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 A Short Glossary Of Low-Side Driver Applications

The following typical applications were developed by using one or more channels on the LOW40 IPack. Most of the common low-side configuration operations may be performed (within limits) by proper connections and software manipulations.

6.2.1 Solenoid Driver

Figure 6-1 is an application example that describes one of many possible configurations for using the LOW40 as a peripheral power driver. This application is a Relay/Solenoid Driver example. The user can turn on or off the relays or solenoids individually with I/O writes to the corresponding data port (with outputs already enabled) or by port (8-bits wide) by writing to the enable bits at IPA = 03 hex.

6.2.2 Incandescent Lamp Driver

Figure 6-2 is an application example of using the LOW40 as an Incandescent Lamp Driver. The user can turn on or off the lamps individually with I/O writes to the corresponding data port (with outputs already enabled) or by port (8-bits wide) by writing to the enable bits at IPA = 03 *hex*. To keep the overall power dissipation per port driver package below the absolute maximum rating (which is 1.82 W) you need to select lamps with proper current ratings. For example you could select eight 170 mA lamps @ a 100% duty cycle would yield 1.69 W package power dissipation, or use eight 200 mA lamps @ a 85% duty cycle yields 1.77 W of package power. Limit lamps in-rush currents to 500 mA to the LOW40 low-side drivers.

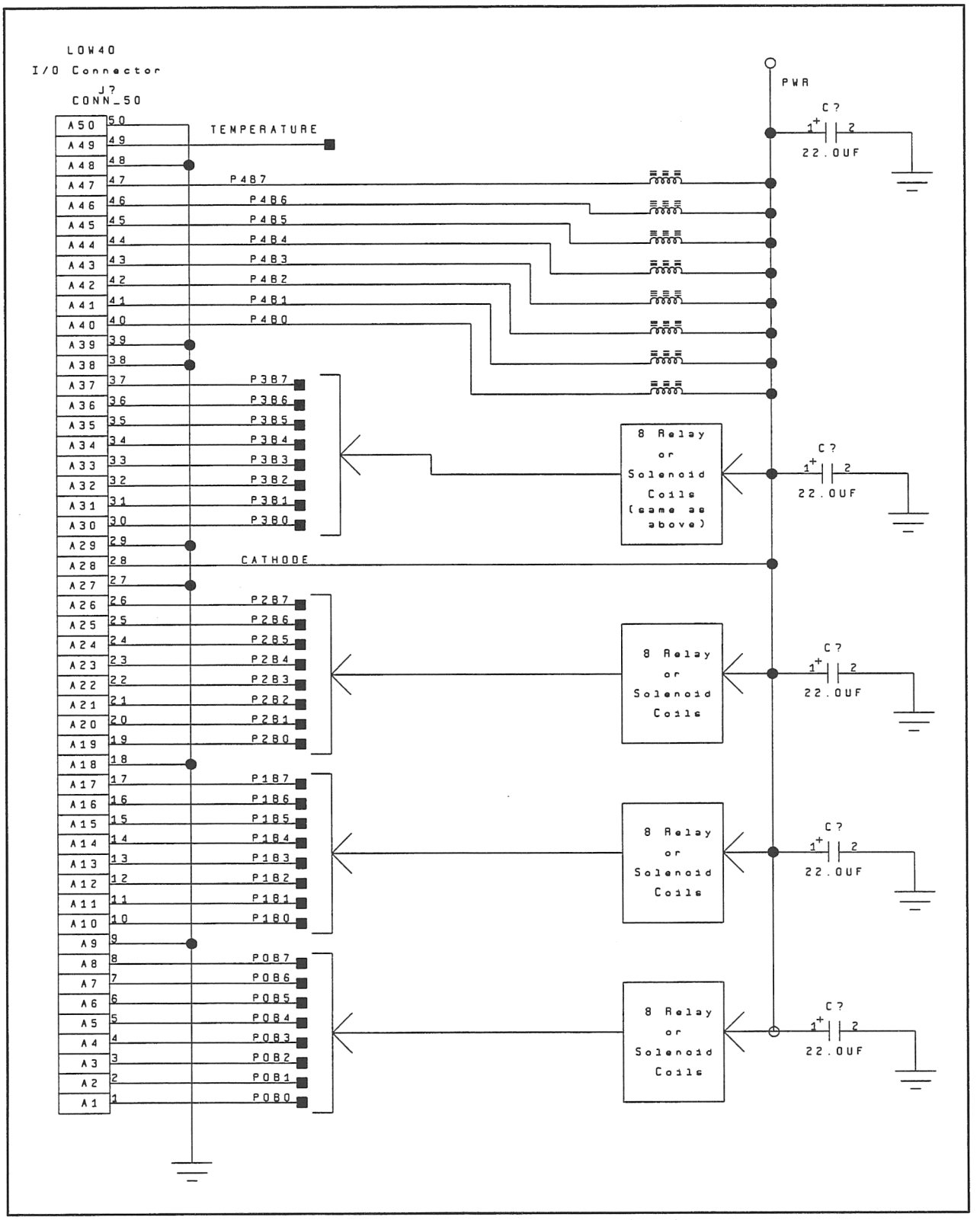


Figure 6-1 LOW40 used for Relay/Solenoid Drivers

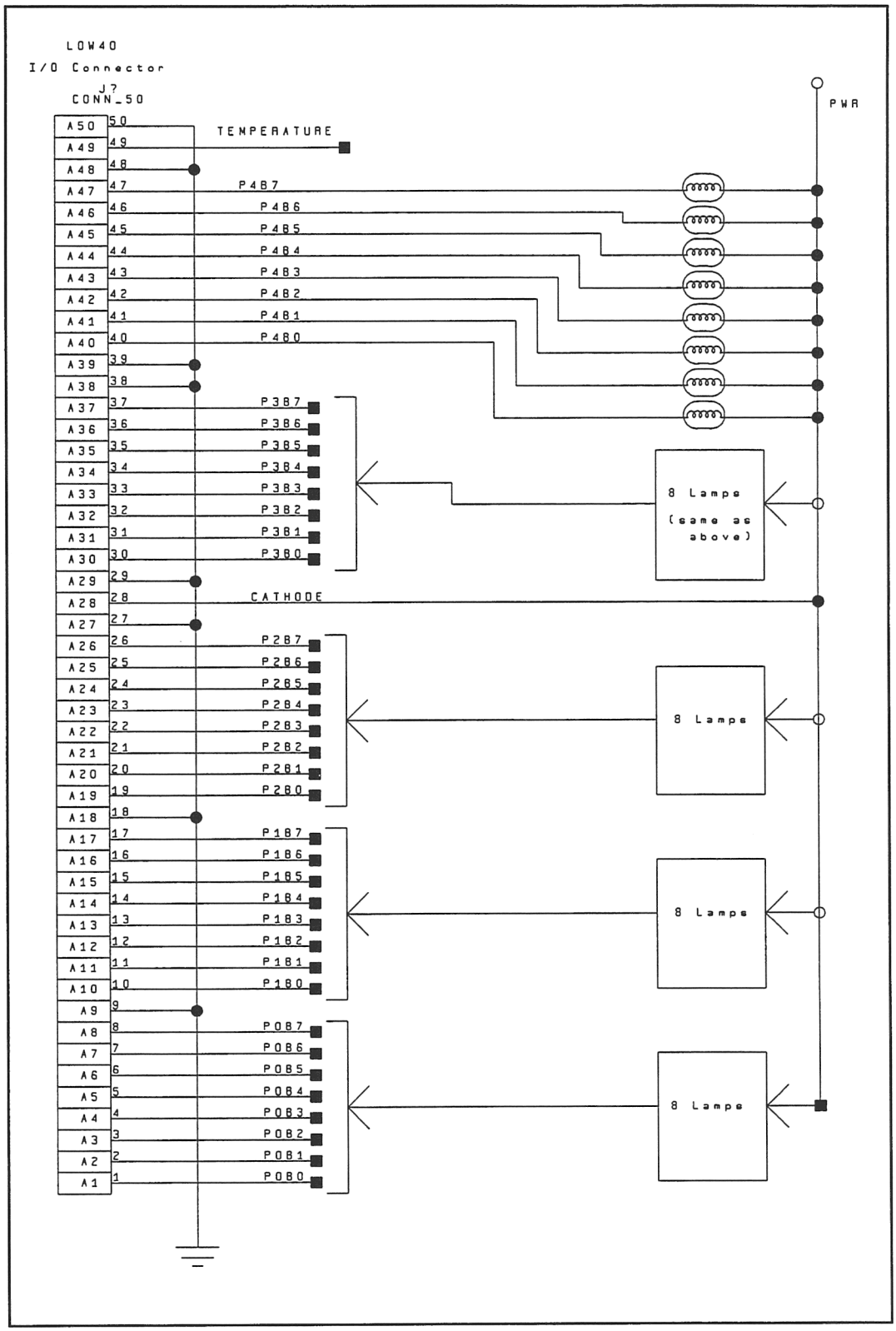


Figure 6-2 LOW40 used for Lamp Drivers

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.1.1 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.1.2 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.1.3 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

7.7 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.
- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:
This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high speed (32MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:
The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0mA (logic low) in parallel with 30ρF. All signals have a 10KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK
This signal, ≡ CLK in the specification, is an 8MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)
These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)
These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200mS following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)
N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)
N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "double-wide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:

+5volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50. +12volts is sourced via pin 23. And, -12volts comes in pin 22.

CYCLE TYPES:

There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:

There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:

Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:

The outside dimensions of a "singlewide" IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a "doublewide" IP are 3.600″ by 3.900″, +.000/-.020″. There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a "singlewide" IP, and 3.6″ by 3.188″ for a "doublewide" IP. The maximum height of components on the IP is 0.315″, with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:

The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

MEMORY TRANSFERS' CYCLE TABLES

CYCLE'	MEM WRITE NO HOLDS NO WAITS				MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS							MEM WRITE 1 HOLD 3 WAITS								DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15·0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH * END OF'			◇					◇			◇											◇					

CYCLE'	MEM READ NO HOLDS NO WAITS				MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS						MEM READ 1 HOLD 3 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15·0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND'

* IPD[15·0] = IPA[22·7] during during the SELECT cycle, and is used for data for all other cycles.

X — DON'T CARE

Z — HIGH IMPEDANCE

1 — HIGH STATE' +5v

0 — LOW STATE' GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPack

◇ IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS' CYCLE TABLES

CYCLE'	ID READ NO HOLDS NO WAITS				ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS							ID READ 2 HOLDS 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7·0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND'

X — DON'T CARE

Z — HIGH IMPEDANCE

1 — HIGH STATE' +5v

0 — LOW STATE' GND

→ DRIVEN INTO IPack

← DRIVEN OUT OF IPac

INT TRANSFERS' CYCLE TABLES

CYCLE'	INT READ NO HOLDS NO WAITS				INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS							INT READ 1 HOLD 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
PD[7·0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS' CYCLE TABLES

CYCLE'	I/O WRITE NO HOLDS NO WAITS			I/O WRITE NO HOLDS 3 WAITS					I/O WRITE 2 HOLDS NO WAITS					I/O WRITE 3 HOLDS 1 WAIT								DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPD[15'0]	X	→	→	X	→	→	→	→	→	X	→	→	→	→	X	X	X	X	X	→	→	→	→	→	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH @ END OF'			◇						◇			◇										◇					

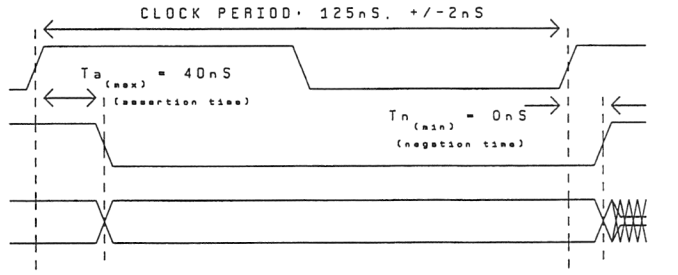
CYCLE'	I/O READ NO HOLDS NO WAITS			I/O READ NO HOLDS 2 WAITS					I/O READ 3 HOLDS NO WAITS					I/O READ 2 HOLDS 3 WAITS						I/O READ 3 HOLDS 2 WAITS						DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IPack	CARRIER
IPA[6'1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15'0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPR/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND'

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE' +5v
- 0 — LOW STATE' GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED' IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE' / SIDE' / ASSERTED LOW'	DOUBLE-WIDE N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IDSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IDSEL	SINGLE-WIDE N_MEMSEL	N_IOSEL	N_INTSEL	N_IDSEL	VALID TRANSFER(s)'
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY' A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY' B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY' BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O' A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O' B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O' BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT' A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT' B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	ID' A-SIDE ONLY

B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B

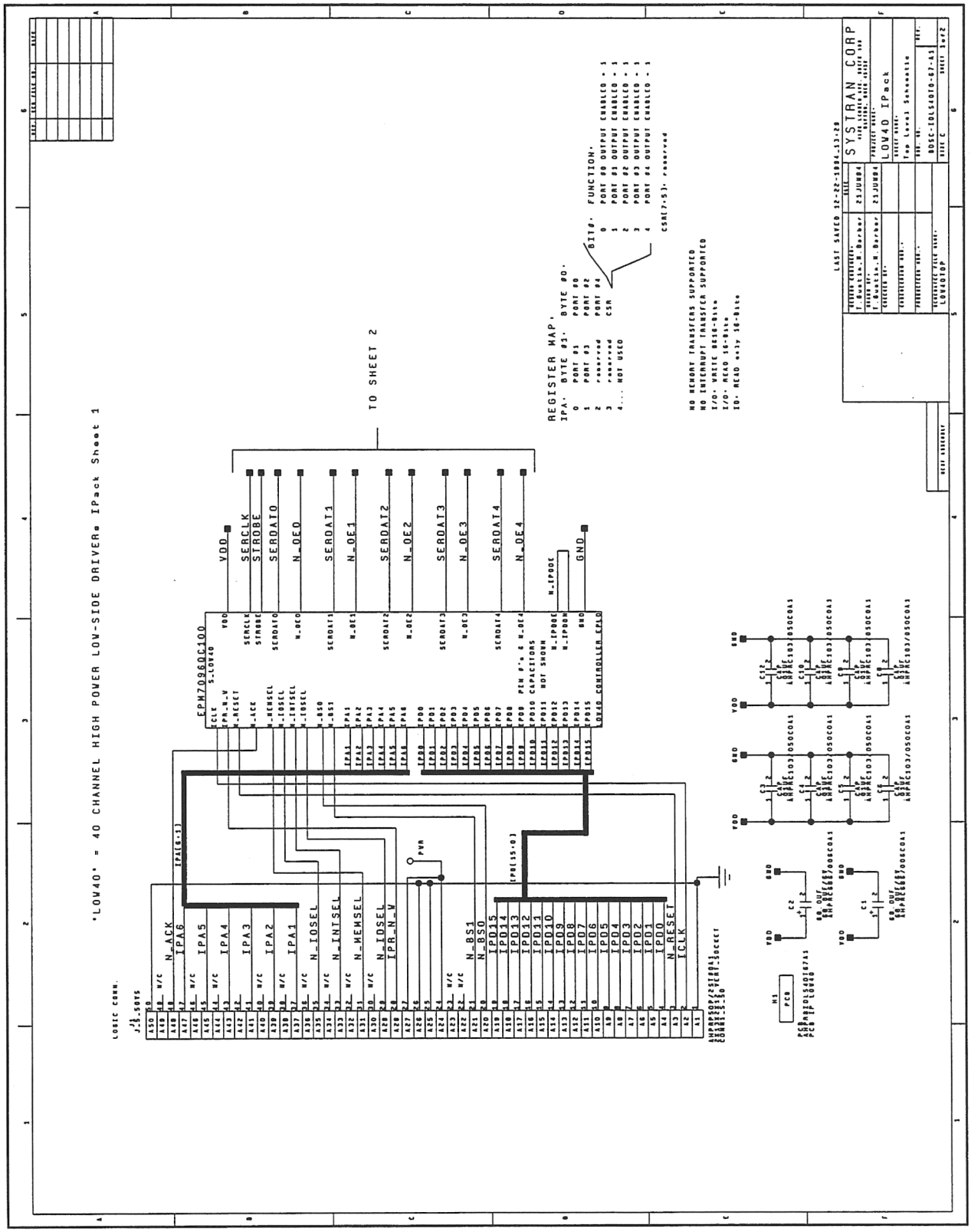


Figure B-1 Schematic #1

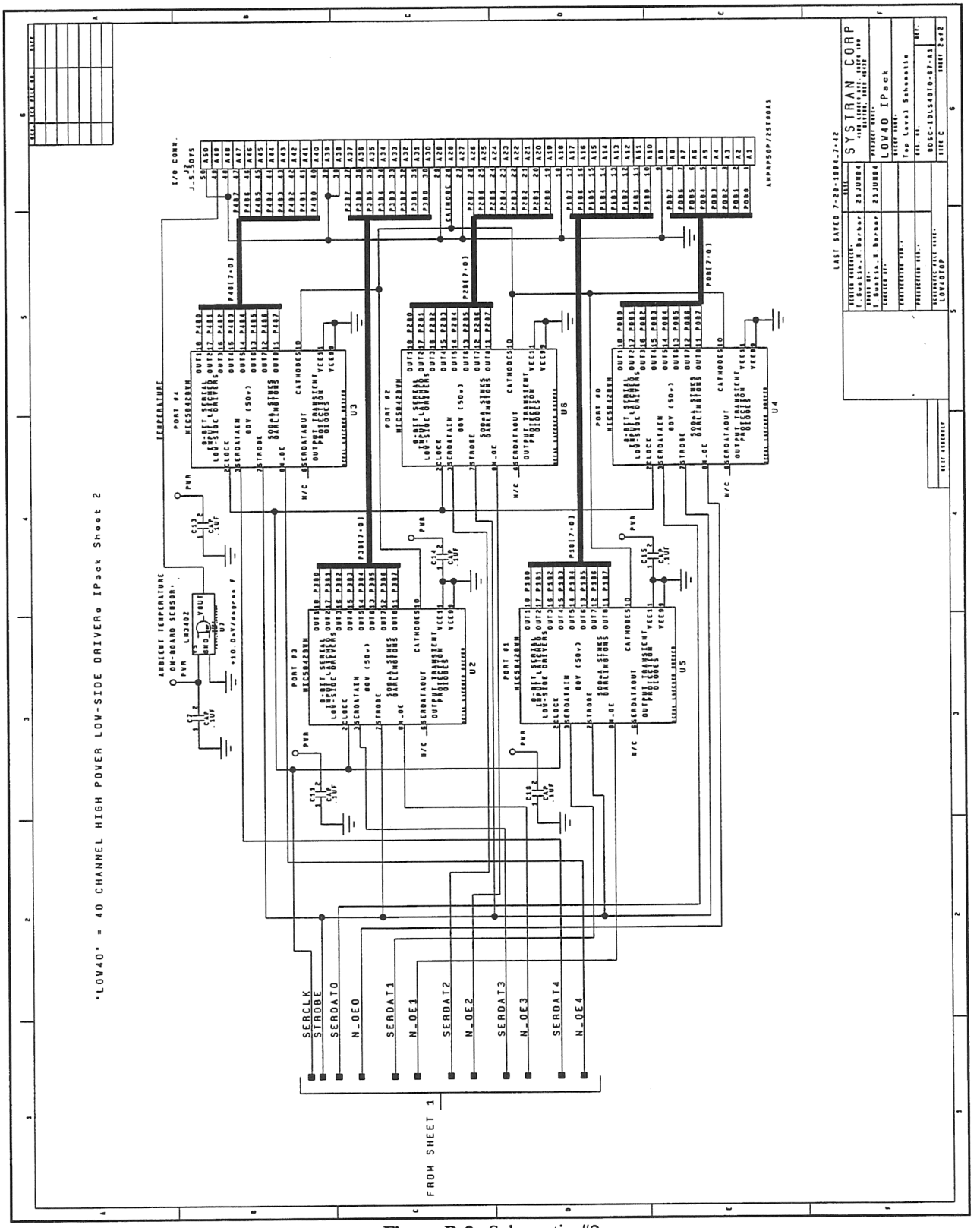


Figure B-2 Schematic #2

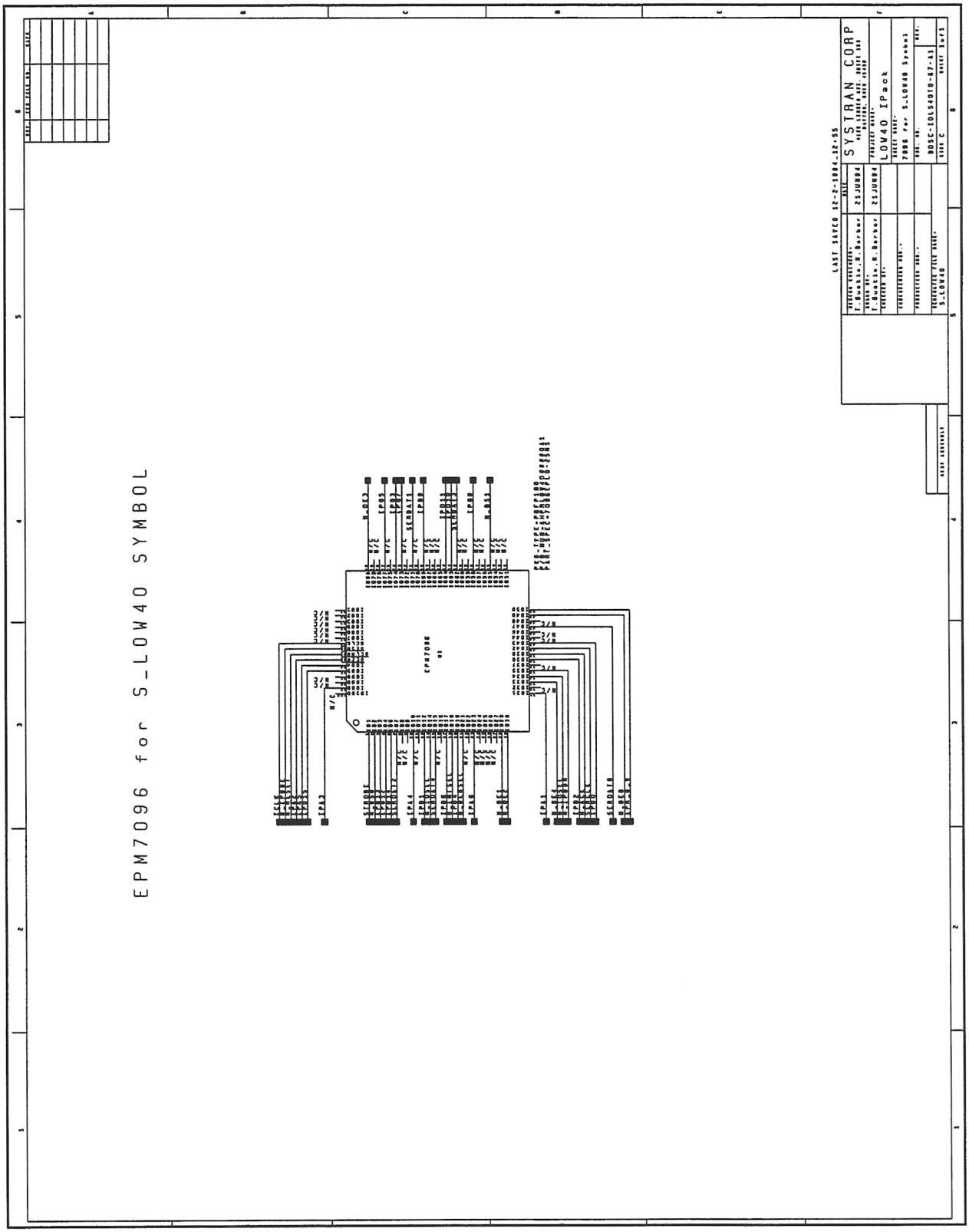


Figure B-3 Schematic #3