VMESC5

VME6U Slave 5-slot IPack Carrier
User Manual

Document No. B-T-MU-VMESC5##-A-0-A2

FOREWORD

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GLOSSARY

[x:y]. Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

byte-lane. 8-bits of a data bus on octal boundaries.

CSR. Control and Status Register.

doublewide. An IPack module that is twice the size of the singlewide board.

EPLD. Erasable Programmable Logic Device.

ID PROM. The circuitry that presents the proper data pattens to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IndustryPack. Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IPack. Refers to the IndustryPack standard.

IPack logic bus. A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6 bits wide (22 bits wide in memory mode).

IPDbus. IPack Data Bus.

ISR. Interrupt Service Routine

MTBF. Mean Time Between Failures.

ns, µs, ms. Nanoseconds, microseconds, and milliseconds respectively.

singlewide. An IPack printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL. Very high speed integrated circuit Hardware Description Language.

1.0 INTRODUCTION

1.1 Purpose

This is a reference manual for the Systran VME6U Slave 5-Slot IPack Carrier herein referred to as the VMESC5 board, part number BHAS-VMESC5.

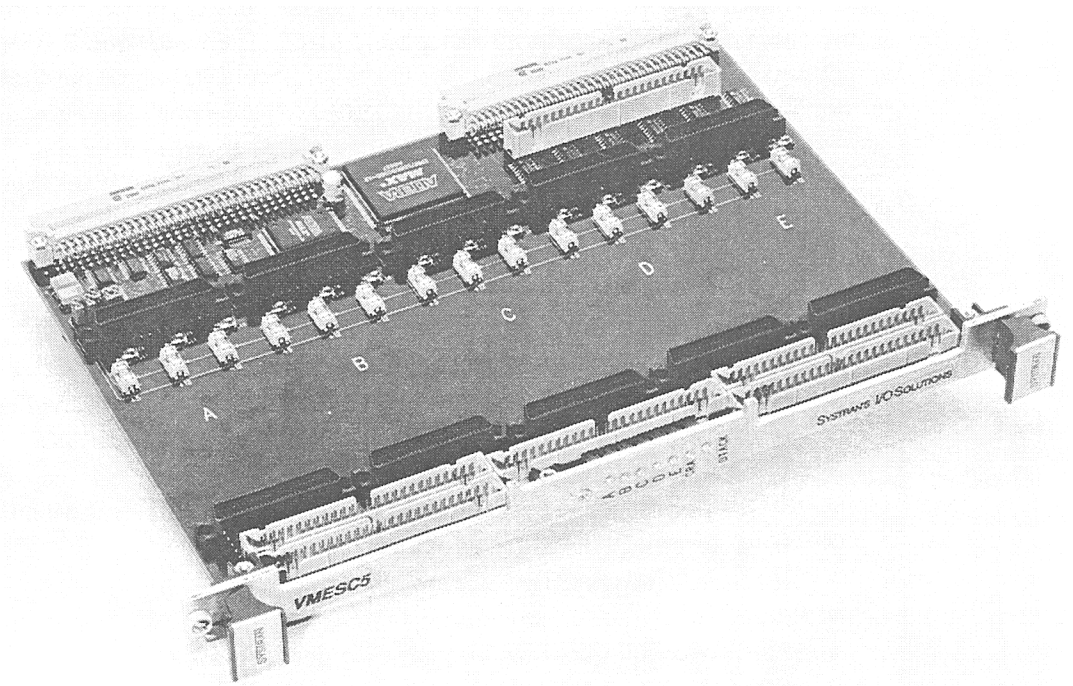

Figure 1-1 VMESC5 Board

1.2 Scope

This reference manual covers the physical and operational description of the VMESC5, both from hardware and software perspectives. This reference manual also contains detailed technical information about the VMESC5's performance characteristics, and a few typical applications. It is assumed that the reader has general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IPacks. Citation of equipment from other vendors within this document does not constitute an endorsement of their product(s).

1.3 Overview

The VMESC5 is a VME6U Slave board that supports five singlewide IPacks, three singlewide and one doublewide, or one singlewide and two doublewide IPacks. This carrier is limited to the support of 8 MHz IPacks. DMA and Memory accesses are not supported. All other IPack transfer types, namely, ID, I/O, and Interrupt are supported. The following sections in this manual describe the board features, overall board layout, data transfer types, and detailed description of the registers. The VMESC5's VMEbus interface is designed in compliance with the *IEEE 1014-1987, VME Specification*

Revision C.1, Oct. 85, and the IPack's interface are designed in accordance with the *IndustryPack Logic Interface Specification, Rev. 0.7.1.*

NOTE: Physical doublewide IPacks are supported. However, logical doublewide 32-bit transfers are not supported because memory transfers are not supported.

The VMESC5 was designed around a very easy to use, intuitive user interface, employing the highest quality (yet, reasonably affordable) components to provide the best performing, highest density VME6U IPack slave carrier available. The VMESC5 is a super-synchronous design that does not insert IPack hold cycles. This results in a very high throughput for this VME-to-IndustryPack bus coupling carrier.

The VMESC5 provides up to 250 I/O points (50 per IPack) per VME6U slot with the entire area under the IPacks as a solid ground plane to provide "quiet" operating conditions for sensitive analog IPacks. The front panel LEDs give the user diagnostic information on accesses to the IPacks, the VMESC5 local status and control registers, and the VME DTACK. The VMESC5 has a very easy to use and flexible VME interrupting capability where the individual interrupts from each IPack can be programmed to assert any VME interrupt request signal.

1.3.1 Features

- Up to 250 I/O points in a single, VME6U slot.
- Sustains 2.7 M transfers/second on READs and WRITEs (8- or 16-bit). *
- Each of 10 IPack interrupt requests (2 per IPack slot) can individually assert any of the 7 VME interrupt levels; equal levels IPack slot prioritized.
- I/O, ID, and INT transfers with no HOLDs. *
- Read-Modify-Write cycles supported to IPacks and VMESC5 registers.
- IPack error signals posted as status.
- IPacks are individually software resettable.
- Board base address jumper selectable.
- Pure ground plane under IPacks for "quiet" operation.
- Supports 5 singlewide, or 3 singlewide and 1 doublewide, or 1 singlewide and 2 doublewide IPacks.
- Can connect IPack Slot E I/O pins to VME P2 connector; doesn't lose IPack slot usage for systems already using P2.
- Seven front-panel IPack/Carrier Access and VME DTACK indicators (with pulse stretchers).
- Five 8-bit General Purpose registers.
- A16/D16/D8 VME transfers (2 KB block of space, address modifiers 29 *hex* and 2D *hex*).
- Supports writes to ID space.

* Rarely used memory transfers not supported for significant cost reductions; *IndustryPack Logic Interface Specification, Rev. 0.7.1* used.

1.3.2 Details

MECHANICAL

- Measurements: Length: 9.187 inches (23.33 cm)
  Width: 6.299 inches (15.99 cm)
- Weight: 9.984 oz., 283 grams (includes front panel)

- Board Thickness: 0.062 inches, 0.157 cm, nominally, (6 layers)

ELECTRICAL

- Power (No IPacks installed): +5 Vdc (+5%) @ 0.53 Amps, +12 Vdc @ 0.0 Amps, - 12 Vdc @ 0.0 Amps

NOTE: The VMEbus ground and IPacks' ground are not isolated through this board

ABSOLUTE MAXIMUM SUPPLY RATINGS

- +5 Vdc Supply voltage with respect to ground: -0.5 Vdc minimum and +7.0 Vdc maximum
- +12 Vdc Supply voltage with respect to ground: Dependent on the IPacks installed.
- -12 Vdc Supply voltage with respect to ground: Dependent on the IPacks installed.

RECOMMENDED OPERATING SUPPLY RATINGS

- Supply Voltage with respect to ground: +4.75 Vdc to +5.25 Vdc

ENVIRONMENTAL SPECIFICATIONS:

- Temperature:
  (Operating): -0°C → +70°C
  (Storage): -65°C → +150°C
- Humidity (Noncondensing): 5% → 95%
- Vibration (Operating): 10 G's RMS, 20 Hz→2 KHz, random
- Shock (Operating): 50 G's maximum, all axes
- Altitude (Operating): 10,000 feet maximum

MEAN TIME BETWEEN FAILURE (MTBF):

- 667,245 hours per MIL-HDBK-217F

1.4 Accessories

IPack Slot E I/O ribbon cable to the VME P2 connector (BHAS-RCVMEP2)

1.5 Related Publications

- *IndustryPack Logic Interface Specification Synopsis* published by SYSTRAN Corp. (This synopsis is included in this document as Appendix A).
- SYSTRAN I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IndustryPack Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001-A-0-A1)
- *IndustryPack Logic Interface Specification Revision 0.7.1* published by GreenSpring Computers, Inc. 1204 O'Brien Drive, Menlo Park, CA 94025.

1.6 Ordering Process

To order SYSTRAN products, call (513) 252-5601. For additional product information you may call the above number, or send an E-Mail message to **info@systran.com**.

1.7 Technical Support

Technical documentation provided with the product discusses the technology, its performance characteristics, and some typical applications. It includes tutorial material, with comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. SYSTRAN also publishes and distributes technical briefs and application notes that cover a wide assortment of topics. The applications selected are derived from real scenarios, but do not cover all possible circumstances.

Direct any programming questions, any concerns about the functional-fit of this product for your particular application, or any questions not satisfactorily answered by this document, to the factory at **(513)252-5601**, or send an E-Mail message to **support@systran.com** for additional assistance. Our goal is to help solve your problem.

Refer to Section 7.0 for warranty and repair information.

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An integral part of SYSTRAN quality and reliability goals is customer feedback. Customers are encouraged to contact the factory with any questions or suggestions regarding unique quality requirements, or to obtain additional information about our programs. SYSTRAN's commitment to customers includes, but is not limited to:

- Professional and quick response to customer problems utilizing SYSTRAN's extensive resources.
- Incorporation of established procedures for product design, test, and production operations, with documented milestones. Procedures are constantly reviewed and improved, ensuring the highest possible quality.

SYSTRAN provides products and services that meet or exceed the best expectations of our customers.

- All products are tested using an Automatic Test Equipment system, with samplings for all product types taken through extended testing scenarios that include stress testing for voltage and temperature ranges beyond specifications.
- All products receive a predictive reliability rating based upon a calculated MTBF utilizing the MIL-HDBK-217F. Field failures are continuously logged and evaluated for potential failure modes and trends.
- Other environmental parameters are guaranteed by design, and not tested.
- Design reliability is ensured by methodology (top-down CAE design, VHDL, synthesis, extensive all-cases simulation, ALPHA build and test, and BETA testing if required) with full concurrent engineering practices throughout.

2.0 DESCRIPTION

NOTE: The IPack signal references, transfer and cycle types discussed in this document are explained in detail in *the IndustryPack Logic Interface Specification Synopsis* included as Appendix A. The extended implementation of write-transfer capabililty over the full ID addressing space for this product is over and above that described in the specification synopsis.

2.1 Overview

This section describes the VMESC5 in detail. It begins by discussing the VMESC5 in terms of its functionality and features. Next, it covers the VMESC5 theory of operation. Finally, it dicusses the VMESC5 schematics.

2.2 Functional Description

2.2.1 VME Memory Mapping Scheme

The mapping scheme of the ID and I/O address spaces for all five IPacks, and the carrier's control and status registers are at fixed relative addresses from a jumper-selectable board base address. The board base address is selectable within the VME short I/O address space (A16) on 2 K boundaries. The VMESC5 responds to Address Modifier codes 29 *hex* and 2D *hex* corresponding to short non-privileged and short supervisory VME accesses, respectively. In Section 4.0, Table 4-1 shows the location of the ID and I/O spaces for each IPack, and carrier-control register locations relative to the board base address.

2.2.2 ID Transfers

IPack ID transfers are supported as A16/D16/D8 VME transfers. ID transfers are performed by a word or byte read/write operation of the slot IPack ID address space from the VMEbus. The ID PROM values are located every other byte at odd-byte locations (IPack byte lane 0). For word-reads the even byte is discarded. The ID PROM area allows read or write accesses to support future IPacks requiring writes to the ID address space. Read-Modify-Write cycles are supported for ID transfers.

2.2.3 I/O Transfers

IPack I/O transfers are supported as A16/D16 VME transfers. I/O transfers are performed by a word or byte read or write operation of the slot IPack I/O address space from the VMEbus. Even and odd single-byte reads are supported. Read-Modify-Write cycles are supported for I/O transfers.

2.2.4 Interrupt Transfers

Interrupts are requested by the IPack module by assertion of N_INTREQ0 or N_INTREQ1. An independent VME interrupter handles each of these IPack interrupt request lines and asserts one of the seven prioritized VME interrupt request lines. This provides a minimum delay in asserting the interrupt request to the VMEbus master.

Which line is asserted depends on the interrupt level programmed into the carrier's IPack slot specific interrupt register. The five interrupt registers, one per IPack slot, support independent selection of interrupt levels for both interrupt request signals N_INTREQ0 and N_INTREQ1. Upon receipt of the interrupt acknowledge from the VMEbus master, the VMESC5 will conduct a D8 transfer of the interrupt vector from the IPack to the VMEbus. The interrupt request release will be dependent upon the individual IPack being used.

2.2.5 Interrupt Prioritization

Interrupts in the VME system are prioritized in a two tier fashion; by Interrupt Request Level (IRQ) and relative position. This tier-effect is demonstrated in Figure 2-1.

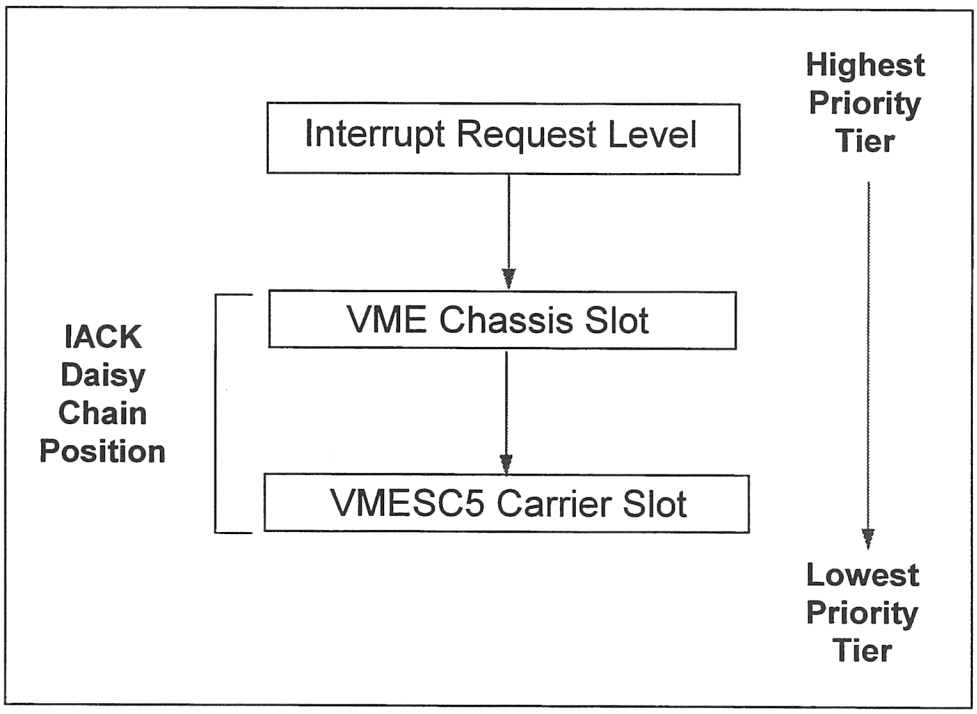


Figure 2-1 Interrupt Priority Tiers

The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest as shown in Table 2-1.

Table 2-1 Interrupt Request Level Priorities

INTERRUPT REQUEST LEVEL	PRIORITY
7	Highest
6	2nd Highest
5	•
4	•
3	•
2	2nd Lowest
1	Lowest

The second tier of prioritization is determined by the relative position in the interrupt daisy chain. The closer the interrupt requester is to the interrupt handler in the daisy chain, the higher its priority for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location (see Figure 2-2) and the IPack slot location on the VMESC5 carrier (see Figure 2-3).

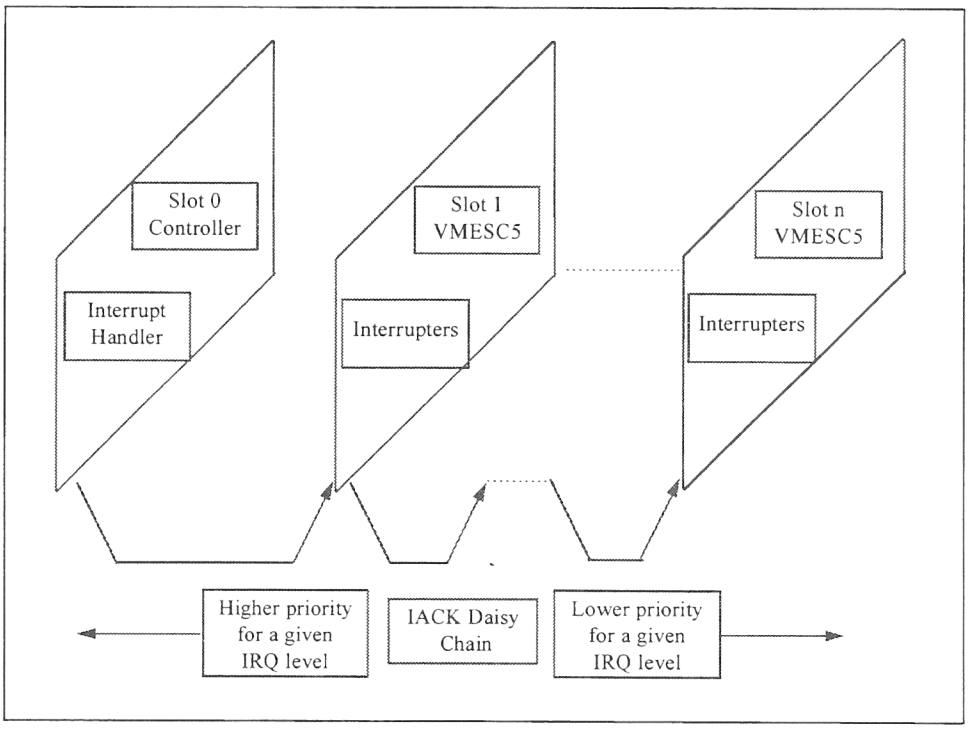


Figure 2-2 VME Chassis Slot Prioritization Through IACK Daisy Chain

The VMESC5 IPack slot priority order from highest to lowest is A0, A1, B0, B1, C0, C1, D0, D1, E0, E1.

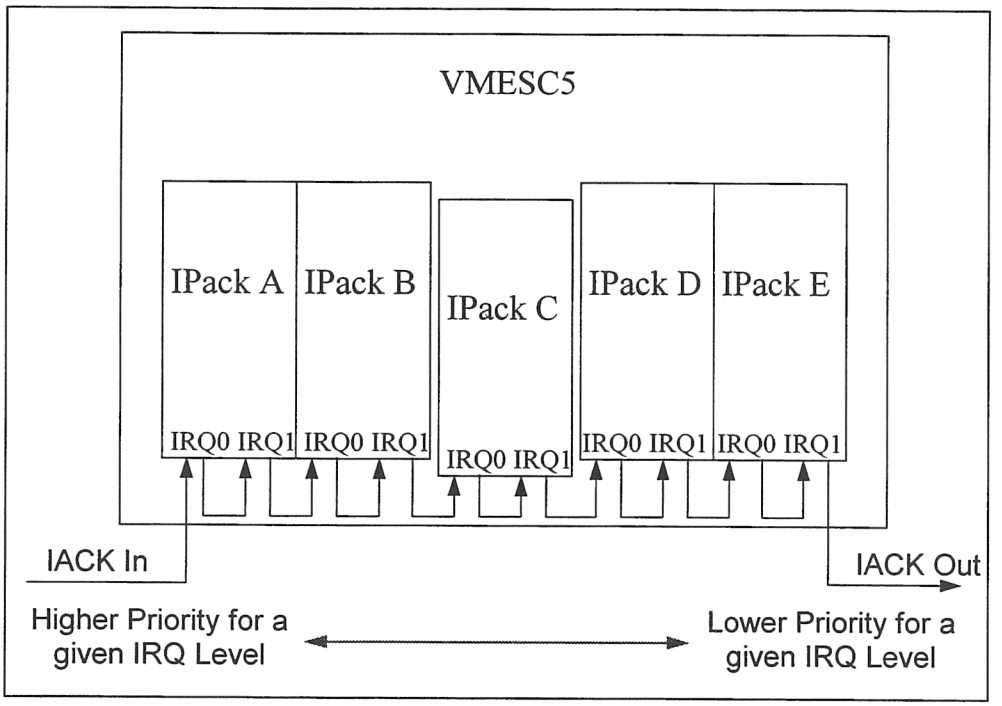


Figure 2-3 IACK Daisy Chain on the Carrier

2.2.6 General Purpose Registers

Five 8-bit general purpose user-defined registers are provided. Read-Modify-Write cycles are supported for general purpose register accesses.

2.2.7 Diagnostic LEDs

Seven diagnostic LEDS are located on the front panel of the VMESC5. Six of the LEDs, labeled A, B, C, D, E, and CRA, indicate when a read or write access is attempted to one of the five IPack slots or the carrier registers. The seventh LED, labeled DTACK, indicates an acknowledgement by the IPack or the VMESC5 of the attempted access. This scheme provides independent verification of the access and the acknowledgement.

2.2.8 IPack Reset

Independent or simultaneous resetting of the IPacks is facilitated through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. See section 4.0 PROGRAMMING GUIDE for a detailed description of this register.

2.2.9 Error Status

Monitoring of the IPack ERROR signals is made possible by reading the Error Status register. See section 4.0 PROGRAMMING GUIDE for a detailed description of this register.

2.2.10 Strobe Signals

The IPack STROBE signals can be connected via a 6-pin header (J17) located near the front panel.

2.2.11 Power Supply Filtering

Independent 'T' type filters are used for the +5, +12, and -12 volt power feeding each IPack. This arangement, while costing a little more, provides superior power supply filtering.

2.2.12 Fuses

Independent field replaceable fuses are used for the +5, +12, and -12 volt power feeding each IPack. Although this arrangement costs a little more, it provides superior short-circuit protection.

NOTE: Replacement fuses can be purchased directly from Littelfuse®, Inc. Phone (708) 829-0400.

2.3 Theory of Operation

2.3.1 Block Diagram Description

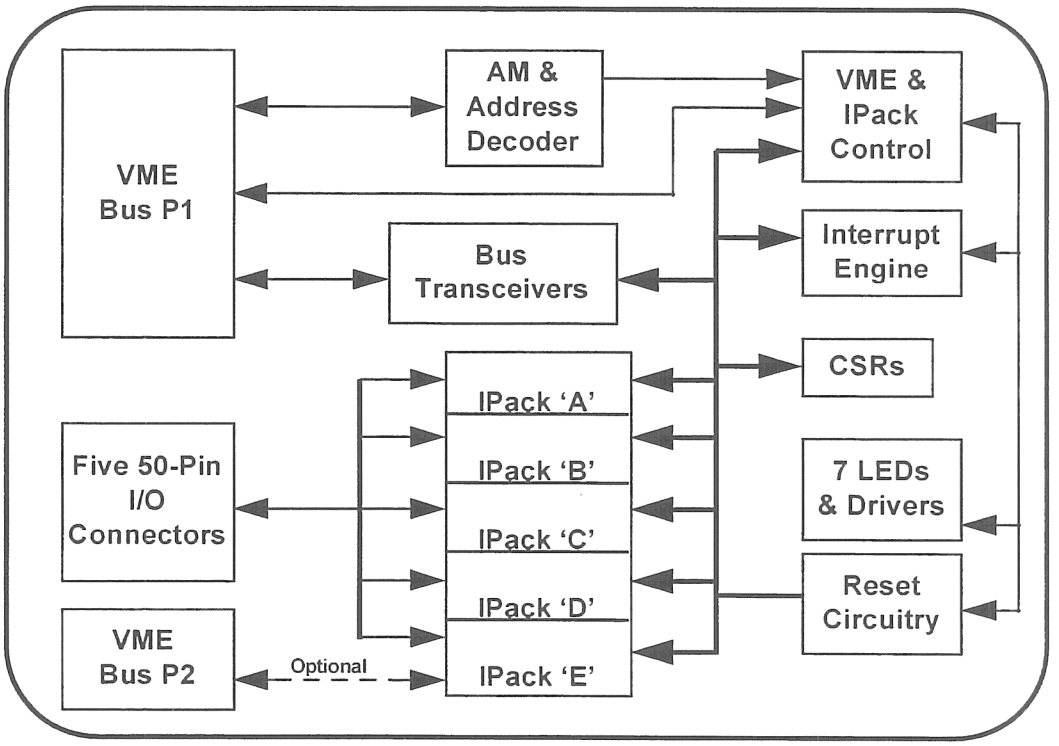


Figure 2-4 VMESC5 Block Diagram

Figure 2-4 is a simplified block diagram of the VMESC5 representing the signal flow between the VMEbus, IPack Logic Bus and the IPack I/O connectors. On the left side of the diagram is the VMEbus P1 connector through which all transfers between the VME host computer and the VMESC5's registers or IPacks are conducted. The VMEbus transfers do not insert any IPack hold cycles into the accesses to the IPacks.

The block labeled "AM & Address Decoder" handles decoding of the VME address and address modifiers. The block labeled "VME & IPack Control" handles the transfer of data between the VME and both the VMESC5 CSRs and the IPacks.

The block labeled "Interrupt Engine" controls the VME Interrupt requests, and prioritization of VME Interrupt Acknowledge cycles. The large block in the center of the diagram represents the five IPack slots labeled IPack 'A' down to IPack 'E'. The IPack I/O connectors are directly connected to the VMESC5's five front panel 50-pin I/O connectors. IPack slot 'E' can be optionally connected to the VMEbus P2 connector via a short ribbon cable. The last two blocks at the lower right hand corner of the diagram contain the reset circuitry for each IPack and drivers for each of the seven front panel LEDs.

The P1 connector is located on the upper left of the VMESC5 Assembly Drawing Figure 2-5. When looking at the "top" or component side of the VMESC5, the IPack slots are labeled from left to right for slot A through slot E. All of the I/O signals are connected through the five 50-pin connectors located at the bottom of Figure 2-5. (except the optional connection of slot E's I/O signals to the VME P2).

2.3.2 Functional Logic Module Overview

The VMESC5 board has VHDL models that are sectioned into four functional logic blocks where two of which are located in the VMESC5 module (which is the VMESC5 primary activity controller on Schematic #1). The VMESC5 module works in conjunction with two other modules called VSC5INT (which is the VME interrupt handler on Schematic #2) and the V5LEDIPR module (on Schematic #3) for driving the front panel LEDs and the IPack's N_RESETx lines. All of the VHDL modules are defined below.

2.3.2.1 VMESC5 Module

VME ADDRESS DECODER

This block detects VME host accesses to local VMESC5 Board Registers and IPack I/O and ID spaces. An address-detect (HIT) signal corresponding to one of these address spaces is asserted when a matching address and address modifier (29 *hex* and 2D *hex*) is detected.

DATA TRANSFER ENGINE

The DTE handles the transfer of data between the VMEbus and the IPack modules. It monitors the HIT signals from the address decoders to determine when a transfer is to take place. The VME control signals and address lines provide the rest of the transfer information. The DTE asserts the appropriate IPack ID or I/O select line and executes an IPack synchronous transfer. The Reset and Error Status registers are also located in this module. The DTE is implemented using conbinational logic and four state machines: The State Machines include:

- One for VME Read cycles from the local control and status registers
- One for VME Write cycles to the local control and status registers
- One for IPack I/O and ID Read cycles
- One for IPack I/O and ID Write cycles

The IPack read and write state machines complete a transfer in three IPack clock cycles (six VME SYSCLOCK cycles). Specifically the IPack Read state machine will place the data on the VMEbus upon detection of the appropriate IPack acknowledge signal N_ACK, and the Write state machine will latch the data from the VMEbus and assert DTACK upon detection of the appropriate IPack N_ACK signal.

REGISTERS

The VMESC5 module contains the Reset, Error Status, and General Purpose registers. See section 4.0 PROGRAMMING GUIDE for a detailed description of these registers.

2.3.2.2 VSC5INT Module

VME INTERRUPT ENGINE

This module detects an interrupt request(s) from an IPack(s), then asserts and selects VME interrupt request level(s). It monitors the VME V_IACKIN and A3-A1 signals and determines if the interrupt being acknowledged is the one it requested. If the level is different than the one requested, the acknowledge signal is passed on via V_IACKOUT daisy chain. If the acknowledge is for this IPack's interrupt, the DTE asserts an internal interrupt HIT signal indicating that the corresponding IPack's interrupt vector is to be transferred. If more than one IPack interrupts at the same level and time, the interrupts are processed in a prioritized fashion. This scheme is from IPack slot A's N_INTREQ0 as the highest priority, then slot A's N_INTREQ1 as the second highest, down to the slot E's N_INTREQ1 as the lowest. Refer to section 2.2.5 for a detailed description of interrupt prioritization.

This interrupt priority scheme is implemented by the user by programming a specific level in the interrupt level registers. The Interrupt Engine is implemented using conbinational logic and three state-machines. One state machine places an interupt vector on the VMEbus just like a VME read cycle, one state machine for VME Read, and one for Write cycles to and from the local interrupt level registers. The IPack Interrupt Acknowledge Cycle places the interupt vector on the VMEbus in three IPack clock cycles (six VME SYSCLOCK cycles). Specifically the IPack interrupt vector state machine will place the vector on the VMEbus upon detection of the appropriate IPack acknowledge signal N_ACK.

REGISTERS

The VSC5INT module contains the Interrupt Level registers for IPack slots A through E. See section 4.0 PROGRAMMING GUIDE for a detailed description of these registers.

2.3.2.3 V5LEDIPR Module

FRONT PANEL LED AND IPACK RESET DRIVERS

The V5LEDIPR module is responsible for monitoring all of the IPack select signals from the VMESC5 module, and conbinationally driving the front panel LEDs from the one-shot drivers, and for logically "ORing" the VME system reset (V_SYSRESET) with the individual IPack reset one-shot signals for driving each IPack Reset signal.

2.4 VMESC5 Schematics, Components and Functions

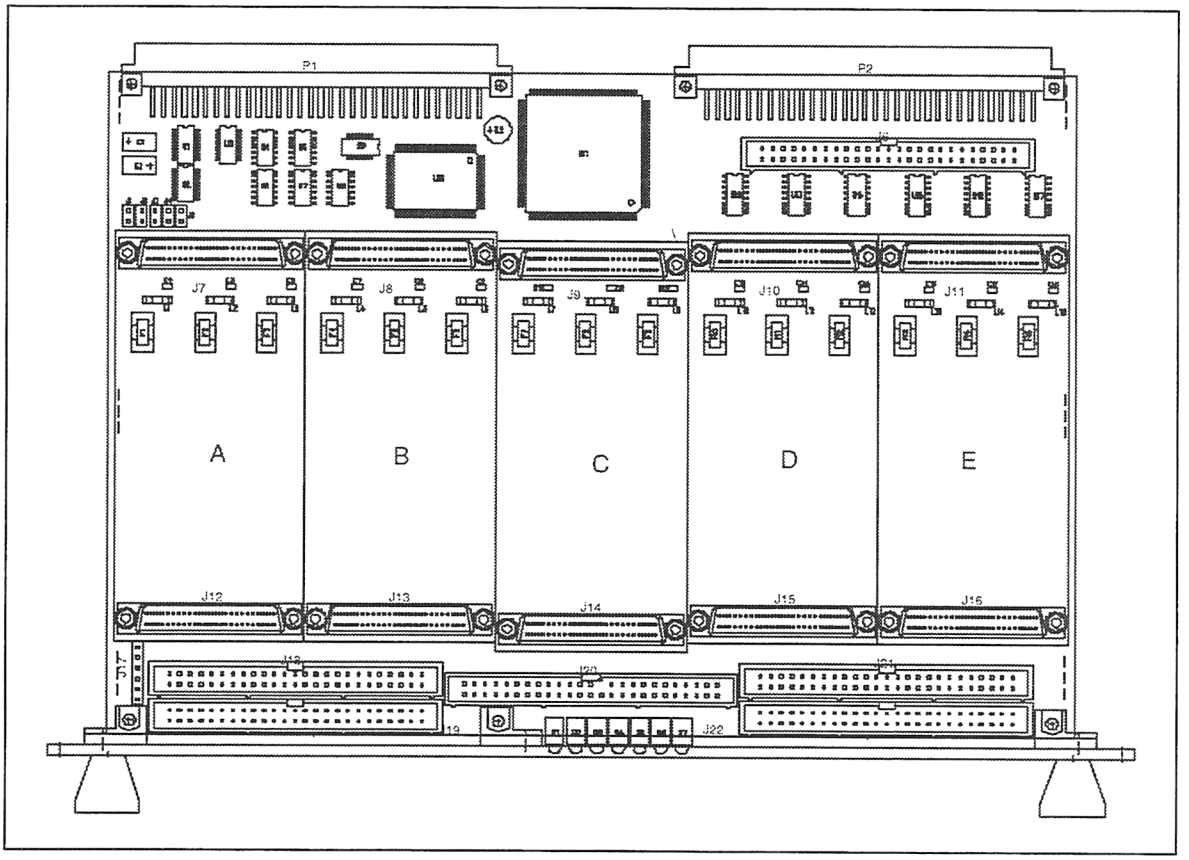


Figure 2-5 VMESC5 Mechanical Assembly

NOTE: Refer to the schematics located in Appendix B while reading this material since individual components are referred to by function name, schematic reference designator, or industry-standard device part number.

The VMESC5 shown in Figure 2-5 was developed using VHDL and Synthesis, and targeted to several Altera EPLDs. The design was schematic-captured and integrated to standard interface devices, connectors and discrete components using VIEWLogic CAE tools. This topdown methodology is evident in the schematics and product design material presented in this document. For those readers not familiar with the topdown methodology used to develop the VMESC5, the following is a short presentation on the schematics of the VMESC5.

NOTE: Signal nomenclature 'V_' prefix represents an active-low VMEbus signal and an 'N_' prefix represents an active-low IPack signal.

Schematic #1

The first sheet (1 of 9), is composed of the VME P1 connector, a large block (U11) labeled "VMESC5" that contains the DTE in an Altera 7128E 160-pin EPLD QFP, three 74FCT652 latching transceivers (U1,2, and 3) for VME to IPack data bus transfers, one 74FCT541 (U9), and two 74F08s (U5 and 8) for signal isolation and buffering; a 74F74

(U4) to generate the IPack 8 MHz clock (synchronous with the 16 MHz VME SYSCLOCK); one buffer of a 74F125 (U6) to drive the VME DTACK signal; five jumpers (J1-5) for setting the board base address; two 33 µF (C1 and 2); one 100 µF (C3) power supply filter capacitors; and many pullup resistors.

SCHEMATIC #2

The second sheet is composed of a large block (U10) labeled "VSC5INT" that contains the VME Interrupt Engine in an Altera 7128E 100-pin EPLD QFP, one 74F08 (U8) for signal buffering, two 74F125s (U6 and 7) to drive the VME interrupt request signals.

SCHEMATIC #3

The third sheet is composed of a large block (U501) labeled "V5LEDIPR" that contains the logic to drive the front panel LEDs and each IPack N_RESET signal in an Altera 7032 44-pin EPLD QFP, and three 74HC4538 one-shot multivibrators (U12,13, and 14) with various resistors and capacitors to stretch the pulses of the IPack reset and front panel LED signals.

SCHEMATIC #4

The fourth sheet is composed of three 74HC4538 one-shot multivibrators (U15,16, and 17) with various resistors and capacitors to stretch the pulses of the front panel LED signals, a 74FCT541 buffer (U500) to drive each LED (D1-D7), and five series 18 Ω resistors for each IPack 8 MHz Clock signal. Five of the front panel LEDs (D1-D5) indicate any access (I/O, ID, or Interrupt) to each IPack slot A-E respectively. LED D6 indicates a VME access to any VMESC5 local control and status register, and LED D7 indicates any valid VME DTACKs. The front panel LEDs provide excellent system diagnostics; ie. if an IPack is installed but is not responding to the VME host CPU, the VMESC5 user can view the LEDs to see if the correct IPack was accessed and if the VME DTACK was asserted.

SCHEMATIC #5

The fifth sheet is composed of two IPack Logic Bus connectors (J7 for slot A and J8 for slot B), six surface-mount fuses in holders (F1-F6) for protecting the power lines into each IPack, six surface-mount T-Type filters (L1-L6), and six 0.1 µF filter capacitors (C4-C9). F1 and L1 and F4 and L4 are for the +5V power inputs, F2 and L2 and F5 and L5 are for the +12 V power inputs; and F3 and L3, and F6 and L6 are for the -12 V power inputs for slots A and B respectively. Any unused signals on the IPack Logic Bus connectors are pulled-up to +5 V via a 10 KΩ resistor.

SCHEMATIC #6

The sixth sheet is composed of two IPack Logic Bus connectors (J9 for slot C and J10 for slot D), six surface-mount fuses in holders (F7-F12) for protecting the power lines into each IPack, six surface-mount T-Type filters (L7-L12), and six 0.1 µF filter capacitors (C10-C15). F7 and L7, and F10 and L10 are for the +5 V power inputs; F8 and L8, and F11 and L11 are for the +12 V power inputs; and F9 and L9, and F12 and L12 are for the -12 V power inputs for slots C and D, respectively. Any unused signals on the IPack Logic Bus connectors are pulled-up to +5 V via a 10 KΩ resistor.

SCHEMATIC #7

On the left side of the seventh sheet is one IPack Logic Bus connector (J11 for slot E), three surface-mount fuses in holders (F13-F15) for protecting the power lines into each IPack, three surface-mount T-Type filters (L13-L15), and three 0.1 µF filter capacitors (C16-C18). F13 and L13 are for the +5 V power inputs; F14 and L14 are for the +12 V power inputs; and F15 and L15 are for the -12 V power inputs for slot E. On the right side is the VME P2 connector (P2) and the second slot E I/O 50-pin connector (J6) that optionally sends the slot E I/O signals out the VME P2 connector via a short 50-pin ribbon cable that connects over the top of IPack slots D and E. Finally, on the bottom of the sheet is the 6-pin header connector (J17) that gives access to each of the N_STROBE signals from the IPacks. Each of the N_STROBE signals on the IPack Logic Bus connectors are pulled-up to +5 V via a 10 KΩ resistor. Refer to Table 3-3 and Table 3-4 for the detailed pinouts of the VME P2 and J17 STROBE connectors. Any unused signals on the IPack Logic Bus connectors are pulled-up to +5V via a 10 KΩ resistor.

SCHEMATIC #8

The eighth sheet is composed of five IPack I/O connectors (J12-J16) for slots A-E respectfully, and five 50-pin connectors (J19 for slot A, J18 for slot B, J20 for slot C, J22 for slot D, J21 for slot E) for the external connection to ribbon cables out the front panel.

SCHEMATIC #9

The ninth sheet contains a group of 0.1 µF filter capacitors and some residual components.

3.0 INSTALLATION

3.1 Unpacking the VMESC5

Table 3-1 lists the contents of the VMESC5 shipping package.

Table 3-1 Contents of VMESC5 Shipping Packages

Qty	Description
1	VMESC5 Printed Circuit Assembly
1	Slot E I/O-to-VMEbus P2 Ribbon Cable (**Optional**) Systran Number: BHAS-RCVMEP2
2	Surfacemount spare fuses (one-1Amp, one-2Amp)
1	VMESC5 User Manual *

* One manual is shipped for each board ordered for orders up to 5 boards. Five manuals will be shipped for orders of over five boards unless additional manuals (up to one per board) are requested. Extra manuals may be purchased by calling SYSTRAN or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR- VMESC5).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visual Inspection of the VMESC5

Examine the VMESC5 to determine if any damage occurred during shipping.

3.3 VMESC5 Installation

NOTE: The VMESC5 is an Electrostatic Sensitive Device (ESD), the hardware installation of the VMESC5 must be conducted on a good anti-static workbench to protect the IPacks and carrier board.

The tools required for the VMESC5 installation are listed in Table 3-2.

Table 3-2 VMESC5 Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

3.3.1 Installation of IPacks on the VMESC5

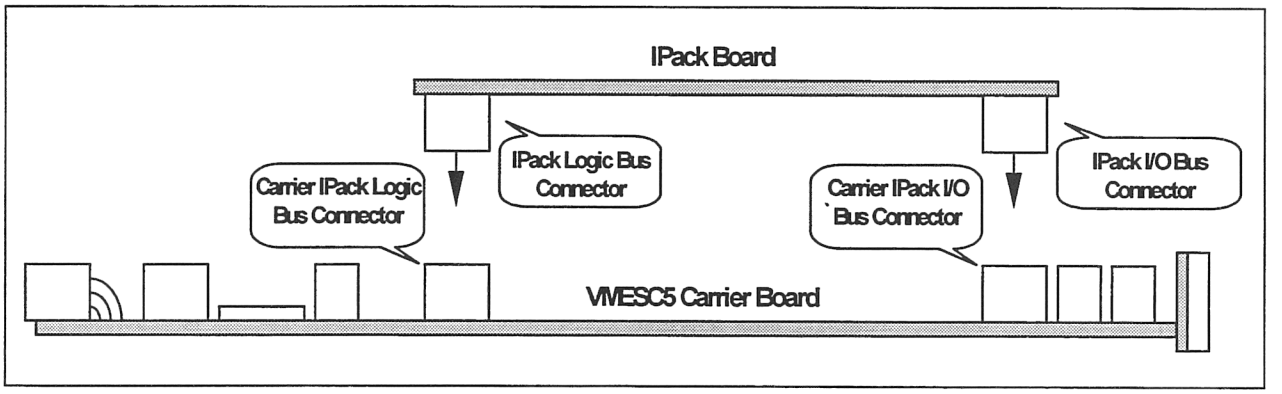


Figure 3-1 Installation of an IPack on the VMESC5

Refering to the appropriate figures and table described below, perform the following steps in removing the VMESC5 from it shipping container (or from an existing installation) and installing IPacks. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.

2a. Remove the VMESC5 from it's shipping container and move it to the ESD controlled area where the installation of the IPacks can be made.

*2b. Remove the VMESC5 from the VME card cage and move it to the ESD controlled area where the installation of the IPacks can be made.

3. Set the VMEbus base address on the J5-J1 jumpers (see Figure 3-2 and Figure 3-3).

4. Install the IPack(s) onto the carrier board by applying adequate and equal pressure to the IPack(s) at both ends and the VMESC5 board.

*5. Install four M2x5mm flat head machine screws onto the IPack's connectors.

*6. Install I/O cables necessary onto VMESC5.

*7. Install the Slot E I/O to VME P2 Ribbon Cable. **See warning below.

8. Install the VMESC5 into desired slot of a VME card cage.

WARNING: When the Slot E I/O-to-VMEbus P2 Ribbon Cable is installed, rows A and C of the VMEbus P2 are connected the 50 I/O pins of slot E and cannot be used in systems with the P2 rows A and C used, but when the cable is NOT installed the VMEbus P2 connector is completely isolated from any on-board signals and can be used in VSB or VXI (with adapter) type systems.

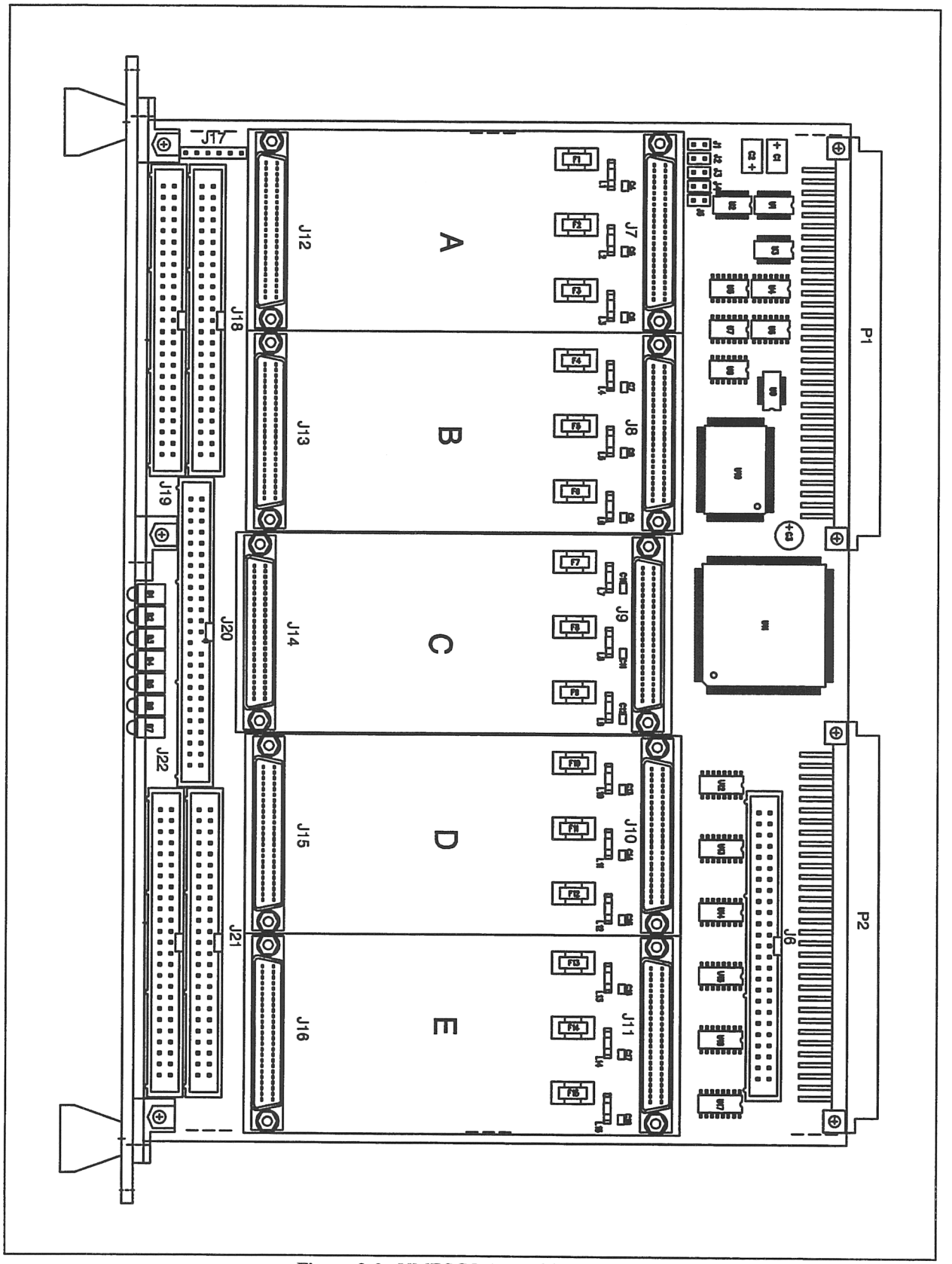


Figure 3-2 VMESC5 Assembly Drawing

3.3.2 VMESC5 VME Base Address

The VMESC5 VME board base address is set with five jumpers J5-J1, correspondence to VME address bits A15 to A11, respectively. Refer to Figure 3-2 and Figure 3-3 for the placement of Jumpers J5-J1 on the VMESC5.

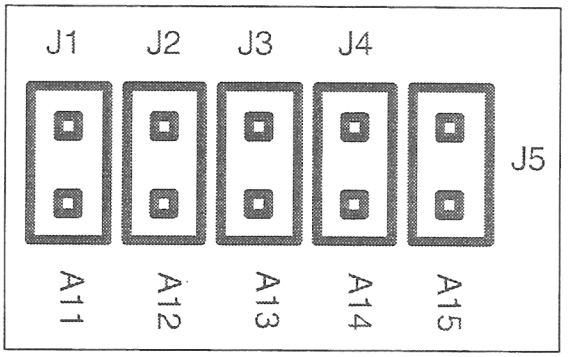


Figure 3-3 VMESC5 Jumpers J5 - J1

Placing a jumper across both posts corresponds to a logic low, or 0, for that address bit. Removing the jumper, or storing it on a single post, corresponds to a logic high, or 1, for that address bit.

EXAMPLE:

The short I/O space on the MVME162 is located from FFFF0000 to FFFFFFFF. In this case, if all jumpers were installed on the VMESC5, it would show up beginning at address FFFF0000. If all jumpers except J3, corresponding to A13, were installed, the VMESC5 would show up at FFFF2000.

Refer to section 4.0 Programming Guide for details of VME accesses to the VMESC5 on-board registers or IPacks.

NOTE: If you are using the MVME162 with OS-9, OS-9 maps the VMEChip2 GCSRs (Global Control Status Registers) to the beginning of short I/O space. This causes a bus conflict with boards placed at this address. To avoid a bus conflict:

1) don't put any VME boards at locations FFFF0000 to FFFF0010;
2) move the GCSR location by changing the Group Select and Board Select values in the VMEChip2 LCSR registers (the 3 bytes starting at FFF4002C); or
3) disable the map decoder by writing an 'F' to the Board Select value (FFF4002E). Refer to the MVME162 manual for more details.

Also, OS-9 probes location FFFF10C0 for a disc controller on power-up. Locating a VME board at this address can cause unpredictable results.

3.3.3 Installation of I/O Cables

The VMESC5 provides easy access to all five IPack I/O connectors. The I/O connectors are located near the front panel where standard 50-pin flat cables can be installed and routed out the edge of the front panel for easy system integration.

All of the VMESC5 IPack I/O connector pin numbers directly correspond to each IPack I/O pinout (i.e. a one-to-one relationship with pin 50 connected to pin 50 down to pin 1 connected to pin 1).

On the VMESC5:

- Connector J19 is the IPack slot "A" I/O cable connector located at the upper left (facing front panel) of Figure 3-2 VMESC5 assembly drawing. It is the closest connector to the front panel at the top of the VMESC5 when installed.
- Connector J18 is for IPack slot "B" and is located just inside of J19.
- The I/O connector J20 is for IPack slot "C" and is located in the middle of the VMESC5's front panel.
- Connector J22 is for IPack slot "D" and is the closest to the front panel at the lower left Figure 3-2 VMESC5 assembly drawing. It is the closest connector to the front panel at the bottom of the VMESC5 when installed.
- Connector J21 is for IPack slot "E". It is the connector just inside of J22. This connector can be used normally like the other four I/O connectors being cabled out the front panel **OR** the IPack slot "E" I/O can be brought out the VMEbus P2 connector via the IPack slot "E" I/O accessory cable to J6 located next to the VMEbus P2.

The short IPack slot "E" I/O cable (Systran part number BHAS-RCVMEP2) is installed over the top of the IPacks in slots "D" and "E". Table 3-3 shows the pin assignments for the VMEbus P2 connector. The signals on the left side of the table the P2 signals, and the signals on the right are those used by the IPack slot E I/O connector.

Table 3-3 VMEbus P2 Row A & C Pin Assignments for the IPack Slot E I/O

VMEbus P2 Pin #	Systran ROWa Signal	Systran ROWc Signal	VMEbus P2 Pin #	Systran ROWa Signal	Systran ROWc Signal
1	SLOTE_IO49	SLOTE_IO50	17	SLOTE_IO17	SLOTE_IO18
2	SLOTE_IO47	SLOTE_IO48	18	SLOTE_IO15	SLOTE_IO16
3	SLOTE_IO45	SLOTE_IO46	19	SLOTE_IO13	SLOTE_IO14
4	SLOTE_IO43	SLOTE_IO44	20	SLOTE_IO11	SLOTE_IO12
5	SLOTE_IO41	SLOTE_IO42	21	SLOTE_IO9	SLOTE_IO10
6	SLOTE_IO39	SLOTE_IO40	22	SLOTE_IO7	SLOTE_IO8
7	SLOTE_IO37	SLOTE_IO38	23	SLOTE_IO5	SLOTE_IO6
8	SLOTE_IO35	SLOTE_IO36	24	SLOTE_IO3	SLOTE_IO4
9	SLOTE_IO33	SLOTE_IO34	25	SLOTE_IO1	SLOTE_IO2
10	SLOTE_IO31	SLOTE_IO32	26	N/C	N/C
11	SLOTE_IO29	SLOTE_IO30	27	N/C	N/C
12	SLOTE_IO27	SLOTE_IO28	28	N/C	N/C
13	SLOTE_IO25	SLOTE_IO26	29	N/C	N/C
14	SLOTE_IO23	SLOTE_IO24	30	N/C	N/C
15	SLOTE_IO21	SLOTE_IO22	31	N/C	N/C
16	SLOTE_IO19	SLOTE_IO20	32	N/C	N/C

NOTE: In Row B, the only pins used on the VMESC5 are pins 1,13, and 32 for +5 V and pins 2, 12, 22, and 31 for ground

3.4 VMESC5 IPack STROBE Connector

IPack Logic Bus connector has a signal called "N_STROBE" and is user defined by the IPack Logic Bus Specification. On the VMESC5 each of the strobe signals are provided through J17 with the IPack slot "A" strobe signal on pin 1 through slot "E" on pin 5 with pin 6 grounded. Each of the strobe signals on the VMESC5 are pulled-up to +5 V via 10 KΩ resistors. The strobe connector (J17) is located at the upper left of Figure 3-2 VMESC5 Assembly Drawing (which is at the top of the VMESC5 when installed).

Table 3-4 VMESC5 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	N_STROBE_A
2	N_STROBE_B
3	N_STROBE_C
4	N_STROBE_D
5	N_STROBE_E
6	GROUND

Table 3-5 show the pin assignments for the VMEbus P1 connector. The signals on the left side are of the original VME specification signal nomenclature, and the signals on the right are those used by SYSTRAN Corp.

Table 3-5 VMEbus P1 Rows A, B and C Pin Assignments

VMEbus P1 Pin #	VMEbus ROWa Signal	Systran ROWa Signal	VMEbus ROWb Signal	Systran ROWb Signal	VMEbus ROWc Signal	Systran ROWc Signal
1	D00	VMED0	BBSY*	N/C	D08	VMED8
2	D01	VMED1	BCLR*	N/C	D09	VMED9
3	D02	VMED2	ACFAIL*	N/C	D10	VMED10
4	D03	VMED3	BG0IN*	N/C	D11	VMED11
5	D04	VMED4	BG0OUT*	N/C	D12	VMED12
6	D05	VMED5	BG1IN*	N/C	D13	VMED13
7	D06	VMED6	BG1OUT*	N/C	D14	VMED14
8	D07	VMED7	BG2IN*	N/C	D15	VMED15
9	GND	GND	BG2OUT*	N/C	GND	GND
10	SYSCLK	SYSCLK_IN	BG3IN*	N/C	SYSFAIL*	N/C
11	GND	GND	BG3OUT*	N/C	BERR*	V_BERR
12	DS1*	VME_DS1	BR0*	N/C	SYSRESET*	V_SYSRESET_IN
13	DS0*	VME_DS0	BR1*	N/C	LWORD*	V_LWORD
14	WRITE*	VME_WRITE	BR2*	N/C	AM5	AM5
15	GND	GND	BR3*	N/C	A23	N/C
16	DTACK*	V_DTACK	AM0	AM0	A22	N/C
17	GND	GND	AM1	AM1	A21	N/C
18	AS*	V_AS	AM2	N/C	A20	N/C
19	GND	GND	AM3	AM3	A19	N/C
20	IACK*	V_IACK	GND	GND	A18	N/C
21	IACKIN*	V_IACKIN	SERCLK*	N/C	A17	N/C
22	IACKOUT*	V_IACKOUT	SERDAT*	N/C	A16	N/C
23	AM4	AM4	GND	GND	A15	VMEA15
24	A07	VME_A7	IRQ7*	V_IRQ7	A14	VMEA14
25	A06	VME_A6	IRQ6*	V_IRQ6	A13	VMEA13
26	A05	VME_A5	IRQ5*	V_IRQ5	A12	VMEA12
27	A04	VME_A4	IRQ4*	V_IRQ4	A11	VMEA11
28	A03	VME_A3	IRQ3*	V_IRQ3	A10	VMEA10
29	A02	VME_A2	IRQ2*	V_IRQ2	A09	VMEA9
30	A01	VMEA1_IN	IRQ1*	V_IRQ1	A08	VMEA8
31	-12V	-12V	+5VSTDBY	N/C	+12V	+12V
32	+5V	VDD	+5V	VDD	+5V	VDD

Table 3-6 shows the pin assignments for each IPack Logic Bus connector. The signals on the left side of the connector are of the original IPack signal nomenclature, and the signals on the right are those used by SYSTRAN Corp. The lower case "x" in the Systran signal name represents the "A", "B", "C", "D", or "E" mnemonic for each IPack slot.

Table 3-6 IPack Logic Bus Pin Assignments

ORIGINAL IPACK SIGNALS NAMES	IPACK LOGIC BUS PIN #	SYSTRAN SIGNAL NAMES	BUSSED OR UNIQUE	X = PULLED UP VIA 10 KΩ RESISTOR
GND	50	GND	GND	GND
Reserved	49	RESERVED1	U	X
Ack*	48	N_IPxACK	U	X
A6	47	VMEA6	B	
Strobe*	46	N_STROBE_x	U	X
A5	45	VMEA5	B	
Intreq1*	44	N_IPxINTREQ1	U	X
A4	43	VMEA4	B	
Intreq0*	42	N_IPxINTREQ0	U	X
A3	41	VMEA3	B	
Error*	40	N_IPxERROR	U	X
A2	39	VMEA2	B	
DMAEnd*	38	N_DMAEND	U	X
A1	37	IPA1	B	
Reserved	36	RESERVED2	U	X
IOSel*	35	N_IPxIOSEL	U	
DMAck0*	34	N_DMACK0	U	X
IntSel*	33	N_IPxINTSEL	U	
DMAReq1	32	N_DMAREQ1	U	X
MemSel*	31	N_MEMSEL	U	X
DMAReq0	30	N_DMAREQ0	U	X
IDSel*	29	N_IPxIDSEL	U	
R/W*	28	V_WRITE	B	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	V_BS1	B	
BS0*	20	V_BS0	B	
D15	19	VLD15	B	X
D14	18	VLD14	B	X
D13	17	VLD13	B	X
D12	16	VLD12	B	X
D11	15	VLD11	B	X
D10	14	VLD10	B	X
D9	13	VLD9	B	X
D8	12	VLD8	B	X
D7	11	VLD7	B	X
D6	10	VLD6	B	X
D5	9	VLD5	B	X
D4	8	VLD4	B	X
D3	7	VLD3	B	X
D2	6	VLD2	B	X
D1	5	VLD1	B	X
D0	4	VLD0	B	X
Reset*	3	N_IPxRESET	U	
CLK	2	ICLK_x	B	
GND	1	GND	GND	GND

NOTE: The IPack data bus, usually defined as IPD[15:0] for all of our IPacks, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "VMESC5 Local Data Bus" designated as VLD[15:0].

4.0 PROGRAMMING GUIDE

4.1 Overview

This section of the manual describes the operation of the VMESC5 from the software perspective, detailing the VMESC5 registers, the overall mapping and addressing scheme for the board, and provides programming examples. A more detailed description of the hardware can be found in section 2.0 DESCRIPTION, and application concepts are discussed in section 6.0 TYPICAL APPLICATIONS.

4.2 Description

The VMESC5 is an easy to use VME6U slave card that holds five singlewide, three singlewide and 1 doublewide, or 1 singlewide and 2 doublewide Industry Pack modules. In addition to providing access to the I/O and ID space of the IPacks via the VME bus, the VMESC5 has 12 onboard control/status registers.

4.3 Board Base Address

The VMESC5 can be located anywhere in the VME short IO space (A16 space address modifier codes 29 *hex* and 2D *hex*) on 2 K byte boundaries by setting the board base address jumpers. These jumpers, J1 to J5, correspond to address lines A11 to A15 respectively. A detailed description of setting the board base address is found in section 2.0.

4.4 Address Map

The IPack IO and ID spaces, and the carrier's control and status registers, reside at a fixed relative address from the VMESC5 base address. Table 4-1 shows the complete memory map for the board.

Table 4-1 VMESC5 Address Map

Address Space or Register Name	VME Address (relative to board base address)	Size
IPack A I/O	Base+000h	128 bytes
IPack A ID	Base+080h	128 bytes
IPack B I/O	Base+100h	128 bytes
IPack B ID	Base+180h	128 bytes
IPack C I/O	Base+200h	128 bytes
IPack C ID	Base+280h	128 bytes
IPack D I/O	Base+300h	128 bytes
IPack D ID	Base+380h	128 bytes
IPack E I/O	Base+400h	128 bytes
IPack E ID	Base+480h	128 bytes
IPack Reset Register	Base+500h - Word Access Base+501h - Byte Access	5 bits
Error Status Register	Base+502h - Word Access Base+503h - Byte Access	5 bits
IPack A Interrupt Register	Base+580h - Word Access Base+581h - Byte Access	6 bits
IPack B Interrupt Register	Base+582h - Word Access Base+583h - Byte Access	6 bits
IPack C Interrupt Register	Base+584h - Word Access Base+585h - Byte Access	6 bits
IPack D Interrupt Register	Base+586h - Word Access Base+587h - Byte Access	6 bits
IPack E Interrupt Register	Base+588h - Word Access Base+589h - Byte Access	6 bits
General Purpose Register A	Base+600h - Word Access Base+601h - Byte Access	8 bits
General Purpose Register B	Base+602h - Word Access Base+603h - Byte Access	8 bits
General Purpose Register C	Base+604h - Word Access Base+605h - Byte Access	8 bits
General Purpose Register D	Base+606h - Word Access Base+607h - Byte Access	8 bits
General Purpose Register E	Base+608h - Word Access Base+609h - Byte Access	8 bits

4.5 Register Descriptions

The VMESC5 registers can be accessed as byte (D8) or word (D16) values. When accessed as words, the upper byte is not driven by the carrier and its value is all '1's due to VLD[15:8] pull-up resistors. The unused bits in the lower byte are driven as 0's on reads. All unused bits are discarded on writes. The hexadecimal VME addresses for the registers shown below are relative to the board base address and are in the format (WORD/BYTE) for word and byte accesses respectively.

4.5.1 Reset Register (500/501)

Setting one of the bits RES_E through RES_A to a one, asserts the corresponding IPack's reset line. The bits can be set individually by writing a '1' to that bit or simultaneously with a single write of '1F' *hex*. When set, a one shot is triggered supplying a minimum 200 ms reset pulse as required by the IPack specification. When read, these bits return the status of the corresponding IPack's reset line (a'0' means the IPack is not being reset, a '1' means it is in a reset condition).

Table 4-2 Reset Register Bit Description

Bit #	B15-B8	B7-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	RES_E	RES_D	RES_C	RES_B	RES_A
R/W	Reads '1's Writes discarded	Read '0's, Writes discarded	R/W	R/W	R/W	R/W	R/W
Power up State	N/A	N/A	0	0	0	0	0

NOTE: RES_E-RES_A: Reset bits for IPack slots E to A.

4.5.2 Error Status Register (502/503)

These bits indicate the state of the corresponding IPack N_xERROR. If the N_xERROR* signal is asserted (active low) for a particular IPack, then the corresponding ERR_N bit will be set to a 1. If the error signal is not asserted, then the corresponding bit will be cleared.

Table 4-3 Error Status Register Bit Description

Bit #	B15-B8	B7-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	ERR_E	ERR_D	ERR_C	ERR_B	ERR_A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R	R	R	R	R
Power up State	N/A	N/A	State of IPack E ERR* Signal	State of IPack D ERR* Signal	State of IPack C ERR* Signal	State of IPack B ERR* Signal	State of IPack A ERR* Signal

NOTE: ERR_E-ERR_A: Error Status bits for IPack slots E to A.

4.5.3 Interrupt Level Registers A to E (580/581 to 588/589)

The three interrupt level bits, IL2-IL0, determine the interrupt request level that will be asserted on the VME bus when the corresponding IPack IRQ line is asserted. Valid interrupt levels are 1 to 7. A value of '0', not a valid interrupt request level, will not assert a VME interrupt request. Thus, a value of '0' can be written to these registers to disable interrupts.

The interrupt requests are prioritized first by interrupt request level, then by slot position. Level 7 interrupt requests are the highest priority and level 1 is the lowest. Equal interrupt request levels are serviced in the slot prioritized order A0, A1, B0, ... D1, E0, E1. See section 2.0 DESCRIPTION for more details regarding interrupt prioritization.

Table 4-4 Interrupt Level Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	0	IRQ 1 IL2	IRQ 1 IL1	IRQ 1 IL0	0	IRQ 0 IL2	IRQ 0 IL1	IRQ 0 IL0
R/W	Reads '1's Writes discarded	Read '0' Writes discarded	R/W	R/W	R/W	Read '0' Writes discarded	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: IRQN IL2-IL0: The interrupt level bits for IRQN.

4.5.4 General Purpose Registers A to E (600/601 to 608/609)

General purpose registers A to E are completely user definable. These read/write registers can be used for semaphores, shared memory, etc. See section 6 "Typical Applications" for more application information regarding these registers.

Table 4-5 General Purpose Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	GPR7	GPR6	GPR5	GPR4	GPR3	GPR2	GPR1	GPR0
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: GPR7-GPR0: The General Purpose Register byte value.

4.6 VMESC5 Programming Examples

The following examples illustrate how to program the VMESC5 to achieve various operational modes.

4.6.1 Reset Example

This example resets one, then all five IPacks, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IPack reset signal (the one-shot asserts the reset signal for approximately 240 ms). The reset signal can then be monitored by reading the Reset register to determine when it is de-asserted.

- Write '0001' *hex* to the Reset register. This resets the IPack module in slot A by asserting the IPack A reset signal.

LOOP1:

- Read the Reset register.
- If Bit 0 is set then go to LOOP1.
- Write '001F' *hex* to the Reset register. This resets all five IPack modules by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of bits [4:0] are set then go to LOOP2.

4.6.2 Interrupt Initialization Example

Interrupts in the VME system are prioritized in a two tier fashion:

- The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest.
- The second tier of prioritization is determined by the relative position in the interrupt daisy chain.

The closer the interrupt requester is to the interrupt handler in the daisy chain, the higher its priority for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location and the IPack slot location on the VMESC5 carrier. The VMESC5 IPack slot priority order from highest to lowest is A0, A1, B0, ... D1, E0, E1. See section 2.0 or section 6.0 for more details regarding interrupt prioritization. The following examples illustrate several interrupt service priority schemes.

EXAMPLE 1

In this example, all interrupters are set to the same interrupt request level.

- Write '0011' *hex* to Interrupt Level register A
- Write '0011' *hex* to Interrupt Level register B
- Write '0011' *hex* to Interrupt Level register C
- Write '0011' *hex* to Interrupt Level register D
- Write '0011' *hex* to Interrupt Level register E

Now all ten interrupt sources are set to interrupt request level 1. If all ten sources assert an interrupt request at the same time, they will be serviced in the following order: A0, A1, B0, B1, C0, C1, D0, D1, E0, E1.

EXAMPLE 2

In this example, the interrupt request levels are set to different values to illustrate that the interrupt request level prioritization take precedence over the slot prioritization.

- Write '0011' *hex* to Interrupt Level register A
- Write '0022' *hex* to Interrupt Level register B
- Write '0032' *hex* to Interrupt Level register C
- Write '0054' *hex* to Interrupt Level register D
- Write '0076' *hex* to Interrupt Level register E

For this configuration, if all ten sources assert an interrupt request at the same time, they will be serviced in the following order: E1, E0, D1, D0, C1, B0, B1, C0, A0, A1.

NOTE: It is not normally possible to assert simultaneous interrupt requests, except via special IPacks like the Systran TESTIP.

5.0 PERFORMANCE

5.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in sections 1.0: INTRODUCTION and 2.0: DESCRIPTION.

5.2 State Timing Diagrams

The VMESC5 test configuration consisted of a typical VME card cage with a MVME-162-23 as the host CPU and one Systran TESTIP installed in slot 'A' (refer to Figure 5-1 for the performance test equipment configuration). For Figures 5-2 through 5-10 the state waveforms were made using the HP 1 GHz Timing Master Module and the Systran IPack Logic Bus Extender (IPLBE) with the IPack Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer's screen are active low, and are represented by a 'V_' or a 'N_' as the first characters to indicate active low signals.

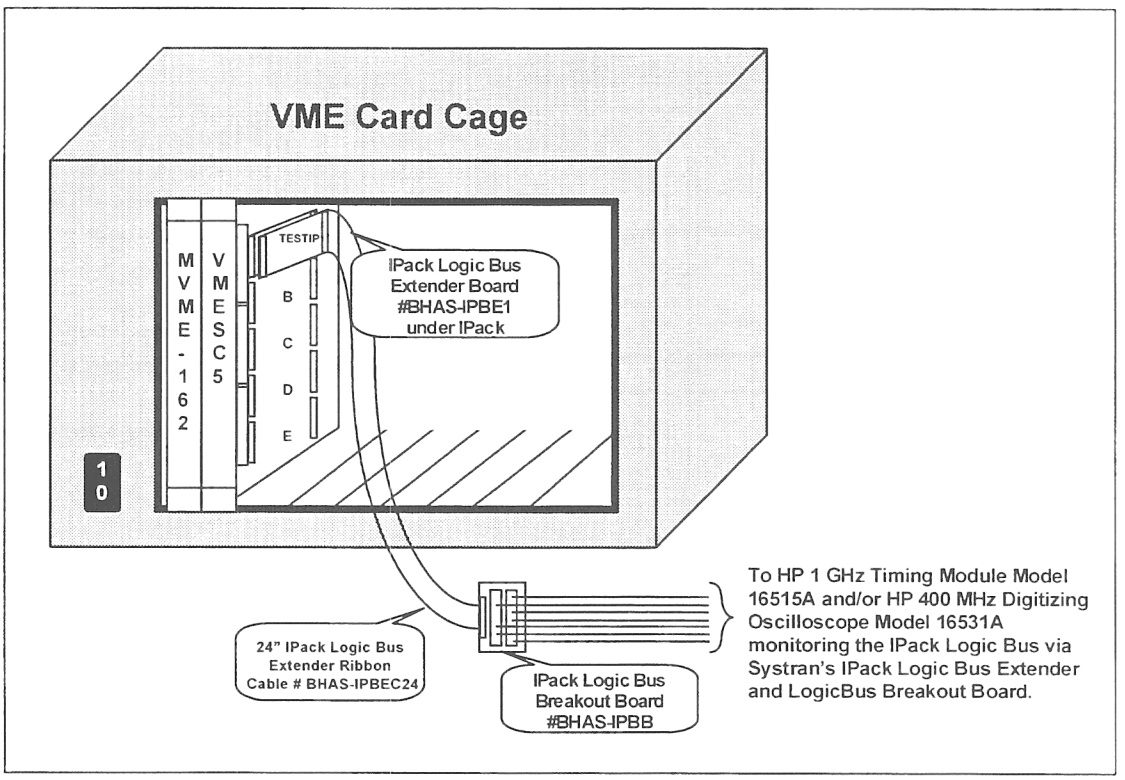


Figure 5-1 Performance Test Equipment Configuration

5.2.1 ID Read Cycle

Figure 5-2 is a complete ID read cycle of the TESTIP on the VMESC5 in slot 'A'. On the left side of the figure the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IPack read cycle by asserting the ID_SEL signal. The VMESC5 always begins an IPack select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IPack terminate cycle. On the right side of the figure the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME Read cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME read cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME read cycle is complete in three IPack (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

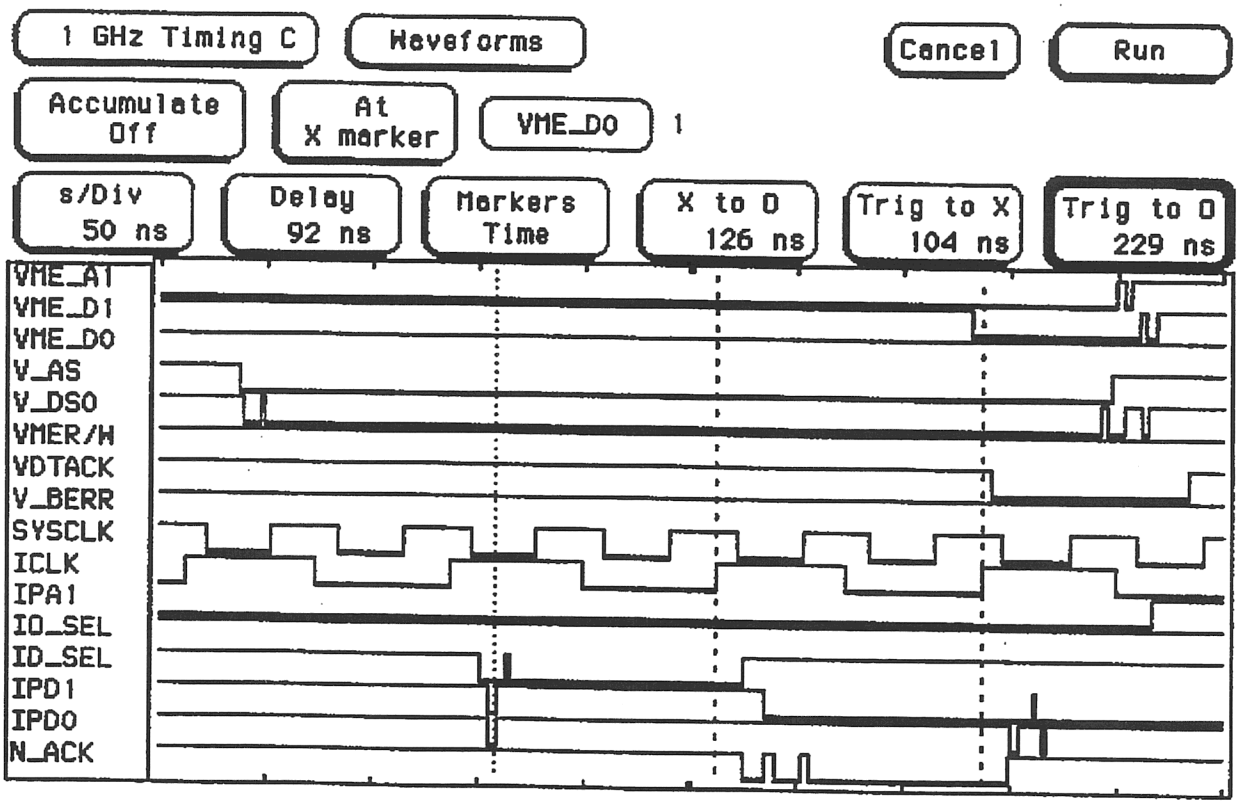


Figure 5-2 ID Read

5.2.2 I/O Read Cycle

Figure 5-3 is a complete I/O read cycle of the TESTIP on the VMESC5 in slot 'A', which is functionally the same as the ID read cycle. On the left side of the figure, the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IPack read cycle by asserting the IO_SEL signal. The VMESC5 always begins an IPack select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IPack terminate cycle. On the right side of the figure, the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME read cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME read cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME read cycle is complete in three IPack (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

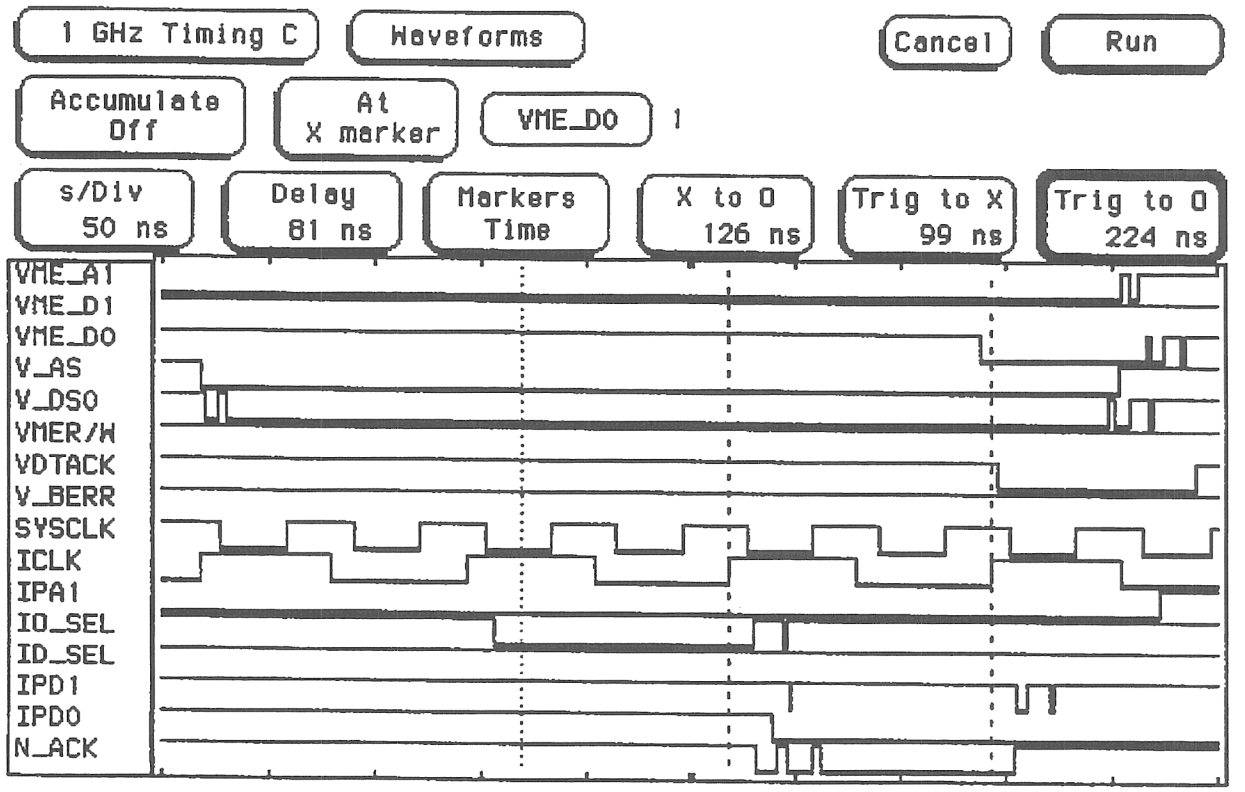


Figure 5-3 I/O Read

5.2.3 I/O Write Cycle

Figure 5-4 is a complete I/O write cycle to the TESTIP on the VMESC5 in slot 'A', which is functionally the same as the ID write cycle. On the left side of the figure, the MVME-162 initiated a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal, and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IPack write cycle by asserting the IO_SEL signal. Again, the VMESC5 begins an IPack select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP asserts the N_ACK signal to complete the IPack terminate cycle, and the VMESC5 drives the IPack data bus with the VMEbus data. The TESTIP latches the data from the VMEbus on the rising edge of ICLK (at the end of the terminate cycle). About 9 or 10 nanoseconds after the TESTIP latched the data, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME write cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME write cycle the VMESC5 de-asserts the VDTACK signal. The entire VME write cycle is complete in three IPack (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

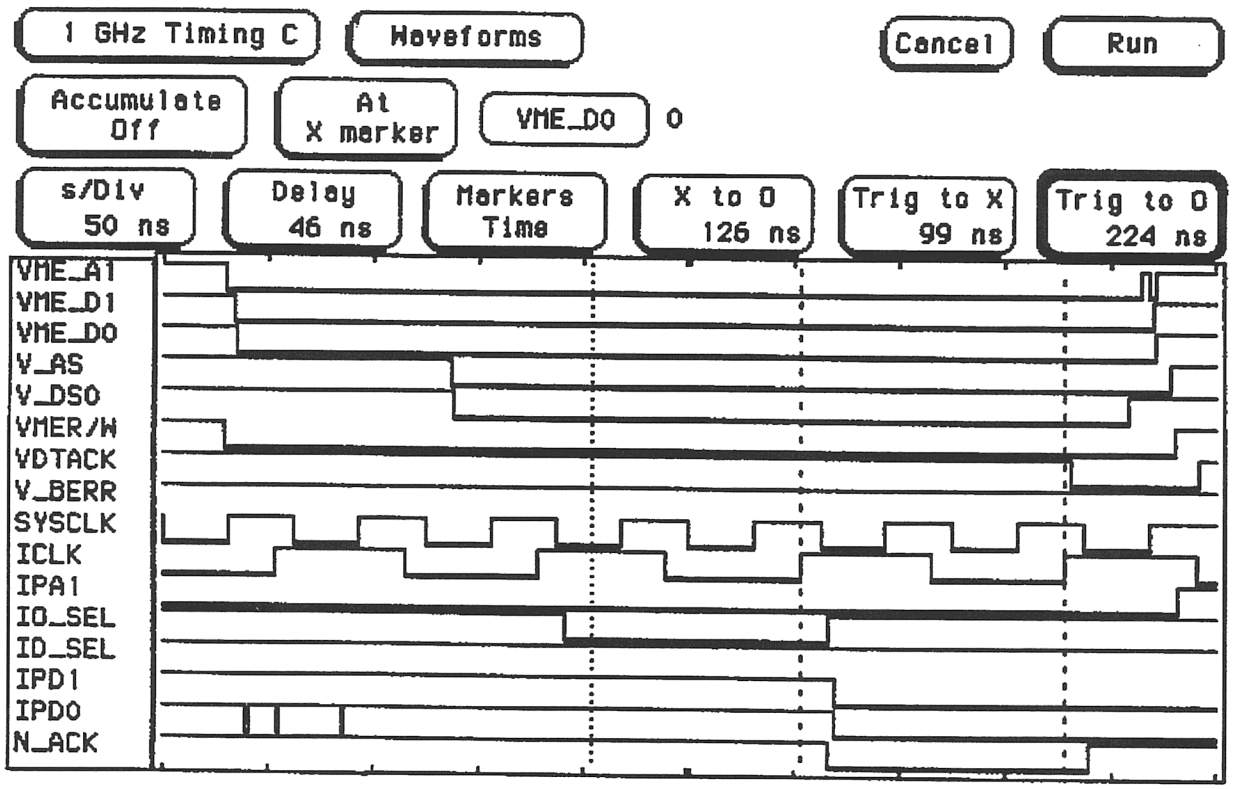


Figure 5-4 I/O Write

5.2.4 I/O Read-Modify-Write Cycle

Figure 5-5 is a complete I/O read-modify-write cycle to the TESTIP on the VMESC5 in slot 'A'. On the left side of the figure, the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. The read cycle completes as in Figure 5-2 and then in the center of the Figure 5-5, the VME host CPU de-asserts the data strobe signal while keeping the address strobe asserted. A few clock cycles later, the host CPU begins a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal and then re-asserting the VME data strobe (V_DS0) signal. On the right side of Figure 5-5, the write cycle terminates normally as in Figure 5-2, completing the VME read-modify-write cycle. Notice that the complete read-modify-write cycle was executed by the host CPU in approximately 1.3 µs.

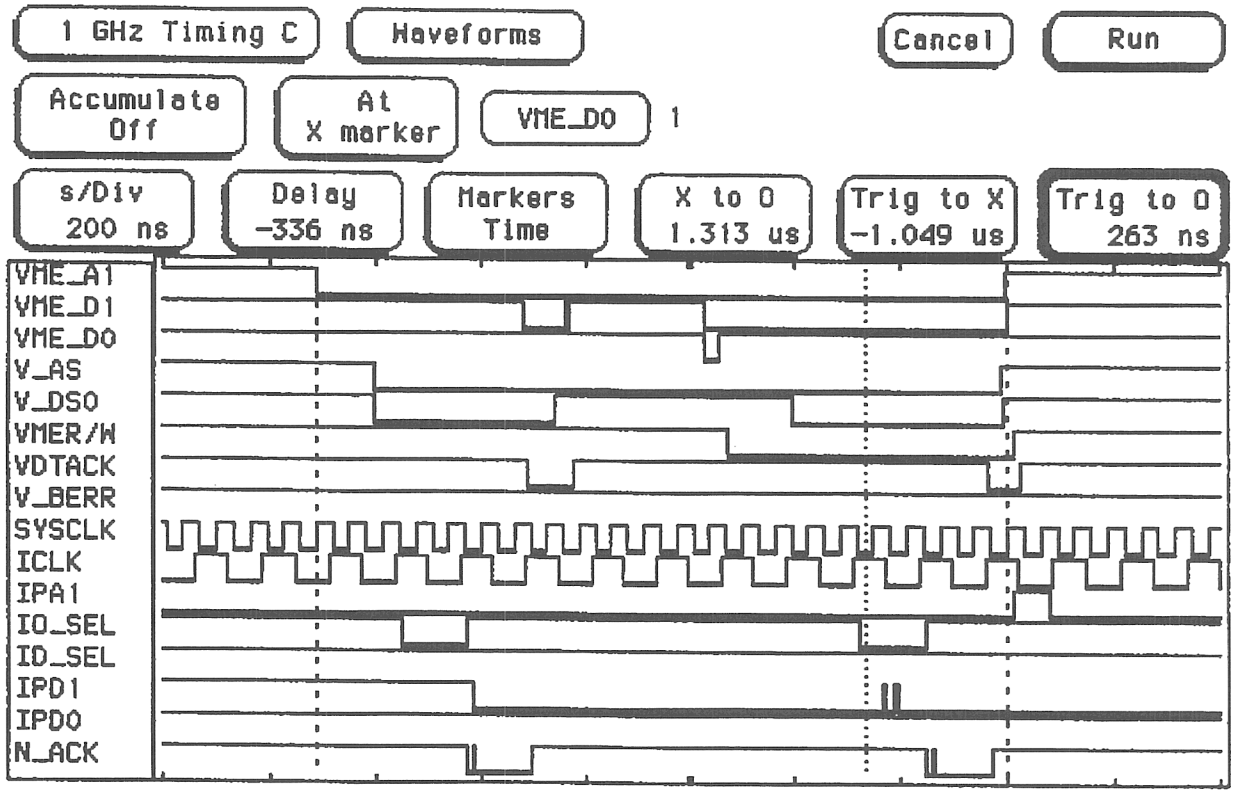


Figure 5-5 Read-Modify-Write

5.2.5 I/O Write Cycle With IPack Wait States

Figure 5-6 is a complete I/O write cycle to the TESTIP on the VMESC5 in slot 'A', similar to Figure 5-4 except with IPack wait states inserted. On the left side of the figure the MVME-162 initiated a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, the VMESC5 DTE begins an IPack write cycle by asserting the IO_SEL signal. In the center of the figure, the TESTIP has inserted five IPack wait states then asserts the N_ACK signal to complete the IPack terminate cycle. Then on the right side of the figure, the write cycle terminates normally as in Figure 5-4 completing the VME write cycle with wait states. Note, the VMESC5 will support ID, IO, and Interrupt IPack cycles with wait states inserted.

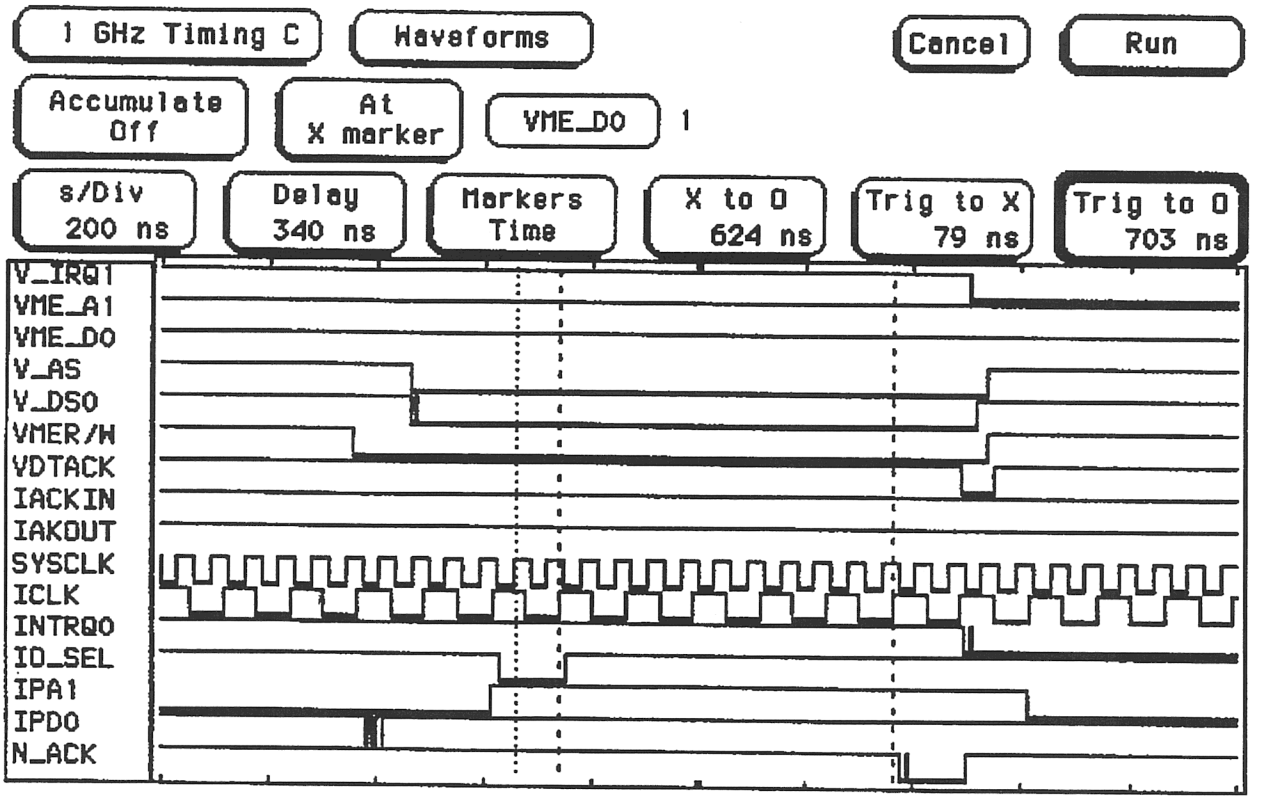


Figure 5-6 I/O Write With Wait States

5.2.6 Interrupt Request

Figure 5-7 is a waveform view of a complete interrupt request from the TESTIP and the following interrupt service routing (ISR) from the MVME-162 host CPU. For this test, the VMESC5 was configured to drive the VME interrupt level one request (V_IRQ1) when the TESTIP asserted the IPack interrupt request signal zero (INTRQ0). On the left side of the figure, the TESTIP has asserted the INTRQ0 and about 1.5 µs later the host CPU began the ISR with an interrupt acknowledge cycle fetching the interrupt vector from the TESTIP. In the center of the figure, the host CPU reads a status register on the TESTIP and then on the right side of the figure, the host CPU terminates the interrupt request and the end of the ISR. Figures 5-8 and 5-9 show more detail timing data of the VMESC5 interrupt cycles.

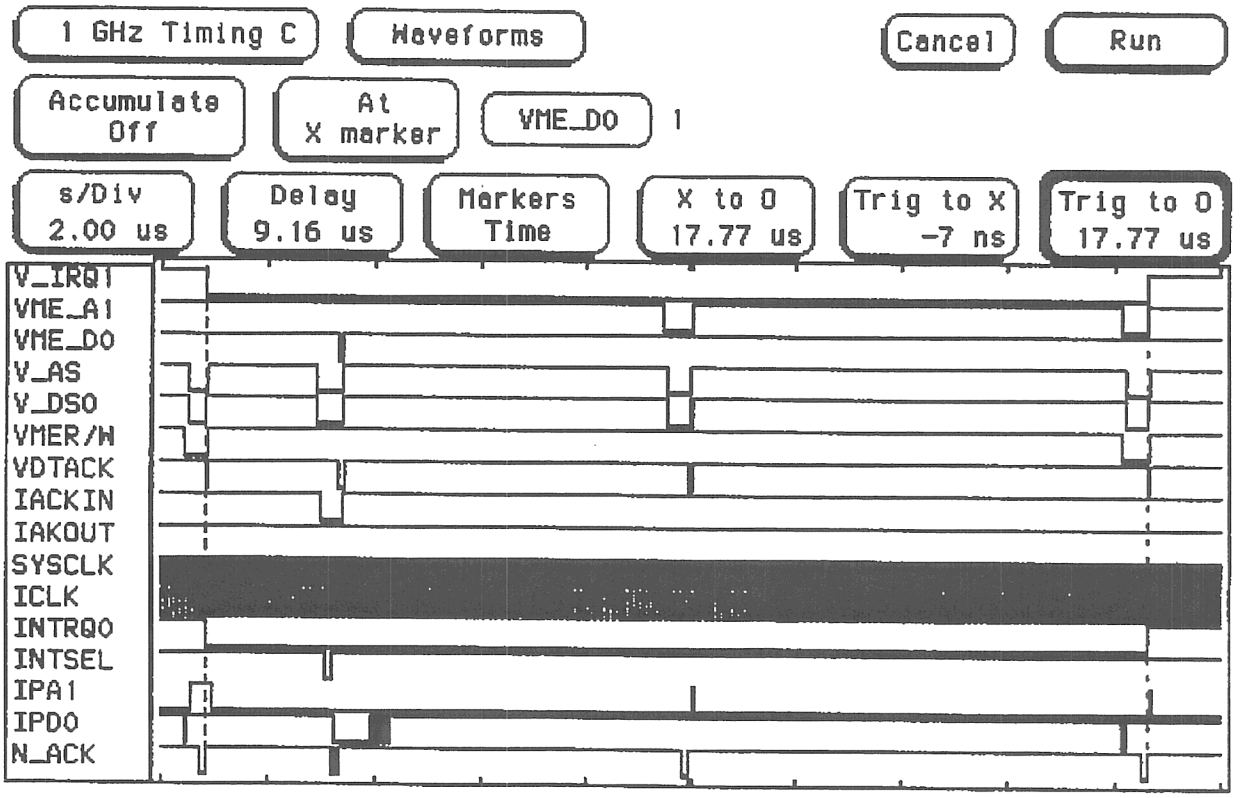


Figure 5-7 Complete Interrupt Request and Service Routine

Figure 5-8 is a zoomed in view of the TESTIP driving the INTRQ0 signal and in turn the VMESC5 driving the VME interrupt request level one signal (V_IRQ1) in about 14 ns.

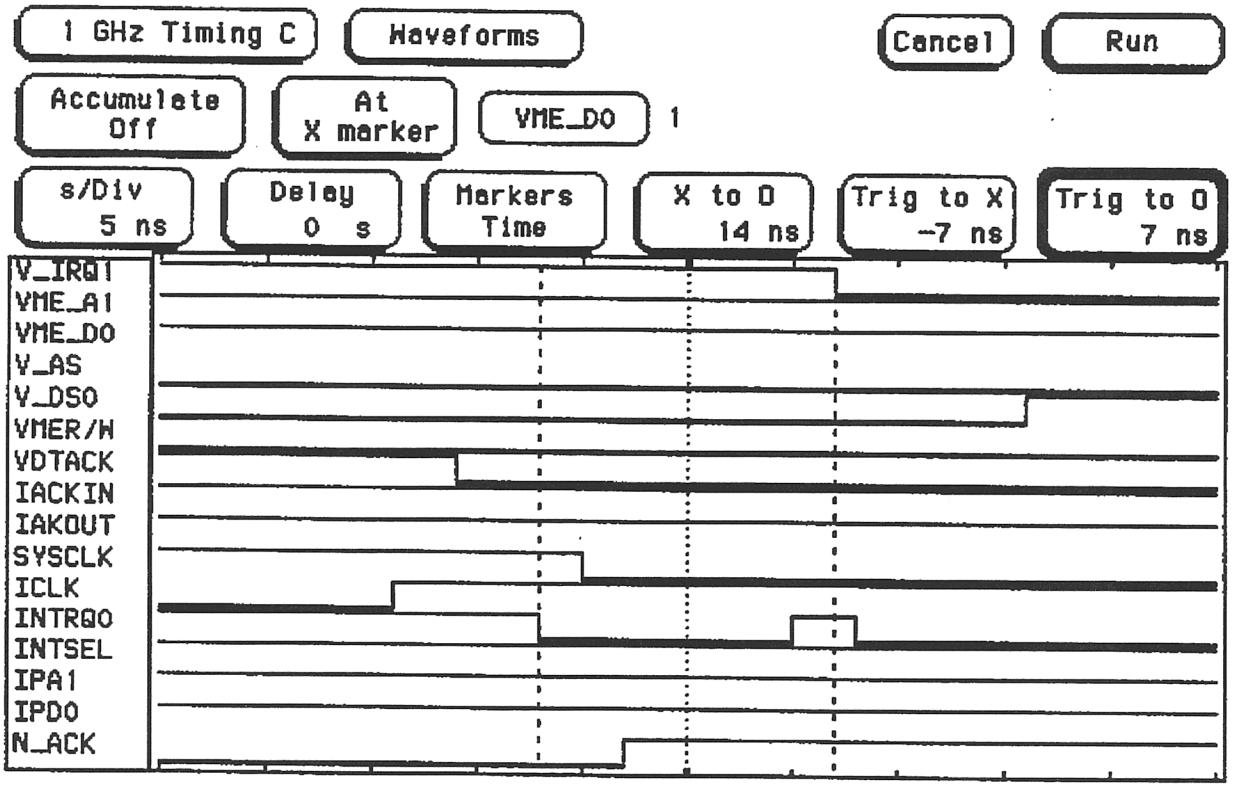


Figure 5-8 IPack INTREQ0 Driving VME IRQ1

Figure 5-9 is a zoomed in view of the TESTIP placing an interrupt vector onto the VME data bus. This interrupt vector cycle functions the same as the ID and IO read cycles. On the left side of the figure, the MVME-162 initiated an interrupt acknowledge cycle by asserting a valid address (for the interrupt level being serviced) and then asserting the VME address, data strobe, and interrupt acknowledge input (V_AS, V_DS0, and IACKIN) signals. Next in the center of the figure, the VMESC5 interrupt engine determines if this interrupt acknowledge cycle is for this IPack and of so begins an IPack interrupt cycle by asserting the INTSEL signal. The VMESC5 always begins an IPack select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IPack terminate cycle. On the right side of the figure, the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME interrupt acknowledge cycle by de-asserting the address and data strobes, and IACKIN signals. After the VME host CPU terminates the VME interrupt acknowledge cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME interrupt acknowledge cycle is complete in three IPack (8 MHz) clock cycles (which is 375 ns). Again the VMESC5 worst and best case access times are plus or minus one 16 Mhz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

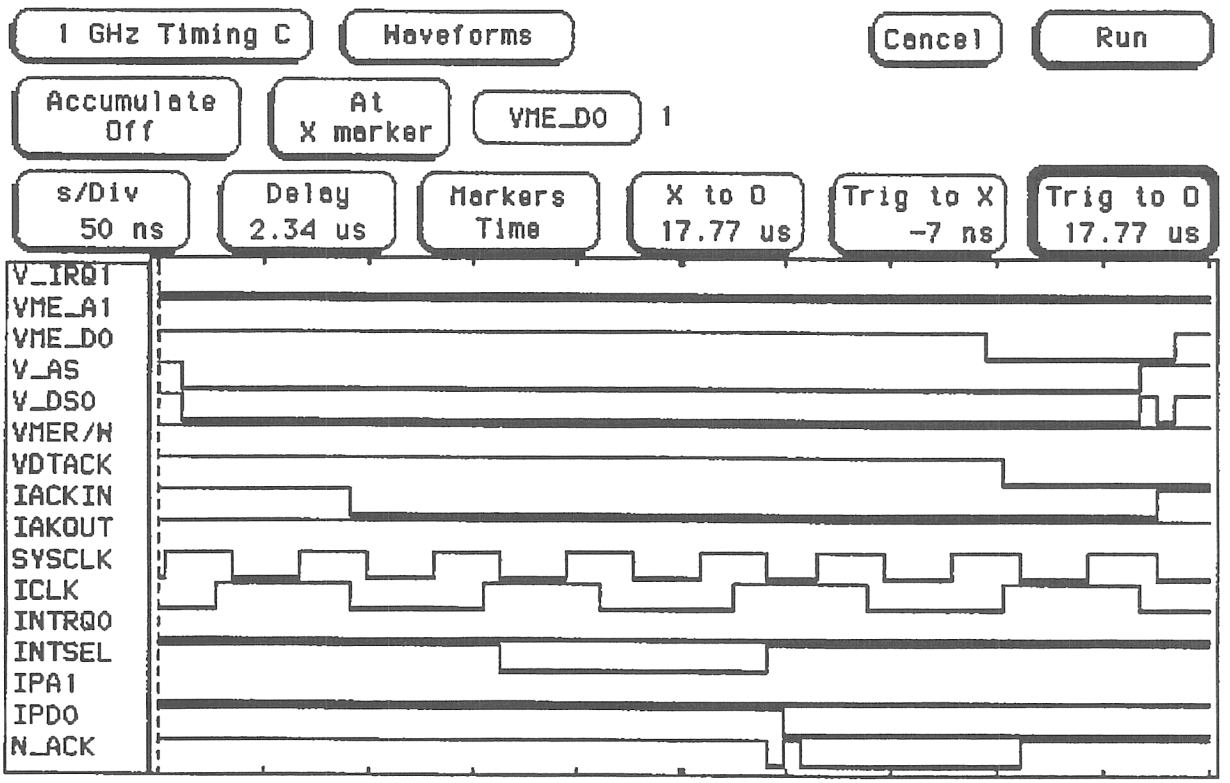


Figure 5-9 IPack Interrupt Vector Cycle

Figure 5-10 is a zoomed in view of the VMESC5 driving the VME IACKOUT (IACKIN on the waveform screen) signal in about 64 ns. In this figure, the VMESC5 interrupt engine determined that this interrupt acknowledge cycle was not for any of its IPacks and very quickly passed on the IACKOUT signal in the VME daisy-chain.

NOTE: Figure 5-10 is very important information for users concerned about system response time with the VME IACKOUT daisy-chain signal being passed along by the VMESC5 in about 64 nanoseconds. This means that the VMESC5 will not cause a VME system time-out or bus error by driving the IACKOUT signal as fast as possible. If a VME card cage had one host CPU (VME bus master) and twenty VMESC5 IPack carriers installed, the last VMESC5 (furthest from the host CPU) with an IPack in slot 'E' will see the IACKIN signal in about 1.3 µs.

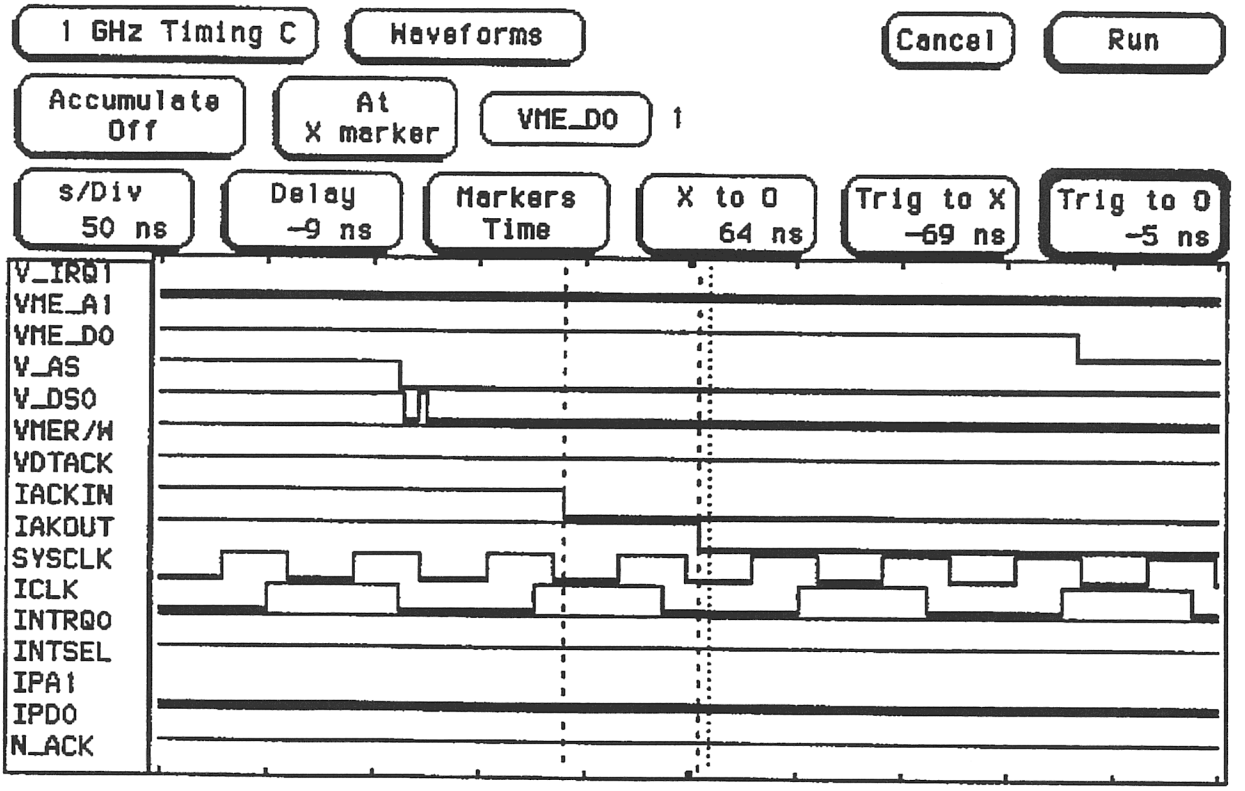


Figure 5-10 VME IACKIN to IACKOUT

6.0 TYPICAL APPLICATIONS

6.1 Applications

SYSTRAN extends an open invitation to all users to freely submit their applications that might, or do, use the VMESC5 Slave Carrier to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the SYSTRAN team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and SYSTRAN reserves the right to modify submissions to provide for more generic appeal, when necessary.

6.2 Sharing IPacks between Multiple VME Masters

It is sometimes desirable for multiple VME bus masters to share IPack module resources. In this case, a semaphore is typically used to lock out access to the resource when it is in use. This example illustrates using the General Purpose registers on the VMESC5 for this purpose.

Figure 6-1 depicts a system that is comprised of two VME masters, and one or more VMESC5 carriers populated with I/O modules, in a process monitor and control application. In this hypothetical system, one master performs the process control functions while the second master monitors all of the I/O data values and reports the

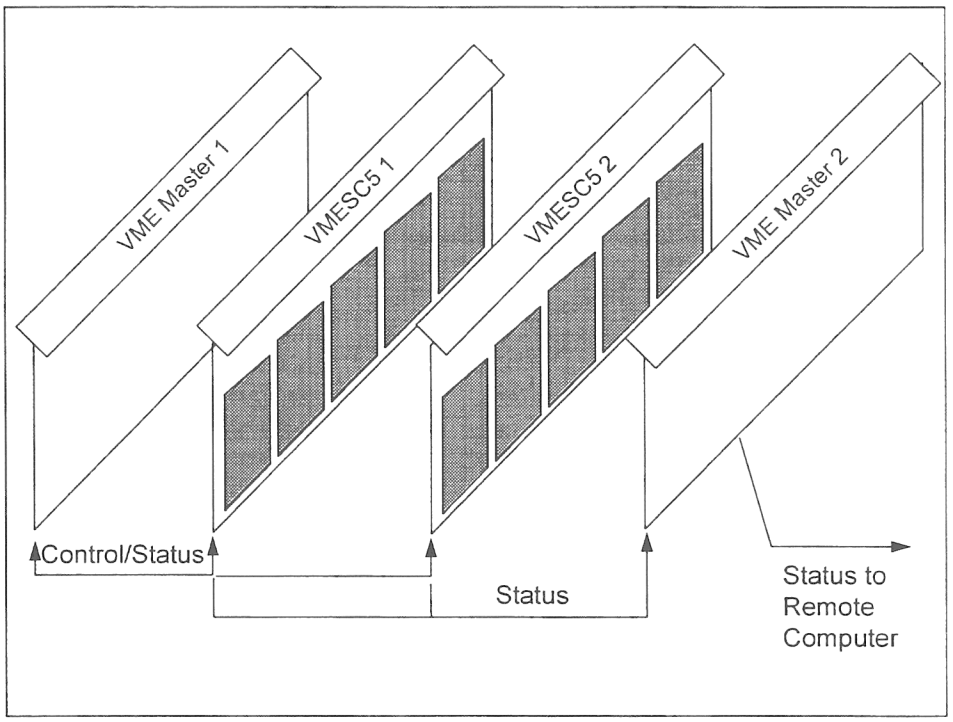


Figure 6-1 A System With Two VME Masters

information to a remote computer. The second master is presumably used because one master cannot handle both the process control and communication functions.

The data being reported to the remote computer from any one IPack must be from the same frame. To insure this requirement is met, a separate semaphore is used for each IPack. The exchange of data between the VME masters and the IPacks would then go something like this, where "x" is the last IPack module on the last carrier:

6.2.1 VME Master 1

- Reserve IPack A semaphore (in General Purpose register A). If not available then wait until it is available.
- Set the new output values for IPack module A.
- Release IPack A semaphore.

•
•
•

- Reserve IPack x semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Set the new output values for IPack module x.
- Release IPack x semaphore.

6.2.2 VME Master 2

- Reserve IPack A semaphore (in General Purpose register A). If not available then wait until it is available.
- Read the data from IPack module A.
- Release IPack A semaphore.
- Send the IPack A data to the remote computer.

•
•
•

- Reserve IPack x semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Read the data from IPack module x.
- Release IPack x semaphore.
- Send the IPack x data to the remote computer.

This is just one example of using the General Purpose registers. They are completely user definable and therefore can be used for any purpose.

6.3 Configuring Interrupts for Multiple Priority Schemes

Some systems must run more than one application for a given hardware configuration. The two applications may require two distinct interrupt priority schemes. This example illustrates how to configure the interrupt level registers on the VMESC5 to achieve two different priority schemes.

The following assumptions are used for this example:

1. The two applications each use five IPacks, A through E.
2. Each IPack utilizes interrupts IRQ0 and IRQ1.
3. Application one requires that the interrupts be serviced in the following order:
   C0, C1, B0, B1, A0, A1, D1, D0, E0, E1.
4. Application two requires that the interrupts be serviced in the following order:
   D1, E1, D0, E0, C0, C1, A0, A1, B0, B1.
5. Interrupt level 7 should not be used.

Recall that the IACK daisy chain slot priority is:
A0, A1, B0, B1, C0, C1, D0, D1, E0, E1
which represents the servicing order for equal level interrupt requests. Therefore, the solution is to set interrupt request levels to override the slot priority, where necessary, to achieve the desired servicing order.

To achieve the desired servicing order for application one, the interrupt levels could be set as follows:

- Write '0033' *hex* to Interrupt Level register A
- Write '0044' *hex* to Interrupt Level register B
- Write '0055' *hex* to Interrupt Level register C
- Write '0032' *hex* to Interrupt Level register D
- Write '0022' *hex* to Interrupt Level register E

To achieve the desired servicing order for application two, the interrupt levels could be set as follows:

- Write '0022' *hex* to Interrupt Level register A
- Write '0022' *hex* to Interrupt Level register B
- Write '0033' *hex* to Interrupt Level register C
- Write '0054' *hex* to Interrupt Level register D
- Write '0054' *hex* to Interrupt Level register E

In both cases, there is more than one possible combination of Interrupt Level register settings that could be used to produce the desired results.

7.0 WARRANTY AND REPAIR

7.1 Warranty Coverage

SYSTRAN makes no warranty of any kind, express or implied, with regard to products, except that SYSTRAN warrants that products delivered will be free from defects in materials or workmanship for a period of three hundred sixty five (365) days from the date of original shipment. During the warranty period, SYSTRAN will provide, free of charge to Buyer, the Warranty Services defined below:

7.1.1 Hardware Warranty Service

Hardware Warranty Service consists of factory exchange or repair (at SYSTRAN's sole option) of defective Hardware Products to correct malfunctions which occur during normal use. In the event SYSTRAN decides to replace a failed part or piece of equipment, SYSTRAN shall have the right to replace it with either a new part or piece of equipment, or factory reconditioned part or piece of equipment. Replaced parts or pieces of equipment become the property of SYSTRAN.

Hardware Warranty Services do not include the repair or replacement of equipment or parts which have otherwise become defective, including, but not limited to, damage caused by accidents, modifications or alterations by Buyer, physical abuse or misuse, operation in an environment or conditions outside SYSTRAN's specifications for the Hardware Products, acts of God, and fires. Hardware Warranty Services also exclude labor and material cost of relocation, rearrangement, additions to, and removal of Hardware Products.

Buyer must report hardware malfunction to SYSTRAN Customer Service and obtain a Return Authorization Number. Defective hardware should then be shipped prepaid to SYSTRAN. Repair or replacement will then be returned prepaid upon receipt of the defective item.

7.1.2 Software Warranty Service

Software Warranty Service consists of update services covering changes to any combination of documentation and software required to maintain Software Products at the revision level most currently released by SYSTRAN. This Software Warranty Service does not include changes or upgrades, or options intended to broaden, enhance or improve the capabilities of the Software Product.

7.1.3 Other Services

Also included in the Warranty Services for the covered Products are periodic newsletters announcing new products and applications, and application notes.

THE FOREGOING WARRANTIES ARE IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ANY WARRANTY THAT EQUIPMENT PURCHASED HEREUNDER IS OF MERCHANTABLE QUALITY.

7.2 Additional Paid Services

Should Buyer request services which are beyond the scope of the Hardware, Software or Other Warranty Services specified above, these will be provided by SYSTRAN on a time-and-materials basis at the prices in SYSTRAN's published Price List. Such services will then be undertaken by SYSTRAN after SYSTRAN has given Buyer an estimate of the services required and only after SYSTRAN receives written authorization from Buyer.

7.3 Term

This Warranty is effective for a period of three hundred sixty five (365) days from the date of the original shipment.

7.4 Conditions

Services provided under this Warranty are performed at the SYSTRAN factory, Monday through Friday, 8:00 a.m. through 5:00 p.m. Eastern Standard/Daylight Savings Time, excluding SYSTRAN's holidays. SYSTRAN's performance goal is to ship to Buyer a repaired or replacement Hardware Product within 48 hours of SYSTRAN's receipt of the defective Hardware Product.

7.5 Identification of Covered Products

Products covered by this Agreement shall be identified by their SYSTRAN Serial Numbers which will be affixed on the respective product.

7.6 Shipping

When factory repair services are required, Buyer shall ship or deliver products, freight prepaid, to the SYSTRAN factory. SYSTRAN will return Products, freight prepaid, to Buyer. SYSTRAN reserves the right to select the carrier and shipping method for return shipments. Upon request, Products will be shipped by Buyer's carrier or by a Buyer-specified shipping method for return shipments. Any shipping charges incurred by SYSTRAN for such Buyer-specified shipping will be invoiced separately to Buyer.

7.7 Life Support and Nuclear Policy

SYSTRAN products are not authorized for and should not be used as critical components in life support systems or nuclear facility applications without the specific written consent of SYSTRAN Corp. As used herein:

- Life support devices or systems are those which support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.
- Examples of nuclear facility applications are those (a) in a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabrication, alloying, storing, or disposal of fissionable material or waste products thereof.

SYSTRAN's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequential damages. Buyer uses or sells such products for life support or nuclear facility applications at Buyer's own risk and agrees to defend, indemnify, and hold SYSTRAN Corp. harmless from any and all damages, claims, suits, or expense resulting from such use.

7.8 Communication

Contact SYSTRAN Customer Support by calling (513) 252-5601, or send an E-Mail message to **support@systran.com** for assistance.

APPENDIX A

SYSTRAN CORPORATION's
IP SPECIFICATION SYNOPSIS
of the IndustryPack® Specification, Rev. 0.7.1

INTRODUCTION:

This document provides an overview of the specifications that form the interface guidelines of a family of versatile mezzanine boards that typically fall into the class of I/O products. These boards reside on carriers that provide the host function interface, and are often bus adapters to many common busses. The small form-factor, low power, and generic features of these boards provide the designer and/or user with a powerful, and inexpensive technique for solving data acquisition, process control, and general purpose interface requirements.

This specification abstract provides technical information to a detail level that is sufficient enough to comprehend the functionality of the specification, if not enough for design purposes. It does not provide the reader with enough information to deal with some of the pending issues concerning DMA operations, and high speed (32 MHz) transfer techniques. The primary focus of the discussions are for "singlewide" boards, with a brief discussion of "doublewide" board characteristics. For additional information beyond that which is contained within this document, we recommend that the reader obtain the full specification upon which this document is based.

Naming conventions adopted for this document vary from the original specification to provide the system level architect a means by which to differentiate IndustryPack signal names from other system component names. Where differences exist between the original specification and those used by SYSTRAN, both names are cited. It is also important to note that the references IndustryPack, "IP", and "IPack" for these boards are synonymous.

The fundamental transfer types, and their maximum sizes, that are currently supported by the specification include: 128 bytes of read/write I/O space, 8 MBytes of read/write memory space, 32 bytes of read-only ID (PROM) space, and read capability of up to 2 separate interrupt vectors. These numbers are all doubled for a "doublewide" board. All transfers between the IP board and its carrier occur synchronously, driven by a carrier-supplied 8MHz clock, all through a single, 50-pin "logic" connector. All I/O interfacing with the "real-world" is accomplished through another, 50-pin "I/O" connector, whose functions are defined by the IP supplier, and not the specification.

The 3.9″ by 1.8″ size allows for convenient modular placement of 1, 2, 4, or 6 IPs per carrier, depending upon the host platform being used as a carrier. Many "smart" and "dumb" bus-based carriers already exist, including: EXMbus, G-96, VME-3U, Nubus, VME-6U, ISA, "C" size VXIbus, and VME-9U, as well as stand-alone (embedded processor) carriers of various sizes. A "doublewide" IP is 3.9″ by 3.6″ in size, and appears mechanically and electrically as two "singlewide" IPs side-by-side, consisting of an a-side and a b-side.

SIGNAL DESCRIPTIONS:

The following text briefly defines the "logic" signals that interface the IP to its carrier (for singlewide configurations). The reader is reminded that the " I/O" signals and their usage are completely independent of this specification (except for the connector used), and are defined by the manufacturer of each individual IP product. The designations used by this document are SIGNAL [msb:lsb] for buses, N_SIGNAL for asserted low signals, and contain "I" or "IP" prefixes where similar signals (data and address buses, clocks, etc.) might exist in system and subsystem configurations for differentiating IP signals from others. For all signals, except ICLK, the maximum IP loading is 3.0 mA (logic low) in parallel with 30 ρF. All signals have a 10 KΩ pull-up resistor on the carrier board, unless they are continously driven signals.

ICLK

This signal, ≡ CLK in the specification, is an 8 MHz ±1.6%, 50% duty cycle clock used for all synchronous operations. The rising edge is used for sampling states and address/data patterns, and changes are made relative to that event. An exception to this is an allowance for IPs to latch carrier-driven signals while the ICLK is low. ICLK's "logic" connection is via pin 2. The loading is 6.0 mA (logic low) maximum in parallel with 30ρF.

IPA[6:1] (Address bus)

These six lines, ≡ A1...A6 (lsb to msb) in the specification, are asserted by the carrier to the IP throughout all valid transfers. These signals may be in any states during idle cycles. IPA[6:1] are used for I/O and MEMORY transfers; IPA[5:1] (with IPA6=0) are used for ID read transfers; and IPA1 is used for INTERRUPT vector read transfers on boards using both interrupt request levels. Their "logic" pin connections are (for IPA6 ... IPA1): 47, 45, 43, 41, 39, and 37, respectively. They define 16-bit data boundaries for "singlewide" boards, and 32-bit data boundaries for "doublewide" boards. It is important to note that the address lines are not used in defining the type of transfer that is being executed, as these are defined by individual select lines from the carrier.

IPD[15:0] (Data bus)

These sixteen lines, ≡ D00...D15 (lsb to msb) in the specification, are the bi-directional data bus, and also serve as an extended address bus = IPA[22:7] driven by the carrier during the select cycle of a memory transfer, regardless of read or write access sense. Except for memory transfer select cycles, the carrier board drives the IPDbus during write operations, and the IP drives it during read acknowledgement cycles. For "doublewide" IPs, the b-side data bus is typically referred to as IPD[31:16]. During ID read transfers, IPD[7:0] are the only valid data lines. INTERRUPT vector reads typically use only IPD[7:0], but can be any number of bits. The "logic" pin connections for IPD15...IPD0 are: 19, 18, 17, 16, 15, 14,

13, 12, 11, 10, 9, 8, 7, 6, 5, and 4, respectively.

N_RESET

This signal, ≡ RESET★ in the specification, is the asserted low reset signal. The carrier is required to assert N_RESET for a minimum of 200 ms following power-up, with no maximum time limit. The IP is required to terminate any transfers in progress, remove any pending or active interrupt requests, and block future requests until enabled via software. It may be asserted asynchronously, but will be negated synchronized to the rising edge of ICLK. IP documentation must clearly indicate what the IP state is following a reset operation. The "logic" connection is via pin 3.

IPR/N_W (Read/Write)

This signal, ≡ R/W★ in the specification, is the data direction control line driven by the carrier to the IP. When IPR/N_W is high, a read transfer is taking place and indicates to the IP that it is to drive IPD[15:0] during the acknowledgement cycle(s). When IPR/N_W is low, the carrier is driving the IPD[15:0] lines throughout valid transfers. This signal may be any state during idle cycles. IPR/N_W's "logic" connection is via pin 28.

N_ACK (ACKnowledge)

This signal, ≡ ACK★ in the specification, is the asserted low data acknowledgement signal driven by the IP to the carrier. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the separate acknowledgement signals are designated by SYSTRAN as N_A_ACK and N_B_ACK, for the a-side and b-side portions of the IP. It is asserted to indicate that the current cycle can be the termination cycle, provided the carrier is not invoking "hold" cycles. If the carrier is invoking "hold" cycles (by not negating the "select" signal after the first "select" cycle, then the asserted N_ACK signal indicates to the carrier a "hold acknowledge" function. The IP captures the carrier driven data during the first acknowledgement for write transfers. IP requested "wait" cycles are invoked by the delay of N_ACK assertions following the "select" cycle. IP documentation must clearly indicate the maximum number of "wait" cycles (delayed acknowledgements) inserted by the IP for all types of transfers. The "logic" connection is via pin 48.

N_BS0 (low Byte Select)

N_BS1 (high Byte Select)

These signals, ≡ BS0★ for N_BS0 and ≡ BS1★ for N_BS1 in the specification, are asserted low byte select lines driven by the carrier to the IP to indicate which byte lanes are valid. An IP may ignore these lines, but a carrier is required to drive them to valid states throughout all valid transfers. N_BS0 selects the low, or odd byte IPD[7:0], while N_BS1 selects the high, or even byte IPD[15:8]. Both N_BS1 and N_BS0 will be asserted when both bytes IPD[15:0] are valid. The "logic" connections are via pins 20 and 21 for N_BS0 and N_BS1, respectively.

N_MEMSEL (MEMory SELect)

This signal, ≡ MemSel★ in the specification, is the asserted low memory transfer select signal, driven by the carrier to the IP for both memory read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_MEMSEL, and the b-side signal is called N_B_MEMSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_MEMSEL is asserted during memory transfer "select" and "hold" cycles. The "logic" connection is via pin 31.

N_IOSEL (I/O SELect)

This signal, ≡ IOSel★ in the specification, is the asserted low input or output (I/O) transfer select signal, driven by the carrier to the IP for both I/O read and write transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IOSEL, and the b-side signal is called N_B_IOSEL. "Doublewide" IPs may respond with a-side only, b-side only, or both sides participating in the transfer. N_IOSEL is asserted during I/O transfer "select" and "hold" cycles. The "logic" connection is via pin 35.

N_INTSEL (INTerrupt vector read SELect)

This signal, ≡ IntSel★ in the specification, is the asserted low interrupt vector (read) transfer select signal, driven by the carrier to the IP. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_INTSEL, and the b-side signal is called N_B_INTSEL. "Doublewide" IPs may respond with a-side only, or b-side only transfers; both sides is not a supportable transfer. N_INTSEL is asserted during the "select" and "hold" cycles of the interrupt acknowledgement operation. The "logic" connection is via pin 33.

N_IDSEL (IDentification SELect)

This signal, ≡ IDSel★ in the specification, is the asserted low ID transfer select signal, driven by the carrier to the IP during ID read transfers. This signal is unique (not bussed) to each "singlewide" IP location. For "doublewide" IPs, the a-side signal designation used by SYSTRAN is N_A_IDSEL, and the b-side signal is called N_B_IDSEL. For "doublewide" IPs, only the a-side is used for information transfers, even though the select signals for both sides are monitored and decoded for valid transfers. N_IDSEL is asserted during ID transfer "select" and "hold" cycles. The "logic" connection is via pin 29.

N_INTREQ0 (INTerrupt REQuest #0)

N_INTREQ1 (INTerrupt REQuest #1)

These signals, ≡ IntReq0★ for N_INTREQ0 and ≡ IntReq1★ for N_INTREQ1 in the specification, are asserted low interrupt requests driven asynchronously from the IP to the carrier. These signals are unique (not bussed) to each "singlewide" IP location. For "double-wide" IPs, the a-side signal designations used by SYSTRAN are N_A_INTREQ0 and N_A_INTREQ1, and the b-side signals are called N_B_INTREQ0 and N_B_INTREQ1. The "logic" connections are via pins 42 and 44 for N_INTREQ0 and N_INTREQ1, respectively.

OTHER SIGNALS:

The following list is that of signals that are not described in detail in this document. DMAReq0★ is found at pin 30. DMAReq1★ is found at pin 32. DMAck0★ is found at pin

34. Pin 36 is a reserved pin, as is pin 49. DMAEnd★ is found at pin 38. Error★ is found at pin 40; and Strobe★ is found at pin 46.

POWER/GROUND:
+5 volts is provided by the carrier at "logic" connections 24 and 27. GND, the zero volts reference, comes in pins 1, 25, 26, and 50; +12 volts is sourced via pin 23, and, -12 volts comes in pin 22.

CYCLE TYPES:
There are five cycle types that define various states of transfers (or no transfers) between the IP and its carrier. They are: select, terminate, wait, hold, and idle. Select and terminate are required for every transfer. A select cycle, which can only be entered following an idle cycle or a terminate cycle, is one where one or two select signals are asserted by the carrier. A terminate cycle is one where simultaneously, the carrier has negated the select signal(s) and the IP has asserted the N_ACK acknowledgement signal. A wait cycle is invoked by the IP due to its inability to terminate a transfer during the second cycle of a transfer by not asserting the acknowledgement signal N_ACK until it is ready to complete the (read or write) transfer. A hold cycle is invoked by the carrier, typically during read transfers, causing the IP to hold its data, by maintaining the assertion of the select signal(s) beyond the first, select cycle. Idle cycles are those between select and terminate cycles indicating no activity. Six transfer tables at the end of this document attempt to depict various combinations of these cycles for various read and write transfers. It is interesting to note that simultaneous wait and hold requests appear as extended select cycles.

TRANSFER TYPES:
There are four transfer types: Memory, I/O, Interrupt (vector read), and ID. The type of transfer being executed is defined by the valid combination of select lines asserted during the (first) select cycle. A table at the end of this document depicts the matrix of currently defined select signal assertion combinations for various defined transfers. It is important to note that future specification revisions may make use of the select lines in other mixed combinations for special transfer types.

As previously indicated, a transfer starts with a select cycle, and ends with a terminate cycle, and may have intermediate wait and/or hold cycles. An IP need not respond to a transfer selection type if it does not support the attempted type. The IP documentation should clearly indicate the transfer types supported, as well as the data widths per supported transfer type. It also needs to indicate the maximum number of wait cycles it injects, and the maximum number of hold cycles that it can tolerate from the carrier, if there is a limit.

ID INFORMATION:
Each IP must have identification information that is read by the carrier during ID transfers. It is presented on IP[7:0] for both "singlewide" and "doublewide" IPs. It is a read-only function, with the stipulation that IPA6 = 0, which provides addressing for 32 bytes of information. The ID PROM can be emulated in programmable logic, if desired. The lowest addresses provide fixed data including an IP identifier, manufacturer and model number codes, revision and software support information, and a cyclic redundancy check value for data verification purposes. These fields are defined in detail in the specification. The remaining locations can be used for IP specific and application specific information, if desired. The IP documentation must indicate the longest time required following the end of reset prior to being able to access the ID information.

PHYSICAL:
The outside dimensions of a "singlewide" IP are 1.800″ by 3.900″, +.000/-.020″. The outside dimensions of a "doublewide" IP are 3.600″ by 3.900″, +.000/-.020″. There are two, 50-pin connectors on the component side of the IP, one on each end of the board, servicing the "logic" interfacing between the carrier and the IP, and providing IP specific I/O interfacing. All other components (also) mount on the component side (only) in a space of 1.8″ by 3.188″ between the connectors for a "singlewide" IP, and 3.6″ by 3.188″ for a "doublewide" IP. The maximum height of components on the IP is 0.315″, with components exceeding 0.250″ in height having non-conductive top surfaces, if possible. There are no components mounted on the "solder" side of the IP, and ALL leads are flush cut. Optionally, a label can be attached on the "solder" side, providing the user with IP pertinent information. The component side of the IP faces the component side of the carrier (IP parts and connectors face down) when the IP is properly installed.

Both "D-shaped", 50-pin straight socket connectors are shrouded and keyed; AMP's part no. 173279-3. The insulation is rated to 500VAC, the contacts are rated at 200 insertion cycles, capable of handling 1A per pin. Due to their shape and placement on the IP, there is only one way to install an IP on its carrier. The entire IP can optionally be bolted to its carrier for high shock and vibration environments.

Typical environmental specifications include an operating (ambient) temperature range of 0° to 70°C, in a relative humidity range of 5 to 95% (non-condensing), with storage temperatures from -40°C up to +85°C.

ADDITIONAL INFORMATION:
The information contained within this document is believed to be reliable and accurate. However, SYSTRAN assumes no responsiblity and no liability resulting from inaccuracies or omissions, or from the use of this information.

It is recommended that the reader obtain the full IndustryPack Logic Interface Specification, from GreenSpring Computers, Inc., 1204 O'Brien Drive, Menlo Park, CA 94025.

MEMORY TRANSFERS' CYCLE TABLES

CYCLE'	MEM WRITE NO HOLDS NO WAITS				MEM WRITE NO HOLDS 2 WAITS					MEM WRITE 3 HOLDS NO WAITS							MEM WRITE 1 HOLD 3 WAITS									DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	IDLE	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPD[15·0]*	X	→	→	X	→	→	→	→	X	→	→	→	→	→	X	X	X	→	→	→	→	→	X	X	X		✓
IPR/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	0	X	X	X	0	0	0	0	0	X	X	X		✓
DATA LATCH * END OF'			◇					◇			◇											◇					

CYCLE'	MEM READ NO HOLDS NO WAITS				MEM READ NO HOLDS 3 WAITS					MEM READ 2 HOLDS NO WAITS					MEM READ 3 HOLDS 2 WAITS						MEM READ 1 HOLD 3 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	WAIT	TERM	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15·0]*	X	→	←	X	→	Z	Z	Z	←	→	←	←	←	X	→	Z	Z	←	←	X	→	Z	Z	Z	←	✓	✓
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	1	0	✓	
N_MEMSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

GENERAL LEGEND'

* IPD[15·0] = IPA[22·7] during during the SELECT cycle, and is used for data for all other cycles.

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE' +5v
- 0 — LOW STATE' GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPack
- ◇ — IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

ID TRANSFERS' CYCLE TABLES

CYCLE'	ID READ NO HOLDS NO WAITS				ID READ NO HOLDS 2 WAITS					ID READ 3 HOLDS NO WAITS					ID READ 1 HOLD 3 WAITS						ID READ 2 HOLDS 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	HOLD	TERM	SELECT	WT&HLD	WAIT	WAIT	TERM	IDLE	IDLE	SELECT	WT&HLD	WT&HLD	TERM	IDLE	IPack	CARRIER
IPA[6·1]	X	→	→	X	→	→	→	→	→	→	→	→	→	→	→	→	→	→	X	X	→	→	→	→	X		✓
IPD[7·0]	X	Z	←	X	Z	Z	Z	←	Z	←	←	←	←	Z	Z	Z	Z	←	X	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	X	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	✓	
N_IDSEL	1	0	1	1	0	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1		✓

GENERAL LEGEND'

- X — DON'T CARE
- Z — HIGH IMPEDANCE
- 1 — HIGH STATE' +5v
- 0 — LOW STATE' GND
- → — DRIVEN INTO IPack
- ← — DRIVEN OUT OF IPac

INT TRANSFERS' CYCLE TABLES

CYCLE'	INT READ NO HOLDS NO WAITS				INT READ NO HOLDS 3 WAITS					INT READ 2 HOLDS NO WAITS					INT READ 3 HOLDS 2 WAITS						INT READ 1 HOLD 2 WAITS					DRIVEN BY'	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	WAIT	TERM	SELECT	HOLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IDLE	SELECT	WT&HLD	WAIT	TERM	IDLE	IPack	CARRIER
IPA1*	X	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→	X	→	→	→	→	X		✓
PD[7·0]**	X	Z	←	X	Z	Z	Z	Z	←	Z	←	←	←	X	Z	Z	Z	←	←	X	Z	Z	Z	←	X	✓	
IPR/N_W	X	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1	X	1	1	1	1	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	✓	
N_INTSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	0	1	1	1		✓

* IPA1 CAN BE IGNORED IF ONLY ONE INTERRUPT IS SUPPORTED (must be at LEVEL 0).

** IPD TYPICALLY IS ONLY 8 BITS, BUT IT CAN BE ANY WIDTH.

WAITS ARE INVOKED BY THE IPACK.

HOLDS ARE INVOKED BY THE CARRIER

SELECT & TERM ARE REQUIRED: IDLE, WAIT HOLD ARE NOT REQUIRED

I/O TRANSFERS, CYCLE TABLES

CYCLE:	I/O WRITE NO HOLDS NO WAITS			I/O WRITE NO HOLDS 3 WAITS					I/O WRITE 2 HOLDS NO WAITS								I/O WRITE 3 HOLDS 1 WAIT					DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	IDLE	IDLE	IDLE	IDLE	SELECT	WT&HLD	HOLD	HOLD	TERM	IDLE	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPD[15:0]	X	→	→	X	→	→	→	→	X	→	→	→	→	X	X	X	X	→	→	→	→	→	X		✓
IPA/N_W	X	0	0	X	0	0	0	0	X	0	0	0	0	X	X	X	X	0	0	0	0	0	X		✓
N_ACK	1	1	0	1	1	1	1	1	0	1	1	0	0	0	1	1	1	1	1	1	0	0	0	1	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	0	1	1		✓
N_BS#	X	0	0	X	0	0	0	0	X	0	0	0	0	X	X	X	X	X	0	0	0	0	0	X		✓
DATA LATCH @ END OF:			◇					◇			◇									◇						

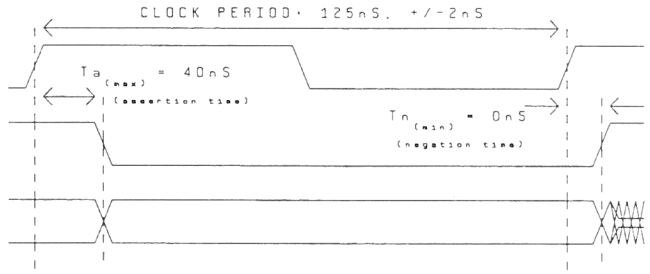
CYCLE:	I/O READ NO HOLDS NO WAITS			I/O READ NO HOLDS 2 WAITS					I/O READ 3 HOLDS NO WAITS					I/O READ 2 HOLDS 3 WAITS					I/O READ 3 HOLDS 2 WAITS						DRIVEN BY:	
	IDLE	SELECT	TERM	IDLE	SELECT	WAIT	WAIT	TERM	IDLE	SELECT	HOLD	HOLD	TERM	SELECT	WT&HLD	WT&HLD	WAIT	TERM	IDLE	SELECT	WT&HLD	WT&HLD	HOLD	TERM	IPack	CARRIER
IPA[6:1]	X	→	→	X	→	→	→	→	X	→	→	→	→	→	→	→	→	→	X	→	→	→	→	→		✓
IPD[15:0]	X	Z	←	X	Z	Z	Z	←	X	Z	←	←	←	←	Z	Z	Z	Z	←	X	Z	Z	Z	←	←	✓	
IPA/N_W	X	1	1	X	1	1	1	1	X	1	1	1	1	1	1	1	1	1	X	1	1	1	1	1		✓
N_ACK	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0	✓	
N_IOSEL	1	0	1	1	0	1	1	1	1	0	0	0	1	0	0	0	1	1	1	0	0	0	0	1		✓

GENERAL LEGEND:

- X = DON'T CARE
- Z = HIGH IMPEDANCE
- 1 = HIGH STATE, +5v
- 0 = LOW STATE, GND
- → = DRIVEN INTO IPack
- ← = DRIVEN OUT OF IPack
- ◇ = IPack LATCHES AT END OF CYCLE

WAITS ARE INVOKED BY THE IPACK.
HOLDS ARE INVOKED BY THE CARRIER
SELECT & TERM ARE REQUIRED: IDLE, WAIT & HOLD ARE NOT REQUIRED.

SYNCHRONOUS CYCLE TIMING DETAIL



ALL STATES SAMPLED ON THE RISING EDGE OF THE CLOCK
STATES ARE CHANGED FOLLOWING THE RISING EDGE OF THE CLOCK

VALID TRANSFER SELECTION MATRIX

TRANSFER TYPE:	DOUBLE-WIDE								SINGLE-WIDE				
SIDE:													
ASSERTED LOW:	N_B_MEMSEL	N_B_IOSEL	N_B_INTSEL	N_B_IOSEL	N_A_MEMSEL	N_A_IOSEL	N_A_INTSEL	N_A_IOSEL	N_MEMSEL	N_IOSEL	N_INTSEL	N_IOSEL	VALID TRANSFER(s):
	1	1	1	1	0	1	1	1	0	1	1	1	MEMORY, A-SIDE ONLY
	0	1	1	1	1	1	1	1					MEMORY, B-SIDE ONLY
	0	1	1	1	0	1	1	1					MEMORY, BOTH SIDES
	1	1	1	1	1	0	1	1	1	0	1	1	I/O, A-SIDE ONLY
	1	0	1	1	1	1	1	1					I/O, B-SIDE ONLY
	1	0	1	1	1	0	1	1					I/O, BOTH SIDES
	1	1	1	1	1	1	0	1	1	1	0	1	INTERRUPT, A-SIDE ONLY
	1	1	0	1	1	1	1	1					INTERRUPT, B-SIDE ONLY
	1	1	1	1	1	1	1	0	1	1	1	0	IO, A-SIDE ONLY

B-T-SH-IPACKSUM-A-0-A2 (07-15-94)

APPENDIX B

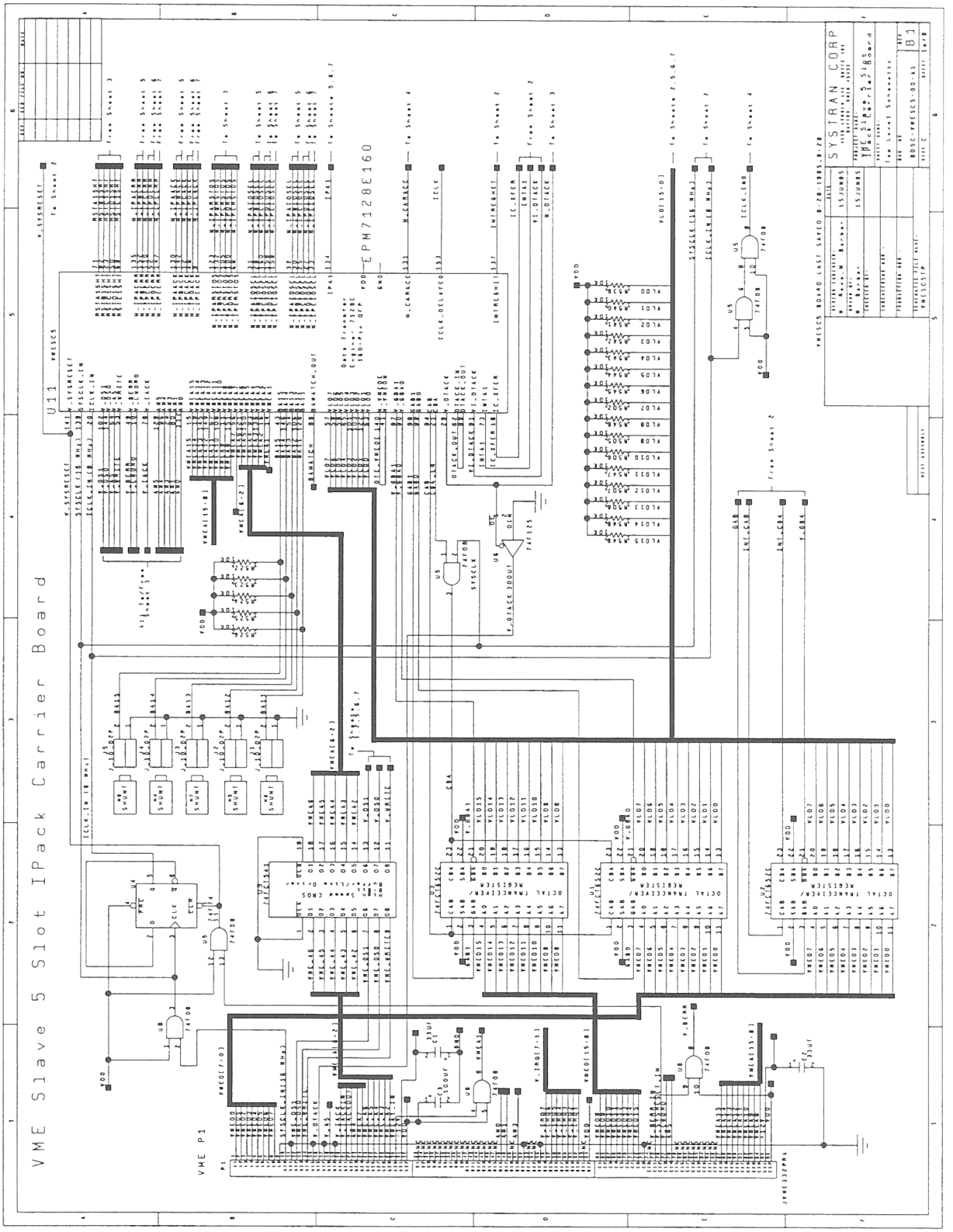


Figure B-1 Schematic #1

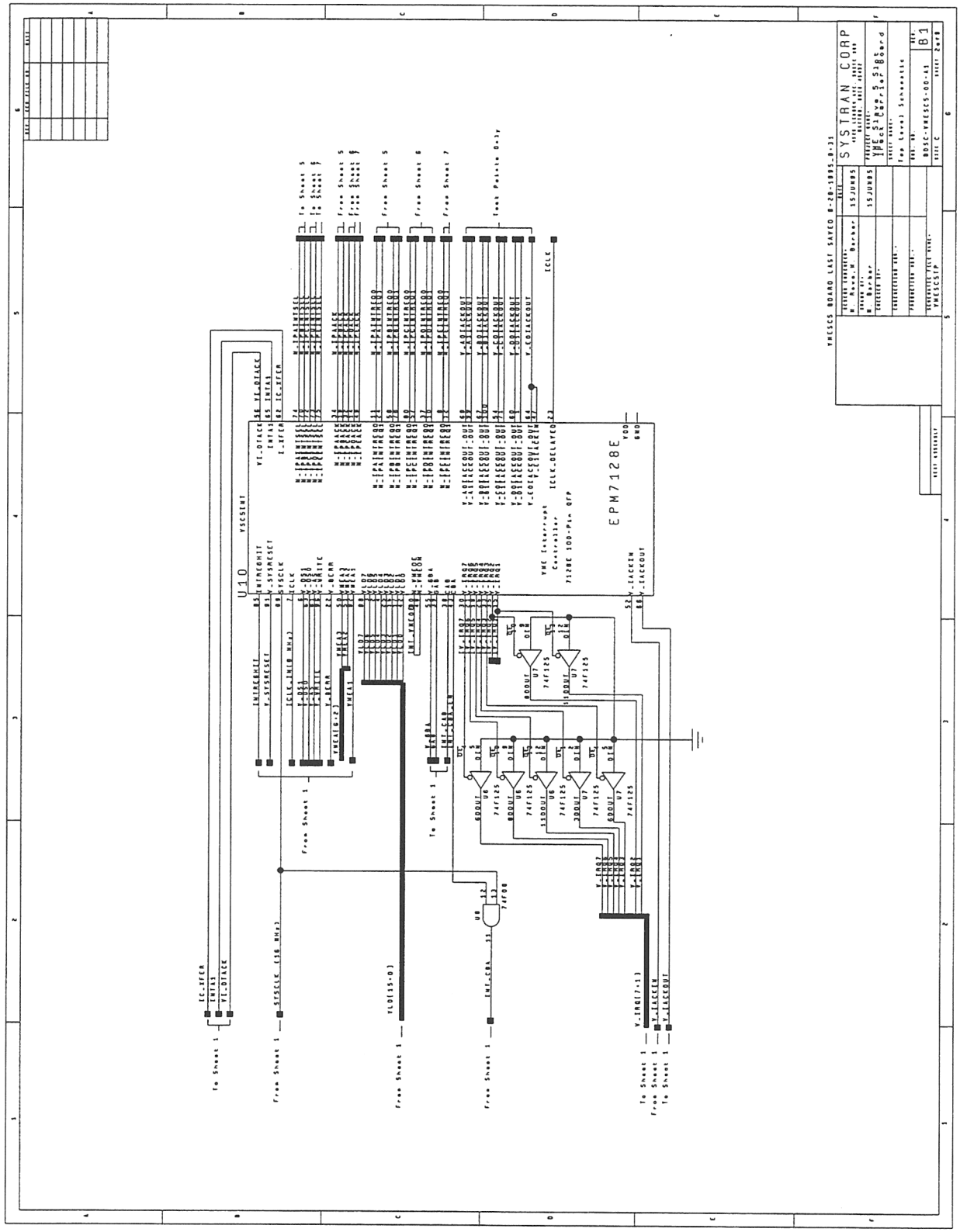


Figure B-2 Schematic #2

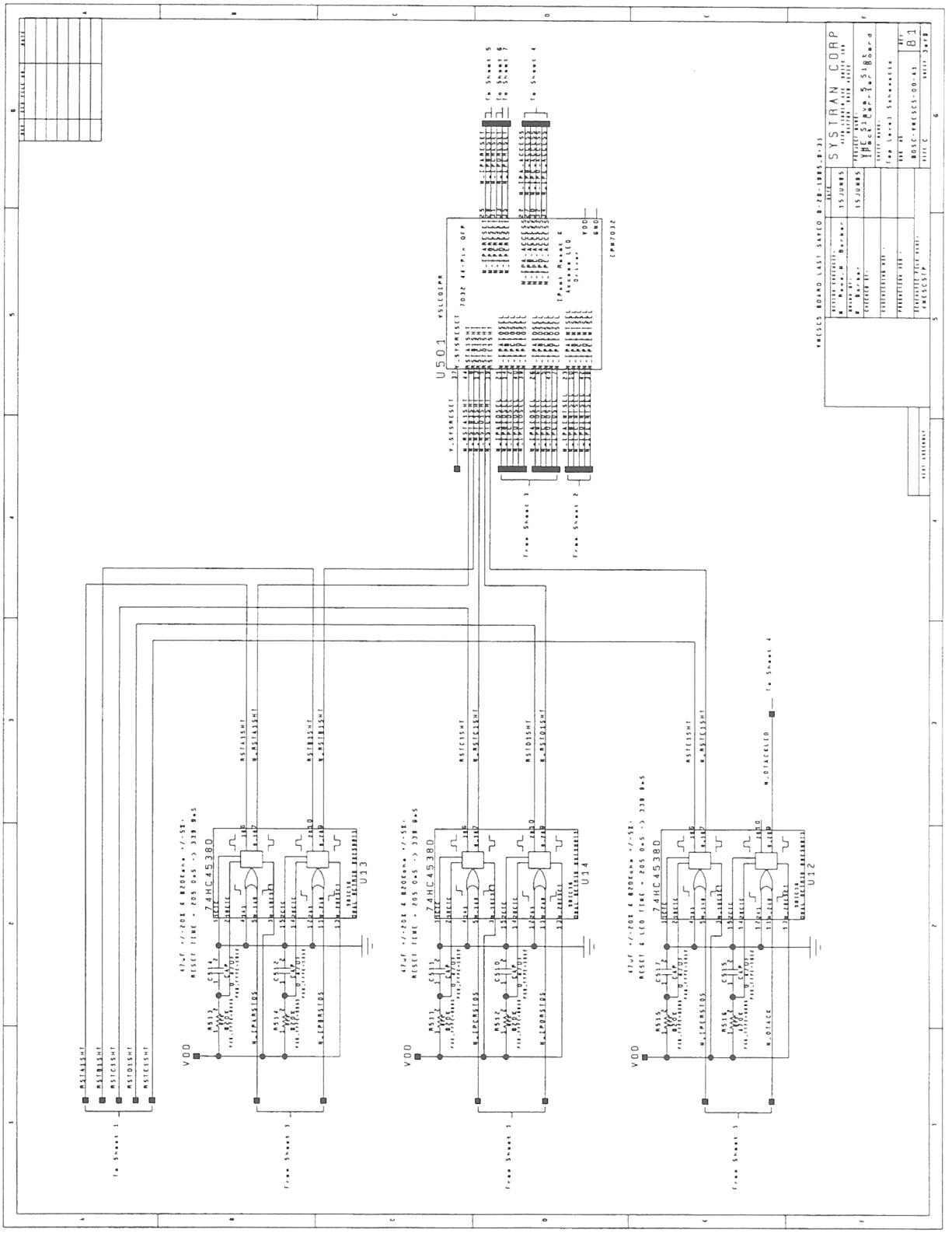


Figure B-3 Schematic #3

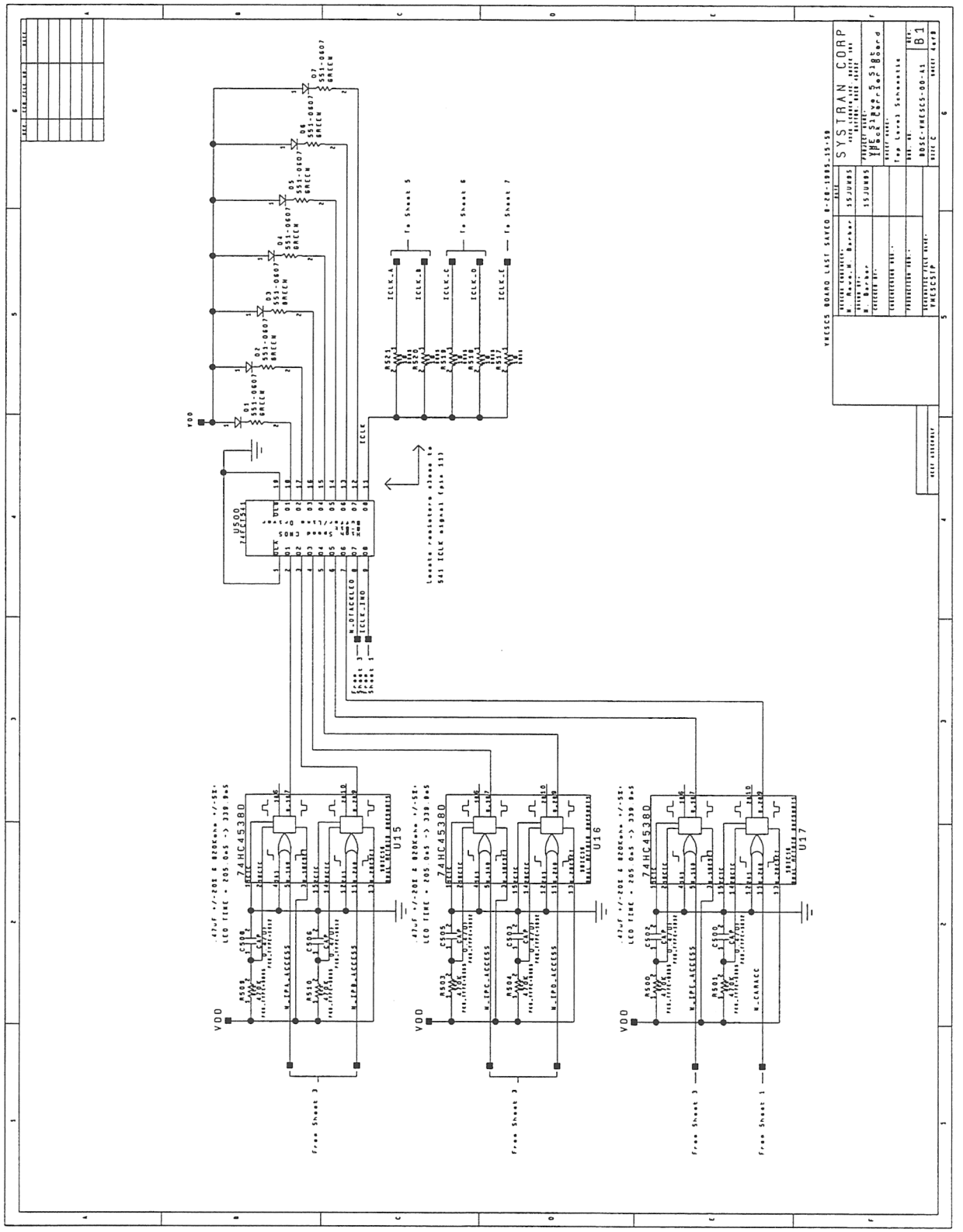


Figure B-4 Schematic #4

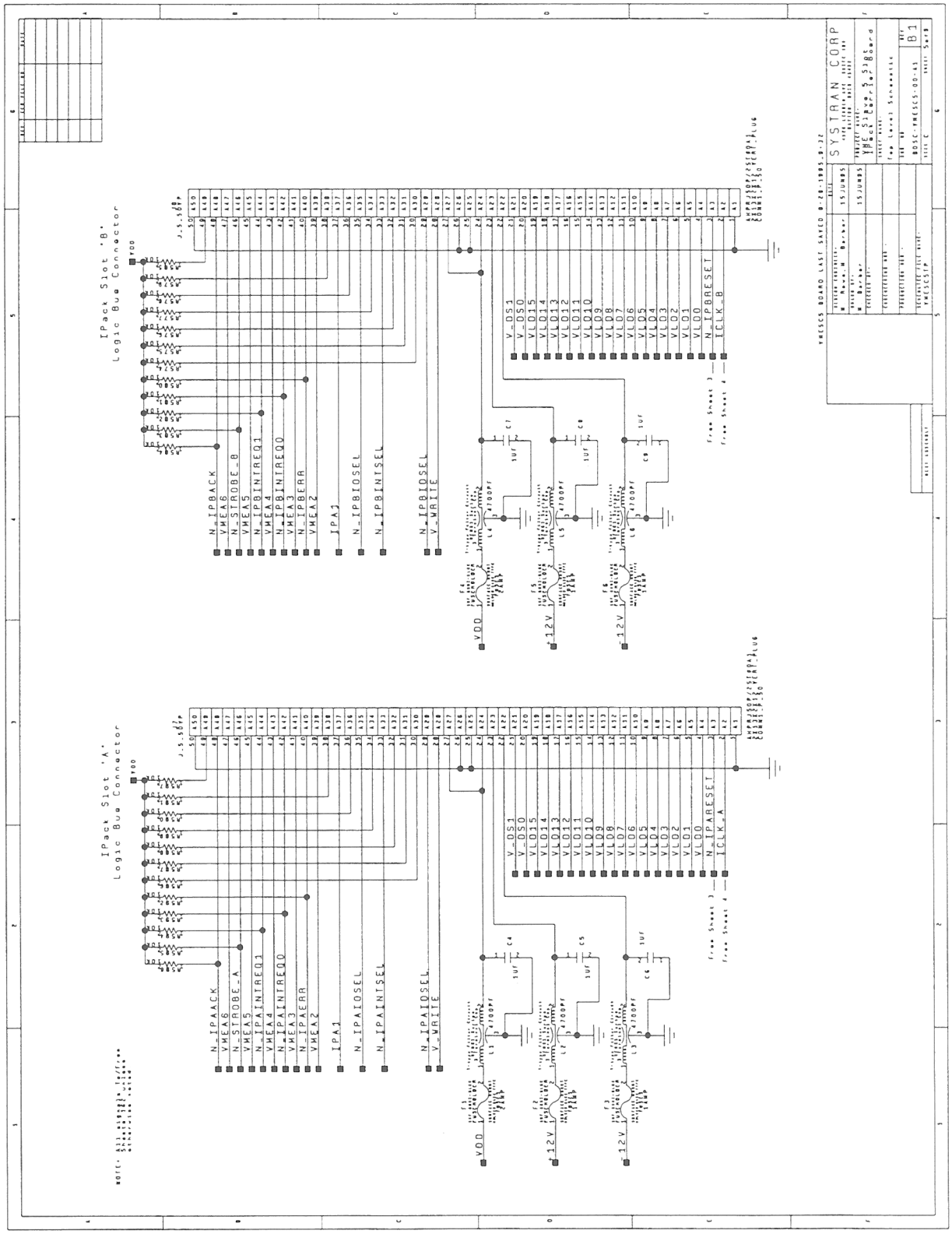


Figure B-5 Schematic #5

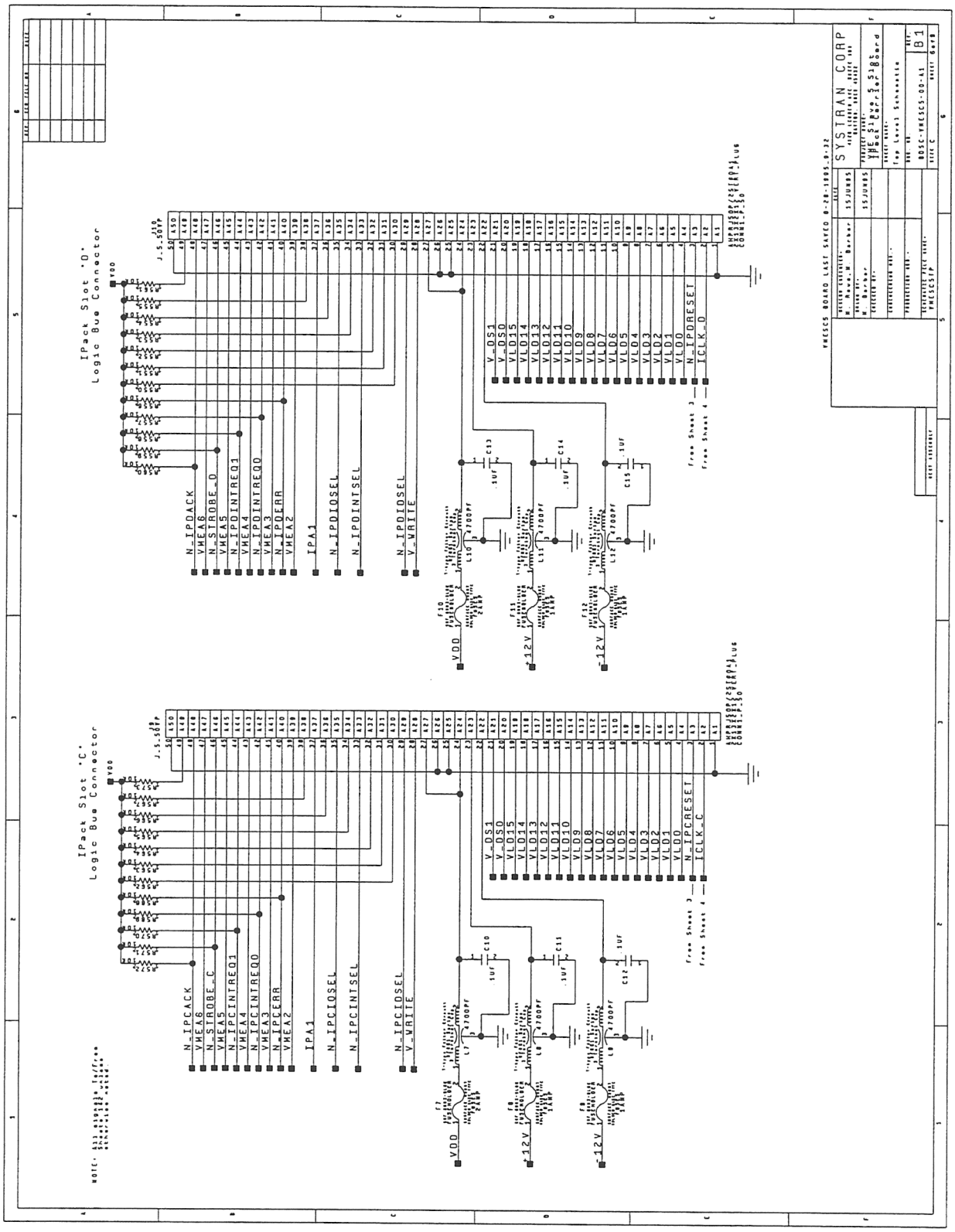


Figure B-6 Schematic #6

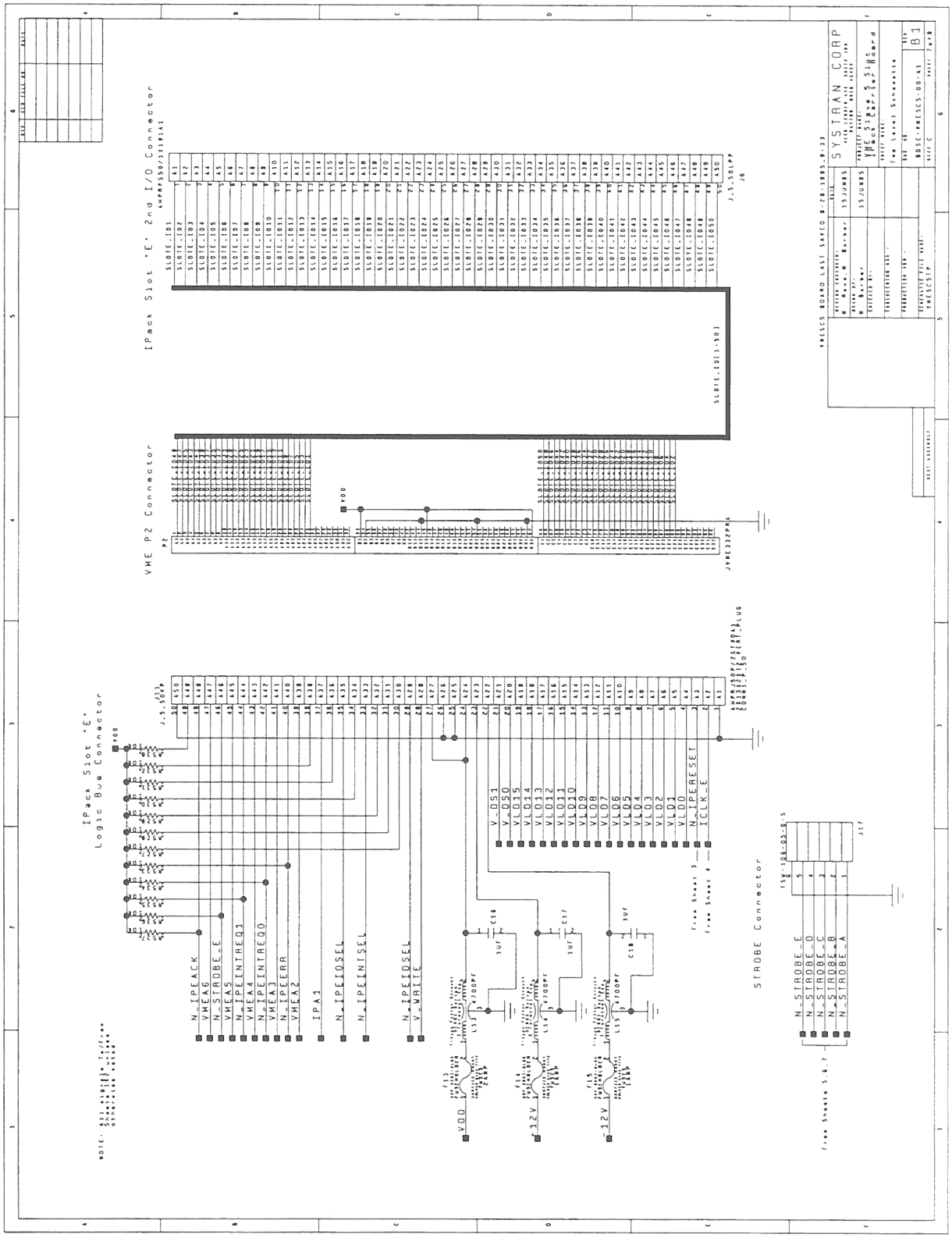


Figure B-7 Schematic #7

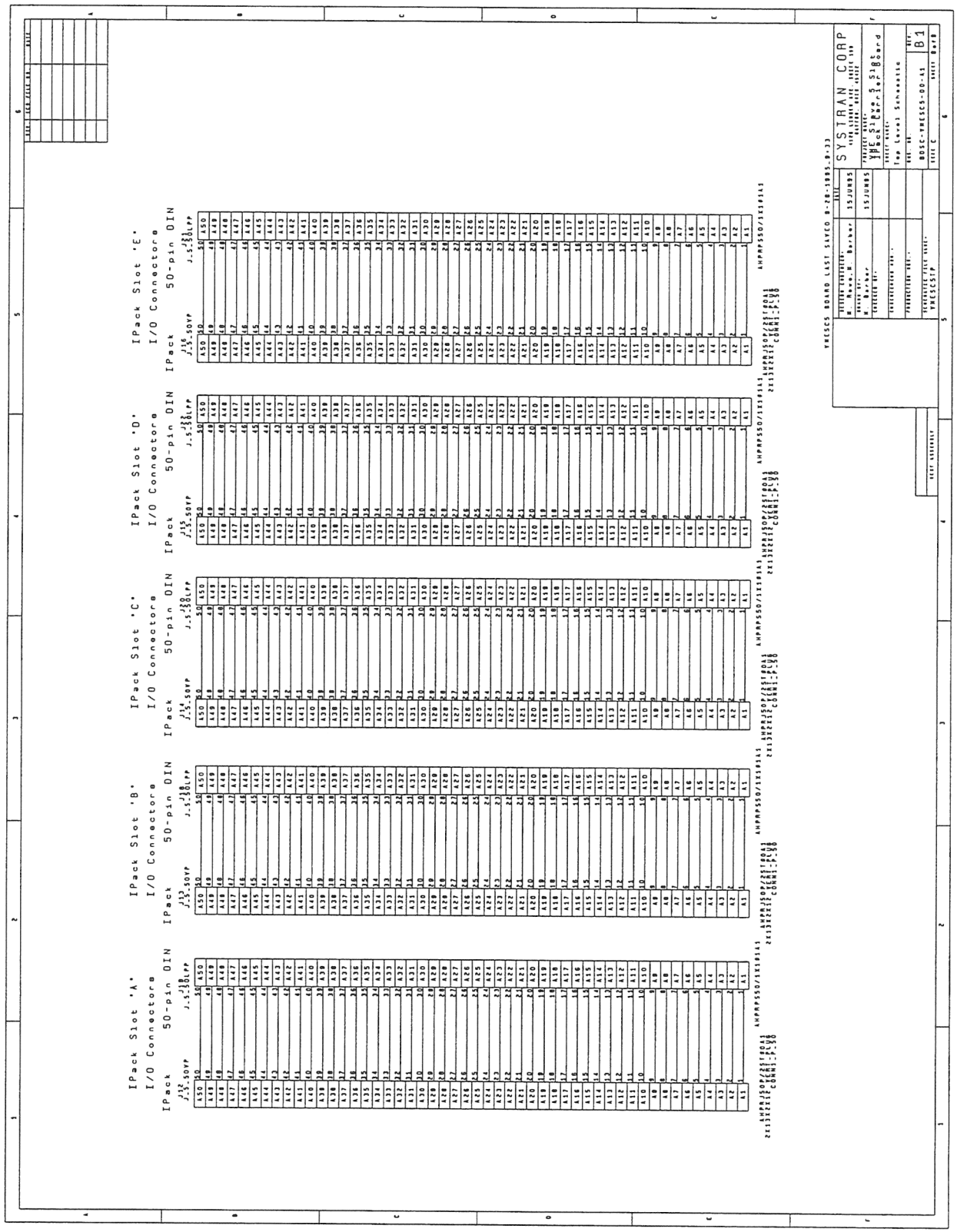


Figure B-8 Schematic #8

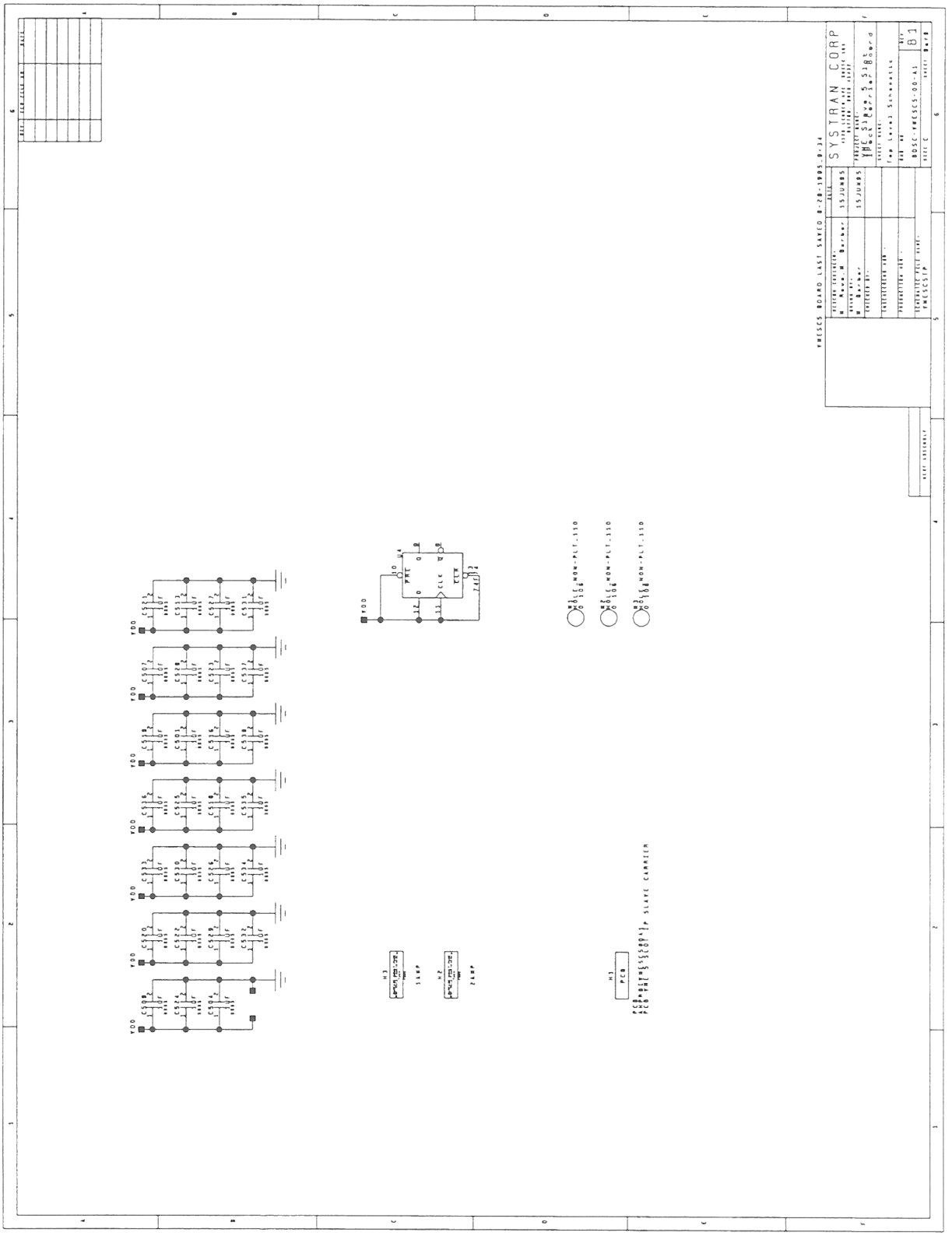


Figure B-9 Schematic #9