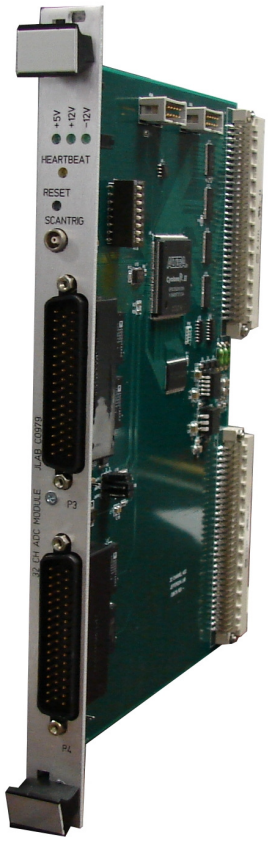
Jefferson Lab



VME 32-Channel ADC Module

July 24, 2009

General Description

The 32-channel ADC module was designed to replace the BiRa CAMAC 5333 scanning ADC card used throughout the accelerator. It supports A16/D16 VMEbus operations in short supervisory and/or non-privileged addressing modes. The base address can be configured for 4 different fixed addresses using switches 7 and 8 on the 8 position dip switch (see table 1). The board consists of 36 16-bit registers used to configure the board and read the analog input data. The front panel contains indicator LED's for power and heartbeat. The analog inputs are fully differential and can be configured for five different ranges (see table 2). The data format can be configured for 2's complement or straight binary depending on the selected input range (bipolar or unipolar). This is done using switch 2 on the dip switch (ON = straight binary). The ADC has 16 bit resolution and supports up to a 100kHz sample rate. Switch 1 on the dip switch is used to configure continuous or external scan triggering (ON = external). The input connectors for the analog inputs are 50-pin "D" style connectors (see JLAB DWG# C0979B01 for pin out details).

SW7	SW8	BASE ADDRESS
OFF	OFF	0xFBFF6400
OFF	ON	0xFBFF6480
ON	OFF	0xFBFF6500
ON	ON	0xFBFF6580

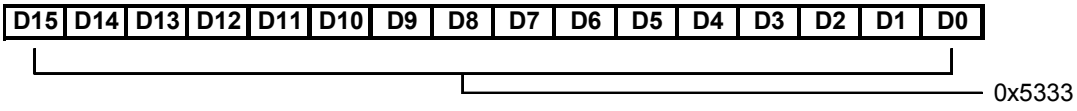
Table 1 Base Address Configuration

RANGE	JMPR1	JMPR2	JMPR3
±10V	1-2	2-3	2-3
±5V	1-2	1-2	1-2
±2.5V	1-2	1-2	1-2
0-10V	1-2	1-2	1-2
0-5V	1-2	1-2	1-2

Table 2 Analog Input Range Configuration

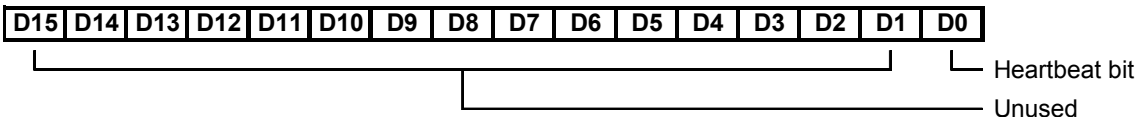
Register Descriptions

Board Identification Register
BASE + 0x00



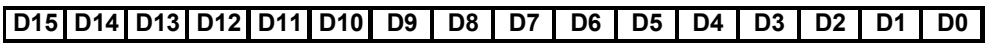
This register is read only and always returns 0x5333 to identify it as the replacement for the BiRa 5333 scanning ADC card.

Heartbeat Register
BASE + 0x02



This register is used to provide a heartbeat signal to VME. The heartbeat (bit D0) will toggle at a rate of 1Hz. All other bits are currently unused and read back zero by default.

ADC Channel Scan Rate Control Register
BASE + 0x04

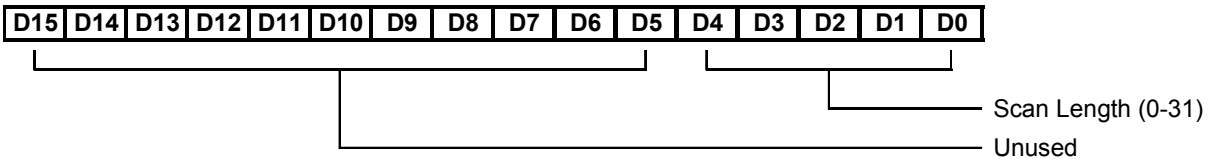


This register controls the sample rate of the ADC. The valid range for this register is 200-65535 (decimal). The value for a given scan rate is calculated as follows.

value = 1 / (scan rate(Hz) * 50E-9)

Default value = 200 (100kHz sample rate)

ADC Channel Scan Length Select Register
BASE + 0x06



This register configures the number of sequential ADC channels to be scanned.

Default = 31 (all 32 channels are scanned)

ADC Registers (16 bit)

ADC Channel 1 Data Register (Read Only)
BASE + 0x10

ADC Channel 2 Data Register (Read Only)
BASE + 0x12

ADC Channel 3 Data Register (Read Only)
BASE + 0x14

ADC Channel 4 Data Register (Read Only)
BASE + 0x16

ADC Channel 5 Data Register (Read Only)
BASE + 0x18

ADC Channel 6 Data Register (Read Only)
BASE + 0x1A

ADC Channel 7 Data Register (Read Only)
BASE + 0x1C

ADC Channel 8 Data Register (Read Only)
BASE + 0x1E

ADC Channel 9 Data Register (Read Only)
BASE + 0x20

ADC Channel 10 Data Register (Read Only)
BASE + 0x22

ADC Channel 11 Data Register (Read Only)
BASE + 0x24

ADC Channel 12 Data Register (Read Only)
BASE + 0x26

ADC Channel 13 Data Register (Read Only)
BASE + 0x28

ADC Channel 14 Data Register (Read Only)
BASE + 0x2A

ADC Channel 15 Data Register (Read Only)
BASE + 0x2C

ADC Channel 16 Data Register (Read Only)
BASE + 0x2E

ADC Channel 17 Data Register (Read Only)
BASE + 0x30

ADC Channel 18 Data Register (Read Only)
BASE + 0x32

ADC Channel 19 Data Register (Read Only)
BASE + 0x34

ADC Channel 20 Data Register (Read Only)
BASE + 0x36

ADC Channel 21 Data Register (Read Only)
BASE + 0x38

ADC Channel 22 Data Register (Read Only)
BASE + 0x3A

ADC Channel 23 Data Register (Read Only)
BASE + 0x3C

ADC Channel 24 Data Register (Read Only)
BASE + 0x3E

ADC Channel 25 Data Register (Read Only)
BASE + 0x40

ADC Channel 26 Data Register (Read Only)
BASE + 0x42

ADC Channel 27 Data Register (Read Only)
BASE + 0x44

ADC Channel 28 Data Register (Read Only)
BASE + 0x46

ADC Channel 29 Data Register (Read Only)
BASE + 0x48

ADC Channel 30 Data Register (Read Only)
BASE + 0x4A

ADC Channel 31 Data Register (Read Only)
BASE + 0x4C

ADC Channel 32 Data Register (Read Only)
BASE + 0x4E

FPGA Programming

The following items are needed to program the FPGA.

Software

1. Altera Quartus II
2. Programming file: C0979.pof (hardware configuration file)

Hardware

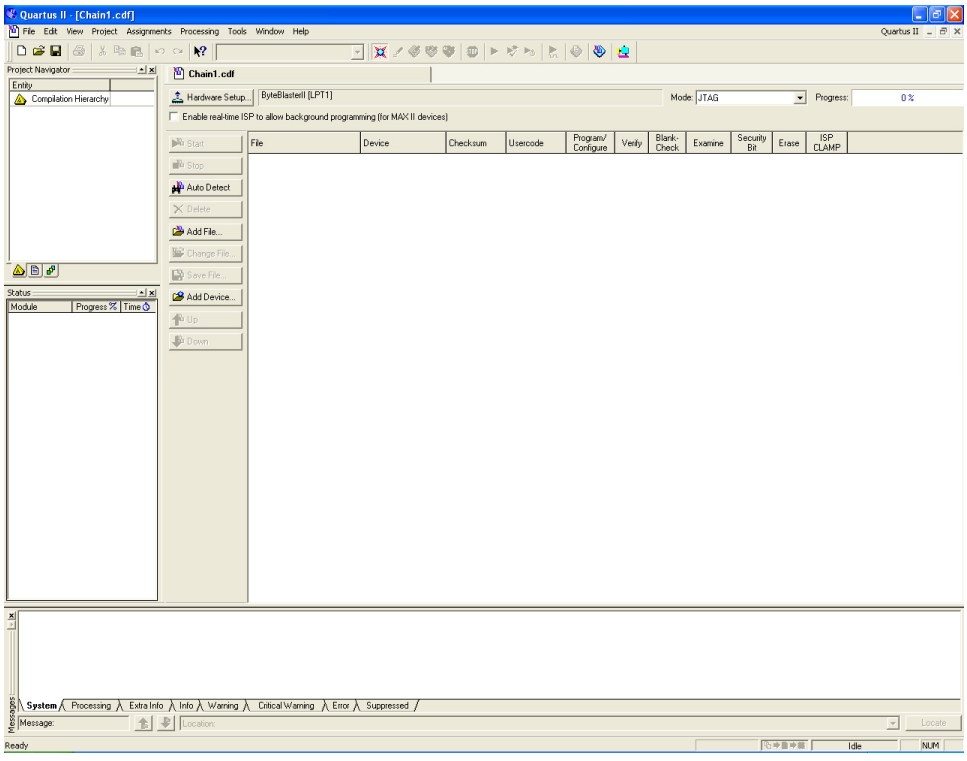
1. Altera USB-Blaster download cable
2. Power supply (+5V from bench supply or VME crate)

Programming Instructions

1. Connect power to the board / insert into VME crate.

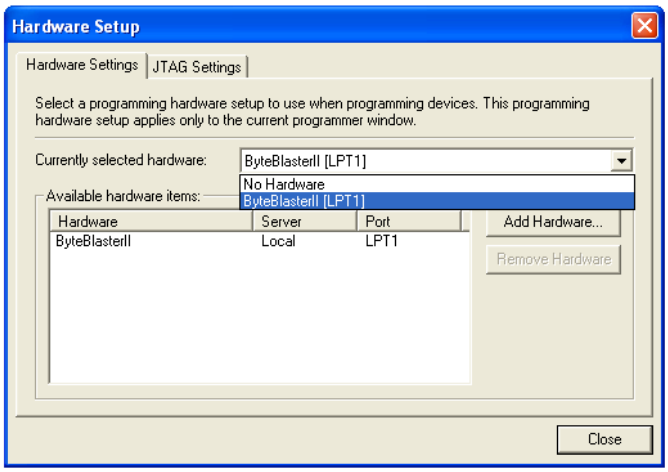
2. Connect the programming cable to the active serial memory interface (ASMI) port (P4).

3. Start up Altera Quartus II and open the programmer (Tools > Programmer)

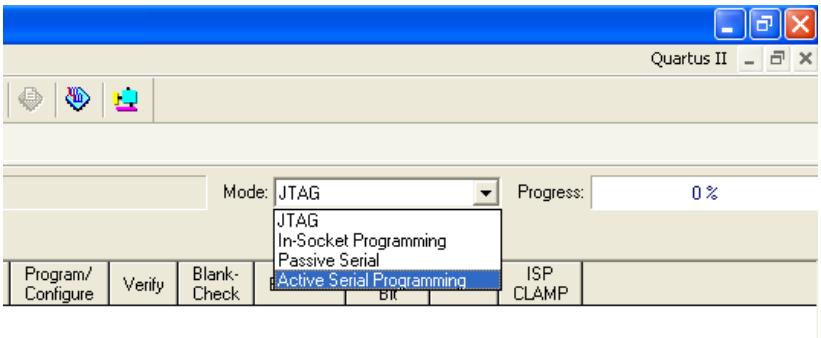


3. Press the “Hardware Setup” button to open the hardware setup dialog box and select USB-Blaster from the “Currently selected hardware” pull-down menu and press “Close”.

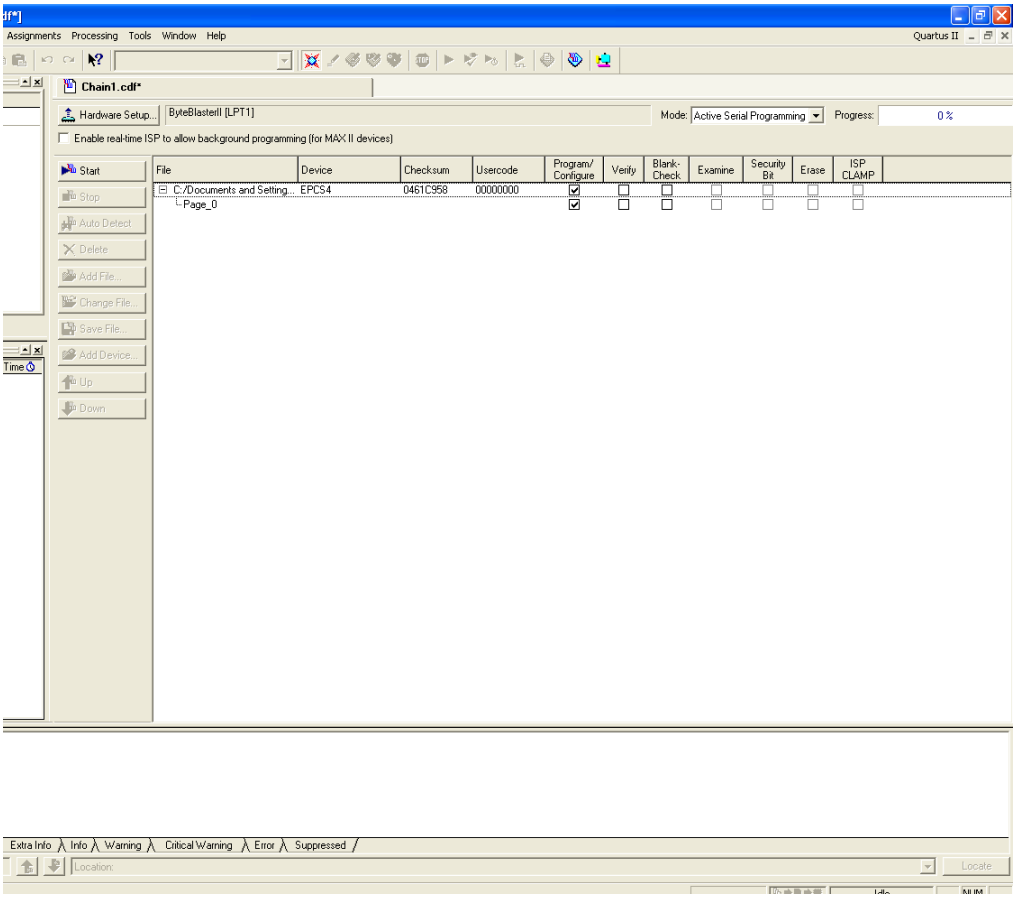
* If USB-Blaster is not available in the drop down menu you will need to install it by clicking on the “Add Hardware…” button. The Windows drivers and instructions are available on the Altera website.



5. Select “Active Serial Programming” from the “Mode” pull-down menu.



6. Press the “Add File” button and select C0943.pof. Check both boxes under the Program/Configure column.



7. Power up the board and press the “Start” button. The “Progress” indicator should go from 0 to 100%