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Physics Division -- *Fast* Electronics Group

Description and Instructions For An ECL 16 Channel Fanout Module With Camac Programmable Pulse Width

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10 October 2000

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1.0 Introduction

The detector subsystems at Jefferson Lab use commercial discriminator modules to create logic level signals from analog pulses. The discriminator or comparator modules allow the user to set a predetermined threshold that prevents undesired analog signals from creating logic level signals. The desired analog signals that cross the threshold limit produce typical logic signals such as NIM or ECL levels that drive the inputs of front end instrumentation modules.

On many occasions the discriminated logic level pulses drive two types of instrumentation modules. For instance, a Time to Digital Converter [TDC] and Scaler module may be connected to the same discriminator unit. If the user desires another logic level output from the discriminator module the need for a logic fanout unit is created.

2.0 Purpose of Module

The sixteen-(16) channel ECL fanout module described in this manual is designed to distribute two differential ECL outputs for each differential ECL input channel. Each input channel can accept a wide range of input pulse widths and the user can program the pulse width output via CAMAC command. All pulse width outputs are controlled from one command. Inputs of various widths will be converted to the programmed pulse width. The default output pulse width is user configurable and is normally set for 200nS. The module will power-up with the default pulse width output setting.

3.0 Brief Functional Description

The ECL Fanout with programmable output width module is comprised of the following four (4) sections:

I. CAMAC Interface and Power Supply Distribution
II. ECL Input
III. Pulse Width Control
IV. ECL Output

- **CAMAC Interface Registers and Power Distribution**

The ECL programmable pulse width fanout module follows the IEEE-583-1975 standard for modular instrumentation, signal levels and interface definitions of the CAMAC standard backplane.

The CAMAC write lines, and bus control lines are connected to a Xilinx® Complex Programmable Logic Device[CPLD]. The CPLD decodes the CAMAC command listed in the following tables as a valid command and initiates the proper read or write function. The proper CAMAC backplane acknowledge signal is returned to the CAMAC controller to verify that a CAMAC cycle was executed properly.

The ECL programmable pulse width fanout module uses three CAMAC backplane supplied voltages. Each voltage passes through a properly rated fuse. The CAMAC backplane power requirement defines a well-regulated very low voltage ripple [noise] and the voltages are not regulated on board the module. Table 2 lists the required voltages and measured current requirements.

Backplane Voltage	Required Current	Total Power: 14.08 Watts	Fuse
+ 6 VDC	0.100 Amps	0.6 W	1 Amp [F1]
+12 VDC	0.081 Amps	0.972 W	1 Amp [F2]
-12 VDC	0.043 Amps	0.516 W	1 Amp [F3]
-6 VDC	2.0 Amps	12 W	3 Amp [F4]

- **ECL Input Section**

The ECL inputs are received differentially from the front panel connector P1. Each input pair is terminated to 100Ω. ECL polarity is labeled on the front panel and the input signals should follow this convention for proper operation.

- **Pulse Width Control Section**

Pulse width is controlled by use of a MC10198 ECL monostable device. The pulse width is set by a combination of external resistor and capacitor. One feature of the MC10198 is the ability to control the output pulse width by

changing the voltage on pin seven of the device. The ECL programmable pulse width is precisely adjusted by changing the voltage applied to the control pin. A twelve bit Digital to Analog Converter is used to set the voltage via CAMAC command.

- **Pulse Width Control Section (Continued)**

The default maximum pulse width at power on is set by the combination of resistor and capacitor values. In this case the default [maximum] setting at power on is 200nS. The user can program the pulse width by CAMAC command, which essentially drives the DAC to a precise voltage setting. The different voltage settings from the DAC change the output pulse width from the MC10198.

Each MC10198 can be configured using a jumper to operate in either a non-updating or updating mode. In non-updating mode the programmed pulse will not produce another pulse, or accept another trigger, until the initial pulse is complete. The monostable device has a finite recovery time before accepting another input [trigger]. The updating mode will produce an output pulse for every input pulse received. If the input pulses arrive at a high rate the output will be at a constant level or "on" until the input [trigger] is removed. The updating or non updating feature can be changed on a channel by channel basis by installing or removing a jumper.

- **ECL Output Section**

Dual outputs for each input channel are driven by use of a MC10H101 ECL line driver. Each output is driven differentially to the front panel output connectors P2 and P3. The polarity of the ECL signals is identical to the input connector scheme and the connectors are polarized. The seventeenth (17^{th}) connector pair is unused.

Each output pin is pulled down to –5.2V through a 470Ω resistor. This enables the user to view the output pulse width using an oscilloscope probe that is terminated to 1MegΩ.

4.0 Specifications

Single Wide CAMAC IEEE-STD 583-1975 module

INPUT Specifications
Front Panel
P1: Two (2) rows by seventeen (17) pin polarized connector.
17^{th} pair not connected
Nominal ECL voltage levels required from source device.

Maximum input frequency:	This is a function of output pulse width setting assuming non-updating mode. For 15ns output pulse width setting, the maximum input frequency is 30Mhz.
Minimum input pulse width:	>3nS.

Output Specifications
Front Panel
P2 and P3: Two (2) rows by seventeen (17) pin polarized connector.
17^{th} pair not connected

Minimum output pulse width:	15nS
Maximum output pulse width:	User adjustable. Default setting is 200nS. Maximum pulse width can be adjusted and will require calibration in the Electronics lab.
Maximum output current	50mA per channel
Input to Output Delay:	<10nS per channel <1nS deviation for all channels
Pulse Width Jitter:	<1nS per channel <3ns deviation for all channels

Digital to Analog Converter: [Pulse Width Control]
12 Bit resolution. User selectable full scale range of +2.5Vdc; +5.0Vdc; or +10.0 volt full scale.
Jumper selectable range. Default setting is +2.5Vdc

12 bit data is straight binary format. 0V = 0000h; +Full Scale = 0FFFh
Data is latched into Xilinx CPLD during Camac Write cycle.

5.0 Instructions

5.0.1 Setting the user selectable jumpers.

a) Updating and Non-Updating Mode [J1 – J16]

The user can select the output mode for each monostable circuit. The user should record the jumper settings for each channel. The jumpers will be installed as default and which places each monostable in the NON-updating mode. Removing the jumper places the monostable in updating mode.

b) Full Scale DAC output [J17 – J19]

The programmable pulse width is achieved by varying the voltage to each monostable circuit's control pin. The full scale DAC output can be changed by a jumper. Normally users should not modify the default jumper position as the board has been calibrated in the lab with the selected DAC setting.

5.0.2 CAMAC Commands

The module produces a valid response, [X=1] for the following CAMAC functions:

F16	A0	Write Data to DAC
F0	A0	Read Data
F9	A0	Clear Command

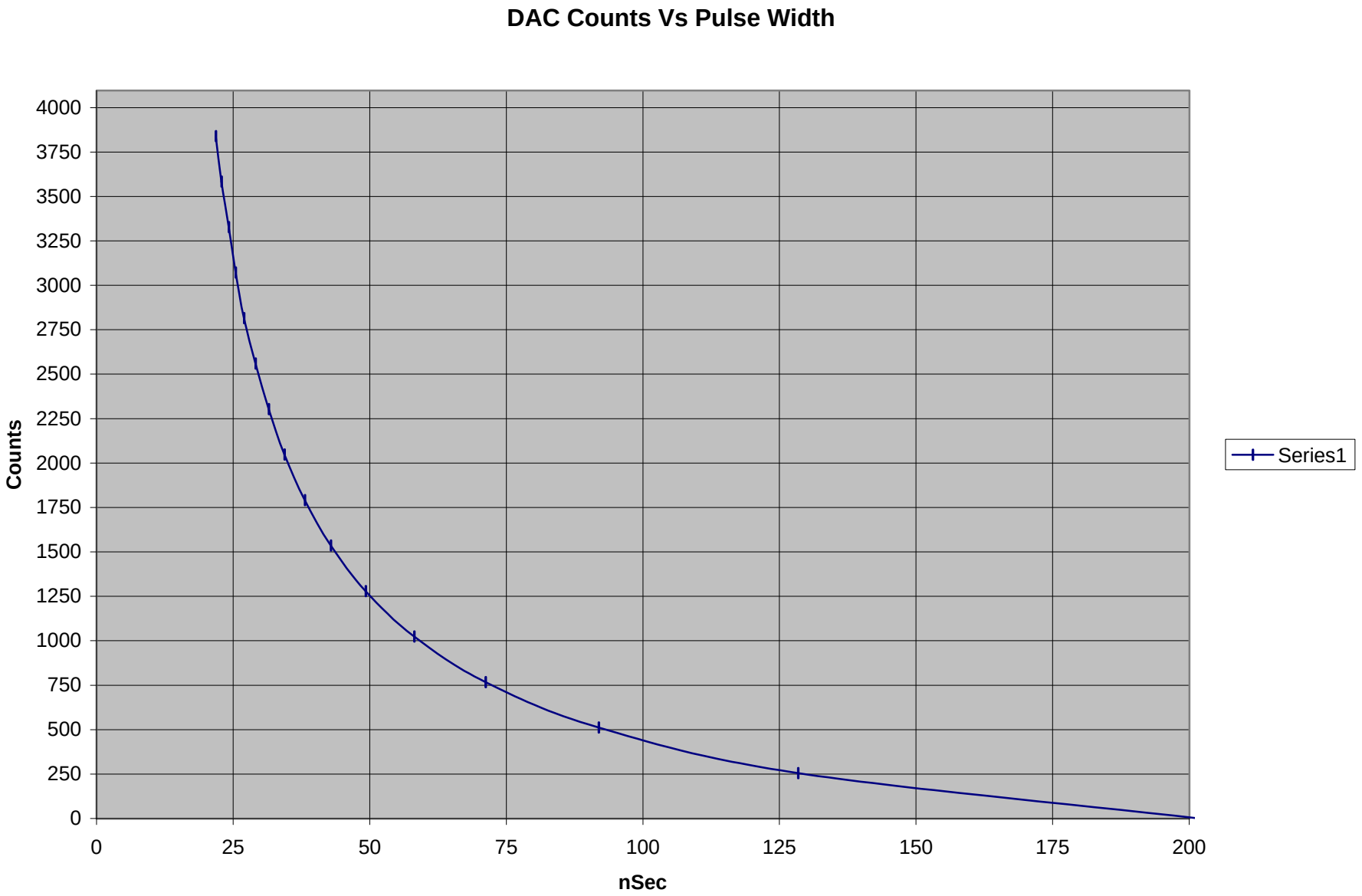
The F16 command is the only command that is implemented on the Xilinx CAMAC decoder chip. The Read [F0] and Clear [F9] functions will produce a valid command response and illuminate the 'N" indicator light on the front panel of the module, but are not used for the present design.

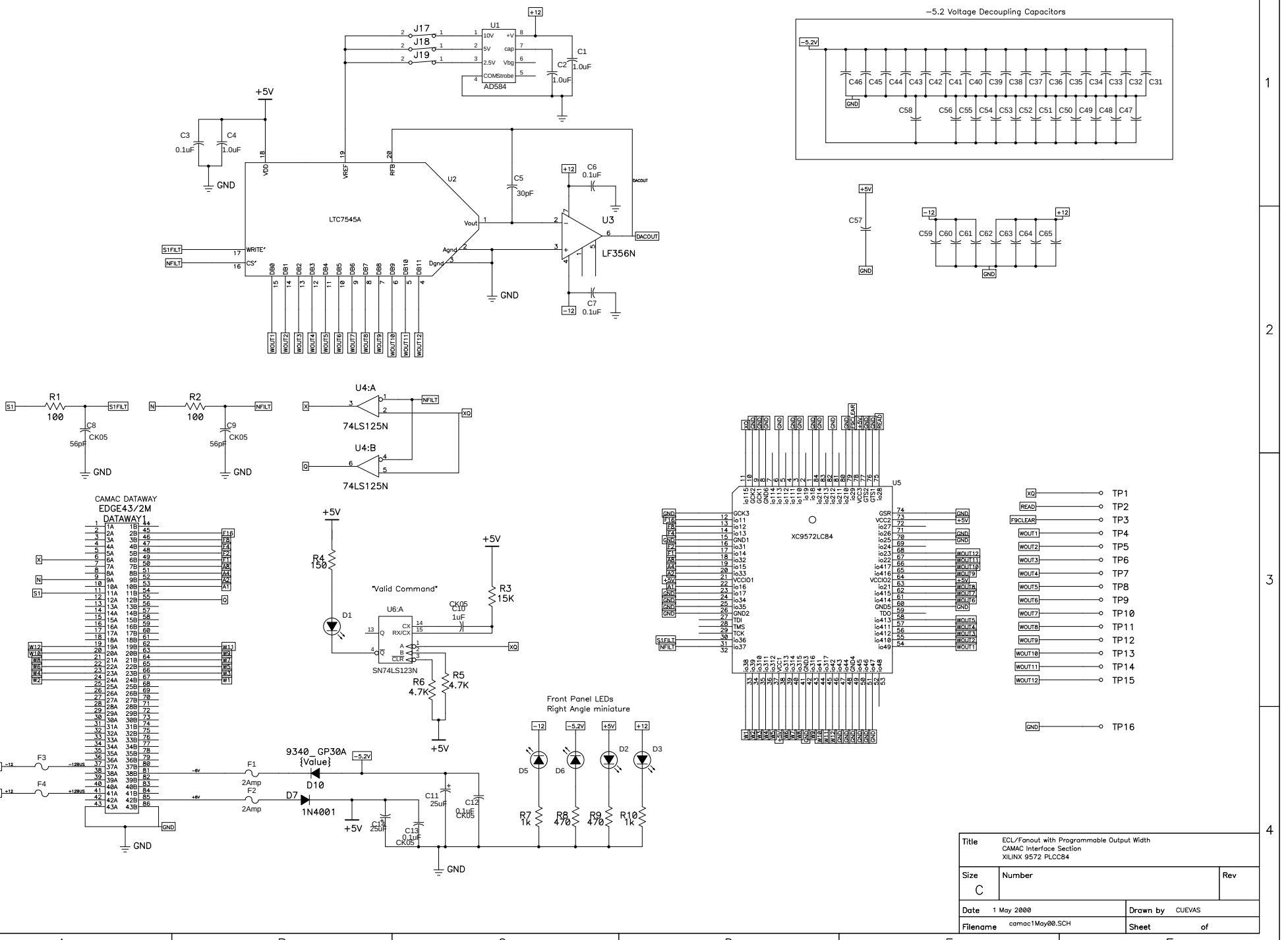
The F16 – A0 command is used to write data to the twelve bit DAC. The data is in "straight" binary format where 0x0000 sets the DAC to zero and 0x0FFF sets the DAC to full scale. Setting the DAC to zero programs the widest [default] output pulse.

Graph 1 on the following page shows the typical curve for DAC counts vs. pulse width output. The curve is typical of all channels on the board.

6.0 Appendices [

6.0.1 Schematics
6.0.2 Component Designator Diagram
6.0.3 Parts List


DAC Counts Vs Pulse Width
Counts
4000
3750
3500
3250
3000
2750
2500
2250
2000
1750
1500
1250
1000
750
500
250
0
0
25
50
75
100
125
150
175
200
nSec
Series1


−5.2 Voltage Decoupling Capacitors
U1
AD584
J17
J18
J19
C1 1.0uF
C2 1.0uF
C3 0.1uF
C4 1.0uF
C5 30pF
C6 0.1uF
C7 0.1uF
U2
LTC7545A
U3
LF356N
C46 C45 C44 C43 C42 C41 C40 C39 C38 C37 C36 C35 C34 C33 C32 C31
C58 C56 C55 C54 C53 C52 C51 C50 C49 C48 C47
C57
C59 C60 C61 C62 C63 C64 C65
R1 100
R2 100
C8 56pF CK05
C9 56pF CK05
U4:A
U4:B
74LS125N
74LS125N
CAMAC DATAWAY
EDGE43/2M
DATAWAY1
U5
XC9572LC84
"Valid Command"
U6:A
SN74LS123N
R3 15K
R4 150
R5 4.7K
R6 4.7K
D1
9340_GP30A
{Value}
D10
1N4001
D7
F1 2Amp
F2 2Amp
F3
F4
C10 1uF
C11 25uF
C12 0.1uF CK05
C13 0.1uF CK05
Front Panel LEDs
Right Angle miniature
D2
D3
D5
D6
R7 1k
R8 470
R9 470
R10 1k
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
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Rev
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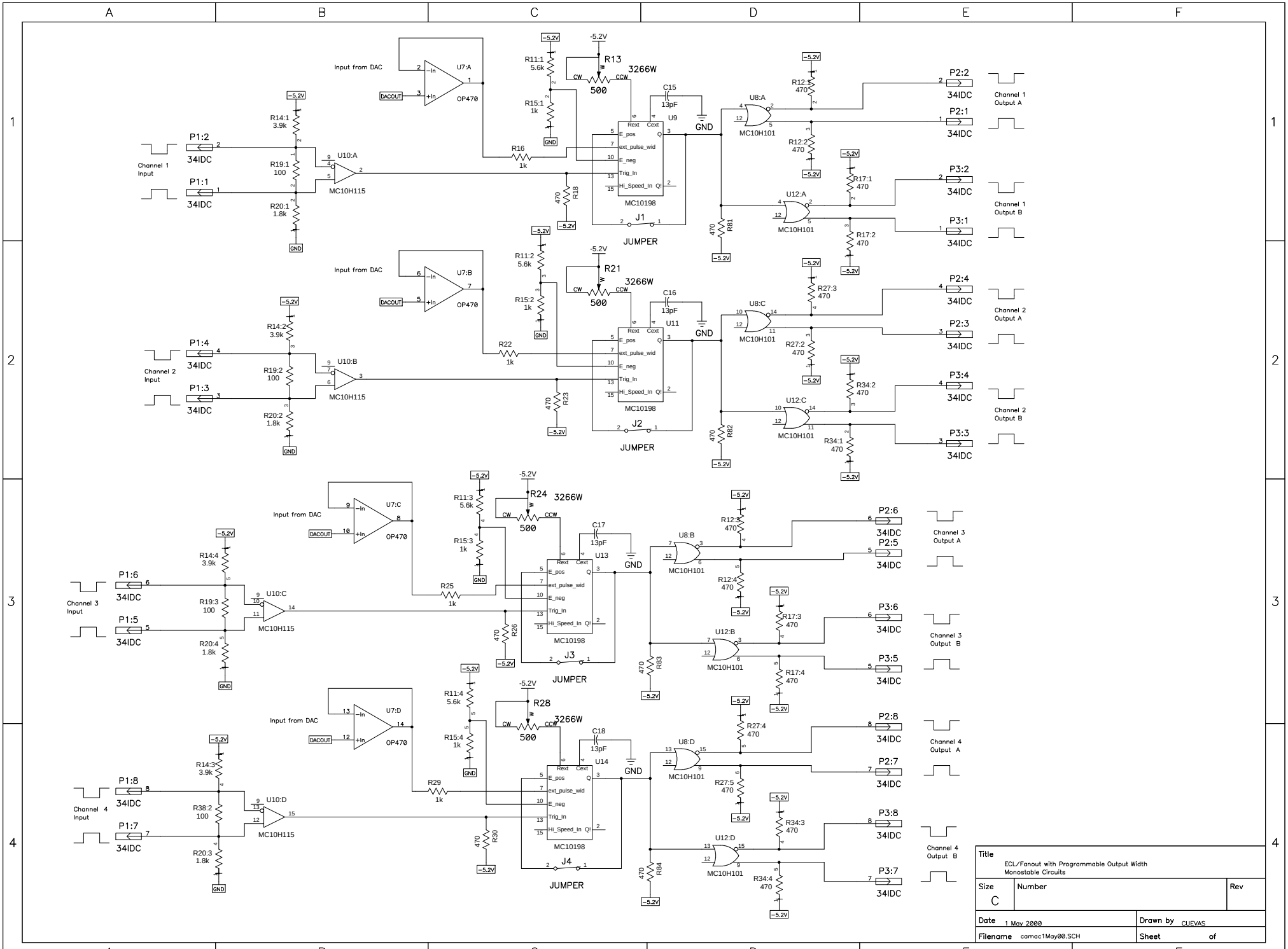
Input from DAC
DACOUT
U7:A
OP470
-5.2V
R11:1 5.6k
R13 3266W
500
CW
CCW
C15 13pF
R15:1 1k
GND
U9
MC10198
Rext
Cext
E_pos
ext_pulse_wid
E_neg
Trig_In
Hi_Speed_In
Q
Q!
R16 1k
R14:1 3.9k
P1:2
34IDC
Channel 1 Input
P1:1
R19:1 100
U10:A
MC10H115
R20:1 1.8k
R18 470
J1
JUMPER
U8:A
MC10H101
R12:1 470
R12:2 470
P2:2
P2:1
Channel 1 Output A
R17:1 470
R17:2 470
P3:2
P3:1
Channel 1 Output B
R81 470
U12:A
Input from DAC
U7:B
R11:2 5.6k
R21 3266W
C16 13pF
R15:2 1k
U11
R22 1k
R14:2 3.9k
P1:4
P1:3
Channel 2 Input
R19:2 100
U10:B
R20:2 1.8k
R23 470
J2
R27:3 470
U8:C
R27:2 470
R34:2 470
P2:4
P2:3
P3:4
P3:3
Channel 2 Output A
Channel 2 Output B
R82 470
U12:C
R34:1 470
Input from DAC
U7:C
R11:3 5.6k
R24 3266W
C17 13pF
R15:3 1k
U13
R25 1k
R14:4 3.9k
P1:6
P1:5
Channel 3 Input
R19:3 100
U10:C
R20:4 1.8k
R26 470
J3
U8:B
R12:3 470
R12:4 470
P2:6
P2:5
Channel 3 Output A
R17:3 470
R17:4 470
P3:6
P3:5
Channel 3 Output B
R83 470
U12:B
Input from DAC
U7:D
R11:4 5.6k
R28 3266W
C18 13pF
R15:4 1k
U14
R29 1k
R14:3 3.9k
P1:8
P1:7
Channel 4 Input
R38:2 100
U10:D
R20:3 1.8k
R30 470
J4
U8:D
R27:4 470
R27:5 470
P2:8
P2:7
Channel 4 Output A
R34:3 470
P3:8
P3:7
Channel 4 Output B
R84 470
U12:D
R34:4 470
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Rev
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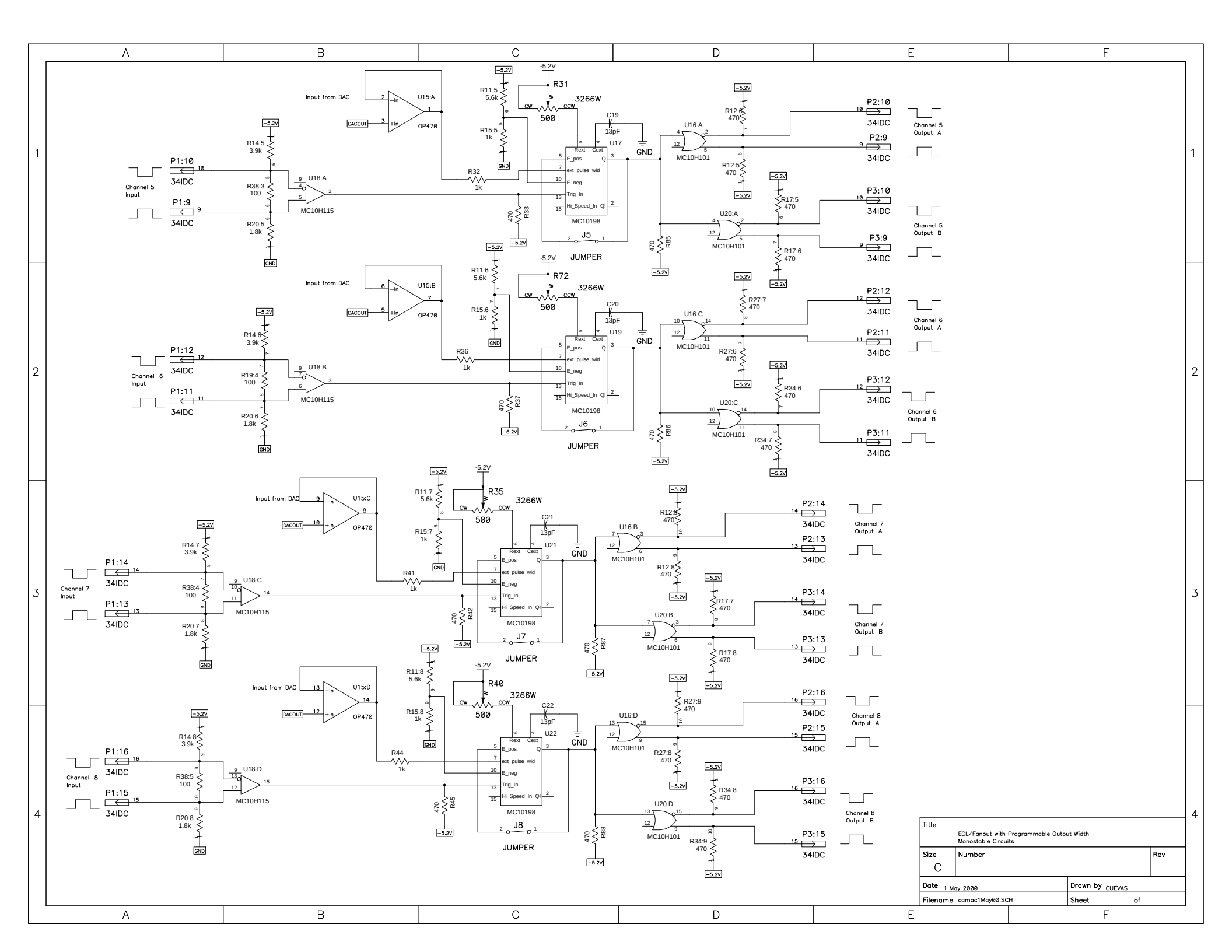

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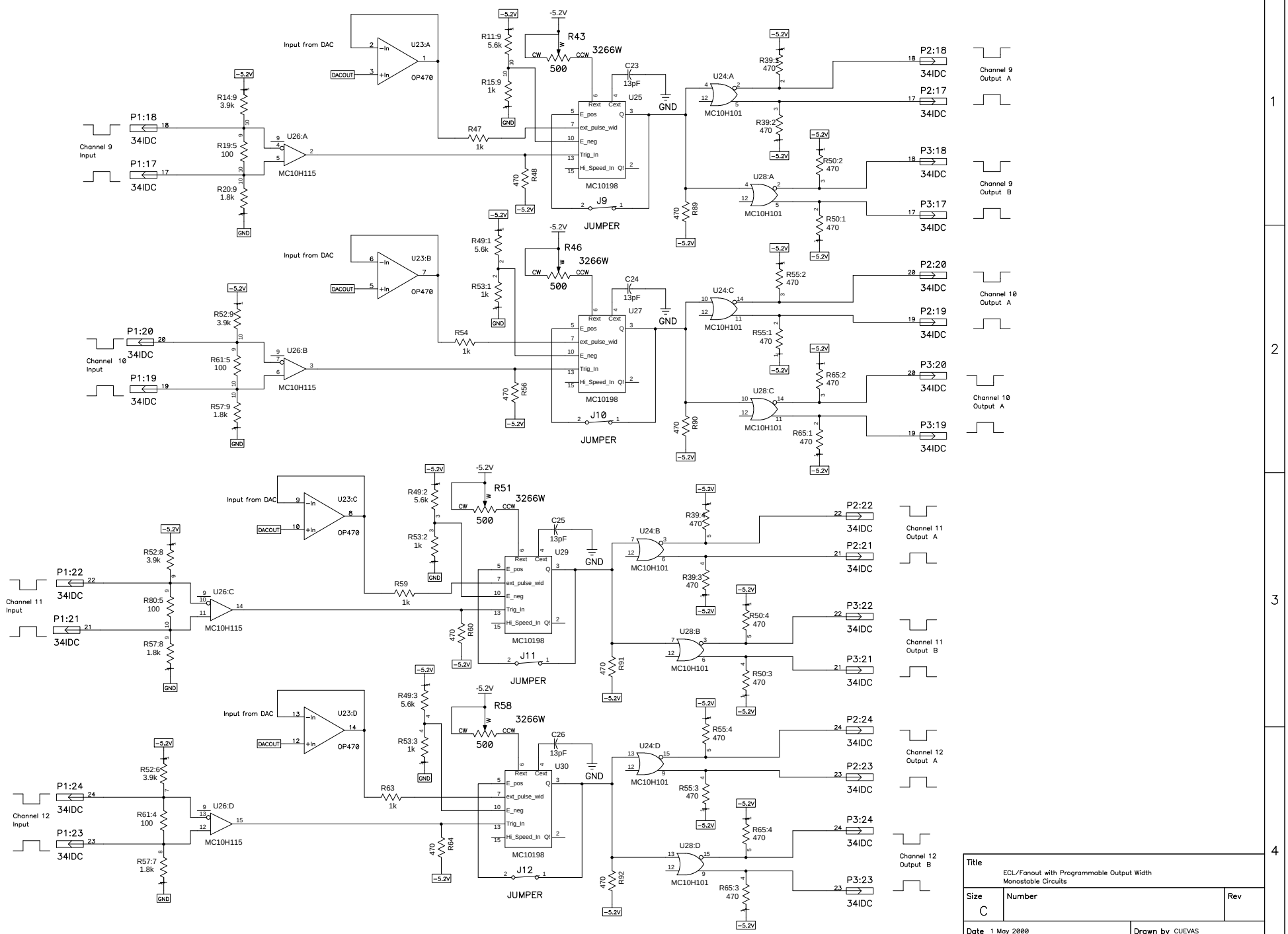
Input from DAC
U23:A
OP470
DACOUT
-5.2V
R11:9
5.6k
R15:9
1k
R43
3266W
CW
CCW
500
C23
13pF
GND
U25
MC10198
R47
1k
R48
470
J9
JUMPER
U24:A
MC10H101
R39:1
470
R89
470
P2:18
34IDC
P2:17
34IDC
R50:2
470
U28:A
R50:1
470
P3:18
34IDC
P3:17
34IDC
Channel 9
Output A
Channel 9
Output B
P1:18
34IDC
P1:17
34IDC
Channel 9
Input
R14:9
3.9k
R19:5
100
R20:9
1.8k
U26:A
MC10H115
U23:B
R49:1
5.6k
R53:1
1k
R46
R54
1k
R56
470
U27
C24
13pF
J10
R55:2
470
U24:C
R55:1
470
R90
470
P2:20
34IDC
P2:19
34IDC
R65:2
470
U28:C
R65:1
470
P3:20
34IDC
P3:19
34IDC
Channel 10
Output A
P1:20
34IDC
P1:19
34IDC
Channel 10
Input
R52:9
3.9k
R61:5
100
R57:9
1.8k
U26:B
MC10H115
U23:C
R49:2
5.6k
R53:2
1k
R51
R59
1k
R60
470
U29
C25
13pF
J11
R39:4
470
U24:B
R39:3
470
R91
470
P2:22
34IDC
P2:21
34IDC
R50:4
470
U28:B
R50:3
470
P3:22
34IDC
P3:21
34IDC
Channel 11
Output A
Channel 11
Output B
P1:22
34IDC
P1:21
34IDC
Channel 11
Input
R52:8
3.9k
R80:5
100
R57:8
1.8k
U26:C
MC10H115
U23:D
R49:3
5.6k
R53:3
1k
R58
R63
1k
R64
470
U30
C26
13pF
J12
R55:4
470
U24:D
R55:3
470
R92
470
P2:24
34IDC
P2:23
34IDC
R65:4
470
U28:D
R65:3
470
P3:24
34IDC
P3:23
34IDC
Channel 12
Output A
Channel 12
Output B
P1:24
34IDC
P1:23
34IDC
Channel 12
Input
R52:6
3.9k
R61:4
100
R57:7
1.8k
U26:D
MC10H115
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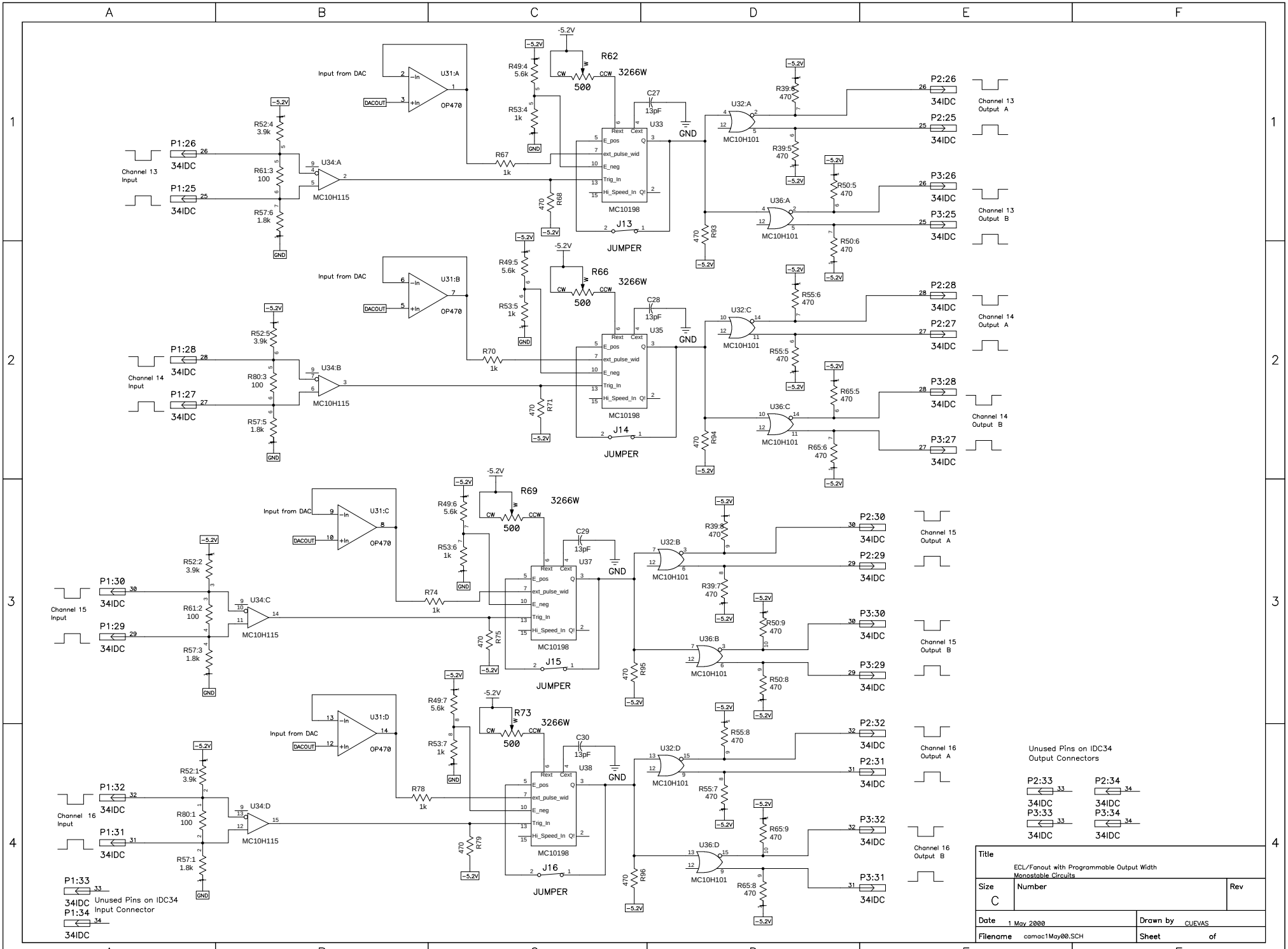
Input from DAC
U31:A
OP470
DACOUT
-5.2V
R49:4 5.6k
R62
3266W
CW
CCW
500
R53:4 1k
C27 13pF
U33
MC10198
GND
R67 1k
R68 470
J13
JUMPER
P1:26
34IDC
P1:25
34IDC
Channel 13 Input
R52:4 3.9k
R61:3 100
R57:6 1.8k
U34:A
MC10H115
U32:A
MC10H101
R39:6 470
R39:5 470
P2:26
P2:25
Channel 13 Output A
U36:A
R50:5 470
R50:6 470
P3:26
P3:25
Channel 13 Output B
R93 470
Input from DAC
U31:B
R49:5 5.6k
R66
R53:5 1k
C28 13pF
U35
R70 1k
R71 470
J14
JUMPER
P1:28
P1:27
Channel 14 Input
R52:5 3.9k
R80:3 100
R57:5 1.8k
U34:B
U32:C
R55:6 470
R55:5 470
P2:28
P2:27
Channel 14 Output A
U36:C
R65:5 470
R65:6 470
P3:28
P3:27
Channel 14 Output B
R94 470
Input from DAC
U31:C
R49:6 5.6k
R69
R53:6 1k
C29 13pF
U37
R74 1k
R75 470
J15
JUMPER
P1:30
P1:29
Channel 15 Input
R52:2 3.9k
R61:2 100
R57:3 1.8k
U34:C
U32:B
R39:8 470
R39:7 470
P2:30
P2:29
Channel 15 Output A
U36:B
R50:9 470
R50:8 470
P3:30
P3:29
Channel 15 Output B
R95 470
Input from DAC
U31:D
R49:7 5.6k
R73
R53:7 1k
C30 13pF
U38
R78 1k
R79 470
J16
JUMPER
P1:32
P1:31
Channel 16 Input
R52:1 3.9k
R80:1 100
R57:1 1.8k
U34:D
U32:D
R55:8 470
R55:7 470
P2:32
P2:31
Channel 16 Output A
U36:D
R65:9 470
R65:8 470
P3:32
P3:31
Channel 16 Output B
R96 470
P1:33
P1:34
Unused Pins on IDC34 Input Connector
Unused Pins on IDC34 Output Connectors
P2:33
P2:34
P3:33
P3:34
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ECL/Fanout with Programmable Output Width Monostable Circuits
Size
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Date
1 May 2000
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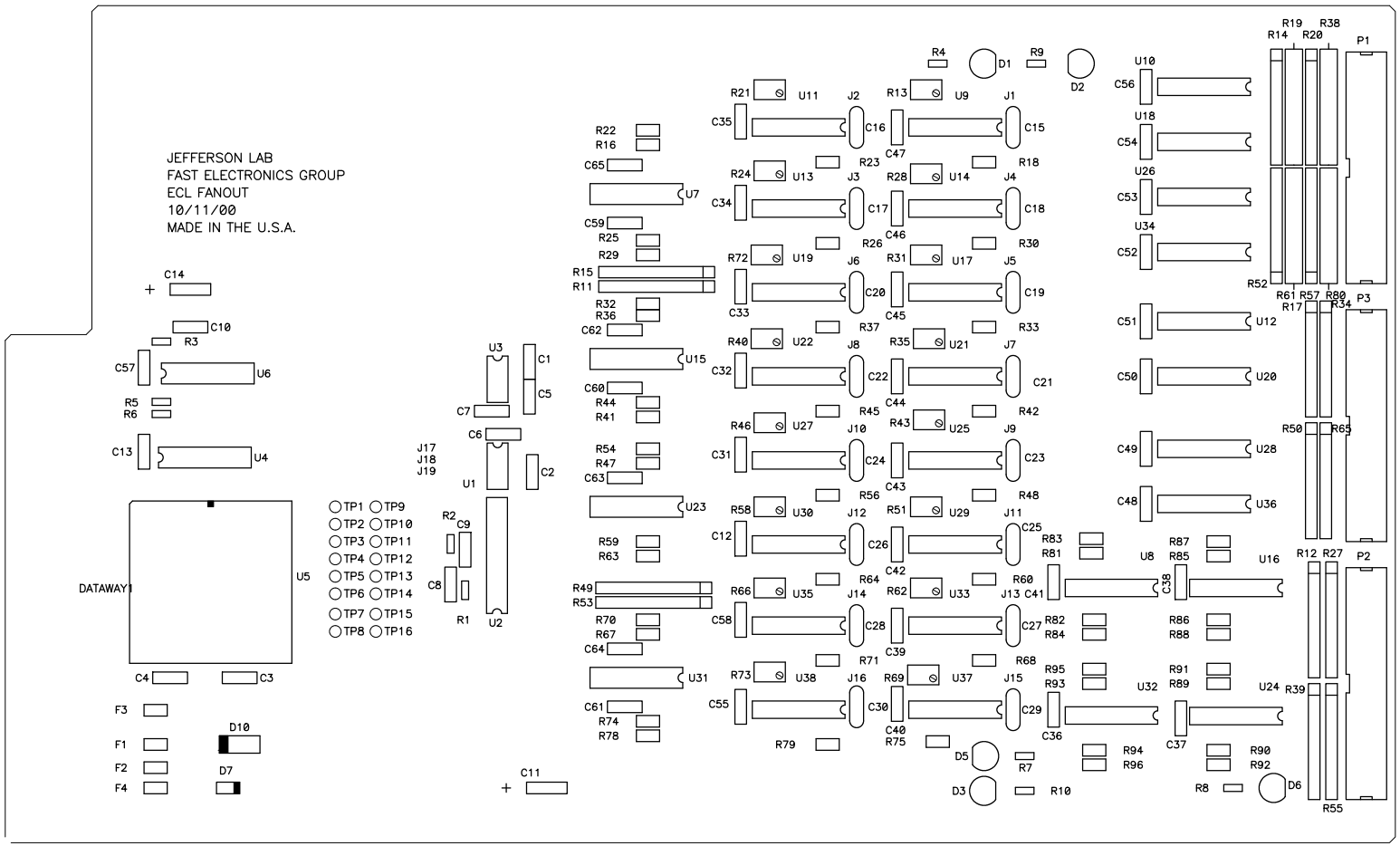

Drill Symbol Table		
Hole Dia (inch)	Symbol	Quantity
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0.022	X	20
0.030	Y	488
0.031	T	32
0.032	XX	52
0.035	XS	134
0.038	S	598
0.055	D	2
0.144	SQ	22

SLKTOP