VMIVME-1182
64-Channel Isolated Digital Input Board with Multifunctional Intelligent Controller

- 64 optically isolated inputs
- Multifunctions available per channel
  - — Change-of-State (COS)
  - — Sequence-of-events (SOEs)
  - — Pulse accumulation
  - — Programmable debounce times
  - — Time tagging
- 5 to 250 VDC or 4 to 240 VAC
- 1,500 VDC or 1,100 VRMS channel-to-channel and channel-to-VMEbus isolation
- Pulse accumulation (0 to 65,535 pulses)
- Sequence-of-events (SOEs) monitoring on channel-by-channel basis
- Debounce times software controlled on channel-by-channel basis
- 1.0 ms measurement interval
- Change-of-State (COS) functions software controlled on a channel-by-channel basis
- COS selections (disabled, rising edge (low-to-high transition), falling edge (high-to-low transition), or any edge
- Short or standard, supervisory, nonprivileged, or either access
- Interrupt level is user selected
- UIOC® compatible
- Complies with ANSI/IEEE STD C37.90.1-1989 surge protection when used with companion suppression panel (for example, VMIVME-3459)

APPLICATIONS

- Data acquisition systems
- Nuclear power plant monitoring
- Control systems

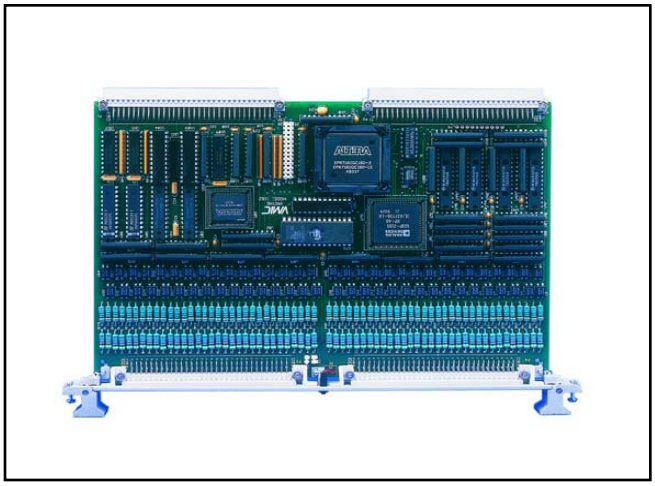
INTRODUCTION — The VMIVME-1182 provides 64 digital inputs with which changes-of-state (COS) can be detected, time tagged, and counted. An on-board buffer can be programmed to store the COS information with a time-tag such that sequences-of-events (SOEs) can be analyzed. A pulse accumulator is provided to count the COSs. The VMIVME-1182 can also be programmed to issue an interrupt when a COS is detected. All COS detection is on a per-channel basis effectively creating 64 pulse accumulators.

The SOE memory is allocated into two buffers. The system host can be processing one buffer while the other buffer is being loaded with new event data.

Each input is optically isolated with input voltage options up to 250 VDC. Inputs may also be configured for contact sensing. A programmable debouncer is provided for each input to reject spurious input pulses.

CHANGE-OF-STATE (COS) TIMING — The VMIVME-1182 latches the input signals every millisecond. After a programmable debounce time, if a valid COS is detected, it is time tagged by the millisecond timer and stored for processing. The debounce time can be from 1 ms to 1,024 s. Therefore, the minimum pulse time that can be reliably detected is 2 ms.

If the VMIVME-1182 is programmed to detect COS on both rising and falling edges, the minimum time in each state is 2 ms. Thus, 4 ms is the minimum period of a continuous input signal.



Each input channel is independent and is processed separately, so activity on one channel has no effect on other channels. A COS on one channel can be detected and stored while the debouncer is timing on another channel. Since all inputs are latched simultaneously every millisecond and they are processed separately, there can be minimum of 1 ms between events that occur on different channels.

Ordering Options

July 30, 1996 800-001182-000 D		A	B	C	–	D	E	F
VMIVME-1182	–	0			–			

A = 0 (Option reserved for future use)

B = Input Voltage Range*
0 = 5 VDC, 4 VAC
1 = 12 VDC, 10 VAC
2 = 24 VDC, 18 VAC
3 = 28 VDC, 20 VAC
4 = 48 VDC, 45 VAC
5 = 60 VDC, 55 VAC
6 = 125 VDC, 110 VAC
7 = 250 VDC, 240 VAC

C = Input Configuration
0 = Voltage Sensing
1 = Contact Sensing

Note*

DC or AC software selectable.

Connector Data
Discrete Wire Input Connector Data

Mating Connector	AMP No. 925486-1
Female Crimp Contacts*	AMP No. 530151-6
Connector Shell Housing	Harting No. 09 03 096 0501
PC Board Connector	Panduit No. 120-964-033A

*An AMP crimp tool part number is 90301-2.

For Ordering Information, Call:
1-800-322-3616 or 1-256-880-0444 • FAX (256) 882-0859
E-mail: info@vmic.com Web Address: www.vmic.com

CHANGE-OF-STATE DETECTION — State change detection can be programmed for rising edge (low-to-high transition), falling edge (high-to-low transition), or both rising and falling edges. In addition, COS detection can generate an interrupt or be disabled.

TIME TAGGING — Each Change-of-State event can be time tagged with a timer value of 0 to 65 s and is initialized or preset by writing to the time tag register.

The timer value is updated every millisecond. When the timer value has reached its maximum value, it rolls over to 0 and notifies the host of a time tag rollover via a bit in the Control Register, or if desired, an interrupt may be issued.

SEQUENCE-OF-EVENTS — Each change-of-state (depending on change select options) can be time-tagged in the sequence-of-event buffer. The SOE buffer collects the channel ID, and the time (time tag register) in which the state changed. This buffer can contain 3,000 events. When the host is accessing the SOE buffer, the VMIVME-1182 will continue to monitor the inputs and store events in a mirrored SOE buffer. The additional buffer also provides 3,000 events of storage. This allows the user the ability to process the SOE data (without time constraint problems) and not lose any event data. The SOE logic can provide an interrupt to the host at the End-of-Buffer or an interrupt at a count provided by the user (programmable).

PULSE ACCUMULATION — Each channel has an associated Pulse Accumulation Count (PAC) Register. These registers have values which represent the number of pulses which have been detected at the field input. A pulse is edge-recognized by either a state change from a 0 to 1 or a state change from 1 to 0. The user will be notified when the count in the PAC Register has reached its maximum value of 65,535 pulses. This condition is indicated by a flag set in the Control Register, or if desired, an interrupt may also be issued.

INPUTS — The VMIVME-1182 can be ordered in the Voltage Sensing option or the Contact Sensing option. The input configurations for each of these options is shown in Figure 2.

The Contact Sensing option is provided with pull-up resistors to the wetting voltage pins. The Voltage sourcing option does not provide pull-ups.

There are eight wetting voltage input pins applied on byte boundaries. The inputs are provided on the P2 connector. An additional feature is the ability to drive the wetting input via channel 32 of the P3 connector. Through the use of jumpers (see Figure 3), channel 32 can be sacrificed as a channel and its HIGH input used to supply a wetting voltage to all channels. The LOW side of channel 32 can be jumpered to acquire Digital ground from the VMIVME-1182.

The electrical specifications for the inputs are shown in Table 1.

Table 1

Input Voltage	Threshold High (V)	Threshold Low (V)	Contact Sensing		Voltage Sensing (mA)
			Open Circuit Voltage (V) ± 8%	Contact Current (mA) ± 15%	Source Current @ V_{input} ± 15%
5 VDC	3.4	1.7	4.4	6.7	1.0
12 VDC	8.2	3.3	11.0	8.0	.9
24 VDC	17	6.0	21.3	6.0	.8
28 VDC	17	6.0	24.8	7.0	.9
48 VDC	33	11.0	41.3	4.8	.8
60 VDC	41.5	14.0	53.5	6.0	.7
125 VDC	85	30.0	87	2.7	.7
250 VDC	189	66.0	157	1.6	.9

FUNCTIONAL CHARACTERISTICS

Interchannel Crosstalk Rejection: 80 dB minimum at 1 kHz

Common-Mode Rejection (CMRR): 80 dB minimum DC to 60 Hz

Isolation: 1,500 VDC or 1,100 VRMS field-to-bus, channel-to-channel for voltage sensing.

1,500 VDC or 1,100 VRMS field-to-bus, byte-to-byte for contact sensing when wetting voltage applied at P2.

VMEbus Compliance: This board complies with the VMEbus specification (ANSI/IEEE STD 1014-1987 IEC 821 and 297) with the following mnemonics:

Addressing Mode	Responding Address Modifiers
A24	$39 (Standard nonprivileged data access) or $3D (Standard supervisory data access)
A16	$29 (Short nonprivileged I/O access) or $2D (Short supervisory I/O access)
Data Access:	D16, D08(EO)
Interrupts:	One, any level, ROAK

Board Address: The base VMEbus address is set by configuration of a jumper field. A jumper exists for each of the addresses A23 through A14; thus, the address space occupied by this board is 8 Kwords.

VMEbus Access: Address modifier bits are jumper selected and decoded to support nonprivileged, supervisory, and either nonprivileged or supervisory board accesses.

Self-Test: Self-test is run automatically after a system reset, and can also be run by activating the Test Mode bit in the CSR. A pass/fail value is stored in the Control Register space. The LED remains illuminated regardless of the pass/fail status of the self-test. The self-test is primarily an integrity check of the microcontroller and the on-board memory.

System Reset: After a system reset, the following default conditions exist:

Input transfers with 1 ms debounce
LED illuminated
Test Mode enabled

Front Panel Status LED: This indicator is illuminated after a system reset. The LED can also be turned ON and OFF under software control.

Interrupts: An interrupt can be issued on any level (software selectable) and a single byte vector will be placed on the bus when acknowledged. There is one ROAK interrupt for the board. The following conditions can initiate the interrupt:

COS on any of the 64 channels
Time-Tag Rollover
Pulse Accumulation Rollover on any of the 64 channels
Sequence-of-Event, End-of-buffer
Sequence-of-Event buffer count equal to programmable maximum count provided by user

Each of these interrupt conditions may be enabled or disabled by the host.

PHYSICAL/ENVIRONMENTAL

Dimensions: Standard VME double height board (160 x 233.5 mm)

Temperature: 0 to +65 °C, operating
-25 to +85 °C, storage

Relative Humidity: 20 to 80 percent, noncondensing

Cooling: Forced air

Power Requirements: 2.0 A (typical) at 5 V plus any power dissipated in pull-up resistors

Altitude: Operation to 10,000 ft (3,048 m)

Weight (Mass): 0.7 kg maximum

TRADEMARKS

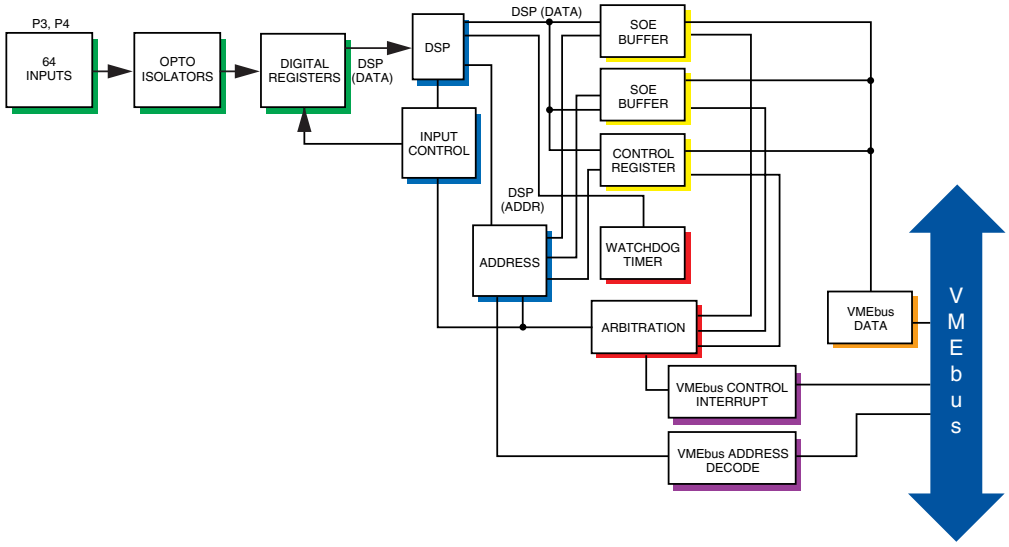


Figure 1. VMIVME-1182 Functional Block Diagram

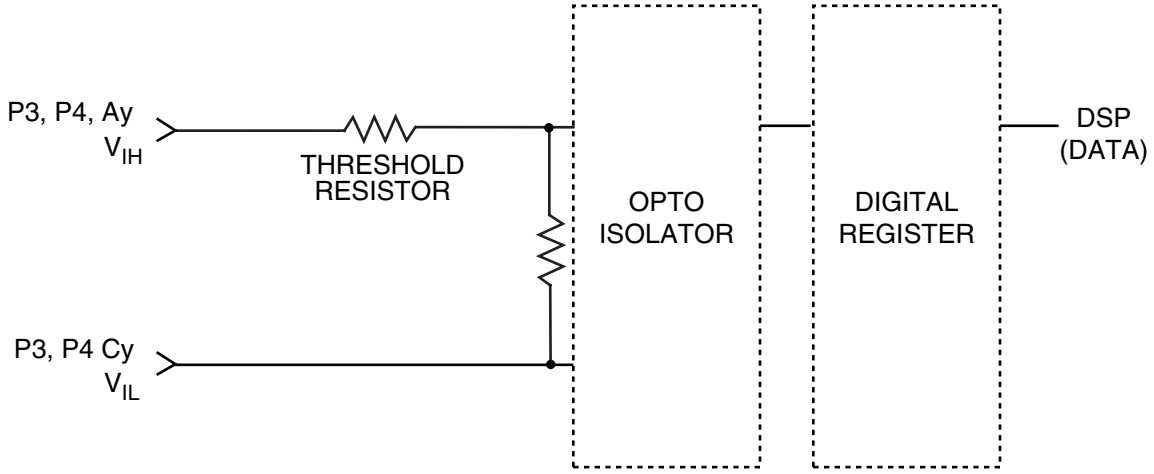


Figure 2a. User Input Connection Circuit (Voltage Sensing)

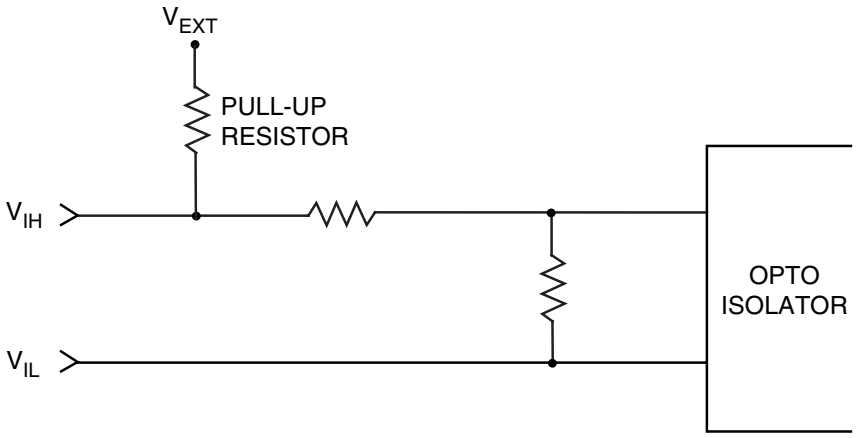


Figure 2b. Contact Sensing

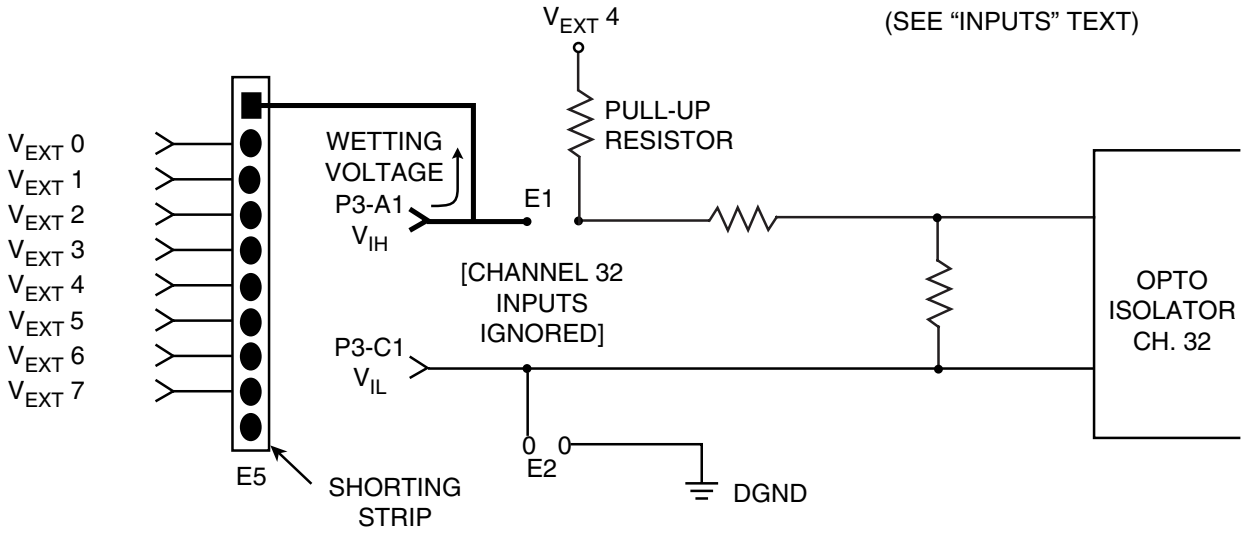


Figure 3. P3 Wetting Voltage Input