



## **VMIVME-1182**

### **64-CHANNEL ISOLATED DIGITAL INPUT BOARD WITH MULTIFUNCTIONAL INTELLIGENT CONTROLLER**

#### **PRODUCT MANUAL**

DOCUMENT NO. 500-001182-000 A

August 2, 1994

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# RECORD OF REVISIONS

| REVISION LETTER                                                                                              | DATE    | PAGES INVOLVED          | CHANGE NUMBER  |
|--------------------------------------------------------------------------------------------------------------|---------|-------------------------|----------------|
| A                                                                                                            | 8/02/94 | Release                 | 94-0635        |
| VME MICROSYSTEMS INT'L CORP.<br>12090 South Memorial Parkway •<br>Huntsville, AL 35803-3308 • (205) 880-0444 |         | DOC. NO. 500-001182-000 | REV LTR<br>A   |
|                                                                                                              |         |                         | PAGE NO.<br>ii |



# VMIC SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

## **GROUND THE SYSTEM**

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

## **DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE**

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

## **KEEP AWAY FROM LIVE CIRCUITS**

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Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

## **DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM**

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

## **DANGEROUS PROCEDURE WARNINGS**

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**W A R N I N G**

**DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.**



# SAFETY SYMBOLS

## GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



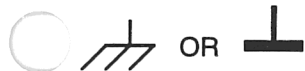
OR



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

**WARNING**

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE:**

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.





# VMIVME-1182

## 64-CHANNEL ISOLATED DIGITAL INPUT BOARD WITH MULTIFUNCTIONAL INTELLIGENT CONTROLLER

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## **APPENDIX**

### A Assembly Drawing, Parts List, and Schematic





## SECTION 1

### INTRODUCTION

#### 1.1 FEATURES

The VMIVME-1182 is a 64-channel optically isolated digital input board that can detect Changes of State (COS) on any of the 64 inputs. This COS data can be used in Sequence-of-Events (SOE) acquisition. The board provides pulse accumulation data, time tag data, and programmable debounce for each input. A variety of interrupt options are available. Figure 1.1-1 page 11 is a block diagram of the VMIVME-1182.

The VMIVME-1182 features are outlined below.

- a. 64 optically isolated inputs
- b. Multiple-functions available per channel:
  - Change-of-State (COS) detection
  - Sequence-of-Events (SOE) reporting
  - Pulse accumulation reporting
  - Time tag reporting
  - Programmable debounce times
- c. Available in 5 to 60 VDC or 110 to 240 VAC options
- d. Available in contact sensing or voltage sensing options
- e. 1000 VDC or 700 Vrms channel-to-channel and channel-to-VMEbus isolation (1 minute)
- f. Pulse accumulation for up to 65,535 pulses per channel
- g. Sequence-of-Events (SOE) monitoring on a channel-by-channel basis
- h. Debounce time software controlled on a channel-by-channel basis
- i. Change-of-State (COS) monitoring software controlled on a channel-by-channel basis
- j. A24/A16 addressing capability
- k. Supervisory bus access, nonprivileged bus access, or both
- l. Release-On-Acknowledge (ROAK) interrupts on all VMEbus levels

## 1.2 FUNCTIONAL DESCRIPTION

The VMIVME-1182 provides Change-of-State (COS) detection on all of its 64 inputs. Each input may be software controlled to detect rising edges, falling edges, or both rising and falling edges, or it may be software controlled to ignore all changes for a given channel. In addition to COS detection, a variety of reporting and interrupt capabilities are available.

Each COS event may be stored in a Sequence-of-Events (SOE) buffer where it is time tagged with a relative timer value of up to 65,535 ms. The timer may be reset from the VMEbus when desired. Each COS event is counted in Pulse Accumulation Count registers which record the number of events per channel.

VMEbus interrupts may be issued on any level (software selectable), and a single byte vector is placed on the bus during the acknowledge cycle. The interrupt is cleared during the acknowledge (ROAK). Addressing is jumper selected and supports both A24 and A16 address space.

Address modifiers are jumper-selected and are decoded to support nonprivileged, supervisory, or both nonprivileged and supervisory access. A self-test is run automatically after a system reset, setting the Self-Test Complete bit in the Control and Status register (CSR) to one when completed. The board is initialized with the following default conditions:

- a. Fail LED is ON.
- b. All interrupts are disabled.
- c. All flags are cleared.
- d. Test mode is enabled.
- e. Interrupt Vector (IVR) register is cleared.
- f. Change-of-State (COS) registers are cleared.
- g. Pulse Accumulation Interrupt (PAI) registers are cleared.
- h. Input Debounce/Select (DSR) registers are cleared.
- i. Input Pulse Accumulation Count (PAC) registers are cleared.
- j. Time tag clock is set to zero (0) and stopped.
- k. Sequence-of-Events (SOE) maximum count is cleared.
- l. Sequence-of-Events (SOE) count is cleared.
- m. Sequence-of-Events (SOE) buffers contain test data, but are cleared when the Test Mode bit is disabled.
- n. Self-Test Complete bit is set in the CSR.

### 1.3 REFERENCE MATERIAL LIST

Refer to "The VMEbus Specification" for a detailed explanation of the priority interrupt bus. "The VMEbus Specification" is available from the following source:

**VITA**  
**VFEA International Trade Association**  
**10229 N. Scottsdale Road**  
**Scottsdale, AZ 85253**  
**(602) 951-8866**

The following application and configuration guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

| <b><u>TITLE</u></b>                                          | <b><u>DOCUMENT NO.</u></b> |
|--------------------------------------------------------------|----------------------------|
| Digital Input Board Application Guide                        | 825-000000-000             |
| Change-of-State Application Guide                            | 825-000000-002             |
| Digital I/O (with Built-in-Test) Production Line Description | 825-000000-003             |
| Connector and I/O Cable Application Guide                    | 825-000000-006             |

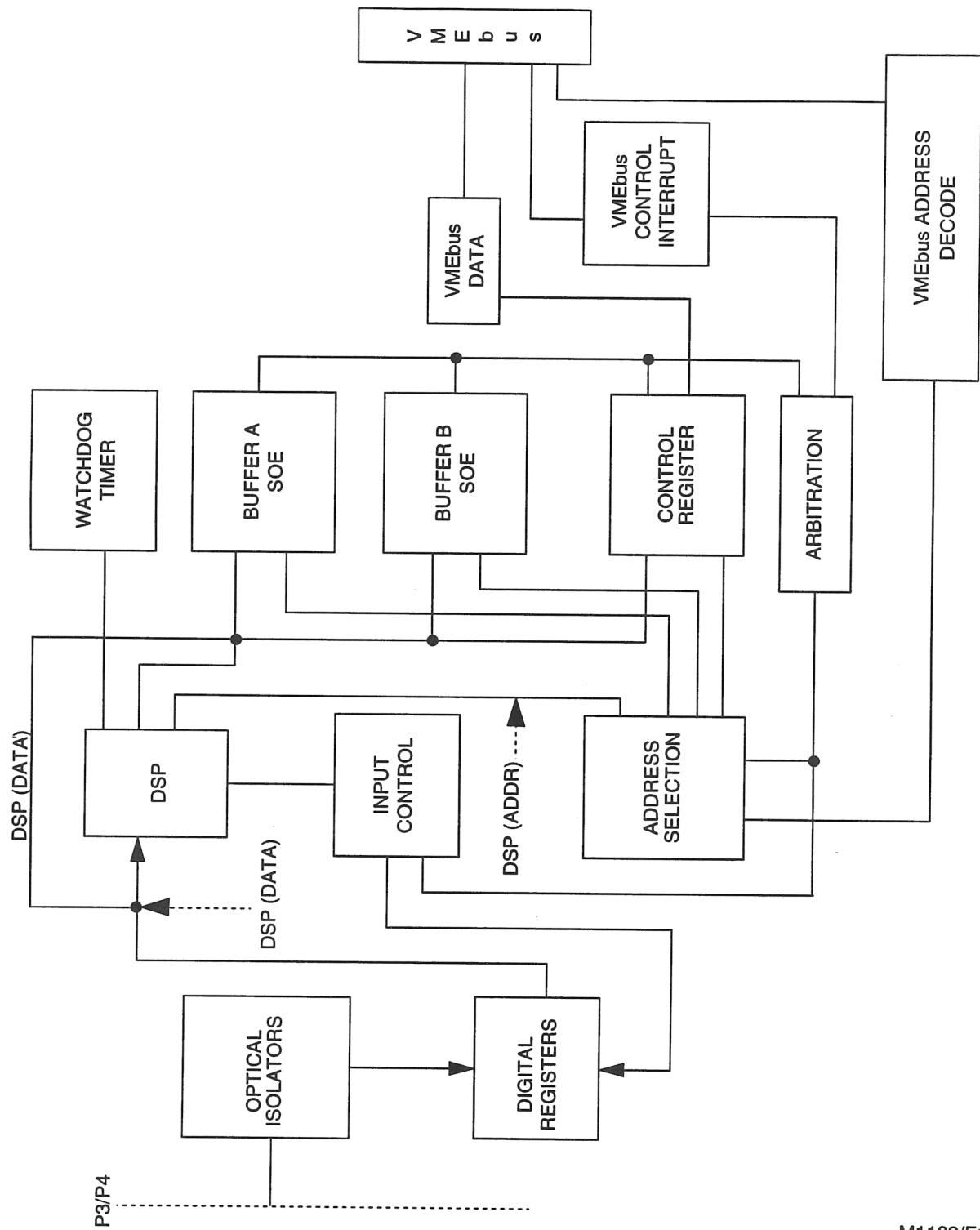


Figure 1.1-1. VMIVME-1182 Functional Block Diagram

## **SECTION 2**

# **PHYSICAL DESCRIPTION AND SPECIFICATIONS**

REFER TO 800-001182-000 SPECIFICATION



## **SECTION 3**

### **THEORY OF OPERATION**

#### **3.1 INTRODUCTION**

This section describes the internal organization of the VMIVME-1182 board and reviews the general principles of operation. Section 3.2 summarizes the major board functions, and the remainder of Section 3 describes each function individually. The information in this section is supplemented by programming details in Section 4 and by the schematic diagram in Appendix A.

#### **3.2 INTERNAL FUNCTIONAL ORGANIZATION**

The VMIVME-1182 is a 64-channel optically isolated digital input board that provides the user with a continuous update of the state of the 64 inputs. The user may elect to interrupt the host upon selected change-of-state events. COS data and time tag information is stored in memory (SOE monitoring) for later processing.

The SOE memory is allocated into two buffers which store the COS data with a sequential time tag for each event in the order that they occurred. The host can process the SOE buffer without losing any COS data from the inputs.

The VMIVME-1182 provides a Pulse Accumulation Count register for each channel. When enabled, these registers each store a count representing the number of times a COS has occurred on its associated input.

Inputs can be programmed individually for a debounce time from 1 ms to 1.023 seconds.

The board design can be logically divided into functional blocks which describe the following principal hardware functions:

- a. Field Inputs
- b. Input Data Processing by the Digital Signal Processor (DSP)
- c. EPROM
- d. VMEbus Interface
- e. Control Logic
- f. Bus Interrupter
- g. Watchdog Timer
- h. Self-Test
- i. Power Requirements

### 3.3 FIELD INPUTS

The field inputs consist of 64 optically isolated inputs. Input options may be ordered to support either contact sensing or voltage sensing in a variety of AC or DC voltage ranges. The inputs are provided through connectors P3 and P4. Section 5 provides detailed information about both of these connectors.

#### 3.3.1 Voltage Sensing

The Voltage Sensing option detects the presence or absence of a voltage at the inputs. Figure 3.3.1-1 shows typical voltage sensing input circuitry.

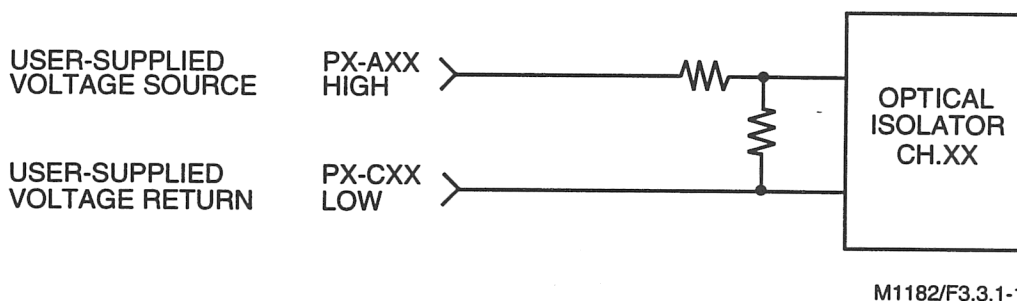


Figure 3.3.1-1. Voltage Sensing Input Circuit

#### 3.3.2 Contact Sensing

The Contact Sensing option detects the presence or absence of a closed contact set across the inputs. Figure 3.3.2-1 shows typical Contact Sensing Input circuitry. The external “wetting” voltage can be applied at the P2 connector on a byte level or can be applied to P3 at channel 32. This is described in detail in Section 5.

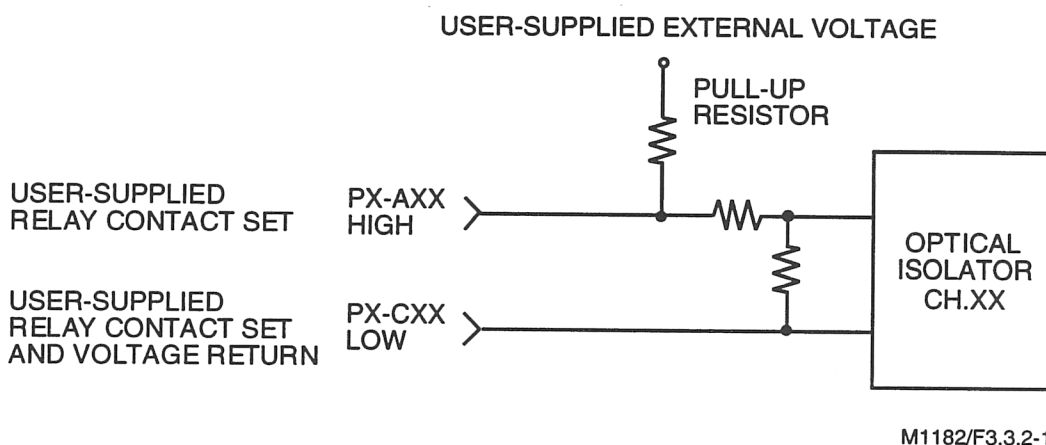


Figure 3.3.2-1. Contact Sensing Input Circuit



### 3.4 INPUT DATA PROCESSING

The VMIVME-1182 provides various programmable features. In default mode, the inputs are stored every millisecond and can be accessed by the user at any time. The programmable features are executed through an on-board Digital Signal Processor (DSP) chip and include:

- a. Debounce time for each input
- b. Pulse accumulation for each input
- c. COS definition/selection for each input
- d. Time tag clock
- e. Sequence-of-Event monitoring

Each feature is described in the following paragraphs.

#### 3.4.1 Debounce Time

The VMIVME-1182 provides 64 registers which contain the desired debounce time for each input. The debounce time ranges from 1 ms (default) to 1.024 seconds. See Section 4 for more information on selecting debounce times.

The debounce algorithm is implemented by the DSP microcontroller. Through the optical isolator, all 64 field inputs are clocked into registers during the DSP time interrupt service routine. The DSP processes this data using an algorithm which determines a true high or low state.

A different algorithm may be used by setting a bit in the Debounce/Select Register (see Section 4). This algorithm accepts inputs from AC signal sources. The rising edge period is determined by the Debounce/Select time provided by the user. The falling edge period requires the DSP to detect a low at four times the debounce time in milliseconds. This ratio, the AC Ratio, is defined in Section 4.

#### 3.4.2 Pulse Accumulation

Each channel has an associated Pulse Accumulation Count (PAC) register. The count represents 0 to 65,535 pulses. A pulse is defined as either a state change from zero (0) to one (1) or a state change from one (1) to zero (0), but not both. If the PAC Interrupt Enabled bit is activated, the PAC register interrupts the host when it rolls over to zero (0).

### 3.4.3 COS Definition

Each channel can be programmed to detect rising edge (low to high) only, falling edge (high to low) only, both edges, or no detection (COS disabled). Interrupts can be issued when any input meets the programmable COS selection. A detailed description of this function is found in Section 4.

### 3.4.4 Time Tag Clock

The Time Tag register is updated every millisecond. The user may reset or preset this data at any time. The Time Tag feature is provided by the DSP Timer Interrupt Logic and microcontroller. The microcontroller is interrupted every millisecond. During the interrupt service routine, the field inputs are stored and a frame flag is updated. A frame is the period in which all 64 inputs have been processed. Every frame, the DSP updates the Time Tag data. Each bit of the count in the Time Tag register represents 1 ms.

### 3.4.5 Sequence of Event

Depending on COS select options, each COS can be time tagged in the SOE buffer. The SOE buffer collects the channel ID and the time in which the state changed. This buffer can contain 3072 events. When the host is accessing the SOE buffer, the VMIVME-1182 continues to monitor the inputs and stores events in a mirrored SOE buffer. The additional buffer also provides 3072 events of storage, allowing the user sufficient time to process the SOE data without losing event data. The SOE logic can provide an interrupt to the host at the end-of-buffer or at a count provided by the user.

The SOE buffer arbitration is controlled by software. To read the data in the SOE buffer, the host first writes to the SOE Request register. A write to this register interrupts the DSP code and switches the pointer in the DSP to the second SOE buffer. The VMEbus then has access to the first SOE buffer while the DSP continues its updates to a second SOE buffer. This method allows the DSP to always have access to one of the SOE buffers in order to prevent data loss.

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**THE DSP WILL AUTO WRAP THE BUFFER AND BEGIN WRITING OVER OLD DATA WHENEVER THE BUFFER REACHES THE PHYSICAL END OF THE BUFFER. THE SOE COUNT ROLLS OVER FROM 3072 TO ZERO (0) AND CONTINUES COUNTING. THE HOST MUST PROCESS THE DATA FROM THE PRIMARY BUFFER BEFORE THE DSP REACHES THE PHYSICAL END OF THE DATA BUFFER OR DATA CAN BE LOST. INTERRUPTS ARE PROVIDED (SOE MAXIMUM COUNT) TO ALERT THE HOST THAT DATA NEEDS TO BE PROCESSED.**

The SOE count is valid for whichever SOE buffer the DSP is currently updating. Once the buffer is requested, the SOE count is written to the SOE index and then reset to zero (0).

### **3.4.6     EPROM**

DSP firmware is stored in the EPROM and is loaded into the DSP during power up or after a reset to the DSP. The DSP can be reset by the VMEbus system reset or by the watchdog timer circuitry.

## **3.5     VMEbus INTERFACE**

The VMEbus interface consists of:

- a. Address decoding for the A24/A16 address space
- b. Address modifier decoding for supervisory/nonprivileged accesses
- c. D16/D8 data transfers
- d. ROAK interrupter circuitry
- e. Two SOE buffers
- f. Control logic memory

### **3.5.1     Control Logic**

The Control Logic offset address begins at \$000. The Board ID register contains an ID code which indicates the VMIVME-1182 is present. The Control and Status register provides control of the front panel LED, the Test Mode Disable, and various interrupt enables. It also provides various flags, including a Self-Test complete flag.

The Self-Test Results register provides pass/fail status of the VMIVME-1182 integrity tests. The Interrupt Vector register provides programmable level and vector data. Debounced input data is provided in four words, each bit representing a channel. Change of State registers are provided in four words, each bit representing a channel. Pulse Accumulation Interrupt registers are provided in four words, each bit representing a channel. Each channel has an associated Debounce/Select register and Pulse Accumulation Count register.

A Time Tag register is provided and is updated every millisecond. Three registers are provided to support SOE buffer function: the Maximum SOE Count, the SOE Count, and the SOE Index.

When used in conjunction with the Debounce/Select registers, the AC Input register provides debounce with AC input.

### **3.6 BUS INTERRUPTER**

A Bus Interrupter provides access to the VMEbus interrupt structure. An interrupt can be issued on any level (software selectable), and a single byte vector is placed on the bus when acknowledged. Any of the following conditions can initiate the interrupt:

- a. COS on any of the 64 channels
- b. Time Tag rollover
- c. Pulse Accumulation rollover on any of the 64 channels
- d. SOE, End-of-Buffer, First Word Received
- e. SOE buffer count equal to programmable maximum count provided by the user

Each of these interrupt conditions may be enabled or disabled by the host. A global disable occurs if the interrupt level is set to zero (0). There is one ROAK interrupt for the VMIVME-1182 board. Details of the interrupter capabilities are described in Section 4.

### **3.7 WATCHDOG TIMER**

The VMIVME-1182 monitors the health of the DSP and resets it if necessary. The DSP must write to a specified address every millisecond or the watchdog timer will issue a reset to the DSP. A reset to the DSP results in reloading the EPROM data and reinitializing the default conditions. The VMIVME-1182 is off-line at this time. This circuitry also monitors the general integrity of the +5 V on the VMEbus and issues a reset to the DSP if it falls below +4.5 V.

### **3.8 SELF-TEST**

The VMIVME-1182 performs Self-Test functions when one of the following conditions occur:

- a. VMEbus SYSRESET activated
- b. Watchdog timer invokes a reset to the DSP
- c. Test Mode bit in CSR activated

The DSP performs the Self-Test of the VMIVME-1182. Control memory and both SOE memory buffers are tested, and the results stored in the Self-Test Status register located in control memory. The Self-Test mode is an integrity test of the DSP and the memory. The field input connectors to the digital registers are not tested on-board. The VMEbus-to-VMIVME-1182 memory is not tested in Self-Test mode. System test software is responsible for determining these functions and for turning the front panel LED off when the system has determined that the VMIVME-1182 has passed.

### **3.9 POWER REQUIREMENTS**

The VMIVME-1182 specification (Document Number 800-001182-000) defines the power requirements.



## SECTION 4

### PROGRAMMING

#### 4.1 INTRODUCTION

The VMIVME-1182 can be programmed for a variety of features. After initial power up, system reset, or watchdog timer reset, the following conditions are initialized:

- a. Fail LED is ON.
- b. All interrupts are disabled.
- c. All flags are cleared.
- d. Test mode enabled.
- e. IVR register is cleared.
- f. COS registers are cleared.
- g. PAI registers are cleared.
- h. DSR registers are cleared.
- i. PAC registers are cleared.
- j. Time tag clock set to zero (0) and stopped.
- k. SOE maximum count is cleared.
- l. SOE count is cleared.
- m. SOE buffers contain test data, but are cleared when the Test Mode bit is disabled.
- n. Self-Test Complete bit is set in the CSR.

If the initial conditions meet default requirements, then the user writes to the CSR to disable test mode and turn off the Fail LED. The user may then begin reading the input data registers which are updated with field data every millisecond. Table 4.1-1 is the address map for the VMIVME-1182. All addresses shown are relative to the board's base address.

#### NOTE

TO BE CONSISTENT WITH CONVENTIONAL VMEbus DEVELOPMENT SYSTEM NOMENCLATURE, HEXADECIMAL NUMBERS IN THIS DOCUMENT ARE DESIGNATED WITH A "\$" PREFIX UNLESS OTHERWISE INDICATED. DECIMAL NUMBERS ARE PRESENTED WITHOUT A PREFIX.

Table 4.1-1. VMIVME-1182 Memory Map

| Relative Address | Description                              | Desig | Read/Write |
|------------------|------------------------------------------|-------|------------|
| \$000            | Board ID Register                        | BID   | Read       |
| \$002            | Control and Status Register              | CSR   | Read/Write |
| \$004            | Self-Test Results Register               | STR   | Read/Write |
| \$006            | Interrupt Vector Register                | IVR   | Read/Write |
| \$008            | Debounce Input Data for Channels 63-48   | IDR 0 | Read/Write |
| \$00A            | Debounce Input Data for Channels 47-32   | IDR 1 | Read/Write |
| \$00C            | Debounce Input Data for Channels 31-16   | IDR 2 | Read/Write |
| \$00E            | Debounce Input Data for Channels 15-00   | IDR 3 | Read/Write |
| \$010            | Change of State for Channels 63-48       | COS 0 | Read/Write |
| \$012            | Change of State for Channels 47-32       | COS 1 | Read/Write |
| \$014            | Change of State for Channels 31-16       | COS 2 | Read/Write |
| \$016            | Change of State for Channels 15-00       | COS 3 | Read/Write |
| \$018            | Pulse Accumulation Interrupt Chan 63-48  | PAI 0 | Read/Write |
| \$01A            | Pulse Accumulation Interrupt Chan 47-32  | PAI 1 | Read/Write |
| \$01C            | Pulse Accumulation Interrupt Chan 31-16  | PAI 2 | Read/Write |
| \$01E            | Pulse Accumulation Interrupt Chan 15-00  | PAI 3 | Read/Write |
| \$020 - \$09E    | Debounce/Select Register (0-63)          | DSR   | Read/Write |
| \$0A0 - \$11E    | Pulse Accumulation Count Register (0-63) | PAC   | Read/Write |
| \$120            | Time Tag Register                        |       | Read/Write |
| \$122            | Maximum SOE Count Register               |       | Read/Write |
| \$124            | SOE Count Register                       |       | Read/Write |
| \$126            | SOE Index Register                       |       | Read/Write |
| \$128            | Reserved (Note 1)                        |       | Read/Write |
| \$12A            | AC Input Register (default = 5)          |       | Read/Write |
| \$12C            | Reserved (Note 1)                        |       | Read       |
| \$12E            | Revision Level Register                  |       | Read       |
| \$130 - \$7FE    | Reserved (Note 1)                        |       |            |
| \$800            | Force LED Register                       |       | Write      |
| \$802            | SOE Request Register                     |       | Write      |
| \$804 - \$9FE    | Reserved (Note 1)                        |       |            |
| \$1000 - \$3FFE  | Sequence-of-Events Buffer Register       |       | Read/Write |

Note 1: Must remain data = 0

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## 4.2 BOARD ID REGISTER (BID)

The BID register is a 16-bit read-only register. Its data is fixed at \$3800. Table 4.2-1 shows the bit map for this register.

Table 4.2-1. Board ID Register Bit Map

| Relative Address \$00 Board ID (read only) |        |        |        |        |        |        |        |
|--------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                     | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| 0                                          | 0      | 1      | 1      | 1      | 0      | 0      | 0      |
| Bit 07                                     | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| 0                                          | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

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## 4.3 CONTROL AND STATUS REGISTER (CSR)

The CSR is a 16-bit register that is used to control the operating parameters of the VMIVME-1182. Table 4.3-1 shows the bit map for this register.

Table 4.3-1. Control and Status Register Bit Map

| Relative Address \$002 CSR (read/write) |            |           |             |               |                |            |                    |
|-----------------------------------------|------------|-----------|-------------|---------------|----------------|------------|--------------------|
| Bit 15                                  | Bit 14     | Bit 13    | Bit 12      | Bit 11        | Bit 10         | Bit 09     | Bit 08             |
| Fail_LED                                | Test Mode  | COS Reset | COS INT DIS | SOE WD INT EN | SOE CNT INT EN | PAC INT EN | TAG INT EN         |
| Bit 07                                  | Bit 06     | Bit 05    | Bit 04      | Bit 03        | Bit 02         | Bit 01     | Bit 00             |
| SOE WD FL                               | SOE CNT FL | PAC FL    | TAG FL      | BUFF END FL   | Reserved       | Reserved   | Self-Test Complete |

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**Bit 15:** Controls the Fail LED. Writing a zero (0) to this bit turns the Fail LED ON; writing a one (1) turns it OFF. The default condition is zero (0).

**Bit 14:** Controls the Test Mode. Writing a zero (0) to this bit initiates Test Mode. The default condition is zero (0). Test mode is enabled at power up, and the results are stored in the Self-Test Results register. To initiate test mode, the bit must be disabled by writing the bit to one (1) and then enabled by writing the bit to zero (0).

- Bit 13:** Clears the COS registers. Writing a one (1) to this bit clears all bits in the COS registers. After the COS registers are cleared, this bit is set to zero (0) by the microcontroller. After power up or reset, this bit is zero (0).
- Bit 12:** Controls the COS interrupts. Writing a one (1) to this bit disables the COS interrupts but allows COS data to be stored in the SOE buffer. The default condition is zero (0), allowing interrupts for any input meeting the requirements of its DSR.
- Bit 11:** Controls the SOE First Word interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the first COS is received. The default condition is zero (0) which prevents an interrupt on this condition.
- Bit 10:** Controls the SOE Buffer Count interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the SOE count reaches the programmed value in the SOE Maximum Count register or when it reaches the physical end of memory. The default condition is zero (0) which prevents an interrupt on this condition.
- Bit 09:** Controls the Pulse Accumulation Count Interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever any of the 64 PAC registers rolls over from a maximum count to zero (0) and sets the corresponding bit in the PAI registers. The default condition is zero (0) which prevents an interrupt on this condition.
- Bit 08:** Controls the Time Tag Interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the Time Tag Counter rolls over from maximum count to zero (0). The default condition is zero (0) which prohibits an interrupt on this condition.
- Bit 07:** Set to one (1) whenever the first COS has been received and the SOE count equals one (1). The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).
- Bit 06:** Set to one (1) whenever the SOE count has reached the preprogrammed value stored in the Maximum SOE Count register. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).
- Bit 05:** Set to one (1) whenever any of the PAC registers (\$0A0 through \$11E) has rolled over. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The corresponding bit (Channel ID) is set in the PAI register. The default condition is zero (0).

**Bit 04:** Set to one (1) whenever a Time Tag overflow has occurred. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).

**Bit 03:** Set to one (1) whenever the physical end of memory has been reached. The user must clear this bit by setting it to zero (0). The default condition is zero (0).

**Bit 02:** Reserved. The data must remain zero (0).

**Bit 01:** Reserved. The data must remain zero (0).

**Bit 00:** Set to one (1) whenever the self-test is complete. This bit is not cleared (set to zero (0)) when test mode is disabled.

#### 4.4 SELF-TEST RESULTS REGISTER (STR)

The VMIVME-1182 performs Self-Test functions when one of the following conditions occur:

- a. VMEbus SYSRESET activated
- b. Watchdog timer invokes a reset to the DSP
- c. Test Mode bit in CSR activated (The bit must be deactivated before it can be reactivated.)

The Self-Test of the VMIVME-1182 is performed by the DSP. Control memory and both SOE memory buffers are tested and the results stored in the Self-Test Status register located in control memory. The Self-Test mode is an integrity test of the DSP and the memory. The microcontroller sets the complete bit in the CSR but the user is responsible for clearing it and the STR register. Table 4.4-1 shows the bit map for this register.

The STR contains a data pattern of \$0CBA whenever the self-test is completed and passed.

Table 4.4-1. Self-Test Results Bit Map

| Relative Address \$004 STR (read/write) |        |        |        |        |        |        |        |
|-----------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                  | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| STR15                                   | STR14  | STR13  | STR12  | STR11  | STR10  | STR09  | STR08  |
| Bit 07                                  | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| STR07                                   | STR06  | STR05  | STR04  | STR03  | STR02  | STR01  | STR00  |

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**Bits 11 through 08:** Set to \$C whenever the Control Register Test has passed. This test is performed by the microcontroller by writing address equal data to the Control Register RAM. The data is then read and compared for accurate results. The control RAM is cleared after the results are posted.

**Bits 07 through 04:** Set to \$B whenever Buffer B has been tested and passed. This test is performed by the microcontroller by writing an incremental (by 1) pattern from 0 through \$17FF to the SOE buffer B RAM. The data is then read and compared for accurate results.

**Bits 03 through 00:** Set to \$A whenever Buffer A has been tested and passed. This test is performed by the microcontroller by switching the buffer to A and writing a decremental pattern from \$17FF through 0 to the SOE buffer A RAM. The data is then read and compared for accurate results.

#### **NOTE**

**SOE BUFFER A AND SOE BUFFER B TEST PATTERNS ARE NOT CLEARED AT THE TIME THE TEST COMPLETE BIT OF THE CSR IS SET. THE BUFFERS ARE CLEARED WHEN THE TEST MODE BIT IS DISABLED.**

## **4.5 INTERRUPT VECTOR REGISTER (IVR)**

The IVR is a 16-bit register used to enable any interrupts that may be set up in the CSR. Table 4.5-1 shows the bit map of the IVR.

Table 4.5-1. Interrupt Control and Vector Register Bit Map

| Relative Address \$006 IVR (read/write) |               |               |               |               |               |               |               |
|-----------------------------------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| Bit 15                                  | Bit 14        | Bit 13        | Bit 12        | Bit 11        | Bit 10        | Bit 09        | Bit 08        |
| Reserved                                | Reserved      | Reserved      | Reserved      | Reserved      | ILVL 2        | ILVL 1        | ILVL 0        |
| Bit 07                                  | Bit 06        | Bit 05        | Bit 04        | Bit 03        | Bit 02        | Bit 01        | Bit 00        |
| Vector bit 07                           | Vector bit 06 | Vector bit 05 | Vector bit 04 | Vector bit 03 | Vector bit 02 | Vector bit 01 | Vector bit 00 |

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**Bits 15 through 11:** These bits are reserved and must be set to zero (0).

**Bits 10 through 08:** Interrupt level bits. This field is used to select the VMEbus interrupt request level as shown in Table 4.5-2. The default is 000 (disabled).

Table 4.5-2. Interrupt Levels

| VMEbus Interrupt Level  | ILVL 2 | ILVL 1 | ILVL 0 |
|-------------------------|--------|--------|--------|
| Interrupts are disabled | 0      | 0      | 0      |
| IRQ1                    | 0      | 0      | 1      |
| IRQ2                    | 0      | 1      | 0      |
| IRQ3                    | 0      | 1      | 1      |
| IRQ4                    | 1      | 0      | 0      |
| IRQ5                    | 1      | 0      | 1      |
| IRQ6                    | 1      | 1      | 0      |
| IRQ7                    | 1      | 1      | 1      |

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**Bits 07 through 00:** Interrupt vector bits. This field is used to select the VMEbus interrupt vector which is presented during the interrupt acknowledge cycle.

## 4.6 DEBOUNCED INPUT DATA REGISTERS (IDR)

The Debounced Input Data registers are a set of four 16-bit registers which indicate the current state of the board inputs. Table 4.6-1 lists the input channels and their associated register bit locations.

Table 4.6-1. Debounced Input Data Register Bit Map

| Relative Address \$008 Input Data Register 0 (read/write) |        |        |        |        |        |        |        |
|-----------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                                    | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 63                                                     | CH 62  | CH 61  | CH 60  | CH 59  | CH 58  | CH 57  | CH 56  |
| Bit 07                                                    | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 55                                                     | CH 54  | CH 53  | CH 52  | CH 51  | CH 50  | CH 49  | CH 48  |
| Relative Address \$00A Input Data Register 1 (read/write) |        |        |        |        |        |        |        |
| Bit 15                                                    | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 47                                                     | CH 46  | CH 45  | CH 44  | CH 43  | CH 42  | CH 41  | CH 40  |
| Bit 07                                                    | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 39                                                     | CH 38  | CH 37  | CH 36  | CH 35  | CH 34  | CH 33  | CH 32  |
| Relative Address \$00C Input Data Register 2 (read/write) |        |        |        |        |        |        |        |
| Bit 15                                                    | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 31                                                     | CH 30  | CH 29  | CH 28  | CH 27  | CH 26  | CH 25  | CH 24  |
| Bit 07                                                    | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 23                                                     | CH 22  | CH 21  | CH 20  | CH 19  | CH 18  | CH 17  | CH 16  |
| Relative Address \$00E Input Data Register 3 (read/write) |        |        |        |        |        |        |        |
| Bit 15                                                    | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 15                                                     | CH 14  | CH 13  | CH 12  | CH 11  | CH 10  | CH 09  | CH 08  |
| Bit 07                                                    | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 07                                                     | CH 06  | CH 05  | CH 04  | CH 03  | CH 02  | CH 01  | CH 00  |

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## 4.7 CHANGE-OF-STATE REGISTERS (COS)

The Change-of-State registers are a set of four 16-bit registers. These registers are updated upon every change of state (if enabled). If the bit is a one (1), the input has had a change of state. These bits can be cleared by writing zero (0) to the registers or by writing a one (1) to bit 13 of the CSR. Bit 13 of the CSR is cleared when the COS registers are cleared. Table 4.7-1 shows the bit map of the COS registers.

Table 4.7-1. COS Bit Map

| Relative Address \$010 COS Register 0 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 63                                              | CH 62  | CH 61  | CH 60  | CH 59  | CH 58  | CH 57  | CH 56  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 55                                              | CH 54  | CH 53  | CH 52  | CH 51  | CH 50  | CH 49  | CH 48  |

| Relative Address \$012 COS Register 1 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 47                                              | CH 46  | CH 45  | CH 44  | CH 43  | CH 42  | CH 41  | CH 40  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 39                                              | CH 38  | CH 37  | CH 36  | CH 35  | CH 34  | CH 33  | CH 32  |

| Relative Address \$014 COS Register 2 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 31                                              | CH 30  | CH 29  | CH 28  | CH 27  | CH 26  | CH 25  | CH 24  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 23                                              | CH 22  | CH 21  | CH 20  | CH 19  | CH 18  | CH 17  | CH 16  |

| Relative Address \$016 COS Register 3 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 15                                              | CH 14  | CH 13  | CH 12  | CH 11  | CH 10  | CH 09  | CH 08  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 07                                              | CH 06  | CH 05  | CH 04  | CH 03  | CH 02  | CH 01  | CH 00  |

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## 4.8 PULSE ACCUMULATION INTERRUPT REGISTERS (PAI)

The Pulse Accumulation Interrupt registers are a set of four 16-bit registers. These registers indicate that the pulse accumulation count for that channel has rolled over from a maximum count to zero (0). The user may clear these bits at any time. Table 4.8-1 shows the bit map of the PAI registers.

Table 4.8-1. PAI Register Bit Map

| Relative Address \$018 PAI Register 0 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 63                                              | CH 62  | CH 61  | CH 60  | CH 59  | CH 58  | CH 57  | CH 56  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 55                                              | CH 54  | CH 53  | CH 52  | CH 51  | CH 50  | CH 49  | CH 48  |

| Relative Address \$01A PAI Register 1 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 47                                              | CH 46  | CH 45  | CH 44  | CH 43  | CH 42  | CH 41  | CH 40  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 39                                              | CH 38  | CH 37  | CH 36  | CH 35  | CH 34  | CH 33  | CH 32  |

| Relative Address \$01C PAI Register 2 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 31                                              | CH 30  | CH 29  | CH 28  | CH 27  | CH 26  | CH 25  | CH 24  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 23                                              | CH 22  | CH 21  | CH 20  | CH 19  | CH 18  | CH 17  | CH 16  |

| Relative Address \$01E PAI Register 3 (read/write) |        |        |        |        |        |        |        |
|----------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                             | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CH 15                                              | CH 14  | CH 13  | CH 12  | CH 11  | CH 10  | CH 09  | CH 08  |
| Bit 07                                             | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CH 07                                              | CH 06  | CH 05  | CH 04  | CH 03  | CH 02  | CH 01  | CH 00  |

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## 4.9 DEBOUNCE/SELECT REGISTERS (DSR)

The Debounce Select registers are a set of 64, 16-bit registers. These registers control what conditions define a COS for that channel as well as the debounce time for that channel. If a COS is defined for a channel, the SOE Buffer is updated each time a COS is detected. Table 4.9-1 shows the bit map for the Debounce/Select register for channel 0. All DSRs follow the same map.

Table 4.9-1. Debounce/Select Registers

| Relative Address \$020 DSR Register (read/write) |        |        |          |          |          |        |        |
|--------------------------------------------------|--------|--------|----------|----------|----------|--------|--------|
| Bit 15                                           | Bit 14 | Bit 13 | Bit 12   | Bit 11   | Bit 10   | Bit 09 | Bit 08 |
| COS 1                                            | COS 0  | AC EN  | Reserved | Reserved | Reserved | DEB 09 | DEB 08 |
| Bit 07                                           | Bit 06 | Bit 05 | Bit 04   | Bit 03   | Bit 02   | Bit 01 | Bit 00 |
| DEB 07                                           | DEB 06 | DEB 05 | DEB 04   | DEB 03   | DEB 02   | DEB 01 | DEB 00 |

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**Bits 15 and 14:** COS Select bits (see Table 4.9-2).

Table 4.9-2. COS Select Bits

| COS 1 | COS 0 | COS DEFINITION/DETECTION                 |
|-------|-------|------------------------------------------|
| 0     | 0     | COS Definition/Detection Disabled*       |
| 0     | 1     | COS Definition/Detection on falling edge |
| 1     | 0     | COS Definition/Detection on rising edge  |
| 1     | 1     | COS Definition/Detection on both edges*  |

\*Pulse Accumulation function disabled.

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**Bit 13:** Controls COS algorithm. Writing a one (1) to this bit enables COS detection for AC input voltages. The default condition is zero (0). Section 4.16 describes typical debounce select time when using AC Input.

**Bits 12 through 10:** These bits are reserved and must be set to zero (0).

**Bits 09 through 00:** Debounce Timer Select may be set from 1 ms through 1.024 seconds. See Table 4.9-3 for a description of the bit weight.

Table 4.9-3. Debounce Timer Select

| Bits 9<br>through 0 | Debounce<br>Rate |
|---------------------|------------------|
| \$000               | 1 ms             |
| \$001               | 2 ms             |
| \$002               | 3 ms             |
| •                   | •                |
| •                   | •                |
| •                   | •                |
| \$3FD               | 1.022 s          |
| \$3FE               | 1.023 s          |
| \$3FF               | 1.024 s          |

#### 4.10 PULSE ACCUMULATION COUNT REGISTERS (PAC)

The Pulse Accumulation Count registers are a set of 64, 16-bit registers. These registers are incremented each time a COS is detected on the corresponding input. In the event of a rollover, the corresponding bit is set in the PAI registers and a flag is set in the CSR. These registers may be preset to any value. Table 4.10-1 shows the bit map for one of the Pulse Accumulation Count registers. All PAC registers follow the same map. This function is **not** implemented if COS 1 and COS 0 of the DSR are both zero (0) or both one (1).

Table 4.10-1. Pulse Accumulation Count Register Bit Map

| Relative Address \$0A0 PAC Register (read/write) |        |        |        |        |        |        |        |
|--------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                           | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| PAC 15                                           | PAC 14 | PAC 13 | PAC 12 | PAC 11 | PAC 10 | PAC 09 | PAC 08 |
| Bit 07                                           | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| PAC 07                                           | PAC 06 | PAC 05 | PAC 04 | PAC 03 | PAC 02 | PAC 01 | PAC 00 |

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## 4.11 TIME TAG REGISTER

The Time Tag register stores the current value of the 16-bit timer which is used for time tagging the COS data in the SOE buffer. The Time Tag counter is a free-running counter which can be preset during non-test mode. At maximum count, the board sets a flag in the CSR and issues an interrupt to the host if the Time Tag Rollover interrupt is enabled in the CSR. Table 4.11-1 shows the bit map of the Time Tag register. The bit weight is 1 ms.

Table 4.11-1. Time Tag Register Bit Map

| Relative Address \$120 Time Tag Register (read/write) |        |        |        |        |        |        |        |
|-------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                                | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| Time Tag MSB                                          |        |        |        |        |        |        |        |
| Bit 07                                                | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| Time Tag LSB                                          |        |        |        |        |        |        |        |

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## 4.12 MAXIMUM SOE COUNT REGISTER

The Maximum SOE Count register is a 16-bit register. This register enables the user to program the maximum count of events before an SOE buffer count interrupt occurs. If the maximum count is reached, the board sets a flag in the CSR and interrupts the host if the SOE count interrupt is enabled in the CSR. See Table 4.12-1 for bit definitions.

The Maximum SOE Count should be set for \$C00 or less. \$C00 represents the last SOE event that can be stored. Any further events overwrite the beginning of the buffer resulting in a loss of data.

Table 4.12-1. Maximum SOE Count Bit Map

| Relative Address \$122 Maximum SOE Count (read/write) |        |        |        |        |        |        |        |
|-------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                                | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| MAX 15                                                | MAX 14 | MAX 13 | MAX 12 | MAX 11 | MAX 10 | MAX 09 | MAX 08 |
| Bit 07                                                | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| MAX 07                                                | MAX 06 | MAX 05 | MAX 04 | MAX 03 | MAX 02 | MAX 01 | MAX 00 |

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### 4.13 SOE COUNT REGISTER

The SOE Count register is a 16-bit register which indicates the present count of events in the SOE buffer currently being updated by the microcontroller. The register is initialized at system reset. When an SOE Request is received, the count is written to the SOE index register and then reset. Table 4.13-1 shows the SOE Count register bit map.

Table 4.13-1. SOE Count Bit Map

| Relative Address \$124 SOE Count (read/write) |        |        |        |        |        |        |        |
|-----------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                        | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CNT 15                                        | CNT 14 | CNT 13 | CNT 12 | CNT 11 | CNT 10 | CNT 09 | CNT 08 |
|                                               |        |        |        |        |        |        |        |
| Bit 07                                        | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CNT 07                                        | CNT 06 | CNT 05 | CNT 04 | CNT 03 | CNT 02 | CNT 01 | CNT 00 |

M1182/T4.3-1

### 4.14 SOE INDEX REGISTER

The SOE Index represents the SOE count of the buffer available to the VMEbus. Table 4.14-1 shows the bit map of the SOE Index register.

Table 4.14-1. SOE Index Bit Map

| Relative Address \$126 SOE Index (read/write) |        |        |        |        |        |        |        |
|-----------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                        | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| CNT 15                                        | CNT 14 | CNT 13 | CNT 12 | CNT 11 | CNT 10 | CNT 09 | CNT 08 |
|                                               |        |        |        |        |        |        |        |
| Bit 07                                        | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| CNT 07                                        | CNT 06 | CNT 05 | CNT 04 | CNT 03 | CNT 02 | CNT 01 | CNT 00 |

M1182/T4.14-1

### 4.15 AC INPUT REGISTER

To designate a particular channel as an AC input, write the default value \$0005 to the AC Input register and set the AC EN control bit to one (1) in the associated DSR. Adjust the debounce time and change-of-state parameters as described in Section 4.9.

AC inputs are detected as pulse trains with assumed duty cycles of approximately 35 percent. Consequently, the delay time for a LOW-to-HIGH transition is determined by input sensitivity and may vary as much as 50 percent from the selected debounce time. Delay times for HIGH-to-LOW transitions, however, are not affected by input sensitivity and should agree closely with selected debounce times.

Debounce times for AC inputs should be selected to include at least five complete cycles of the AC input waveform. For example, debounce times for 50 Hz inputs (period equals 20 ms) should not be less than 100 ms.

#### 4.16 REVISION LEVEL REGISTER

The value in this register corresponds to the part description in the assembly drawing for the EPROM on the VMIVME-1182.

#### 4.17 FORCE LED REGISTER

The Force LED is a write-only (data = don't care) register which forces the front panel LED on. If Force LED is activated, the CSR bit 15 is ignored, and the LED can only be turned off by a VMEbus system reset. See Table 4.17-1 for the Force LED bit map.

Table 4.17-1. Force LED Bit Map

| Relative Address \$800 Force LED (write) |        |        |        |        |        |        |        |
|------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                   | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| X                                        | X      | X      | X      | X      | X      | X      | X      |

| Bit 07 | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| X      | X      | X      | X      | X      | X      | X      | X      |

X = Don't Care

M1182/T4.17-1

## 4.18 SOE REQUEST REGISTER

The SOE Request is a write-only (data = don't care) register. A write to this register allows the user access to the SOE data, copies the SOE count to the SOE Index register, and resets the SOE count. Table 4.18-1 shows the bit map of the SOE Request register.

Table 4.18-1. SOE Request Bit Map

| Relative Address \$802 Buffer Access (write) |        |        |        |        |        |        |        |
|----------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                       | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| X                                            | X      | X      | X      | X      | X      | X      | X      |
| Bit 07                                       | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| X                                            | X      | X      | X      | X      | X      | X      | X      |

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X = Don't Care

## 4.19 SEQUENCE-OF-EVENTS BUFFER REGISTERS

The Sequence-of-Events Buffer is a set of 6144, 16-bit registers capable of storing 3072 events. If the user issues a SOE Request, the board may continue to store up to 3072 more events while the user is processing the present buffer.

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**THE DSP WILL AUTO WRAP THE BUFFER AND BEGIN WRITING OVER OLD DATA WHENEVER THE BUFFER REACHES THE PHYSICAL END OF THE BUFFER. THE SOE COUNT ROLLS OVER FROM 3072 TO ZERO (0) AND CONTINUES COUNTING. THE HOST MUST PROCESS THE DATA FROM THE PRIMARY BUFFER BEFORE THE DSP REACHES THE PHYSICAL END OF THE DATA BUFFER OR DATA CAN BE LOST. INTERRUPTS ARE PROVIDED (SOE MAXIMUM COUNT) TO ALERT THE HOST THAT DATA NEEDS TO BE PROCESSED.**

The event data stored in the SOE buffer consists of two words. Word 1 is a 16-bit time stamp as read from the Time Tag register when the COS occurred. The Channel ID is located in word 2 in the lower byte (bits 7 through 0). If the state changed from a zero (0) to a one (1), bit 8 of word 2 is set to a one (1). If the state changed from a one (1) to a zero (0), bit 8 of word 2 is set to a zero (0). Table 4.19-1 is a bit map of one SOE buffer. All SOE buffers follow the same map.

Table 4.19-1. Sequence-of-Events Buffers Bit Map

| Relative Address \$1000 SOE Buffer Word 1 (read/write) |        |        |        |        |        |        |        |
|--------------------------------------------------------|--------|--------|--------|--------|--------|--------|--------|
| Bit 15                                                 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| Time Tag MSB                                           |        |        |        |        |        |        |        |
| Bit 07                                                 | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| Time Tag LSB                                           |        |        |        |        |        |        |        |
| Relative Address \$1002 SOE Buffer Word 2 (read/write) |        |        |        |        |        |        |        |
| Bit 15                                                 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 09 | Bit 08 |
| 0                                                      | 0      | 0      | 0      | 0      | 0      | 0      | LVL    |
| Bit 07                                                 | Bit 06 | Bit 05 | Bit 04 | Bit 03 | Bit 02 | Bit 01 | Bit 00 |
| Channel ID                                             |        |        |        |        |        |        |        |

M1182/T4.19-1





## SECTION 5

### CONFIGURATION AND INSTALLATION

#### 5.1 UNPACKING PROCEDURES

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

#### 5.2 PHYSICAL INSTALLATION

\*\*\*\*\*  
\* CAUTION \*  
\*\*\*\*\*

**DO NOT INSTALL OR REMOVE THE BOARDS WHILE POWER IS APPLIED.**

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

### 5.3 OPERATIONAL CONFIGURATION

VMEbus access modes, address modes, and input configurations are controlled by field replaceable jumpers. This section describes the use of these jumpers and their effects on board performance. Locations and functions of all VMIVME-1182 jumpers are shown in Figure 5.3-1 on page 5-3 and Table 5.3.1-1.

#### 5.3.1 Factory-Installed Jumpers

Each VMIVME-1182 is configured at the factory with the specific jumper arrangement shown in Table 5.3.1-1. The factory configuration ensures that all essential jumpers are installed and establishes the following functional baseline for the VMIVME-1182 board:

- Board Identification is located at \$000000 in the Standard I/O Space, with either Supervisory or Nonprivileged access.
- Wetting voltage application at P3 is disabled.
- Reference ground to P3 is disabled.
- Shorting plug of all external wetting voltages is disabled.

Table 5.3.1-1. Programmable Jumper Functions

| Jumper ID | Function (Installed)           | Factory Configuration |
|-----------|--------------------------------|-----------------------|
| E3-1,2    | Standard                       | Installed             |
| E3-3,4    | Supervisory or Nonprivileged   | Installed             |
| E3-5,6    | Nonprivileged                  | Omitted               |
| E3-7,8    | Address Bit A14 = 0            | Installed             |
| E3-9,10   | Address Bit A15 = 0            | Installed             |
| E3-11,12  | Address Bit A16 = 0            | Installed             |
| E3-13,14  | Address Bit A17 = 0            | Installed             |
| E3-15,16  | Address Bit A18 = 0            | Installed             |
| E3-17,18  | Address Bit A19 = 0            | Installed             |
| E3-19,20  | Address Bit A20 = 0            | Installed             |
| E3-21,22  | Address Bit A21 = 0            | Installed             |
| E3-23,24  | Address Bit A22 = 0            | Installed             |
| E3-25,26  | Address Bit A23 = 0            | Installed             |
| E1-1,2    | CH32 Wetting Input at P3       | *                     |
| E2-1,2    | Reference Ground at P3         | Omitted               |
| E4        | Jumper Carrier                 | Installed             |
| E5        | Wetting Voltages tied together | Omitted               |

\* VMIVME-1182 Factory Option AB1      Omitted  
 VMIVME-1182 Factory Option AB0      Installed

M1182/T5.3.1-1

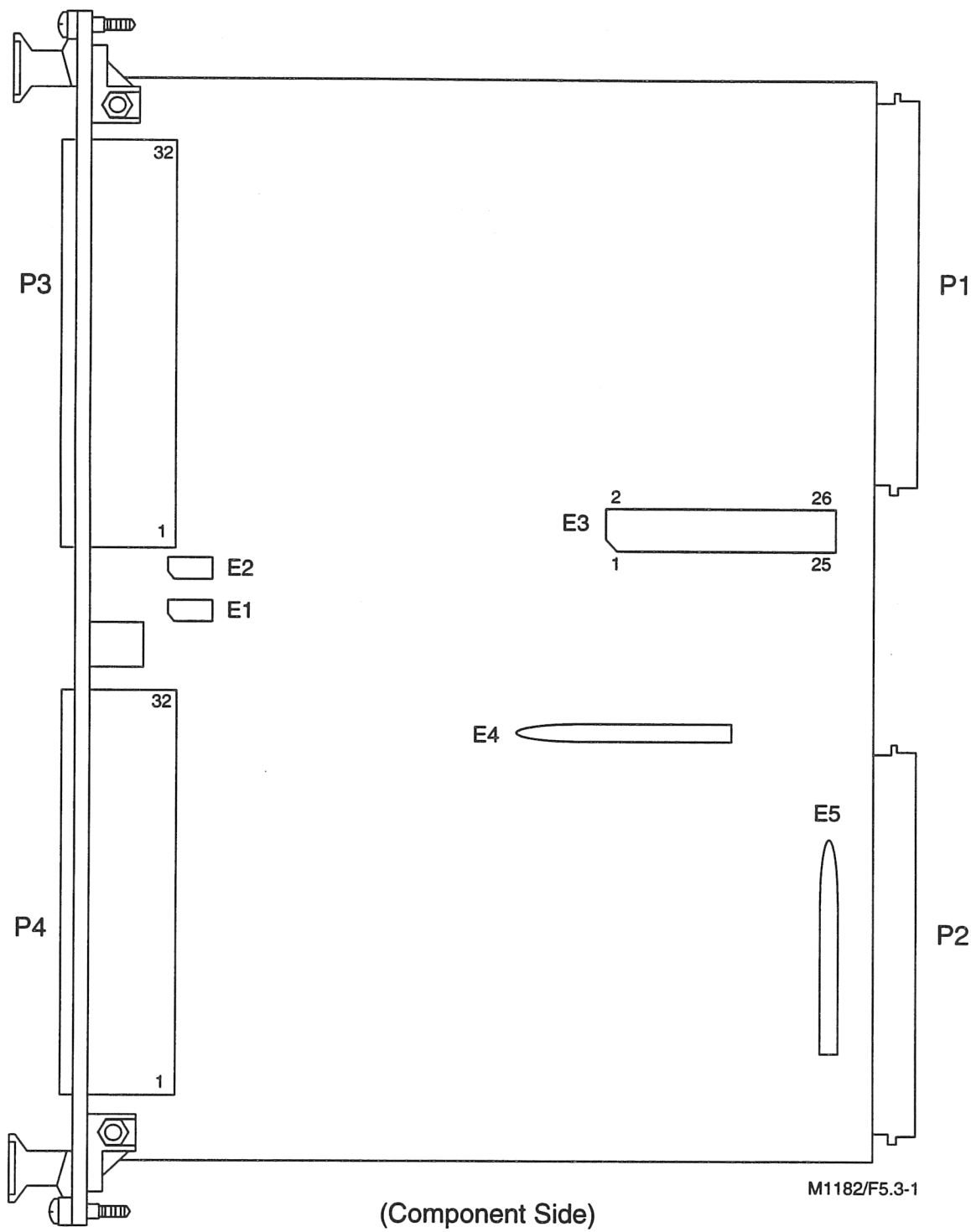


Figure 5.3-1. Configuration Jumpers and System Connectors

### 5.3.2 Access Modes

Supervisory or nonprivileged access is selected by pins 3 through 6 of jumper E3. Figure 5.3.2-1 shows the jumper locations and access modes.

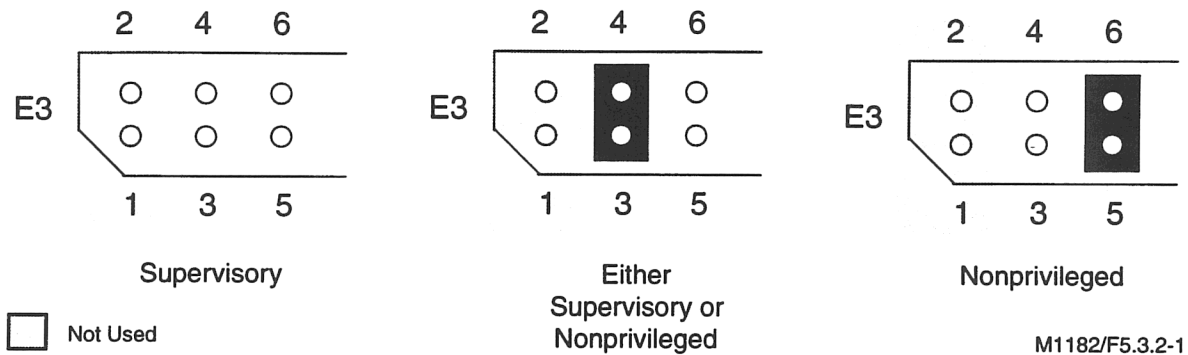


Figure 5.3.2-1. Supervisory and Nonprivileged Access Modes and Jumper Locations

### 5.3.3 Address Modes

Short I/O or Standard Addressing is selected by pins 1 and 2 of jumper E3. Figure 5.3.3-1 shows the jumper locations and address modes.

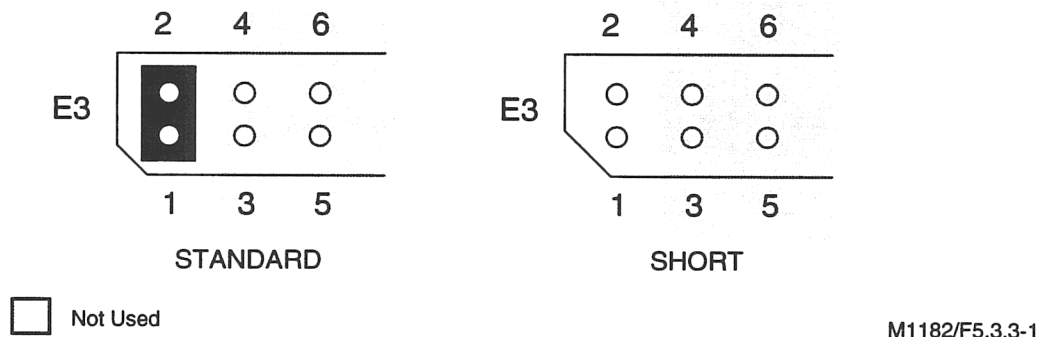
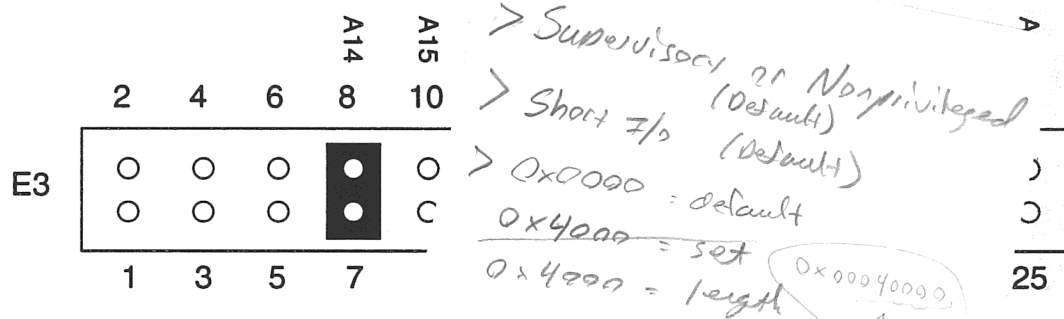
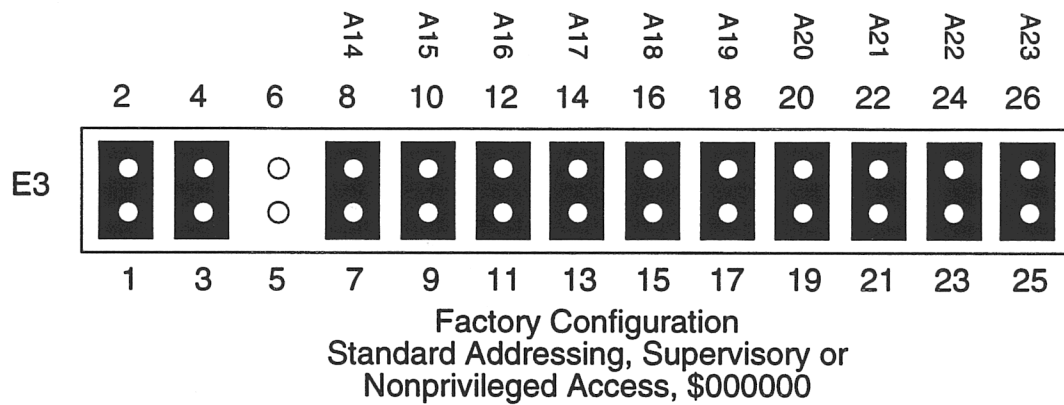


Figure 5.3.3-1. Short I/O and Standard Addressing Modes and Jumper Locations

### 5.3.4 Board Address

The board address is configured by pins 7 through 26 of jumper E3. The board supports A24/A16 addressing. The jumpers corresponding to the address bits are shown in Figure 5.3.4-1 on page 5-5. This figure also shows the factory configuration of E3 and example configurations.

The board address is programmed by installing shorting plugs at all zero (0) or LOW address bit positions in jumper field E3 and by omitting the shorting plugs at the one (1) or HIGH positions (ON = 0; OFF = 1).

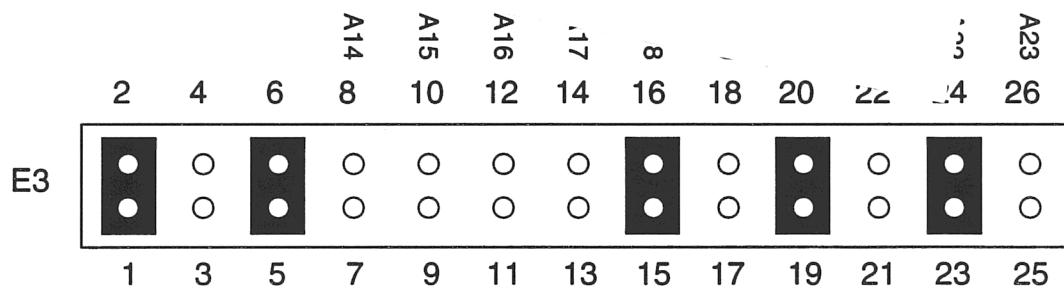


☐ Not Used

Short I/C

> Voltage sensing

5-6 } Removed  
15-16 }



Example Configuration  
Standard Addressing, Nonprivileged Access,  
\$ABC000

M1182/F5.3.4-1

Figure 5.3.4-1. Board Configuration Jumpers

## 5.4 FIELD INPUT CONFIGURATIONS

The VMIVME-1182 provides factory configuration of voltage sensing or contact sensing input configurations. The four, user-defined jumper fields for field inputs are described in the following sections. The connector pinout descriptions are shown in Figures 5.5-2 and 5.5-3.

### 5.4.1 Voltage Sensing

The user input connection circuit for voltage sensing is shown in Figure 5.4.1-1. Jumpers E1 and E4 are installed for this configuration. Jumpers E2 and E5 are omitted (see Table 5.4.1-1). This disables the wetting voltage input at P3 and allows channel 32 to be used as an input channel.

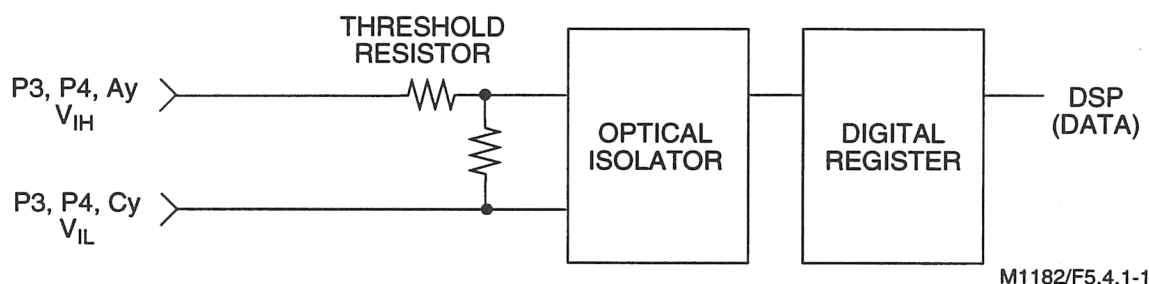


Figure 5.4.1-1. User Input Connection Circuit (Voltage Sensing)

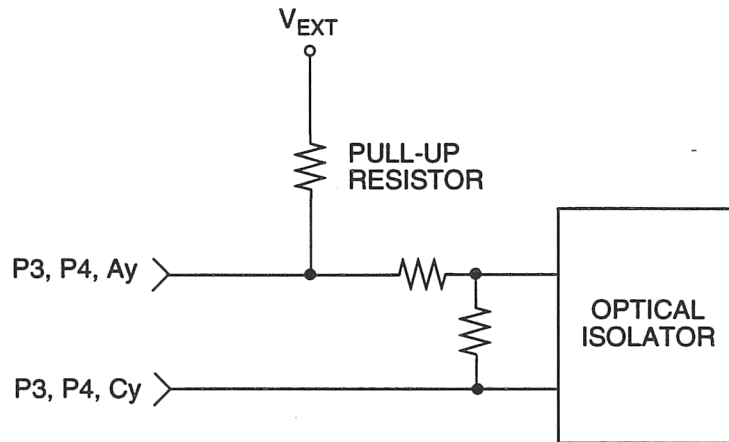
Table 5.4.1-1. VMIVME-1182 AB0 Jumper Placement for Voltage Sensing

| Jumper Field | Function                             | Configuration |
|--------------|--------------------------------------|---------------|
| E1           | Channel 32 enabled                   | Installed     |
| E2           | Reference Ground (Not at P3)         | Omitted       |
| E4           | Carrier (No function)                | Installed     |
| E5           | Wetting Voltages (Not tied together) | Omitted       |

M1182/T5.4.1-1

### 5.4.2 Contact Sensing - Wetting Voltage at P2

The user input connection circuit for contact sensing is shown in Figure 5.4.2-1. The connector pinout description is shown in Figures 5.5-2 and 5.5-3. Jumpers E1 and E4 are installed for this configuration and jumpers E2 and E5 are omitted (see Table 5.4.2-1). This disables the wetting voltage input at P3 and allows channel 32 to be used as an input channel. The wetting voltages can be applied at P2 on byte boundaries. See Table 5.4.2-2 for identification of wetting voltages to channels. When the contact sensing mode is used, the isolation specification is from byte-to-byte **not** channel-to-channel.



M1182/F5.4.2-1

Figure 5.4.2-1. User Input Connection Circuit (Contact Sensing)

Table 5.4.2-1. VMIVME-1182 AB1 and AB0 Wetting Voltage Applied at P2 on Byte Boundaries

| Jumper | Function                             | Configuration |
|--------|--------------------------------------|---------------|
| E1     | Channel 32 enabled                   | Installed     |
| E2     | Reference Ground (Not at P3)         | Omitted       |
| E4     | Carrier (No function)                | Installed     |
| E5     | Wetting Voltages (Not tied together) | Omitted       |

M1182/T5.4.2-1

Table 5.4.2-2. Wetting Voltages to Channels

| External Voltage at P2* | P2 Connection | Channel                     |
|-------------------------|---------------|-----------------------------|
| V <sub>EXT</sub> 32     | C10           | Input Channel 32 through 39 |
| V <sub>EXT</sub> 40     | C13           | Input Channel 40 through 47 |
| V <sub>EXT</sub> 48     | C16           | Input Channel 48 through 55 |
| V <sub>EXT</sub> 56     | C19           | Input Channel 56 through 63 |
| V <sub>EXT</sub> 0      | C22           | Input Channel 00 through 07 |
| V <sub>EXT</sub> 8      | C25           | Input Channel 08 through 15 |
| V <sub>EXT</sub> 16     | C28           | Input Channel 16 through 23 |
| V <sub>EXT</sub> 24     | C31           | Input Channel 24 through 31 |

\*External wetting voltage pin description in Table 5.5-1.

M1182/T5.4.2-2

### 5.4.3 Contact Sensing - Wetting Voltage at P3

The user input connection circuit for wetting voltage at P3 is shown in Figure 5.4.3-1. The wetting voltage may be applied for all channels through P3 instead of P2. Channel 32 cannot be used as a channel input and must be configured (by jumpers) to accept external wetting voltage. See Table 5.4.3-2 for a description. The wetting voltage input of all channels are tied together with the installation of E5. E4 is used as a carrier for the jumper. Reference ground may be output on P3 by installation of E2. The user is required to move the jumpers to the proper location. (See Table 5.4.3-1.)

\*\*\*\*\*  
 \* CAUTION \*  
 \*\*\*\*\*

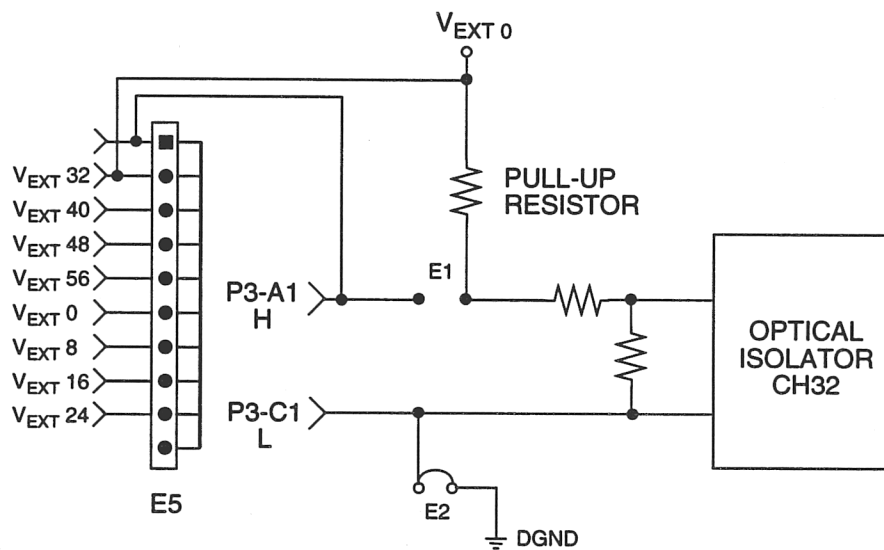
**INSTALLATION OF JUMPER E1 WHILE ALSO USING EXTERNAL VOLTAGES ON THE P2 CONNECTOR MAY RESULT IN PHYSICAL DAMAGE TO THE CIRCUIT BOARD AND OR THE EXTERNAL POWER SUPPLY.**



Table 5.4.3-1. VMIVME-1182 AB1 Wetting Voltage Applied at P3  
Reference Ground at P3

| Jumper | Function                           | Configuration |
|--------|------------------------------------|---------------|
| E1     | Channel 32 disabled                | Omitted       |
| E2     | Reference Ground                   | Installed     |
| E4     | Carrier (No function)              | Omitted       |
| E5     | All wetting voltages tied together | Installed     |

M1182/T5.4.3-1



M1182/F5.4.3-1

Figure 5.4.3-1. P3 Wetting Voltage Input (Contact Sensing)

Table 5.4.3-2. Wetting Voltage

| External Voltage at P3-A1                    | Channels                                                     |
|----------------------------------------------|--------------------------------------------------------------|
| V_EXT 0 through V_EXT 56 tied together by E5 | Input Channels 0 through 31 and Input Channels 33 through 63 |

M1182/T5.4.3-2

## 5.5 SYSTEM CONNECTIONS

Table 5.5-1 lists P2 connector pinout, Table 5.5-2 lists P3 connector pinout, and Table 5.5-3 lists P4 connector pinout. The locations of the system interface connectors are shown in Figure 5.4-1. All inputs are available using two 64-pin front panel connectors.

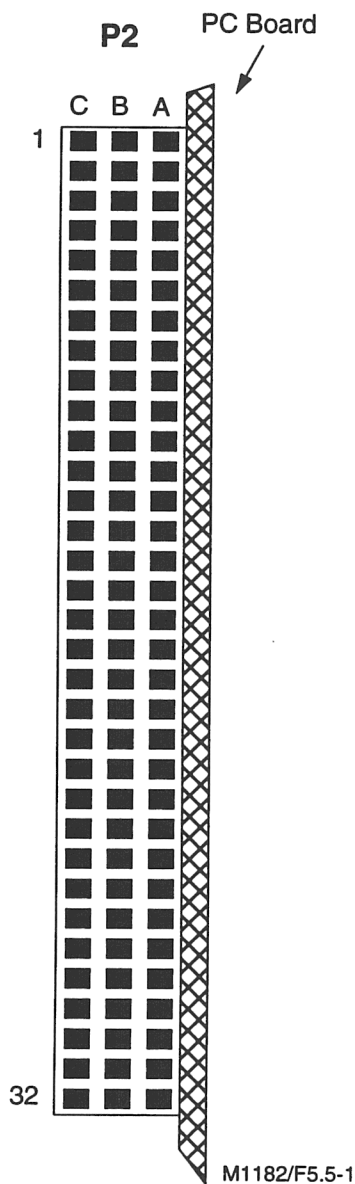


Figure 5.5-1. P2 Connector

Table 5.5-1. P2 Connector Pinout

| Pin | Row C               | Row B | Row A |
|-----|---------------------|-------|-------|
| 01  | B0*                 | +5 V  | DGND  |
| 02  | B1*                 | DGND  | DGND  |
| 03  | B2*                 | N/C   | DGND  |
| 04  | B3*                 | N/C   | DGND  |
| 05  | B4*                 | N/C   | DGND  |
| 06  | B5*                 | N/C   | DGND  |
| 07  | B6*                 | N/C   | DGND  |
| 08  | B7*                 | N/C   | DGND  |
| 09  | N/C                 | N/C   | N/C   |
| 10  | V <sub>EXT</sub> 32 | N/C   | N/C   |
| 11  | DGND                | N/C   | N/C   |
| 12  | DGND                | DGND  | N/C   |
| 13  | V <sub>EXT</sub> 40 | +5 V  | N/C   |
| 14  | DGND                | N/C   | N/C   |
| 15  | DGND                | N/C   | N/C   |
| 16  | V <sub>EXT</sub> 48 | N/C   | N/C   |
| 17  | DGND                | N/C   | N/C   |
| 18  | DGND                | N/C   | N/C   |
| 19  | V <sub>EXT</sub> 56 | N/C   | N/C   |
| 20  | DGND                | N/C   | N/C   |
| 21  | DGND                | N/C   | N/C   |
| 22  | V <sub>EXT</sub> 0  | DGND  | N/C   |
| 23  | DGND                | N/C   | N/C   |
| 24  | N/C                 | N/C   | N/C   |
| 25  | V <sub>EXT</sub> 8  | N/C   | N/C   |
| 26  | DGND                | N/C   | N/C   |
| 27  | DGND                | N/C   | N/C   |
| 28  | V <sub>EXT</sub> 16 | N/C   | DGND  |
| 29  | DGND                | N/C   | N/C   |
| 30  | DGND                | N/C   | N/C   |
| 31  | V <sub>EXT</sub> 24 | DGND  | N/C   |
| 32  | N/C                 | +5 V  | DGND  |

N/C = No Connection

M1182/T5.5-1

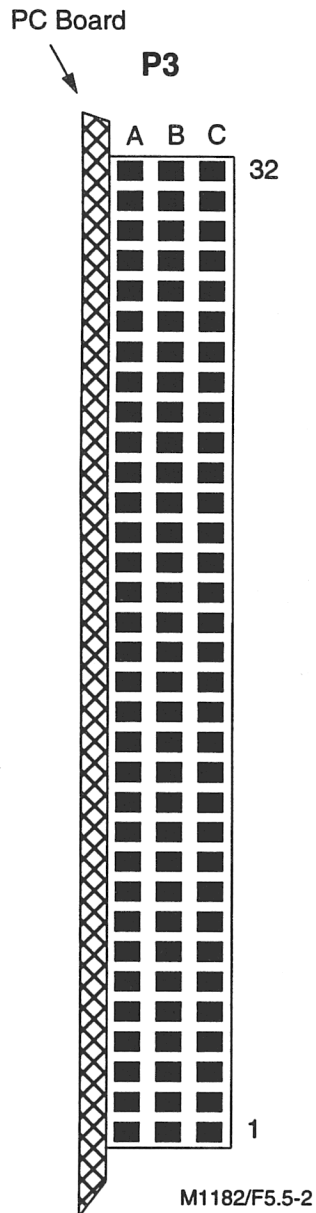


Figure 5.5-2. P3 Connector

Table 5.5-2. P3 Connector Pinout

| Pin | Row A       | Row B | Row C       |
|-----|-------------|-------|-------------|
| 32  | CH 63 HIGH  | N/C   | CH 63 LOW   |
| 31  | CH 62 HIGH  | N/C   | CH 62 LOW   |
| 30  | CH 61 HIGH  | N/C   | CH 61 LOW   |
| 29  | CH 60 HIGH  | N/C   | CH 60 LOW   |
| 28  | CH 59 HIGH  | N/C   | CH 59 LOW   |
| 27  | CH 58 HIGH  | N/C   | CH 58 LOW   |
| 26  | CH 57 HIGH  | N/C   | CH 57 LOW   |
| 25  | CH 56 HIGH  | N/C   | CH 56 LOW   |
| 24  | CH 55 HIGH  | N/C   | CH 55 LOW   |
| 23  | CH 54 HIGH  | N/C   | CH 54 LOW   |
| 22  | CH 53 HIGH  | N/C   | CH 53 LOW   |
| 21  | CH 52 HIGH  | N/C   | CH 52 LOW   |
| 20  | CH 51 HIGH  | N/C   | CH 51 LOW   |
| 19  | CH 50 HIGH  | N/C   | CH 50 LOW   |
| 18  | CH 49 HIGH  | N/C   | CH 49 LOW   |
| 17  | CH 48 HIGH  | N/C   | CH 48 LOW   |
| 16  | CH 47 HIGH  | N/C   | CH 47 LOW   |
| 15  | CH 46 HIGH  | N/C   | CH 46 LOW   |
| 14  | CH 45 HIGH  | N/C   | CH 45 LOW   |
| 13  | CH 44 HIGH  | N/C   | CH 44 LOW   |
| 12  | CH 43 HIGH  | N/C   | CH 43 LOW   |
| 11  | CH 42 HIGH  | N/C   | CH 42 LOW   |
| 10  | CH 41 HIGH  | N/C   | CH 41 LOW   |
| 09  | CH 40 HIGH  | N/C   | CH 40 LOW   |
| 08  | CH 39 HIGH  | N/C   | CH 39 LOW   |
| 07  | CH 38 HIGH  | N/C   | CH 38 LOW   |
| 06  | CH 37 HIGH  | N/C   | CH 37 LOW   |
| 05  | CH 36 HIGH  | N/C   | CH 36 LOW   |
| 04  | CH 35 HIGH  | N/C   | CH 35 LOW   |
| 03  | CH 34 HIGH  | N/C   | CH 34 LOW   |
| 02  | CH 33 HIGH  | N/C   | CH 33 LOW   |
| 01  | CH 32 HIGH* | N/C   | CH 32 LOW** |

\* Channel 32 high can be used as a wetting voltage input by the proper placement of on-board jumpers.

\*\* Channel 32 low can be used to obtain digital ground by the proper placement of on-board jumpers.

N/C = No Connection

M1182/T5.5-2

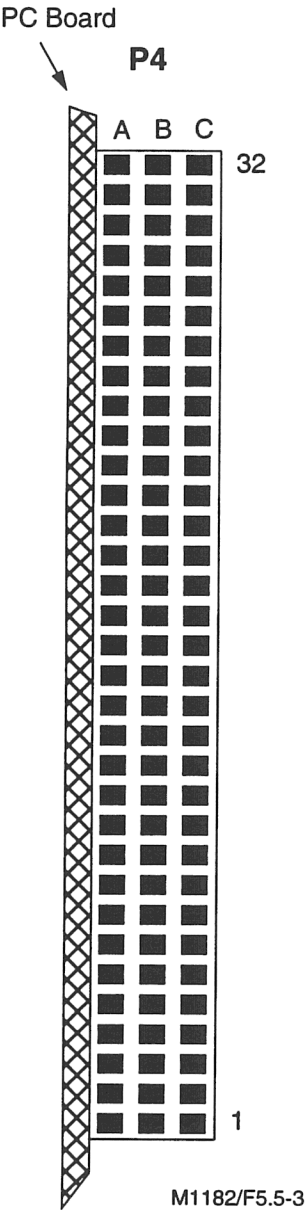


Figure 5.5-3. P4 Connector

Table 5.5-3. P4 Connector Pinout

| Pin | Row A      | Row B | Row C     |
|-----|------------|-------|-----------|
| 32  | CH 31 HIGH | N/C   | CH 31 LOW |
| 31  | CH 30 HIGH | N/C   | CH 30 LOW |
| 30  | CH 29 HIGH | N/C   | CH 29 LOW |
| 29  | CH 28 HIGH | N/C   | CH 28 LOW |
| 28  | CH 27 HIGH | N/C   | CH 27 LOW |
| 27  | CH 26 HIGH | N/C   | CH 26 LOW |
| 26  | CH 25 HIGH | N/C   | CH 25 LOW |
| 25  | CH 24 HIGH | N/C   | CH 24 LOW |
| 24  | CH 23 HIGH | N/C   | CH 23 LOW |
| 23  | CH 22 HIGH | N/C   | CH 22 LOW |
| 22  | CH 21 HIGH | N/C   | CH 21 LOW |
| 21  | CH 20 HIGH | N/C   | CH 20 LOW |
| 20  | CH 19 HIGH | N/C   | CH 19 LOW |
| 19  | CH 18 HIGH | N/C   | CH 18 LOW |
| 18  | CH 17 HIGH | N/C   | CH 17 LOW |
| 17  | CH 16 HIGH | N/C   | CH 16 LOW |
| 16  | CH 15 HIGH | N/C   | CH 15 LOW |
| 15  | CH 14 HIGH | N/C   | CH 14 LOW |
| 14  | CH 13 HIGH | N/C   | CH 13 LOW |
| 13  | CH 12 HIGH | N/C   | CH 12 LOW |
| 12  | CH 11 HIGH | N/C   | CH 11 LOW |
| 11  | CH 10 HIGH | N/C   | CH 10 LOW |
| 10  | CH 09 HIGH | N/C   | CH 09 LOW |
| 09  | CH 08 HIGH | N/C   | CH 08 LOW |
| 08  | CH 07 HIGH | N/C   | CH 07 LOW |
| 07  | CH 06 HIGH | N/C   | CH 06 LOW |
| 06  | CH 05 HIGH | N/C   | CH 05 LOW |
| 05  | CH 04 HIGH | N/C   | CH 04 LOW |
| 04  | CH 03 HIGH | N/C   | CH 03 LOW |
| 03  | CH 02 HIGH | N/C   | CH 02 LOW |
| 02  | CH 01 HIGH | N/C   | CH 01 LOW |
| 01  | CH 00 HIGH | N/C   | CH 00 LOW |

N/C = No Connection

M1182/T5.5-3

## **SECTION 6**

### **MAINTENANCE AND WARRANTY**

#### **6.1 MAINTENANCE**

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

- a. Software
- b. System configuration
- c. Electrical connections
- d. Jumper or configuration options
- e. Boards fully inserted into their proper connector location
- f. Connector pins are clean and free from contamination
- g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
- h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

#### **6.2 MAINTENANCE PRINTS**

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

#### **6.3 WARRANTY**

VMIC's Standard Products are warranted to be free from defects in material and workmanship for a period of two years (24 months) from the date of shipment. In discharge of this warranty, VMIC, at its option, agrees to either repair or replace, at VMIC's facility and at VMIC's discretion, any part, component, subassembly accessory, or any hardware, software, or system product, which under proper and normal use proves defective in material and workmanship.

The customer shall provide notice to VMIC of each such defect within a reasonable time after the customer's discovery of such defect.

In order to return the defective product(s) or part(s), the customer must contact VMIC's Customer Service Department to obtain a Call Ticket Number. The defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

**THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.**

#### **6.4 OUT-OF-WARRANTY REPAIR POLICY**

The following sections describe VMIC's policy on repairs and warranties on repaired products.

#### **6.4.1    Repair Category**

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

- a. Product Exchange
- b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

#### **6.4.2    Repair Pricing**

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

#### **6.4.3    Payment**

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation  
12090 South Memorial Parkway  
Huntsville, Alabama 35803-3308  
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

#### **6.4.4    Shipping Charges**

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

#### **6.4.5    Shipping Instructions**

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

#### **6.4.6    Warranty on Repairs**

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

#### **6.4.7    Exclusions**

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.



## **APPENDIX A**

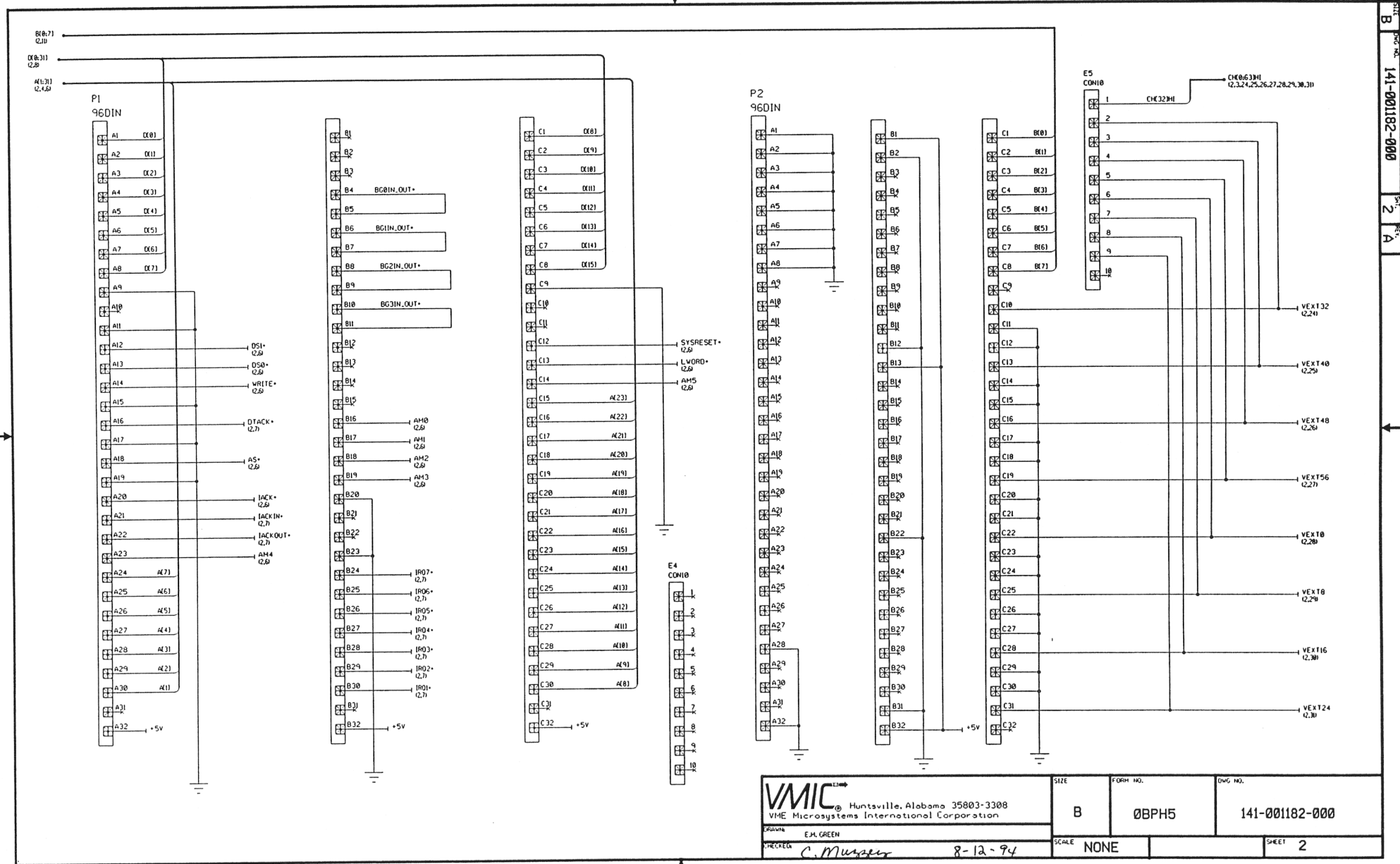
### **ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC**

## NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS.
2. UNLESS OTHERWISE SPECIFIED:
  - A. ALL RESISTORS ARE 1/4 WATT, 5%.
  - B. ALL CAPACITOR VALUES ARE SHOWN IN MICROFARADS

| REVISIONS |                         |         |                    |
|-----------|-------------------------|---------|--------------------|
| REV       | DESCRIPTION             | DATE    | APPROVAL           |
| A         | RELEASE PER ECO 94-0556 | 9-23-94 | <i>[Signature]</i> |
|           |                         |         |                    |

|                                                                                                                                                                                                                                                      |            |                    |          |                                                                                             |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|----------|---------------------------------------------------------------------------------------------|
|                                                                                                                                                                                                                                                      | SIGNATURES |                    | DATE     | <b>VMIC</b><br>Huntsville, Alabama 35893-3308<br>VME Microsystems International Corporation |
|                                                                                                                                                                                                                                                      | DRAWN      | E.H. GREEN         | 9/8/93   |                                                                                             |
|                                                                                                                                                                                                                                                      | PROJ. ENGR | J. CROUCH          | 2/7/94   |                                                                                             |
|                                                                                                                                                                                                                                                      | ENG. MGR   | D. MELROSE         | 2/23/94  |                                                                                             |
|                                                                                                                                                                                                                                                      | PROD. MGR  | <i>[Signature]</i> | 9/26/94  | TITLE<br>VMIVME - 1182 SCHEMATIC                                                            |
|                                                                                                                                                                                                                                                      | LCR        | <i>[Signature]</i> | 9/26/94  |                                                                                             |
| <small>THIS DRAWING AND SPECIFICATION<br/>HEREON ARE THE PROPERTY OF VMIC<br/>AND SHALL NOT BE REPRODUCED OR<br/>COPIED OR USED IN WHOLE OR IN<br/>PART AS A BASIS FOR THE REPRODUCTION<br/>OR SALE OF ITEMS WITHOUT<br/>WRITTEN PERMISSION.</small> | SIZE       |                    | FORM NO. | DWG NO.                                                                                     |
|                                                                                                                                                                                                                                                      | B          |                    | 08PH5    | 141-001182-000                                                                              |
|                                                                                                                                                                                                                                                      | SCALE      |                    | NONE     | SHEET 1                                                                                     |



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| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE<br><b>B</b>       | FORM NO.<br><b>08PH5</b> | DWG. NO.<br><b>141-001182-000</b> |
| DESIGNED<br>E.H. GREEN                                                                      |  | SCALE<br><b>NONE</b>   |                          | SHEET<br><b>2</b>                 |
| CHECKED<br><i>C. Munster</i>                                                                |  | DATE<br><b>8-12-94</b> |                          |                                   |

CH0633.0  
0.24,25,26,27,28,29,30,31

CH0633H  
0.2,3,24,25,26,27,28,29,30,31

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96DIN

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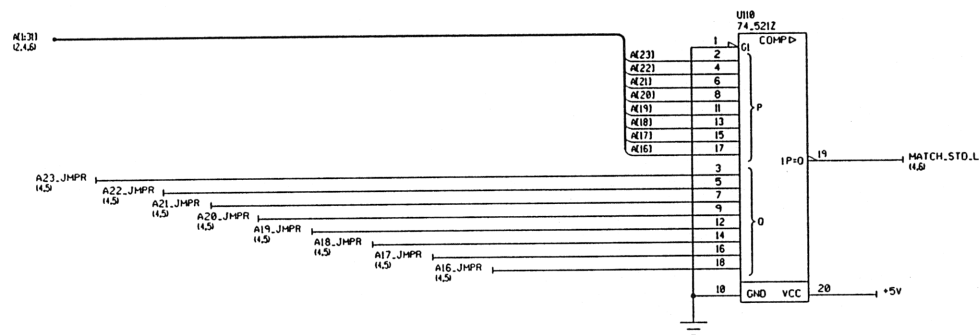
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P4  
96DIN

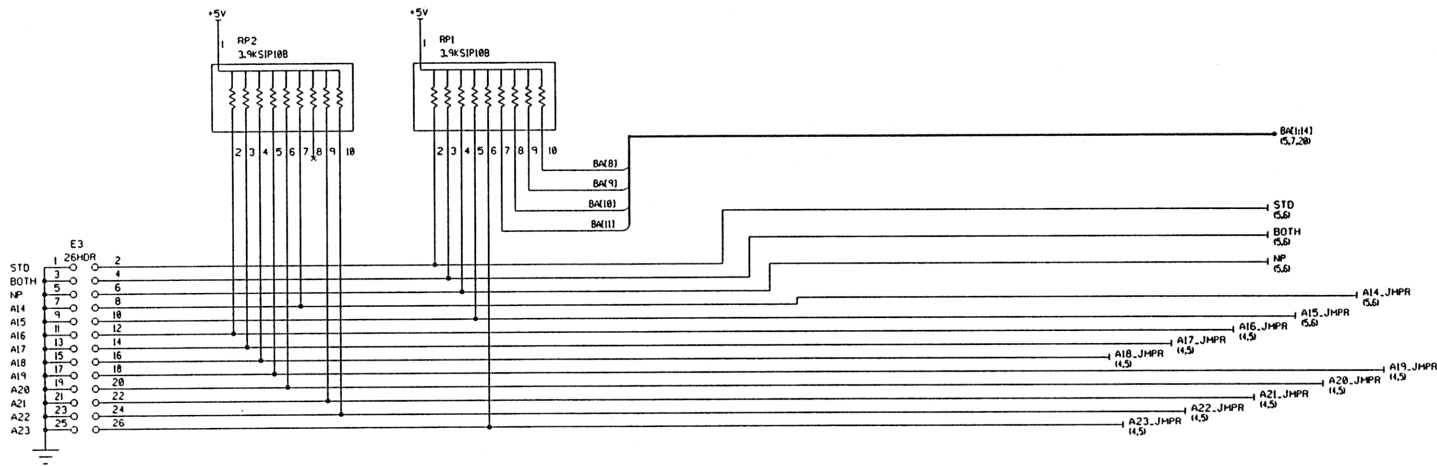
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| C7  | CH063.0 |
| C8  | CH073.0 |
| C9  | CH083.0 |
| C10 | CH093.0 |
| C11 | CH103.0 |
| C12 | CH113.0 |
| C13 | CH123.0 |
| C14 | CH133.0 |
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| C32 | CH313.0 |

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|---------------------------------------------------------------------------------------------|---------------------|---------------|--------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                     | SIZE<br>B     | FORM NO.<br>08BPH5 | DWG NO.<br>141-001182-000 |
| DRAWN<br>E.M. GREEN                                                                         | CHECKED<br>C. M. M. | SCALE<br>NONE | SHEET<br>3         |                           |



VMEbus ADDRESS COMPARE

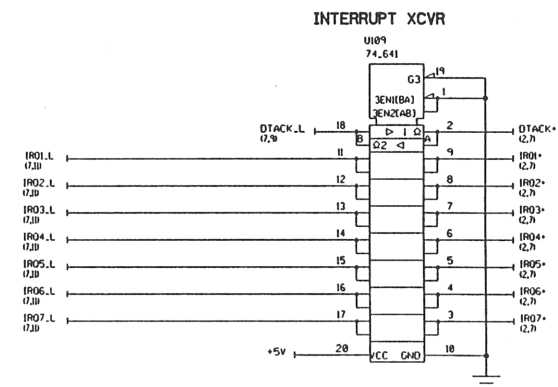
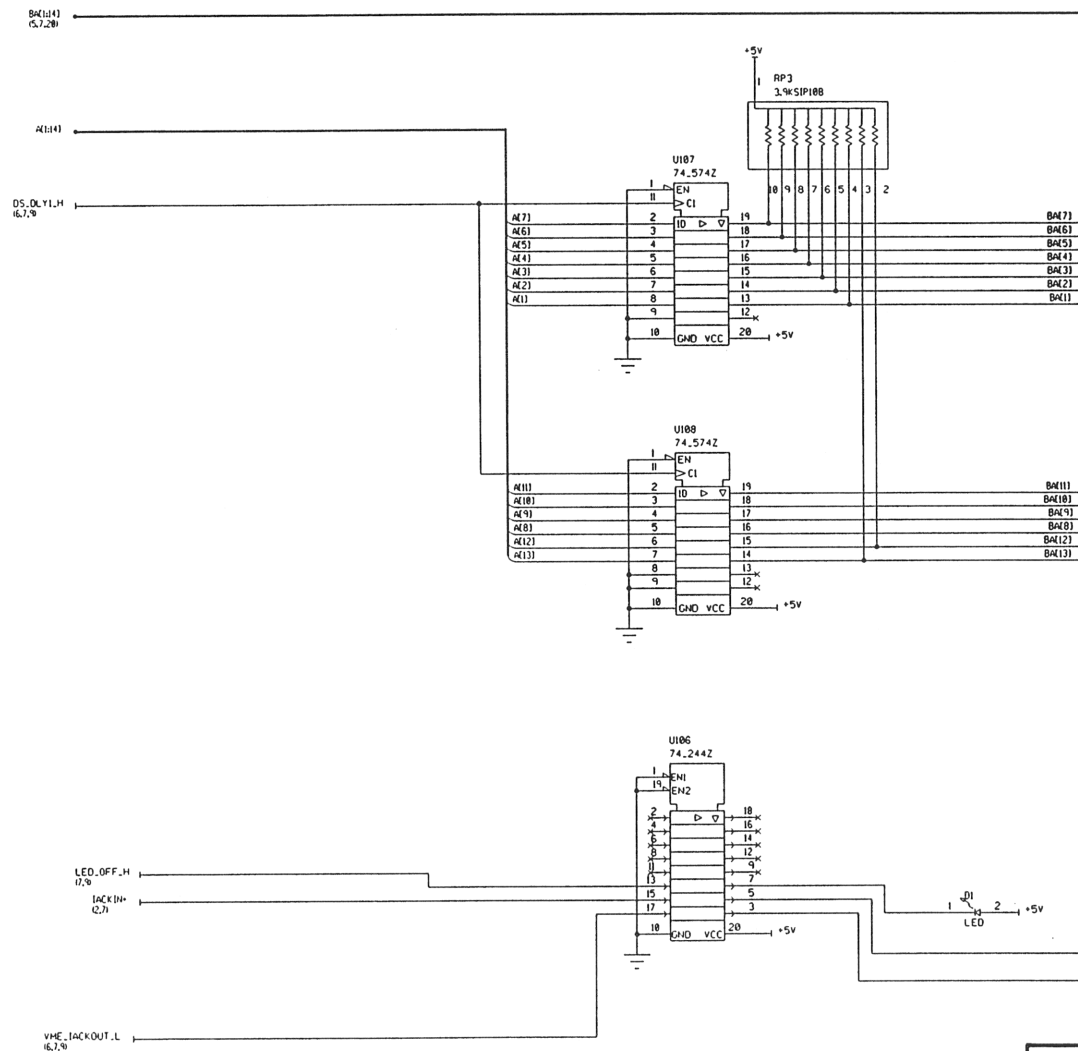
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| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br>C. M. <i>Murray</i> | SCALE<br>NONE | SHEET<br>4        | DATE<br>8-12-94           |



ADDRESS AND ACCESS MODE CONFIGURATION

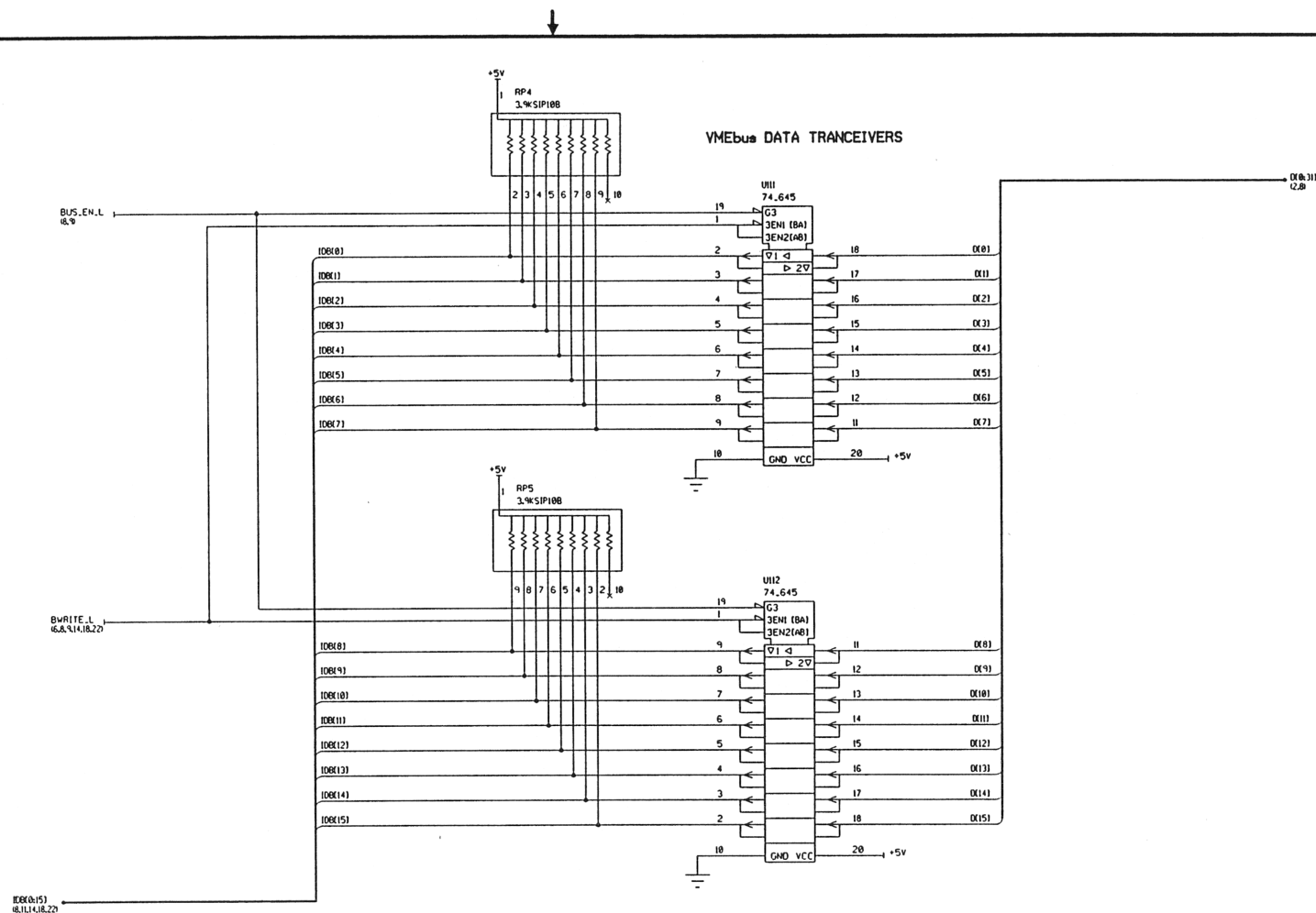
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| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br><i>C. Muxer</i> | DATE<br><b>8-12-94</b> | SCALE<br><b>NONE</b>     | SHEET<br><b>5</b>                |





|                                                                                                                                                                    |  |               |                   |                           |
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|  Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE<br>B     | FORM NO.<br>00PH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.M. GREEN                                                                                                                                             |  | SCALE<br>NONE | SHEET<br>7        |                           |
| CHECKED<br>C.M. <i>Waller</i> 8-12-94                                                                                                                              |  |               |                   |                           |



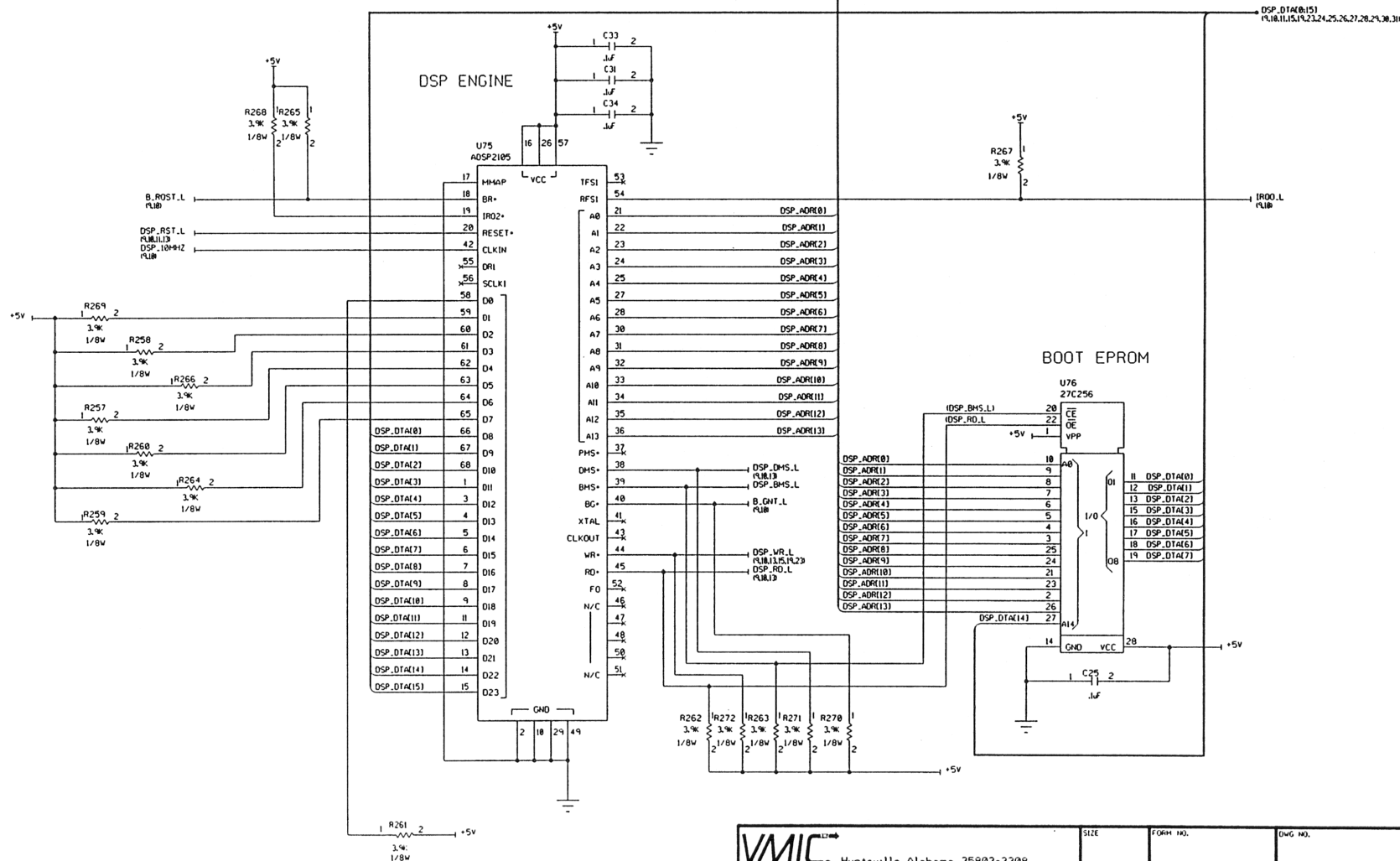


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| <b>VMIC</b> Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                       | SIZE<br>B       | FORM NO.<br>08BPH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.H. GREEN                                                                   | CHECKED<br>C.M. WATTS | DATE<br>8-12-94 | SCALE<br>NONE      | SHEET<br>8                |

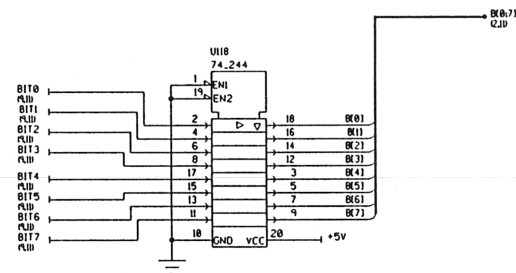


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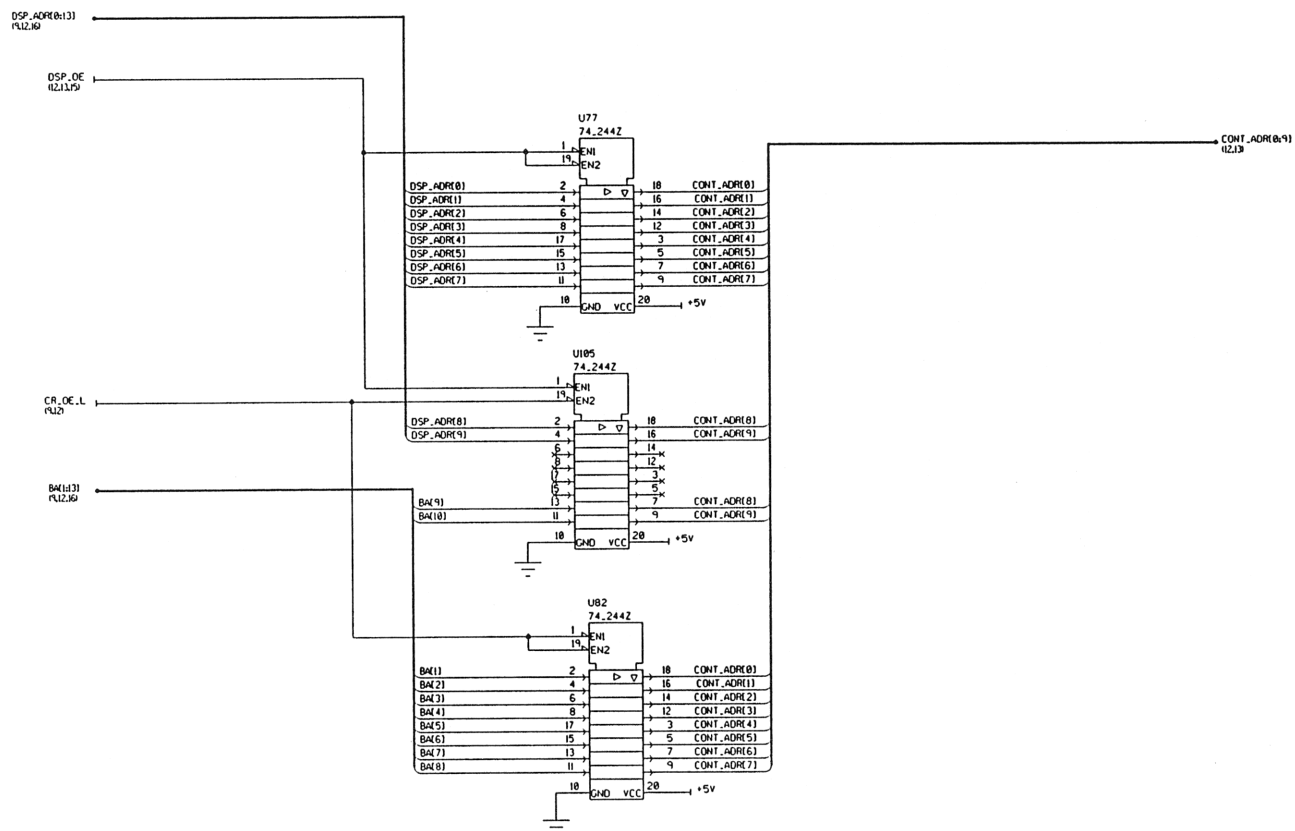
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|                                                                                                                   |  |               |                    |                           |
|-------------------------------------------------------------------------------------------------------------------|--|---------------|--------------------|---------------------------|
| <b>VMI</b> Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation<br>E.H. GREEN<br>C. Muggs |  | SIZE<br>B     | FORM NO.<br>08BPH5 | DWG NO.<br>141-001182-000 |
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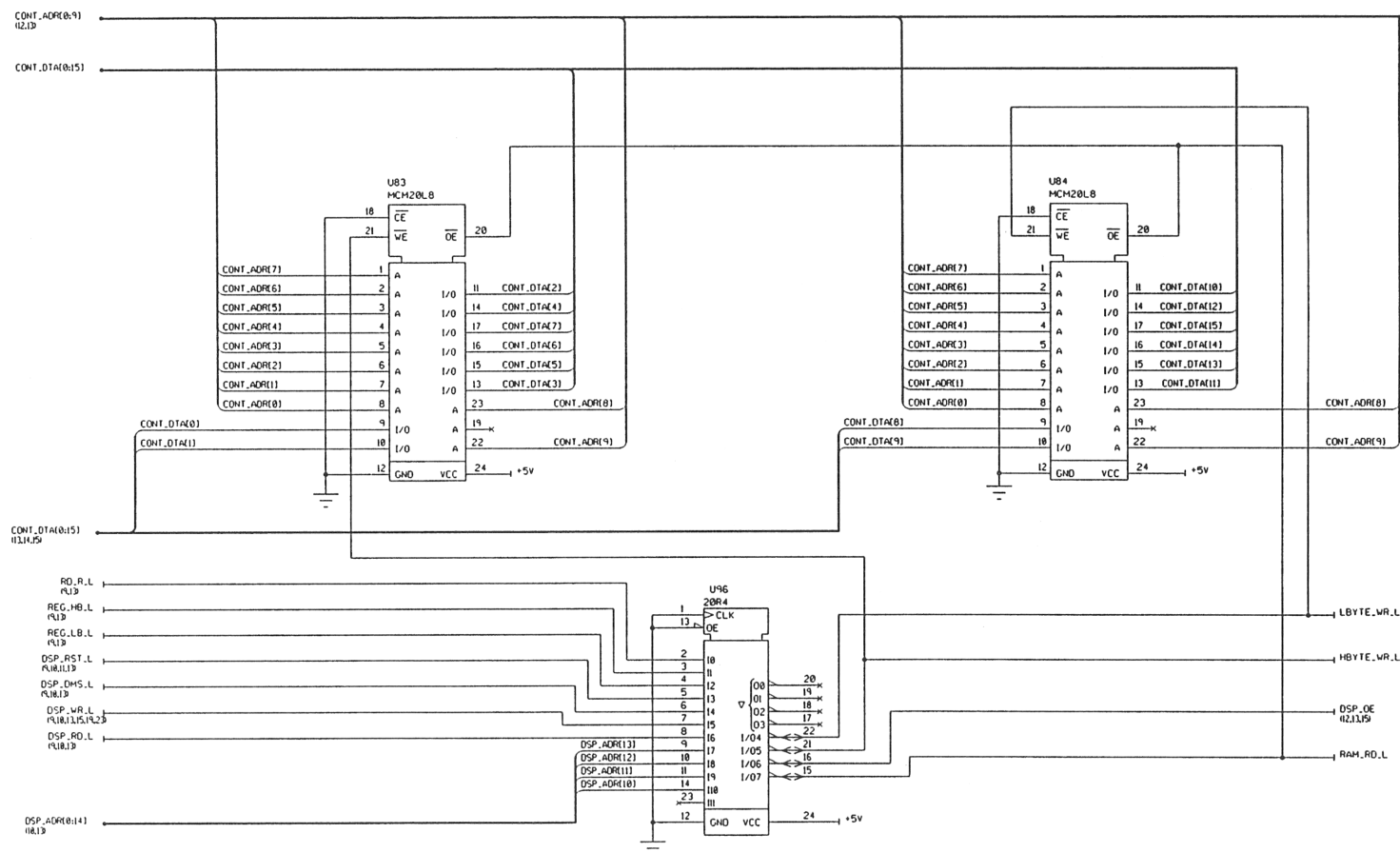


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|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|--------------------------|------------------------------|--------------------------------------|
|  <b>VMIC</b> ® Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                                         | SIZE<br><br><b>B</b>     | FORM NO.<br><br><b>08PH5</b> | DWG NO.<br><br><b>141-001182-000</b> |
| DESIGNED<br><br>E.M. GREEN                                                                                                                                                       | CHECKED<br><br><i>C. M. [signature]</i> | SCALE<br><br><b>NONE</b> |                              | SHEET<br><br><b>11</b>               |
| DATE<br><br><b>8-12-84</b>                                                                                                                                                       |                                         |                          |                              |                                      |

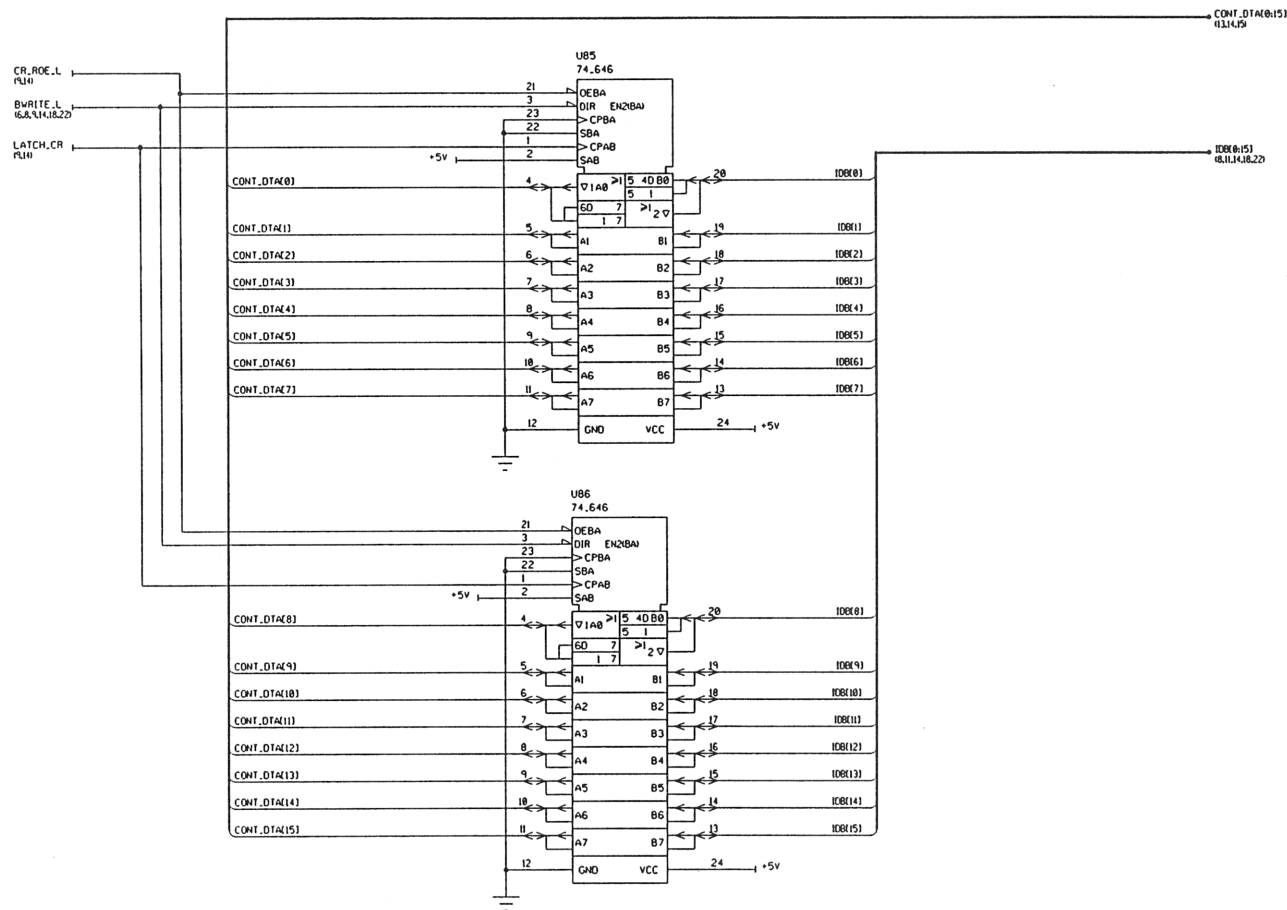


CONTROL ADDRESS BUFFERS

|                                                                                             |                      |               |                   |                           |
|---------------------------------------------------------------------------------------------|----------------------|---------------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B     | FORM NO.<br>08PH5 | Dwg No.<br>141-001182-000 |
| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br>C. Murphy | SCALE<br>NONE | SHEET<br>12       |                           |
| DATE<br>8-12-94                                                                             |                      |               |                   |                           |

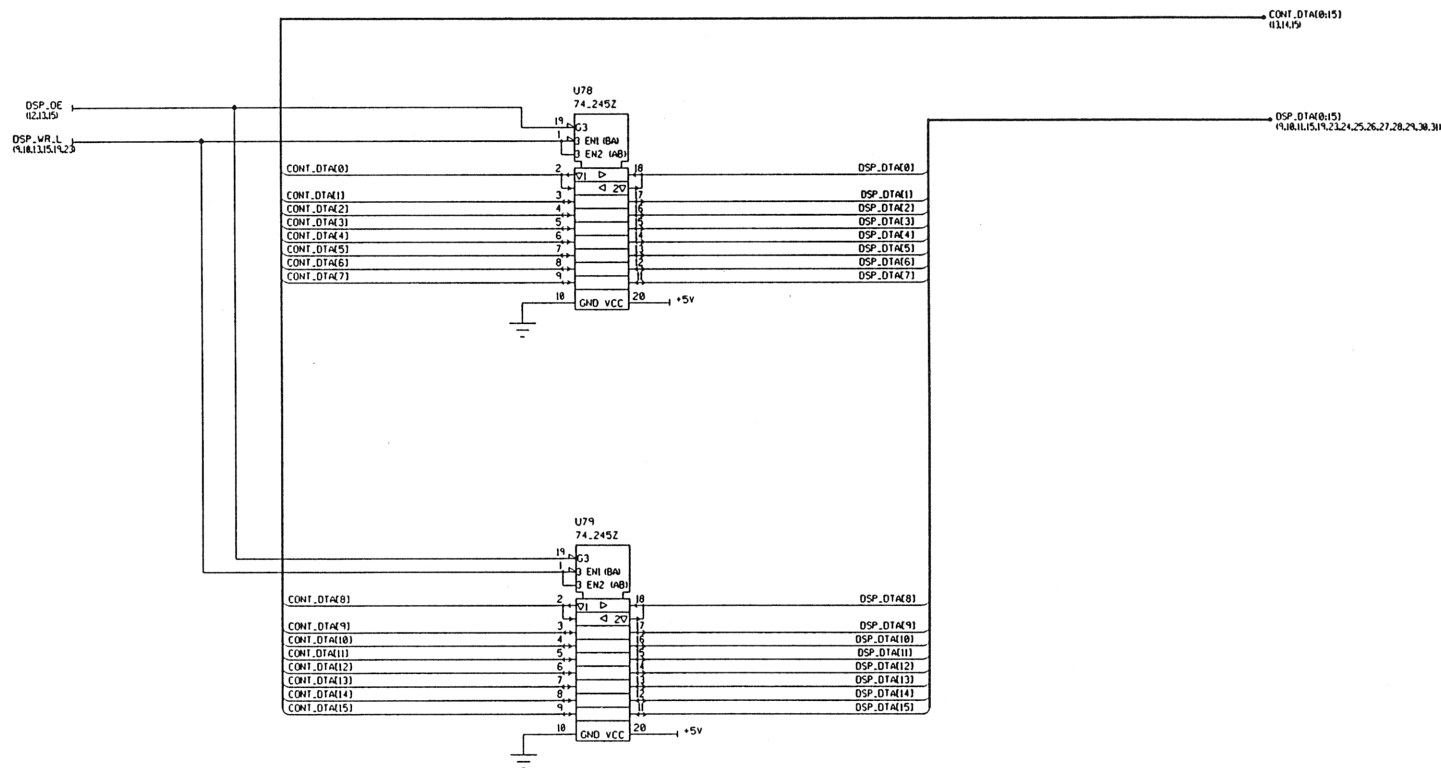


|                                                                                             |  |                 |                   |                            |
|---------------------------------------------------------------------------------------------|--|-----------------|-------------------|----------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE<br>B       | FORM NO.<br>08PH5 | Dwg. NO.<br>141-001182-000 |
| DESIGNED<br>E.M. GREEN                                                                      |  | SCALE<br>NONE   |                   | SHEET<br>13                |
| CHECKED<br>C. M. Muffey                                                                     |  | DATE<br>8-12-94 |                   | CONTROL RAM                |



# VME/CONTROL DATA BUFFERS

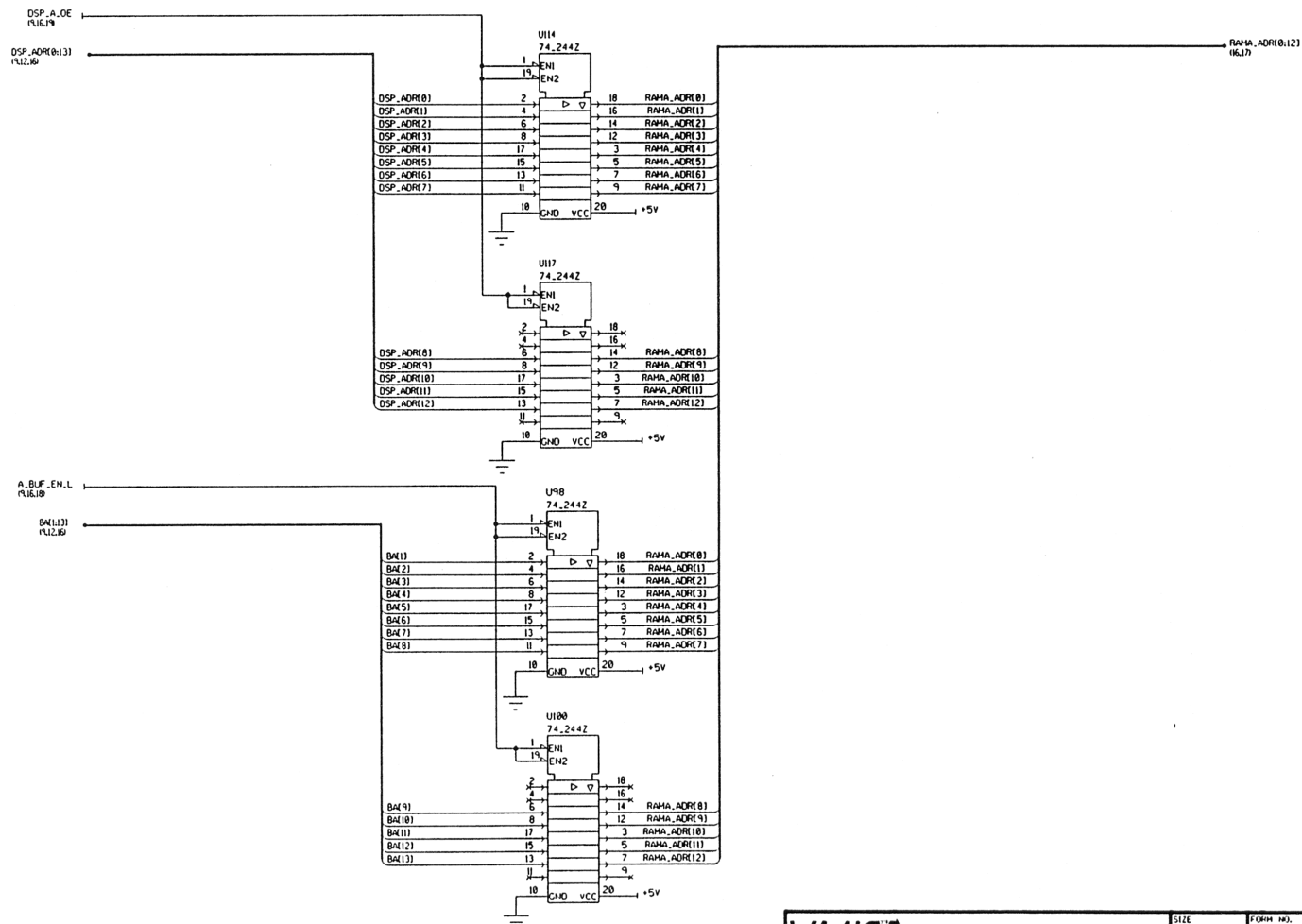
|                                                                                             |                       |               |                   |                           |
|---------------------------------------------------------------------------------------------|-----------------------|---------------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                       | SIZE<br>B     | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DRAWN<br>E.M. GREEN                                                                         | CHECKED<br>C. M. M... | SCALE<br>NONE | SHEET<br>14       |                           |
| DATE<br>8-12-94                                                                             |                       |               |                   |                           |



DSP/CONTROL DATA BUFFERS

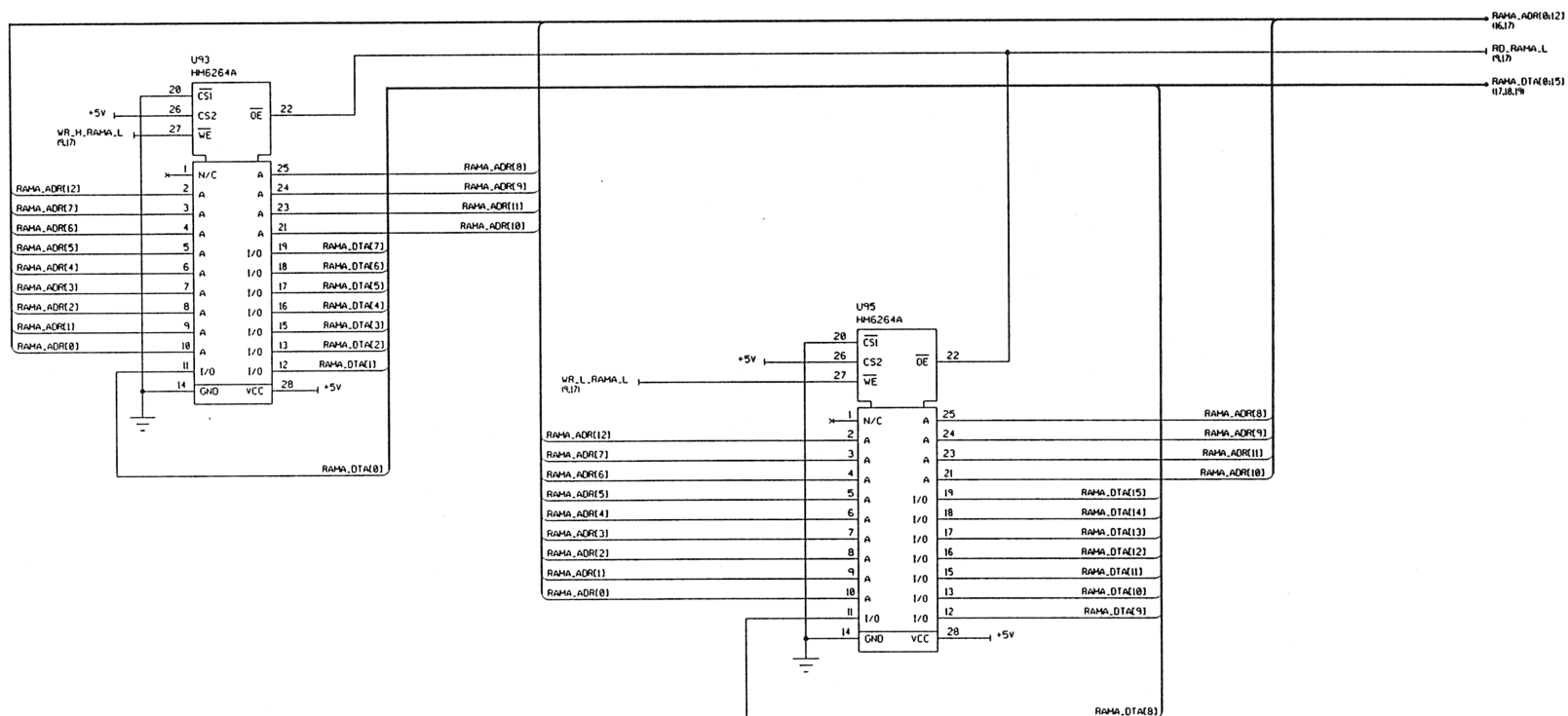
|                                                                                             |                      |                 |                   |                            |
|---------------------------------------------------------------------------------------------|----------------------|-----------------|-------------------|----------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B       | FORM NO.<br>08PH5 | DWG. NO.<br>141-001182-000 |
| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br>C. Muzzey | DATE<br>8-12-94 | SCALE<br>NONE     | SHEET<br>15                |





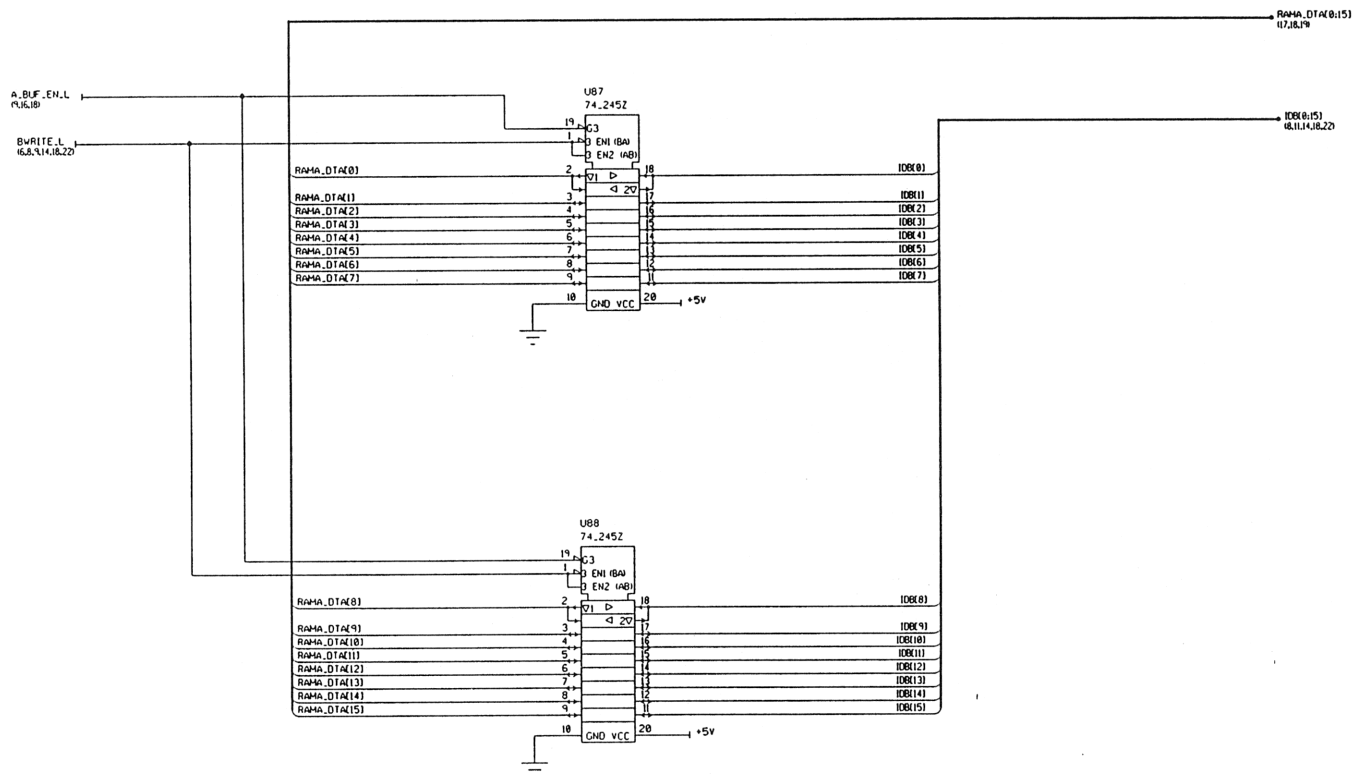
# SOE A ADDRESS BUFFERS

|                                                                                             |                     |                  |                          |                                   |
|---------------------------------------------------------------------------------------------|---------------------|------------------|--------------------------|-----------------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                     | SIZE<br><b>B</b> | FORM NO.<br><b>08PH5</b> | DWG. NO.<br><b>141-001182-000</b> |
| DESIGNED<br>E.M. GREEN                                                                      | CHECKED<br>C. Muzer | DATE<br>8-12-94  | SCALE<br>NONE            | SHEET<br>16                       |



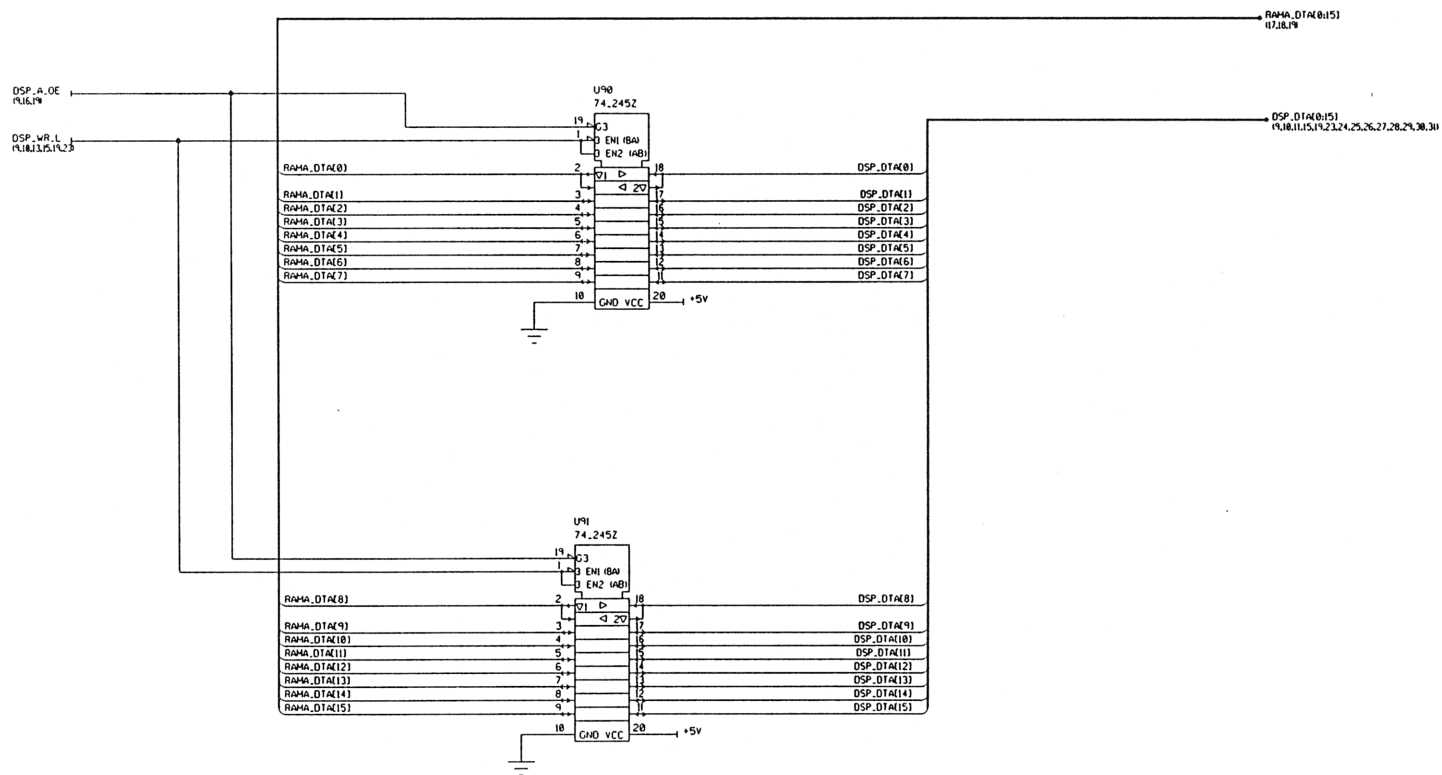
SOE BUFFER A

|                                                                                             |                         |               |                    |                           |
|---------------------------------------------------------------------------------------------|-------------------------|---------------|--------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                         | SIZE<br>B     | FORM NO.<br>08BPH5 | DWG NO.<br>141-001182-000 |
| DRAWN<br>E.H. GREEN                                                                         | CHECKED<br>C. M. MURPHY | SCALE<br>NONE | SHEET<br>17        | DATE<br>8-12-94           |



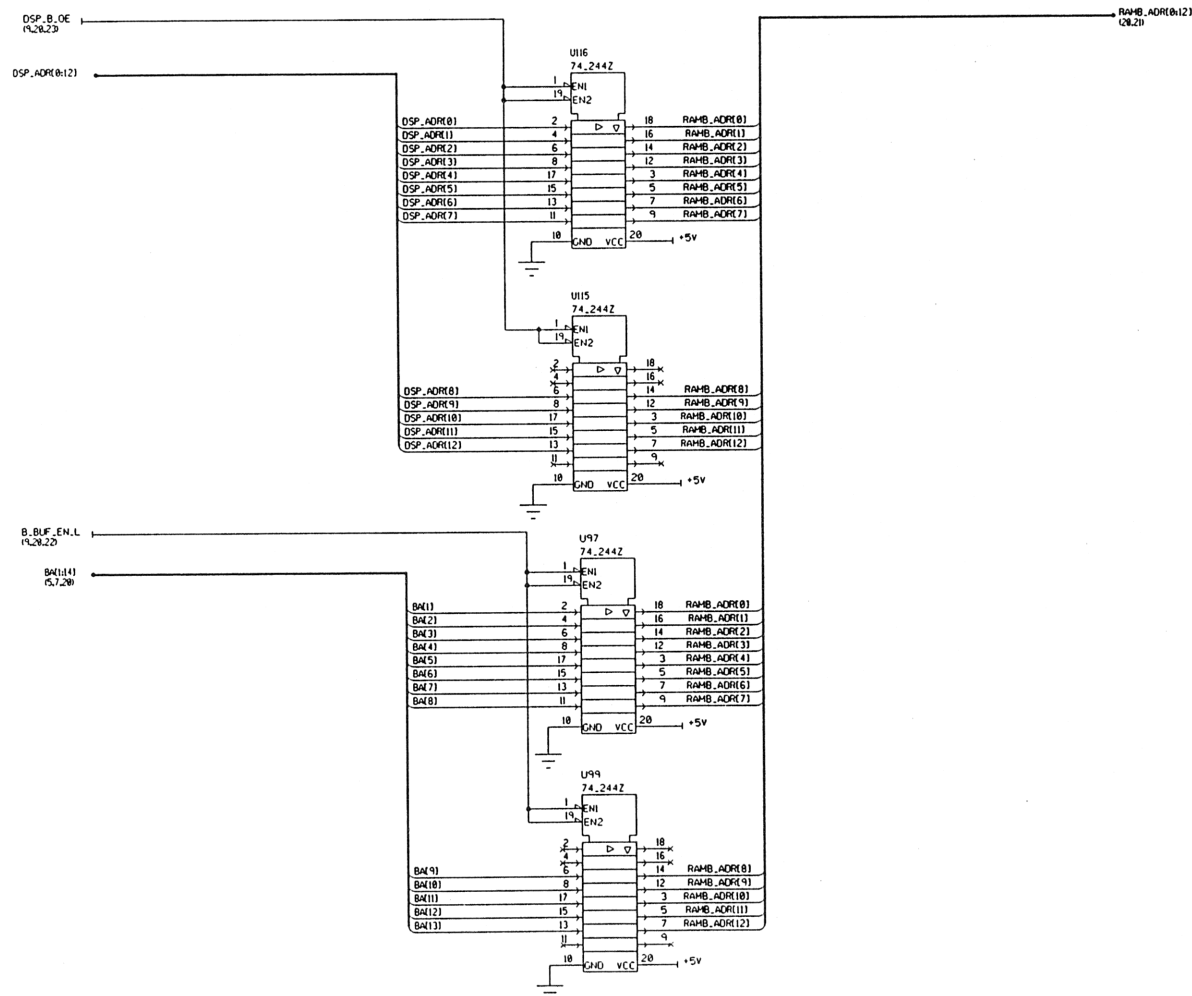
BUFFER A/VME DATA BUFFERS

|                                                                                             |                         |                 |                   |                            |
|---------------------------------------------------------------------------------------------|-------------------------|-----------------|-------------------|----------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                         | SIZE<br>B       | FORM NO.<br>08PH5 | DWG. NO.<br>141-001182-000 |
| DESIGNED BY<br>E.M. GREEN                                                                   | CHECKED BY<br>C. Muffey | DATE<br>8-12-94 | SCALE<br>NONE     | SHEET<br>18                |



DSP/BUFFER A DATA BUFFERS

|                                                                                             |                            |                      |                          |                                  |
|---------------------------------------------------------------------------------------------|----------------------------|----------------------|--------------------------|----------------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35893-3308<br>VME Microsystems International Corporation |                            | SIZE<br><b>B</b>     | FORM NO.<br><b>08PH5</b> | DWG NO.<br><b>141-001182-000</b> |
| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br><i>C. Muzey</i> | SCALE<br><b>NONE</b> | SHEET<br><b>19</b>       |                                  |

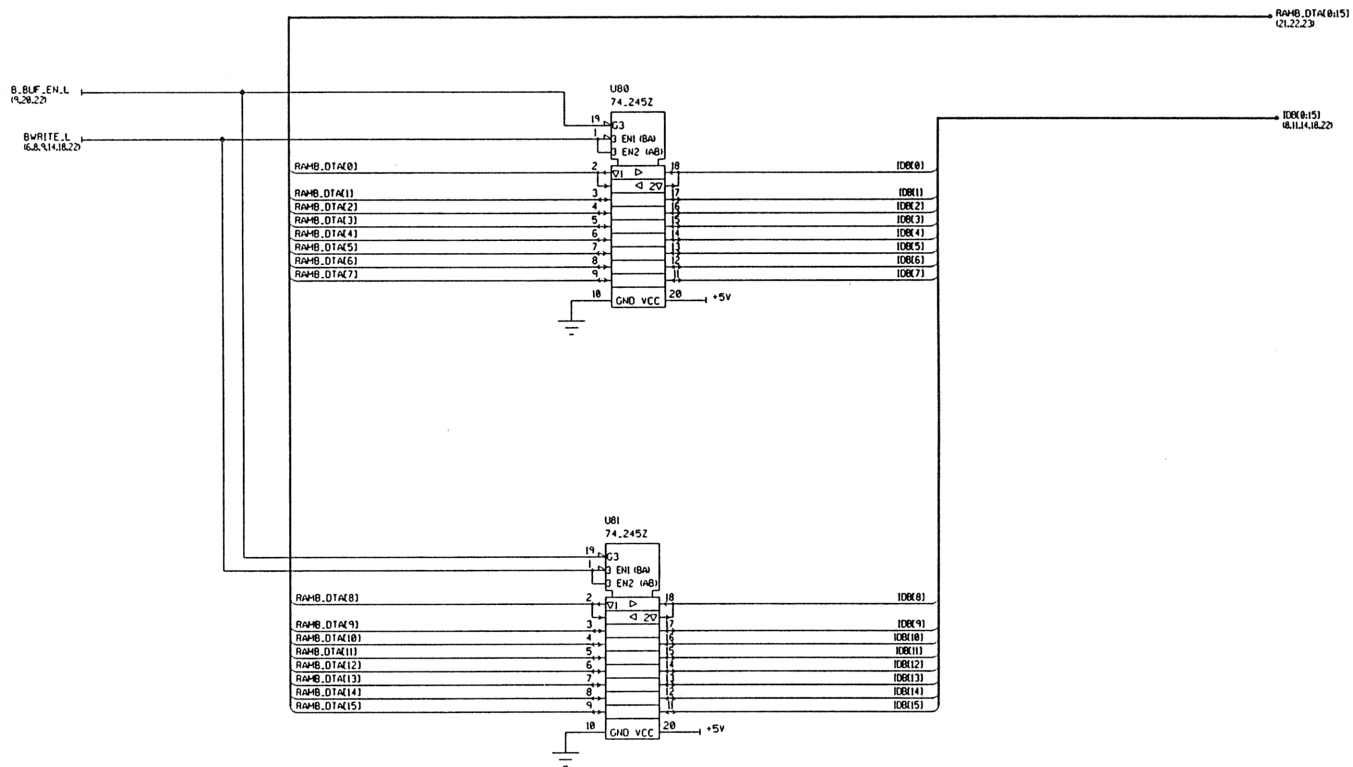


SOE B ADDRESS BUFFERS

|                                                                                            |  |                 |                   |                            |
|--------------------------------------------------------------------------------------------|--|-----------------|-------------------|----------------------------|
| <b>VMIC</b> ® Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE<br>B       | FORM NO.<br>08PH5 | DWG. NO.<br>141-001182-000 |
| DRAWN<br>E.M. GREEN                                                                        |  | SCALE<br>NONE   |                   | SHEET<br>20                |
| CHECKED<br>C. M. MURPHY                                                                    |  | DATE<br>8-12-94 |                   |                            |

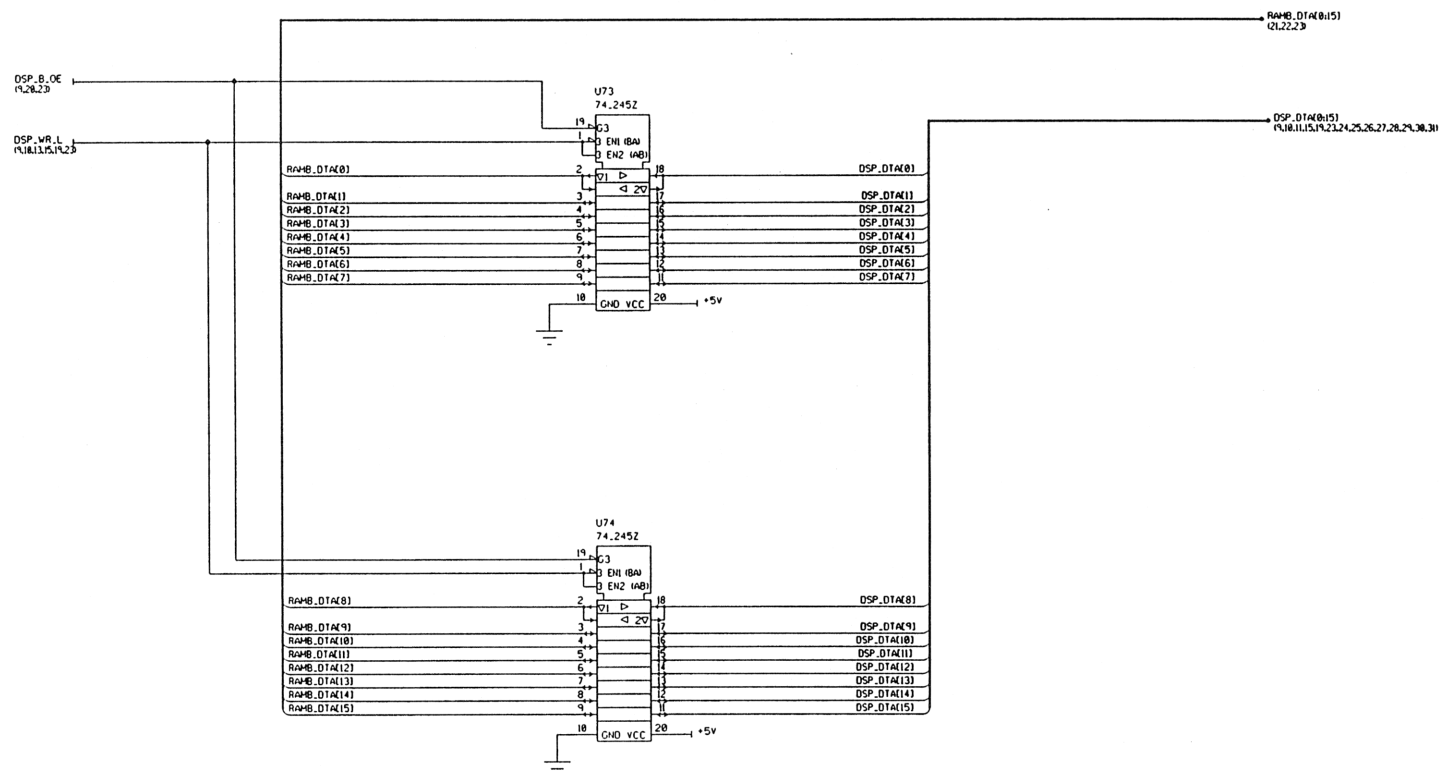


|       |    |
|-------|----|
| SHEET | 21 |
|-------|----|



BUFFER B/VME DATA BUFFERS

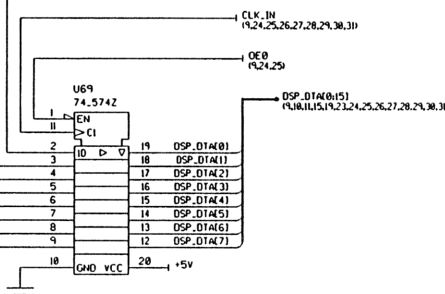
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|---------------------------------------------------------------------------------------------|----------------------|-----------------|-------------------|----------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B       | FORM NO.<br>08PH5 | DWG. NO.<br>141-001182-000 |
| DESIGNED<br>E.M. GREEN                                                                      | CHECKED<br>C. Murphy | DATE<br>8-12-94 | SCALE<br>NONE     | SHEET<br>22                |



# DSP/BUFFER B DATA BUFFERS

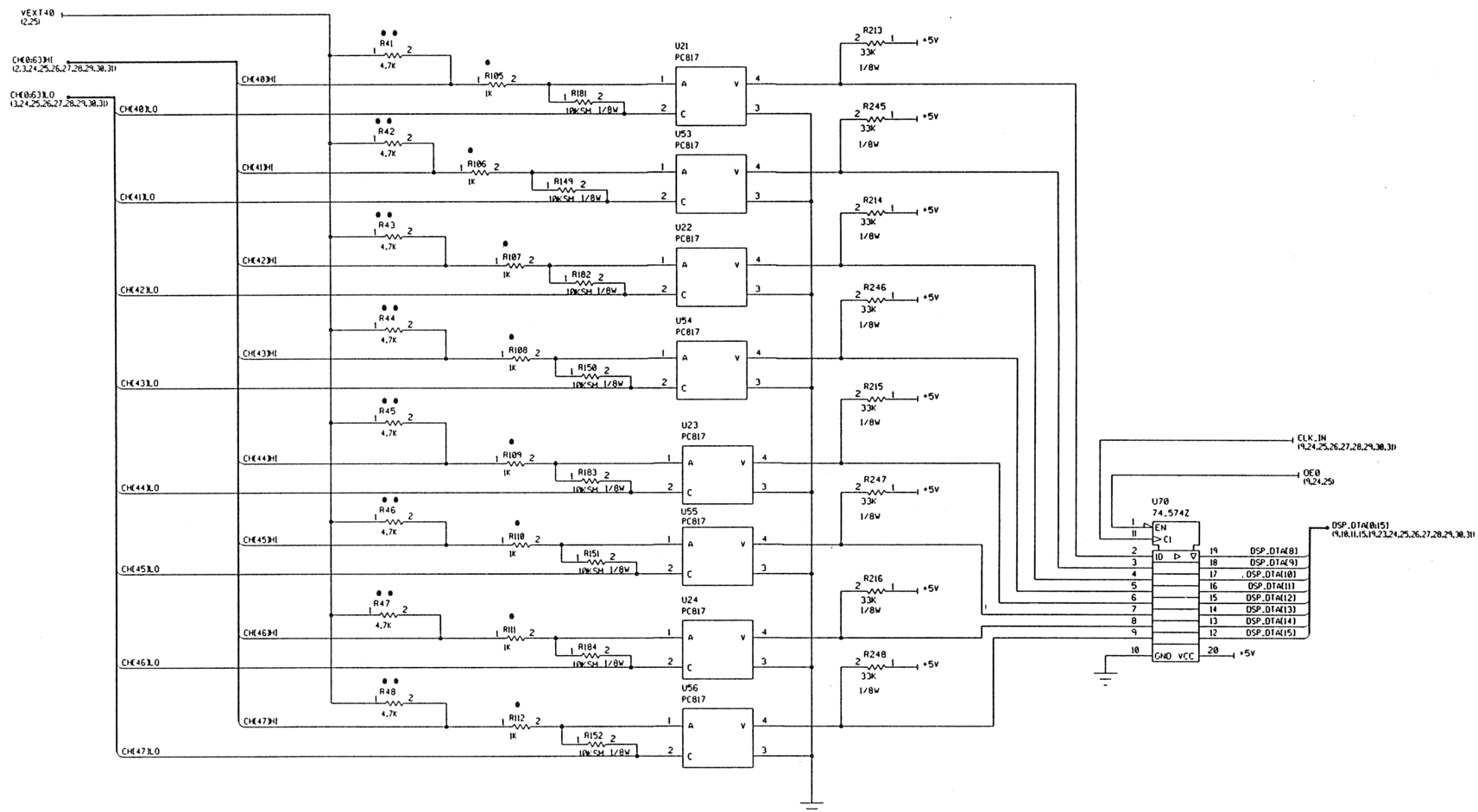
|                                                                                          |                             |                  |                          |                                  |
|------------------------------------------------------------------------------------------|-----------------------------|------------------|--------------------------|----------------------------------|
| <b>VMIC</b> Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                             | SIZE<br><b>B</b> | FORM NO.<br><b>08PH5</b> | DWG NO.<br><b>141-001182-000</b> |
| DRAWN<br>E.M. GREEN                                                                      | CHECKED<br>C. M. W. 8-12-94 | SCALE<br>NONE    | SHEET<br><b>23</b>       |                                  |





•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

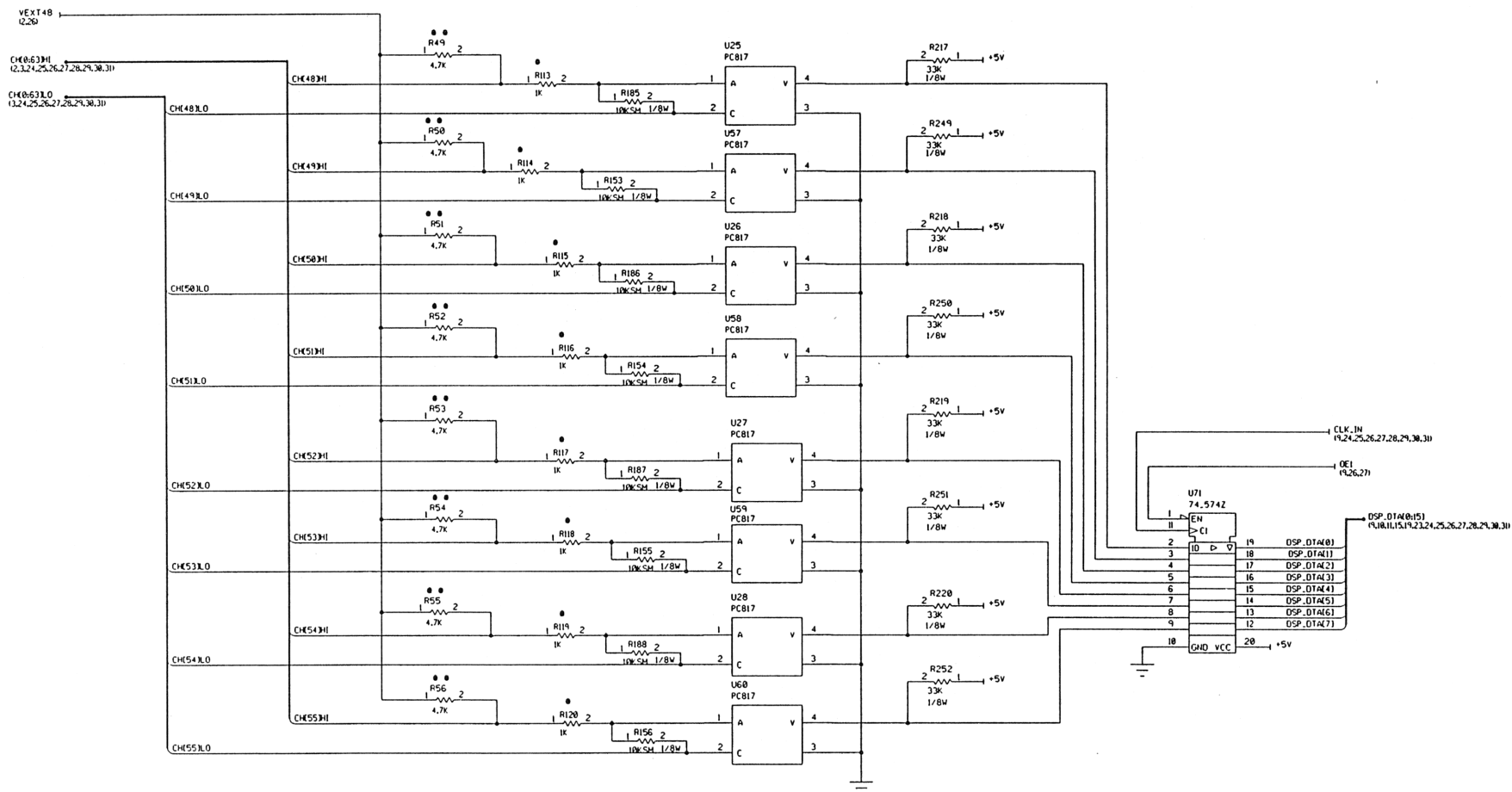
|                                                                                                                                                                    |  |       |          |                |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|-------|----------|----------------|
|  Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE  | FORM NO. | DWG NO.        |
| DESIGNER<br>E.M. GREEN                                                                                                                                             |  | B     | 08PH5    | 141-001182-000 |
| CHECKED<br>C. Murphy 8-12-94                                                                                                                                       |  | SCALE | NONE     | SHEET 24       |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

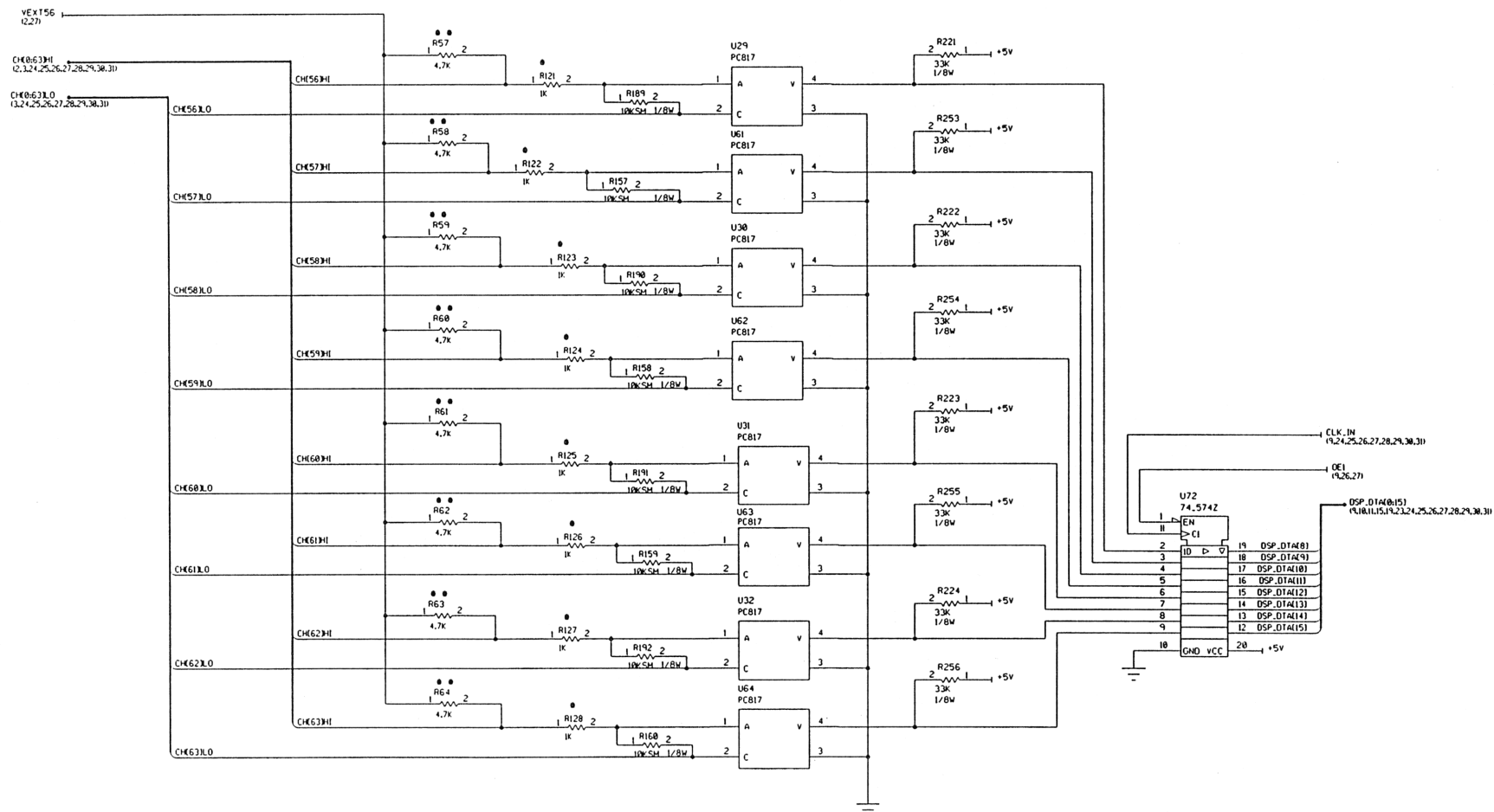
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|---------------------------------------------------------------------------------------------|------------------------------|-----------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                              | SIZE<br>B | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br>C. M. [signature] | 8-12-94   | SCALE<br>NONE     | SHEET<br>25               |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

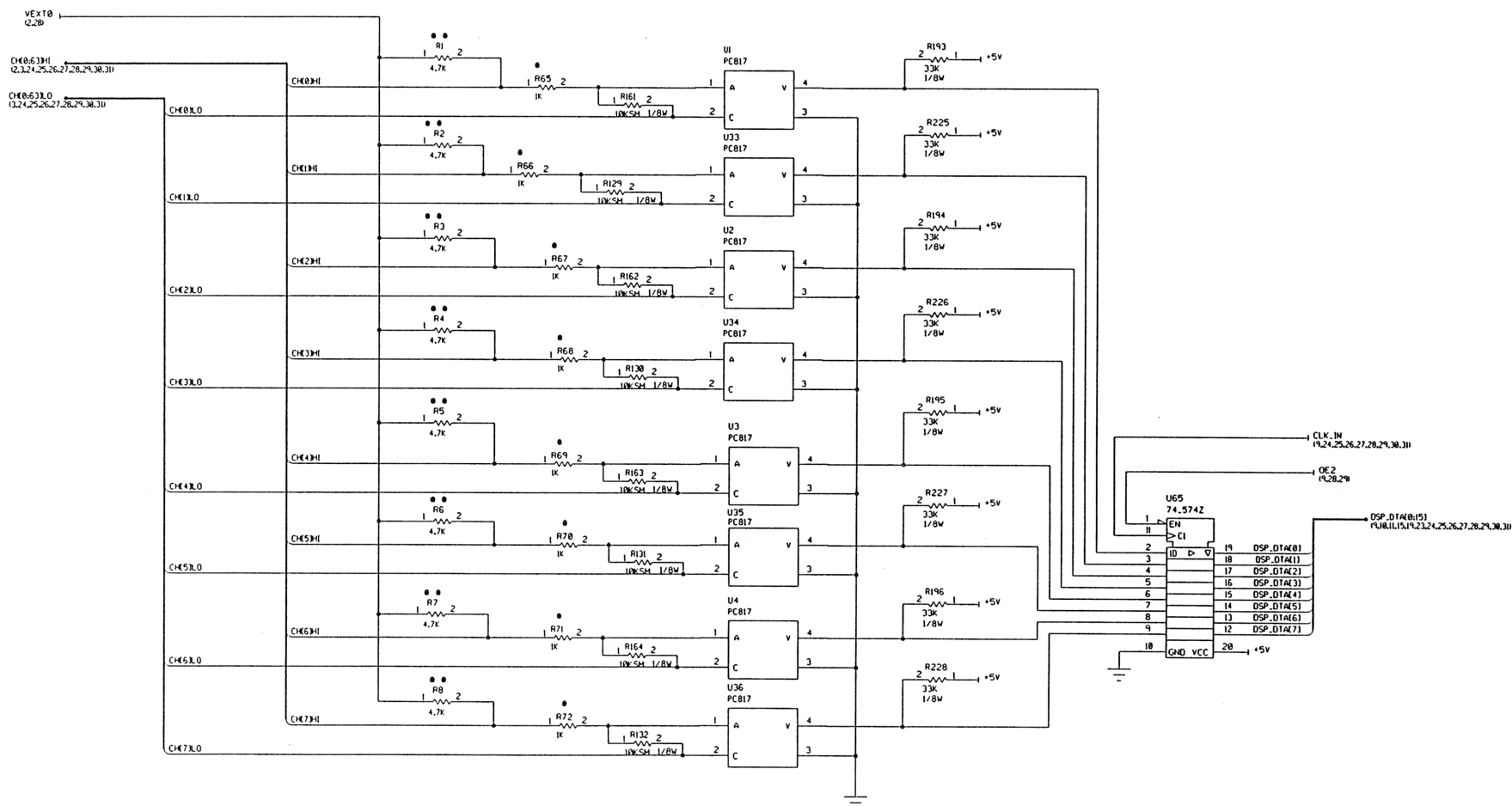
|                                                                                                                                                                    |         |               |                   |                           |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|---------------|-------------------|---------------------------|
|  Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |         | SIZE<br>B     | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.M. GREEN                                                                                                                                             | 8-12-94 | SCALE<br>NONE |                   | SHEET<br>26               |
| CHECKED<br>C. Murphy                                                                                                                                               |         |               |                   |                           |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL.  
SEE PARTS LIST FOR VALUE AND APPLICATION.

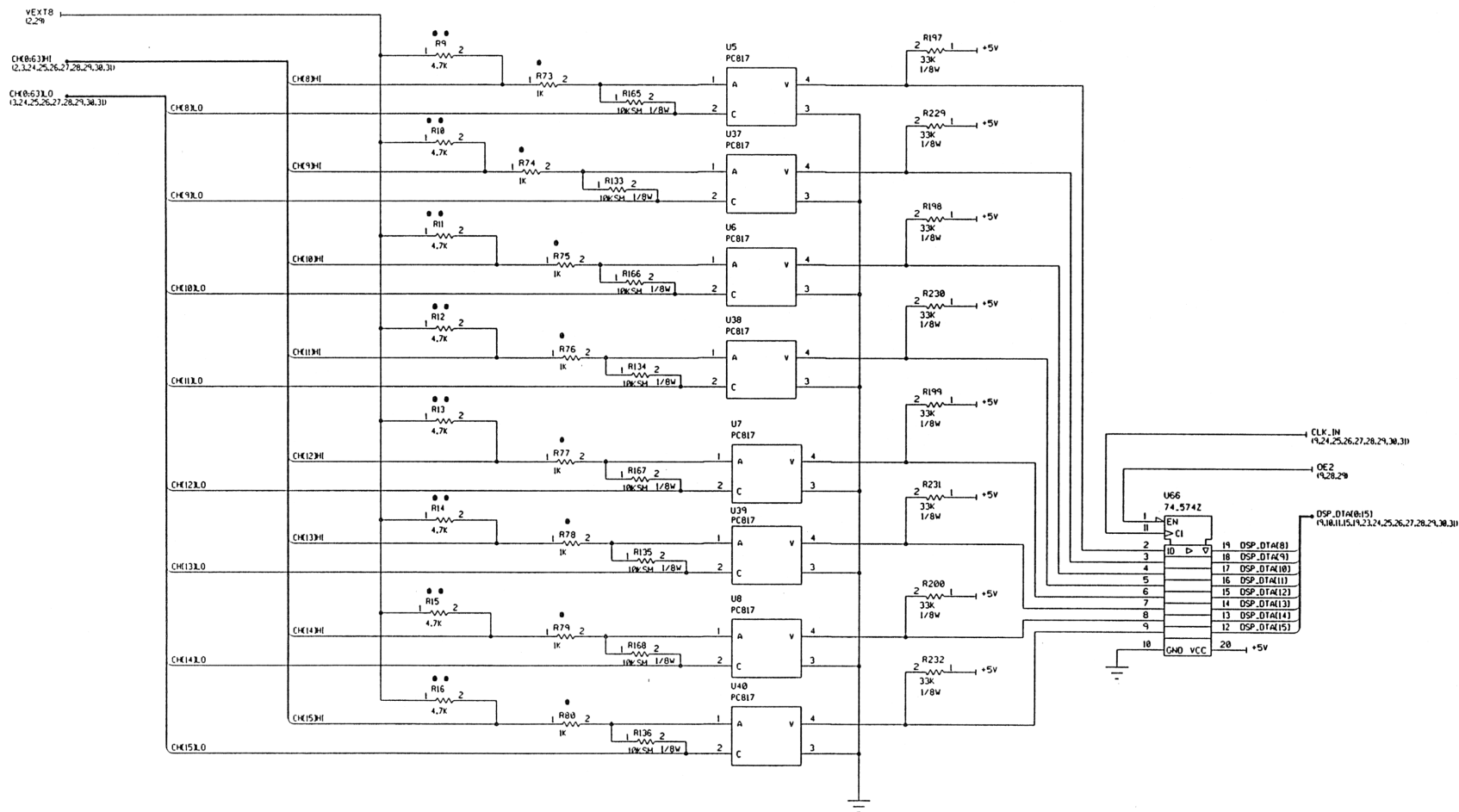
|                                                                                          |                      |           |                   |                           |
|------------------------------------------------------------------------------------------|----------------------|-----------|-------------------|---------------------------|
| <b>VMIC</b> Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.M. GREEN                                                                   | CHECKED<br>C. Murphy | 8-12-94   | SCALE<br>NONE     | SHEET<br>27               |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

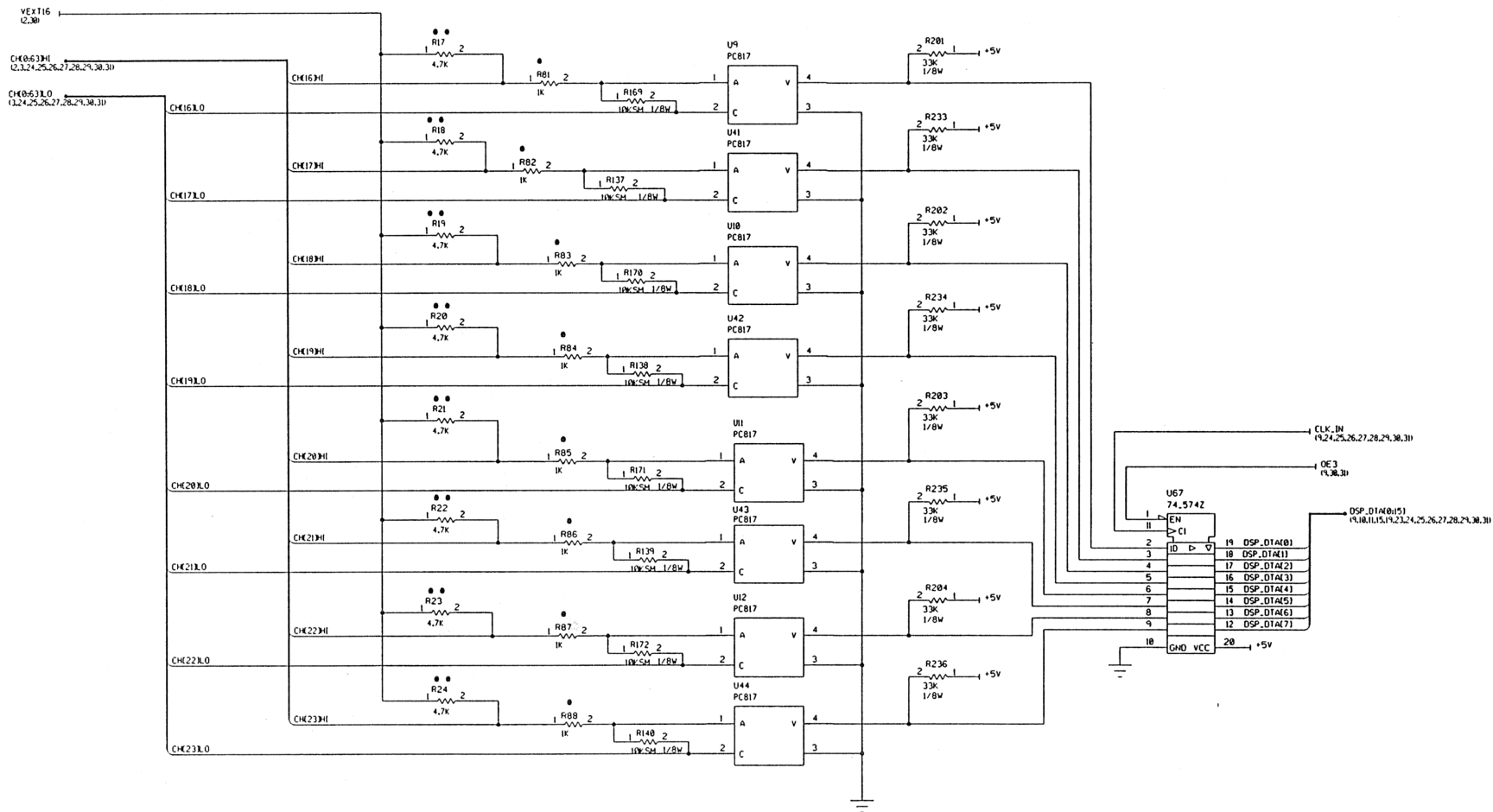
|                                                                                             |                         |                 |                   |                           |
|---------------------------------------------------------------------------------------------|-------------------------|-----------------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                         | SIZE<br>B       | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DRAWN<br>E.H. GREEN                                                                         | CHECKED<br>C. M. MURPHY | DATE<br>8-12-94 | SCALE<br>NONE     | SHEET<br>28               |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

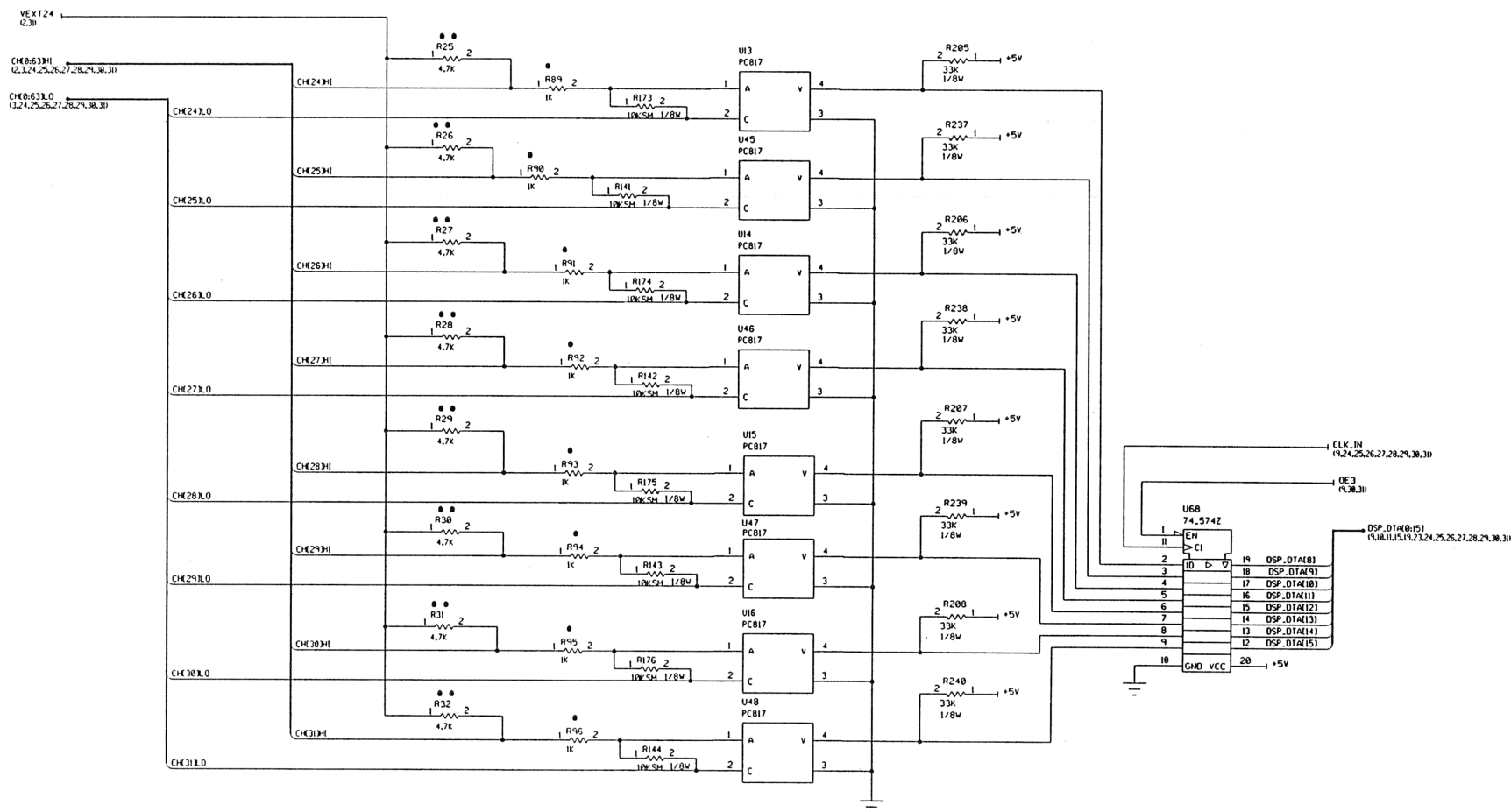
|                                                                                             |                      |               |                   |                           |
|---------------------------------------------------------------------------------------------|----------------------|---------------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B     | FORM NO.<br>08PH5 | DWG NO.<br>141-001182-000 |
| DESIGNED<br>E.H. GREEN                                                                      | CHECKED<br>C. Murphy | SCALE<br>NONE | SHEET<br>29       | DATE<br>8-12-94           |



••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

|                                                                                             |                        |                      |                           |                                   |
|---------------------------------------------------------------------------------------------|------------------------|----------------------|---------------------------|-----------------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                        | SIZE<br><b>B</b>     | FORM NO.<br><b>08BPH5</b> | DWG. NO.<br><b>141-001182-000</b> |
| DESIGNED BY<br><b>E.H. GREEN</b>                                                            | DATE<br><b>8-12-94</b> | SCALE<br><b>NONE</b> | SHEET<br><b>30</b>        |                                   |

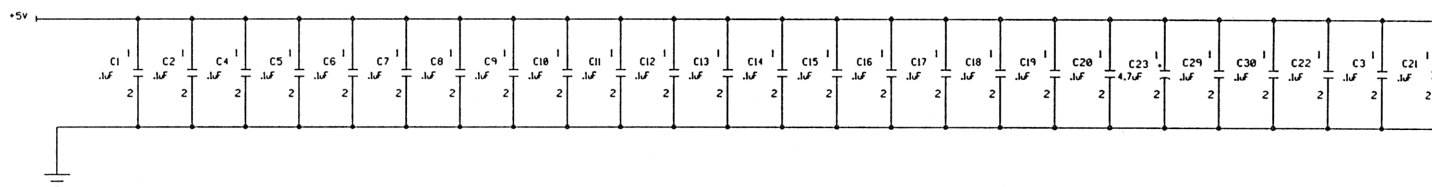


••DENOTES 1/2 WATT RESISTOR

•THESE PARTS ARE OPTIONAL,  
SEE PARTS LIST FOR VALUE AND APPLICATION.

|                                                                                             |                                    |                      |                          |                                  |
|---------------------------------------------------------------------------------------------|------------------------------------|----------------------|--------------------------|----------------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                                    | SIZE<br><b>B</b>     | FORM NO.<br><b>08PH5</b> | DWG NO.<br><b>141-001182-000</b> |
| DESIGNED<br><b>E.H. GREEN</b>                                                               | CHECKED<br><b>C. M. M. 8-12-94</b> | SCALE<br><b>NONE</b> | SHEET<br><b>31</b>       |                                  |





|                                                                                             |                      |               |                   |                            |
|---------------------------------------------------------------------------------------------|----------------------|---------------|-------------------|----------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |                      | SIZE<br>B     | FORM NO.<br>08PH5 | Dwg. NO.<br>141-001182-000 |
| DRAWN<br>E.H. GREEN                                                                         | CHECKED<br>C. Murphy | SCALE<br>NONE | SHEET<br>32 OF 32 |                            |

|           |                          |         |          |
|-----------|--------------------------|---------|----------|
| SIZE<br>A | DWG NO<br>132-001182-000 | SH<br>1 | REV<br>A |
|-----------|--------------------------|---------|----------|

REVISION  
STATUS  
OF 332

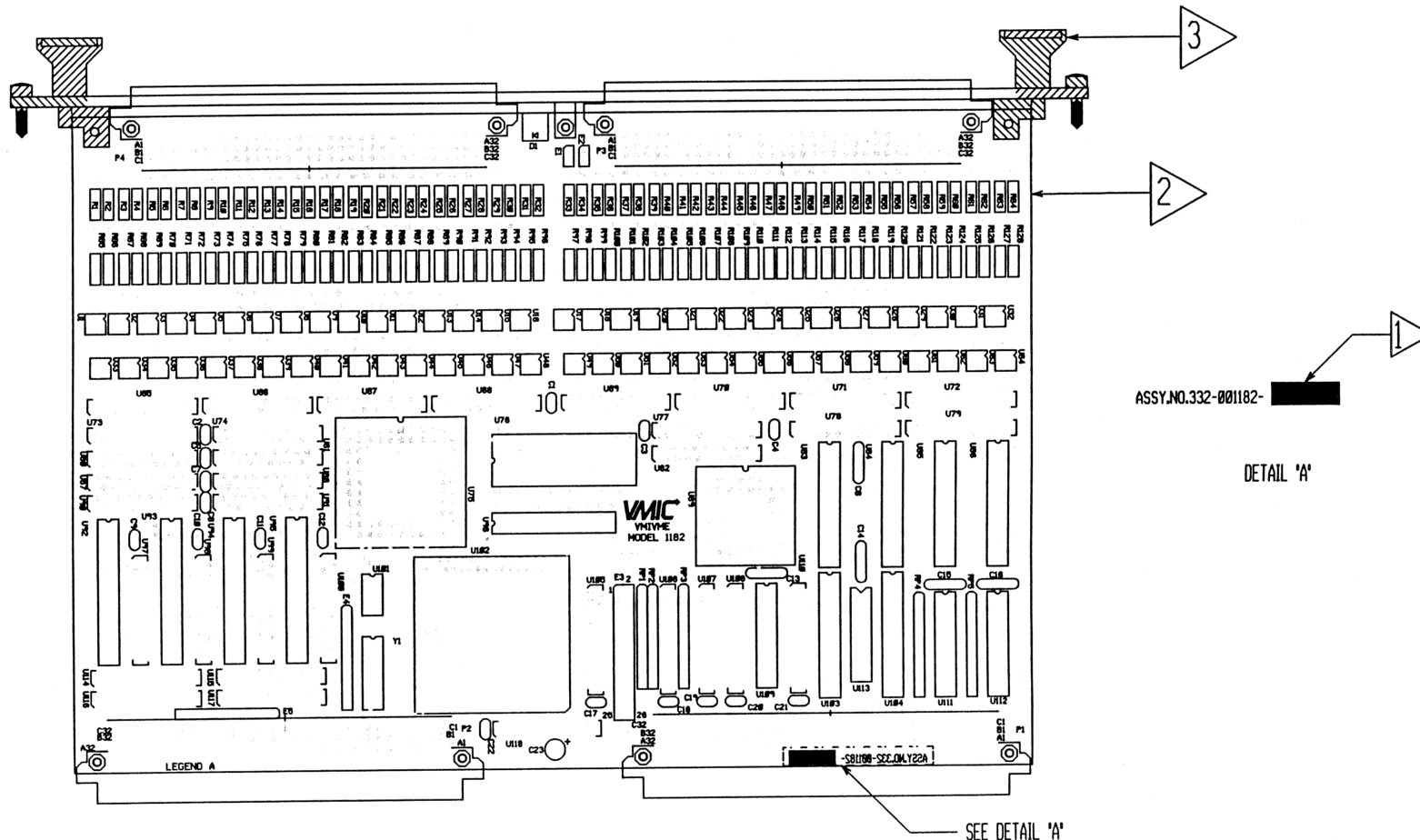
REVISIONS

| REV | DESCRIPTION             | DATE    | APPROVED           |
|-----|-------------------------|---------|--------------------|
| A   | RELEASE PER ECO 94-0556 | 9-23-94 | <i>[Signature]</i> |

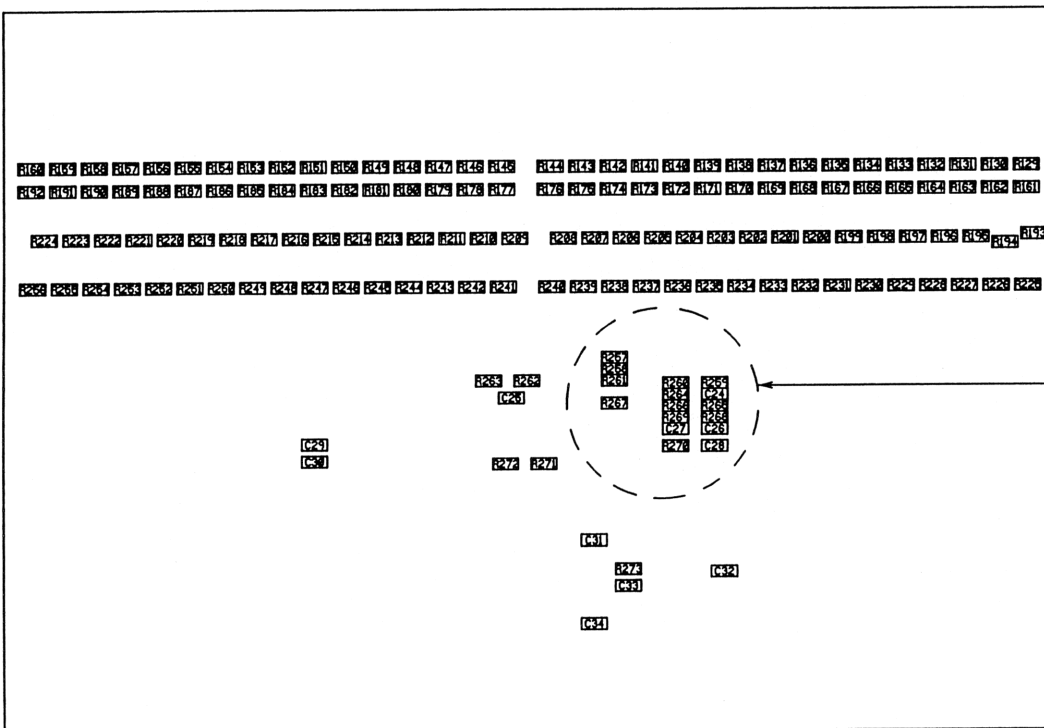
NOTES:

1. FOR SCHEMATIC DIAGRAM SEE 141-001182-000.
2. FOR TEST PROCEDURE SEE 510-001182-000.
3. FOR DOCUMENT SET SEE 110-001182-000.

|                                                                                                                                                                                                                                    |                                                      |                   |                                                                                                                                  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------|
| UNLESS OTHERWISE SPECIFIED<br><br>DIMENSIONS ARE IN INCHES<br>TOLERANCES ON:<br>2 PL DECIMALS ±<br>3 PL DECIMALS ±<br>ANGLES ±<br>FRACTIONS ±                                                                                      | SIGNATURES                                           | DATE              | <b>VMIC.</b> HUNTSVILLE, ALABAMA 35803-3308<br>VME MICROSYSTEMS INTERNATIONAL CORPORATION<br><br>ASSEMBLY DRAWING<br>VMIVME-1182 |
|                                                                                                                                                                                                                                    | DRAWN: E. JORY                                       | 1/25/94           |                                                                                                                                  |
|                                                                                                                                                                                                                                    | PROJ.ENG.: J. CROUCH                                 | 3/7/94            |                                                                                                                                  |
|                                                                                                                                                                                                                                    | ENG.MOR.: R. MELROSE                                 | 3/11/94           |                                                                                                                                  |
|                                                                                                                                                                                                                                    | PROD. <i>[Signature]</i>                             | 9/26/94           |                                                                                                                                  |
| THIS DRAWING AND SPECIFICATION<br>HEREIN ARE THE PROPERTY OF VMIC<br>AND SHALL NOT BE REPRODUCED OR<br>COPIED OR USED IN WHOLE OR IN<br>PART AS A BASIS FOR THE MANU-<br>FACTURE OR SALE OF ITEMS WITH-<br>OUT WRITTEN PERMISSION. | Q.A.: <i>[Signature]</i>                             | 9/26/94           |                                                                                                                                  |
|                                                                                                                                                                                                                                    | MAGNETIC MEDIA FILENAME FOR PACKAGE:<br>A001182A.EXE |                   |                                                                                                                                  |
|                                                                                                                                                                                                                                    | SIZE<br>A                                            | FSCM NO.<br>OBPH5 | DWG NO.<br>132-001182-000                                                                                                        |
|                                                                                                                                                                                                                                    | SCALE<br>NONE                                        |                   | SHEET<br>1 OF 8                                                                                                                  |

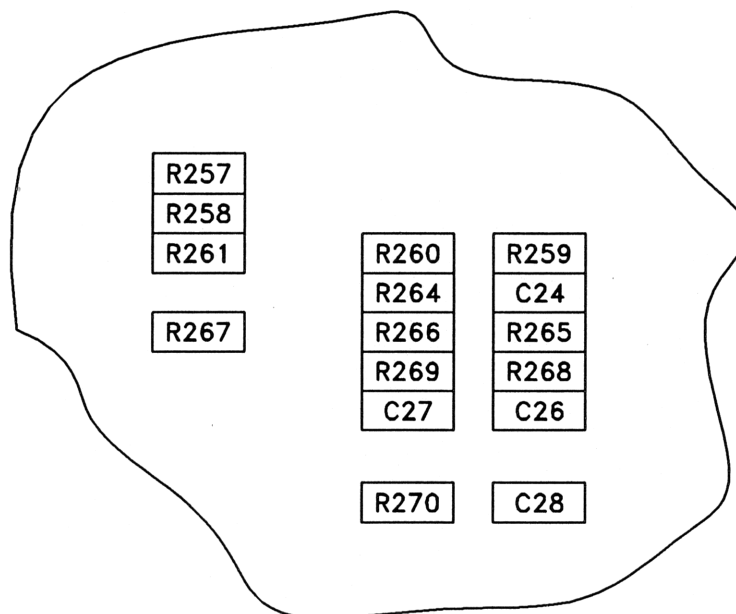


|                                                                                             |  |       |          |                |
|---------------------------------------------------------------------------------------------|--|-------|----------|----------------|
| <b>VMIC</b><br>VME Microsystems International Corporation<br>Huntsville, Alabama 35803-3308 |  | SIZE  | FORM NO. | DWG NO.        |
|                                                                                             |  | B     | 0BPH5    | 132-001182-000 |
| DRAWN BY K. COWAN<br>CHECKED BY C. M. W. 332 9-1-94                                         |  | SCALE | SHEET 2  |                |
|                                                                                             |  | NONE  |          |                |



SEE DETAIL 'B'

|                                                                                             |  |               |                   |                           |
|---------------------------------------------------------------------------------------------|--|---------------|-------------------|---------------------------|
| <b>VMIC</b><br>Huntsville, Alabama 35803-3308<br>VME Microsystems International Corporation |  | SIZE<br>B     | FORM NO.<br>08PH5 | DWG NO.<br>132-001182-000 |
| DRAWN<br>K.COWAN                                                                            |  | SCALE<br>NONE |                   | SHEET<br>2A               |
| CHECKED<br>C. Muzzey 9-1-94                                                                 |  |               |                   |                           |



DETAIL "B"

|                                                                                  |                                                   |                   |                           |
|----------------------------------------------------------------------------------|---------------------------------------------------|-------------------|---------------------------|
| <b>VMIC</b><br>HUNTSVILLE, AL 35803-3308<br>VME MICROSYSTEMS INTERNATIONAL CORP. | SIZE<br>A                                         | FSCM NO.<br>OBPH5 | DWG NO.<br>132-001182-000 |
|                                                                                  | DRAWN: E. JORY<br>CHECKED: <i>C. Muzey</i> 9-1-94 |                   |                           |
| SCALE                                                                            |                                                   | SHEET 2B          |                           |

**NOTE:**

DO NOT REMOVE THE QFP CARRIER FROM THE DEVICE UNTIL INSTALLATION INTO THE BOARD SOCKET. UTILIZE THE EXISTING INSERTION TOOL FROM AMP (AMP P/N 822253-4), OR FOLLOW THE PROCEDURE BELOW.

**STEP 1**

PLACE THE DEVICE WITH QFP CARRIER AGAINST A FLAT, STATIC FREE WORK SURFACE.

**STEP 2**

WITHOUT APPLYING PRESSURE, HOLD DOWN THE DEVICE WITH THE BLUNT END OF A PENCIL OR SIMILAR DEVICE.

**STEP 3**

USE THUMB AND FOREFINGER TO BEND UP THE YELLOW RETAINING CLIPS LOCATED ON DIAGONAL CORNERS OF THE CARRIER (IF CARRIER HAS RETAINING CLIPS ON ALL FOUR CORNERS, LIFTING TWO CORNERS SHOULD STILL ALLOW THE CARRIER TO LIFT FREE).

**STEP 4**

INSTALL QFP DEVICE COVER, ITEM 24, IN REVERSE ORDER OF THE CARRIER REMOVAL.

**CAUTION:**

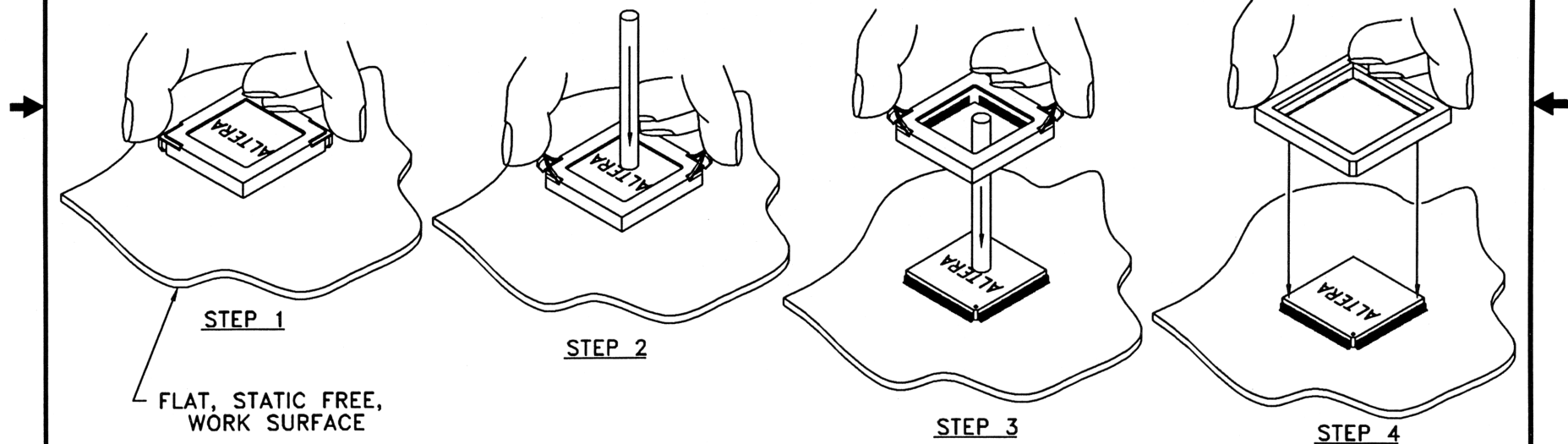
WHEN INSTALLING THE DEVICE COVER INSURE THE FOUR CORNER CLIPS CLEAR THE DEVICE PINS AND PIN 1 ORIENTATION OF THE COVER AND DEVICE MATCH.

**STEP 5**

AFTER THE COVER IS FLAT AGAINST THE WORK SURFACE AND OVER THE DEVICE, LIFT THE COVER WITH THE DEVICE AND INSURE THE UNDERSIDE DEVICE PINS ARE PROPERLY ALIGNED AND SEATED WITHIN THE COVER GUIDES.

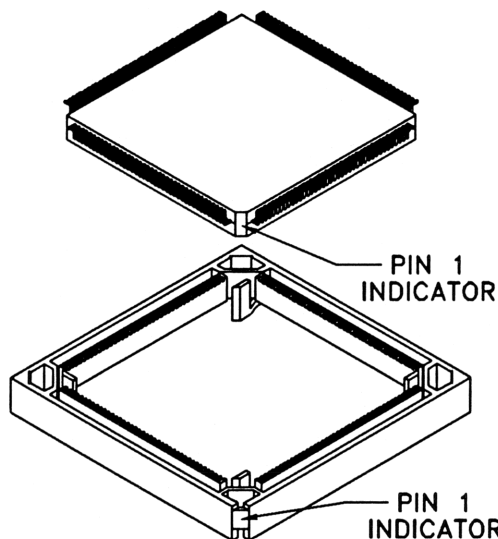
**STEP 6**

INSERT DEVICE WITH COVER INTO THE PROPER BOARD SOCKET INSURING PIN 1 ORIENTATION IS CORRECT.

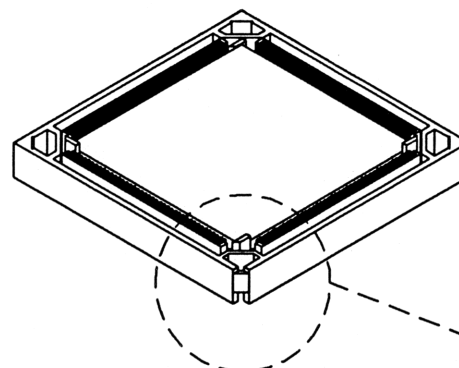


DETAIL "C"

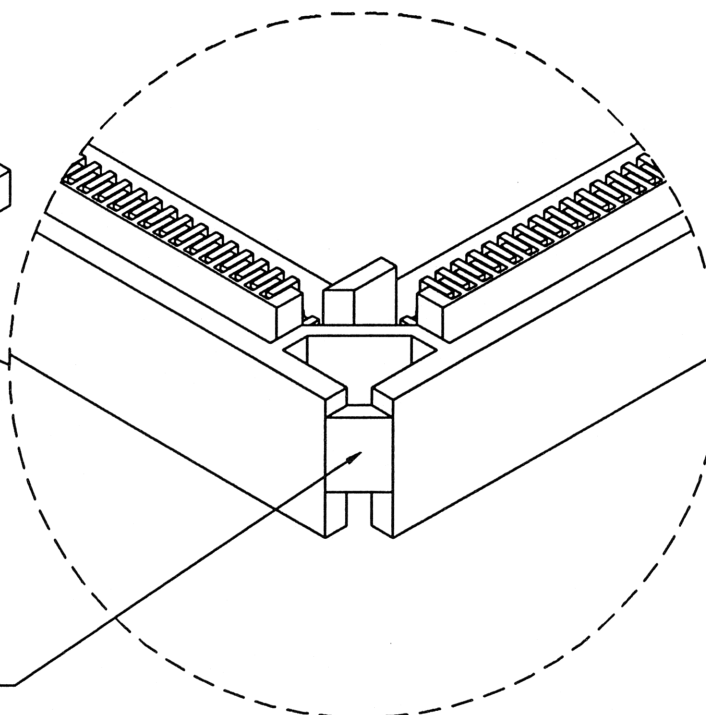
|                                                                               |  |              |                   |                           |
|-------------------------------------------------------------------------------|--|--------------|-------------------|---------------------------|
| <b>VMIC</b> HUNTSVILLE, AL 35803-3308<br>VME MICROSYSTEMS INTERNATIONAL CORP. |  | SIZE<br>A    | FSCM NO.<br>OBPH5 | DWG NO.<br>132-001182-000 |
| DRAWN: E. JORY                                                                |  | SCALE .375=1 |                   | SHEET 2C                  |
| CHECKED: C. Musser 9-1-94                                                     |  |              |                   |                           |



BOTTOM VIEWS OF COVER  
AND DEVICE PRIOR TO  
STEP 4



BOTTOM VIEW OF ASSEMBLED  
COVER AND DEVICE  
STEP 5



BOTTOM VIEW OF ASSEMBLED COVER AND DEVICE  
SHOWING CORRECT PIN ALIGNMENT

DETAIL "C" (CONTINUED)

|                                                                               |                                                    |                   |                           |
|-------------------------------------------------------------------------------|----------------------------------------------------|-------------------|---------------------------|
| <b>VMIC</b> HUNTSVILLE, AL 35803-3308<br>VME MICROSYSTEMS INTERNATIONAL CORP. | SIZE<br>A                                          | FSCM NO.<br>OBPH5 | DWG NO.<br>132-001182-000 |
|                                                                               | DRAWN: E. JORY<br>CHECKED: C.M. [signature] 9-1-94 |                   | SCALE<br>SHEET 2D         |

# REWORK LEGEND:

- A. REWORK INSTRUCTIONS SHALL BE ACCOMPLISHED ON THE COPPER REVISION(S) INDICATED AND WILL BECOME A PART OF THE ASSEMBLED BOARD.
- B. REWORK INSTRUCTION SYMBOLS:
  1. PIN ONE DOT ■
  2. DRILL HOLE ●
  3. DISCONNECT TRACE ×
  4. TRACE ON INTERNAL LAYER - - - - -
  5. TRACE ON EXTERNAL LAYER ———

# INSTRUCTIONS:

## NOTES:

1

- A. ALL ASSEMBLED BOARDS SHALL BE IDENTIFIED WITH THE ASSEMBLED BOARD PART NUMBER. THIS NUMBER INCLUDES THE CURRENT REVISION LETTER LISTED IN THE "REVISION STATUS OF 332" BLOCK (SEE SHEET 1). THE RESULTING PART SHALL BECOME A 332-001182-ABC (REV).
- B. THE PART NUMBER FIELDS "ABC" WILL COINCIDE WITH THE OPTIONAL PARTS INSTALLED IN THE COMPLETED ASSEMBLY. IF NO OPTIONAL PARTS ARE USED IN A FIELD, THAT FIELD WILL DEFAULT TO "0".

2

- C. IF NECESSARY, REMOVE AND REPLACE 332 REVISION LETTER WITH CURRENT REVISION LETTER USING EITHER A REMOVABLE NON-SMEARING BLACK INK OR A LABEL.

3

SOLDER COMPOSITION COMPLIES WITH MIL-STD-2000.

SEE DRAWING 150-000022-000 FOR THE ASSEMBLY AND INSTALLATION OF THE FRONT PANEL.

**VMIC**

HUNTSVILLE, AL 35803-3308  
VME MICROSYSTEMS INTERNATIONAL CORP.

DRAWN: E. JORY

CHECKED: *C. Murphy* 9-1-94

SIZE

A

FSCM NO.

OBPH5

DWG NO.

132-001182-000

SCALE

SHEET

3



| OPT. |   |   | Q<br>U<br>A<br>N<br>T<br>I<br>T<br>Y | I<br>T<br>E<br>M<br># | <b>VMIC<sup>®</sup></b> <b>PARTS LIST</b><br><b>VME MICROSYSTEMS INT'L CORP.</b> | CODE           | REV.                                                                        | DRAWING NUMBER | CHECKED                                | SH NO.     |
|------|---|---|--------------------------------------|-----------------------|----------------------------------------------------------------------------------|----------------|-----------------------------------------------------------------------------|----------------|----------------------------------------|------------|
| A    | B | C |                                      |                       |                                                                                  | OBPH5          | A                                                                           | 132-001182-000 | <i>C. Muzger</i><br>DATE <i>9/1/94</i> | 4          |
|      |   |   |                                      |                       | REFERENCE DESIGNATOR                                                             | PART NO.       | NOMENCLATURE OR DESCRIPTION                                                 |                | MANUFACTURER'S PART NO.                |            |
|      |   |   | 1                                    | 1                     |                                                                                  | 333-001182-000 | BOARD: PC, RAW, 8 LAYERS                                                    |                |                                        |            |
|      |   |   | 1                                    | 2                     |                                                                                  | 317-000106-000 | F/P ASSY: EXTRUDED EJECTOR, TWO 96 PIN CUTOUT, PANEL MOUNT LED (SEE NOTE 3) |                |                                        |            |
|      |   |   | 1                                    | 3                     |                                                                                  | 324-001182-100 | LABEL: ID, 1182, FRONT PANEL (SEE NOTE 3)                                   |                |                                        |            |
|      |   |   | 1                                    | 4                     | U103                                                                             | 303-001068-000 | PROGRAMMED PAL: FILE: 1182103A.JED<br>A PROGRAMMED 20R4 (331-300105-600)    |                |                                        |            |
|      |   |   | 1                                    | 5                     | U104                                                                             | 303-001069-000 | PROGRAMMED PAL: FILE: 1182104A.JED<br>A PROGRAMMED 20R4 (331-300105-600)    |                |                                        |            |
|      |   |   | 1                                    | 6                     | U96                                                                              | 303-001070-000 | PROGRAMMED PAL: FILE: 1182-96A.JED<br>A PROGRAMMED 20R4 (331-300105-600)    |                |                                        |            |
|      |   |   | 1                                    | 7                     | U76                                                                              | 306-001071-000 | PROGRAMMED PROM: FILE: 1182-76A.MX,<br>A PROGRAMMED 27C256 (331-309061-000) |                |                                        |            |
|      |   |   | 1                                    | 8                     | U89                                                                              | 303-001072-000 | PROGRAMMED PAL: FILE: 1182-89A.POF<br>A PROGRAMMED EPM7032 (331-300147-003) |                |                                        |            |
|      |   |   | 1                                    | 9                     | U102                                                                             | 303-001073-000 | PROGRAMMED PAL: FILE: 1182102A.POF<br>A PROGRAMMED EPM7160 (331-300154-012) |                |                                        |            |
|      |   |   | 5                                    | 10                    | C6,13-16                                                                         | 315-005002-104 | CAP: .1uF, .300 LEAD SPACE, 10%, 50V, X7R, CERAMIC MOLDED                   |                | CW80C104KM                             | (PHILLIPS) |
|      |   |   | 1                                    | 11                    | C23                                                                              | 315-103001-475 | CAP: 4.7uF, .100 LEAD SPACE, 20%, 35V, TANTALUM                             |                | T35(0,1)E475M035AS                     | (KEMET)    |
|      |   |   | 17                                   | 12                    | C1-5,7-12,17-22                                                                  | 315-205000-104 | CAP: .1uF, .100 LEAD SPACE, 20%, 50V, 25U, CERAMIC MONOLYTHIC               |                | C3(15,20)C104M5U5CA                    | (KEMET)    |
|      |   |   | 11                                   | 13                    | C24-34                                                                           | 315-305000-104 | CAP: SMT, CERAMIC, 0.1uF, 10%, 50V, X7R EIA 1206                            |                | C1206C104K5RAC                         | (KEMET)    |
|      |   |   | A/R                                  | 14                    | P1-4                                                                             | 316-000002-000 | LOCTITE: SMALL SCREW THREADLOCKER 222                                       |                |                                        |            |

| OPT. |   |   | QUANTITY | ITEM # | <b>VMIC<sup>®</sup></b> <b>PARTS LIST</b><br><b>VME MICROSYSTEMS INT'L CORP.</b> |                | CODE<br>OBPH5                                                                     | REV.<br>A | DRAWING NUMBER<br>132-001182-000 | CHECKED<br><i>C. Munn</i><br>DATE 9/1/94 | SH NO.<br>5  |
|------|---|---|----------|--------|----------------------------------------------------------------------------------|----------------|-----------------------------------------------------------------------------------|-----------|----------------------------------|------------------------------------------|--------------|
| A    | B | C |          |        | REFERENCE DESIGNATOR                                                             | PART NO.       | NOMENCLATURE OR DESCRIPTION                                                       |           |                                  | MANUFACTURER'S PART NO.                  |              |
|      |   |   | 2        | 15     | E4,5                                                                             | 321-000007-210 | SOCKET: IC, BREAKAWAY STRIP, 10 CONTACTS, TIN/GOLD                                |           |                                  | SBE100-S-(TG,TG30)                       | (R/N)        |
|      |   |   | 3        | 16     | E1-3                                                                             | 321-000015-001 | JUMPER: PC BOARD, 2 POSITION, FEMALE, GOLD PLATED CONTACT, BLACK                  |           |                                  | MSB-2360-G-C-STP                         | (McKENZIE)   |
|      |   |   | 2        | 17     | E1,2                                                                             | 321-000016-021 | TERMINAL: PC BOARD, SINGLE ROW, .025 THICK, GOLD PLATED, TWO POSTS                |           |                                  | 92983401-02                              | (PANDUIT)    |
|      |   |   | 1        | 18     | E3                                                                               | 321-000017-131 | TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, THIRTEEN POSTS             |           |                                  | PEG260S-(T,F)BR                          | (CRANE)      |
|      |   |   | 1        | 19     | P1                                                                               | 321-000054-001 | CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C                          |           |                                  | 536437-6                                 | (AMP)        |
|      |   |   | 3        | 20     | P2-4                                                                             | 321-000054-002 | CONNECTOR: DIN, 96 PIN WITH EXTENDED GROUND PINS, TYPE C                          |           |                                  | 536437-5                                 | (AMP)        |
|      |   |   | 1        | 21     | U89                                                                              | 321-000062-044 | CARRIER: CHIP, 44 PIN PLCC                                                        |           |                                  | 821575-1 (PREFERRED)                     | (AMP)        |
|      |   |   | 1        | 22     | U75                                                                              | 321-000062-068 | CARRIER: CHIP, 68 PIN PLCC                                                        |           |                                  | 821574-1                                 | (AMP)        |
|      |   |   | 1        | 23     | U102                                                                             | 321-000122-160 | SOCKET: IC, EIAJ METRIC QUAD FLAT PACK, (QFP) 160 PIN                             |           |                                  | 822114-4                                 | (AMP)        |
|      |   |   | 1        | 24     | U102                                                                             | 321-000122-161 | SOCKET COVER: QUAD FLAT PACK, 160 PIN                                             |           |                                  | 822115-4                                 | (AMP)        |
|      |   |   | 3        | 25     | U96,103,104                                                                      | 321-001324-001 | SOCKET: DIP, 24 PIN, .300 ROW, STAMPED & FORMED                                   |           |                                  | 2-641932-(3,1,5)                         | (AMP)        |
|      |   |   | 1        | 26     | U76                                                                              | 321-001628-001 | SOCKET: DIP, 28 PIN, .600 ROW, STAMPED & FORMED                                   |           |                                  | 2-641605-(3,1,5)                         | (AMP)        |
|      |   |   | 1        | 27     | Y1                                                                               | 323-000007-400 | OSCILLATOR: TTL, HIGH SPEED CMOS, +-100ppm, 5Vdc, 40.0 MHz, -10 TO 70 DEGREES C , |           |                                  | P5C-KT-40MHZ                             | (FOX)        |
|      |   |   | 1        | 28     | U113                                                                             | 323-500002-030 | DELAY LINE: DIGITAL, TTL, 5 TAP, 8 PIN SIL, 30ns                                  |           |                                  | DDU-222-30                               | (DATA DELAY) |
|      |   |   | 4        | 29     | P1,2                                                                             | 328-250000-010 | SCREW: METRIC, 2.5 X 10MM, SS                                                     |           |                                  |                                          |              |
|      |   |   | 8        | 30     | P1-4                                                                             | 328-250001-025 | NUT: METRIC, 2.5MM, HEX, SS                                                       |           |                                  |                                          |              |

| OPT. |   |   | Q<br>U<br>A<br>N<br>T<br>I<br>T<br>Y | I<br>T<br>E<br>M<br># | <b>VMIC<sup>®</sup></b> <b>PARTS LIST</b><br><b>VME MICROSYSTEMS INT'L CORP.</b> |                | CODE<br>OBPH5                                                                      | REV.<br>A | DRAWING NUMBER<br>132-001182-000 | CHECKED<br><i>C. Muzzey</i> | SH NO.<br>6                |
|------|---|---|--------------------------------------|-----------------------|----------------------------------------------------------------------------------|----------------|------------------------------------------------------------------------------------|-----------|----------------------------------|-----------------------------|----------------------------|
| A    | B | C |                                      |                       | REFERENCE<br>DESIGNATOR                                                          | PART NO.       | NOMENCLATURE OR DESCRIPTION                                                        |           |                                  | DATE<br>9/1/94              | MANUFACTURER'S<br>PART NO. |
|      |   |   | 13                                   | 31                    | U77,82,97-100,105<br>U106,114-118                                                | 331-304244-133 | IC: DIGITAL, OCTAL BUFFER/LINE DRIVER, TRI-STATE,<br>NON-INVERTING, ZIP PACKAGE    |           |                                  | QS74FCT244ATZ               | (QUALITY SEMI)             |
|      |   |   | 10                                   | 32                    | U73,74,78-81,87,88<br>U90,91                                                     | 331-304245-723 | IC: DIGITAL, OCTAL BIDIRECTIONAL TRANSEIVER, TRI-<br>STATE, ZIP PACKAGE            |           |                                  | QS74FCT245TATZ              | (QUALITY SEMI)             |
|      |   |   | 1                                    | 33                    | U110                                                                             | 331-304521-303 | IC: DIGITAL, 8 BIT COMPARATOR, FAST, ZIP PACKAGE                                   |           |                                  | QS74FCT521TZ                | (QUALITY SEMI)             |
|      |   |   | 10                                   | 34                    | U65-72,107,108                                                                   | 331-304574-703 | IC: DIGITAL, OCTAL D-TYPE FLIP-FLOP, THREE STATE,<br>PLASTIC ZIP                   |           |                                  | QS74FCT574(A)TZ             | (QUALITY SEMI)             |
|      |   |   | 1                                    | 35                    | U109                                                                             | 331-304641-610 | IC: DIGITAL, OCTAL BUS TRANSCEIVER, OPEN COLLECTOR<br>PLASTIC DIP                  |           |                                  | SN74LS641-1N                | (TI)                       |
|      |   |   | 2                                    | 36                    | U111,112                                                                         | 331-304645-110 | IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP                                    |           |                                  | SN74(ALS,AS)645A-1N         | (TI)                       |
|      |   |   | 2                                    | 37                    | U85,86                                                                           | 331-304646-400 | IC: DIGITAL, TRI-STATE OCTAL BUS TRANSCEIVER AND<br>REGISTER, PLASTIC DIP          |           |                                  | SN74F646N                   | (TI)                       |
|      |   |   | 2                                    | 38                    | U83,84                                                                           | 331-309065-001 | IC: MEMORY, 2048 X 8, 16K BIT STATIC RAM, 35ns OR<br>LESSER, .300 WIDE PLASTIC DIP |           |                                  | MCM2018AN35                 | (MOTOROLA)                 |
|      |   |   | 4                                    | 39                    | U92-95                                                                           | 331-309105-250 | IC: MEMORY CMOS RAM, 8K X 8, 25ns, 495/575mW<br>ACTIVE LOW POWER .300 WIDE         |           |                                  | P4C164-25PC                 | (PERFORMANCE)              |
|      |   |   | 1                                    | 40                    | U75                                                                              | 331-309132-000 | IC: DSP MICROCOMPUTER, 68 PIN PLCC                                                 |           |                                  | ADSP-2105(K,B)P-40          | (A/D)                      |
|      |   |   | 1                                    | 41                    | U101                                                                             | 331-309148-000 | IC: MICROMONITOR CHIP, 8-PIN DIP                                                   |           |                                  | DS1232                      | (DALLAS SEMI)              |
|      |   |   | 1                                    | 42                    | D1                                                                               | 337-000001-110 | DIODE: LED, RED, 5V, 15mA, INTEGRAL RESISTOR,<br>WIRE LEADS                        |           |                                  | 558-0102-003                | (DIALIGHT)                 |
|      |   |   | 65                                   | 43                    | R129-192,273                                                                     | 347-000021-103 | RESISTOR: CHIP, 10K OHM, 1/8W, 5%, EIA SIZE 1206                                   |           |                                  | CRCW1206103JRT2             | (DALE)                     |
|      |   |   | 64                                   | 44                    | R193-256                                                                         | 347-000021-333 | RESISTOR: CHIP, 33K OHM, 1/8W, 5%, EIA SIZE 1206                                   |           |                                  | CRCW1206333JRT2             | (DALE)                     |
|      |   |   | 16                                   | 45                    | R257-272                                                                         | 347-000021-392 | RESISTOR: CHIP, 3.9K OHM, 1/8W, 5%, +- 200PPM                                      |           |                                  | CRCW1206392JRT2             | (DALE)                     |

| OPT. |   |   | Q<br>U<br>A<br>N<br>T<br>I<br>T<br>Y | I<br>T<br>E<br>M<br># | VME MICROSYSTEMS INT'L CORP. |                | CODE<br>OBPH5                                           | REV.<br>A | DRAWING NUMBER<br>132-001182-000 | CHECKED<br>C. Muzzey        | SH NO.<br>7 |
|------|---|---|--------------------------------------|-----------------------|------------------------------|----------------|---------------------------------------------------------|-----------|----------------------------------|-----------------------------|-------------|
|      |   |   |                                      |                       | DATE<br>9/1/94               |                |                                                         |           |                                  |                             |             |
| A    | B | C |                                      |                       | REFERENCE<br>DESIGNATOR      | PART NO.       |                                                         |           |                                  | NOMENCLATURE OR DESCRIPTION |             |
|      |   |   | 5                                    | 46                    | RP1-5                        | 347-001002-392 | SIP: 3.9K OHM, BUSSED, 10 PIN, LOW PROFILE              |           | 4610X-101-392 (BOURNS)           |                             |             |
|      |   |   | 1                                    | 47                    | E4                           | 347-001032-010 | SIP: 0 OHM, BUSSED, 10 PIN, LOW PROFILE                 |           | AK0X10G (ACCUTEK)                |                             |             |
|      |   |   | 64                                   | 48                    | U1-64                        | 348-000012-005 | OPTOCOUPLER: SINGLE CHANNEL, 4-PIN IC                   |           | PC817(B,BC,BD,C,CD,D) (SHARP)    |                             |             |
|      |   |   | 2                                    | 49                    | P3,4                         | 321-000048-003 | BRACKET: MULTIPLE FIXING, MALE CONNECTOR FOR 19", LEFT  |           | 09 02 000 9919 (HARTING)         |                             |             |
|      |   |   | 2                                    | 50                    | P3,4                         | 321-000048-004 | BRACKET: MULTIPLE FIXING, MALE CONNECTOR FOR 19", RIGHT |           | 09 02 000 9920 (HARTING)         |                             |             |
| 0    | 0 | 1 | 64                                   | 51                    | R1-64                        | 347-000005-750 | RESISTOR: 750 OHM, 1/4W, 1%, METAL FILM                 |           |                                  |                             |             |
| 0    | 0 | C | 64                                   | 52                    | R65-128                      | 347-000006-402 | RESISTOR: 4.02K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
|      |   |   | 4                                    | 53                    | P3,4                         | 328-250000-012 | SCREW: PAN HEAD, METRIC, 2.5 X 12MM, SS                 |           |                                  |                             |             |
| 0    | 1 | 1 | 64                                   | 54                    | R1-64                        | 347-000006-150 | RESISTOR: 1.50K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
| 0    | 1 | C | 64                                   | 55                    | R65-128                      | 347-000007-143 | RESISTOR: 14.3K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
|      |   |   |                                      | 56                    |                              |                |                                                         |           |                                  |                             |             |
| 0    | 2 | 1 | 64                                   | 57                    | R1-64                        | 347-000006-402 | RESISTOR: 4.02K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
| 0    | 2 | C | 64                                   | 58                    | R65-128                      | 347-000007-301 | RESISTOR: 30.1K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
|      |   |   |                                      | 59                    |                              |                |                                                         |           |                                  |                             |             |
| 0    | 3 | 1 | 64                                   | 60                    | R1-64                        | 347-000006-402 | RESISTOR: 4.02K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
| 0    | 3 | C | 64                                   | 61                    | R65-128                      | 347-000007-301 | RESISTOR: 30.1K OHM, 1/4W, 1%, METAL FILM               |           |                                  |                             |             |
|      |   |   |                                      | 62                    |                              |                |                                                         |           |                                  |                             |             |

| OPT. |   |   | Q<br>U<br>A<br>N<br>T<br>I<br>T<br>Y | I<br>T<br>E<br>M<br># | <b>VMIC<sup>®</sup></b> <b>PARTS LIST</b><br><b>VME MICROSYSTEMS INT'L CORP.</b> |                | CODE<br>OBPH5                                                | REV.<br>A                  | DRAWING NUMBER<br>132-001182-000 | CHECKED<br><i>C. Muzzey</i> | SH NO.<br>8 |
|------|---|---|--------------------------------------|-----------------------|----------------------------------------------------------------------------------|----------------|--------------------------------------------------------------|----------------------------|----------------------------------|-----------------------------|-------------|
| A    | B | C |                                      |                       | REFERENCE<br>DESIGNATOR                                                          | PART NO.       | NOMENCLATURE OR DESCRIPTION                                  | MANUFACTURER'S<br>PART NO. |                                  |                             |             |
| 0    | 4 | 1 | 64                                   | 63                    | R1-64                                                                            | 347-000032-100 | RESISTOR: 10.0K OHM, 1/2W, 1%, METAL FILM                    |                            |                                  |                             |             |
| 0    | 4 | C | 64                                   | 64                    | R65-128                                                                          | 347-000032-604 | RESISTOR: 60.4K OHM, 1/2W, 1%, METAL FILM                    |                            |                                  |                             |             |
|      |   |   |                                      | 65                    |                                                                                  |                |                                                              |                            |                                  |                             |             |
| 0    | 5 | 1 | 64                                   | 66                    | R1-64                                                                            | 347-000032-100 | RESISTOR: 10.0K OHM, 1/2W, 1%, METAL FILM                    |                            |                                  |                             |             |
| 0    | 5 | C | 64                                   | 67                    | R65-128                                                                          | 347-000032-806 | RESISTOR: 80.6K OHM, 1/2W, 1%, METAL FILM                    |                            |                                  |                             |             |
|      |   |   |                                      | 68                    |                                                                                  |                |                                                              |                            |                                  |                             |             |
| 0    | 6 | 1 | 64                                   | 69                    | R1-64                                                                            | 347-000032-402 | RESISTOR: 40.2K OHM, 1/2W, 1%, METAL FILM                    |                            |                                  |                             |             |
| 0    | 6 | C | 64                                   | 70                    | R65-128                                                                          | 347-000033-150 | RESISTOR: 150K OHM, 1/2W, 1%, 100PPM, METAL FILM, RN60C TYPE |                            |                                  |                             |             |
|      |   |   |                                      | 71                    |                                                                                  |                |                                                              |                            |                                  |                             |             |
| 0    | 7 | 1 | 64                                   | 72                    | R1-64                                                                            | 347-000033-150 | RESISTOR: 150K OHM, 1/2W, 1%, 100PPM, METAL FILM, RN60C TYPE |                            |                                  |                             |             |
| 0    | 7 | C | 64                                   | 73                    | R65-128                                                                          | 347-000033-280 | RESISTOR: 280K OHM, 1/2W, 1%, 50PPM, METAL FILM, RN50C TYPE  |                            |                                  |                             |             |
|      |   |   |                                      |                       |                                                                                  |                |                                                              |                            |                                  |                             |             |