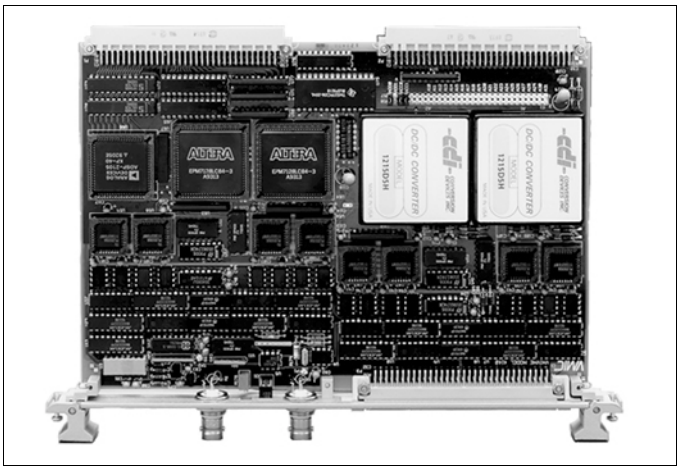
Embedded Systems

VMIVME-4140

32-Channel 12-bit Analog Output Board

- ***32 analog output channels***
  - ***10 mA maximum output current per channel***
  - ***One 12-bit D/A converter (DAC) per output channel***
- ***0.8 Ω output impedance***
- ***Random update (nonscanning)***
- ***Software or external synchronous update of double-buffered outputs***
- ***Single reference potentiometer – no other manual calibration required***
- ***Automatic calibration initiated by reset or by software command***
- ***Unipolar (0 to +10 V, 0 to +5 V, 0 to +2.5 V) or bipolar (±2.5, ±5, ±10 V) software selectable***
- ***Discrete wire or mass-terminated cables***
- ***Self-test***
  - ***Extensive onboard diagnostic testing capability***
  - ***Outputs can be disconnected from the field for offline self-testing***
- ***Front panel status LED***
- ***Front panel analog output connector***
- ***Front panel reference voltage access***
- ***Applications***
  - ***Data acquisition systems***
  - ***Control systems***
  - ***Precision analog stimulus***
  - ***Automatic test equipment (ATE)***



Front Panel Status LED: The LED is illuminated after a system reset. The LED is extinguished on the successful completion of self-test and autocalibration. The LED can also be turned ON and OFF under software control.

Functional Characteristics

Introduction: The VMIVME-4140 Analog Output Board provides 32 high quality analog output channels with 12-bit resolution, and can source or sink 10 mA at ±10 V. Each output has a dedicated D/A Converter (DAC) assigned to it. The analog outputs can be disconnected from the field wiring for offline testing. Calibration and self-test are initiated by a VMEbus system reset or by execution of a software command. During calibration, a table of offset and gain coefficients is compiled and stored in RAM. There is an entry for offset and gain corresponding to each of the 32 channels configured in each of the 6 output voltage ranges.

Self-Test: Self-Test is run automatically after system reset. The Self-Test Register indicates success or failure and can indicate the channel which has failed.

Ordering Options

July 22, 2004 800-004140-000 B		A	B	C	D	E	F
VMIVME-4140	–	**0**			**0**	**0**	**0**

A = 0 (Option reserved for future use.)
B = Output Connector Type
0 = Discrete Wire
1 = IDC (Mass-Terminated)
C = Number of Channels
0 = 32 Channels
1 = 16 Channels
DEF = 0 (Options reserved for future use.)

IDC Output Connector Data	
Mating Cable Connector	Panduit No. 120-964-435
Strain Relief	Panduit No. 100-000-072
PC Board I/O Connector	Panduit No. 120-964-033A
Discrete Wire Output Connector Data	
Mating Connector	AMP No. 925486-1
Female Crimp Contacts*	AMP No. 530151-6
Connector Shell Housing	Harting No. 09 03 096 0501
PC Board Connector	Panduit No. 120-964-033A
*An AMP crimp tool part number is 90301-2.	
Front Panel Reference Voltage and Front Panel External Sync Connector Data	
Front Panel Connector	AMP No. 22726-3
Note	
Panduit is also known as ITW/Pancon.	

For Ordering Information, Call:
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Web Address: www.gefanuc.com/embedded

Front Panel Reference Voltage Access: An isolated BNC connector on the front panel allows access to the internal reference voltage.

Front panel access to the corresponding reference voltage adjustment is provided.

Calibration: When autocalibration is initiated, either by a system reset or software command, an embedded DSP loads calibration output values into each of the output DACs which are read back into the DSP through a 16-bit ADC. This is repeated until a sufficient number of calibration points have been measured. A calibration table consisting of offset and gain corrections for each of the 32 outputs in each of the 6 voltage ranges is compiled and stored in RAM. These correction factors are recalled each time an output is changed.

System Reset: After a system reset, all outputs are in the offline mode, all Control Registers are in their default state, self-test is initiated, and autocalibration is initiated.

VMEbus Compliance: This board complies with the VMEbus specification (ANSI/IEEE STD 1014-1987 IEC 821 and 297) with the following mnemonics:

Addressing Mode	Responding Address Modifiers
A32	$09 (Extended nonprivileged data access) or $0D (Extended supervisory data access)
A24	$39 (Standard nonprivileged data access) or $3D (Standard supervisory data access)
A16	$29 (Short nonprivileged I/O access) or $2D (Short supervisory I/O access)
Data Accesses:	D16, D08(EO)

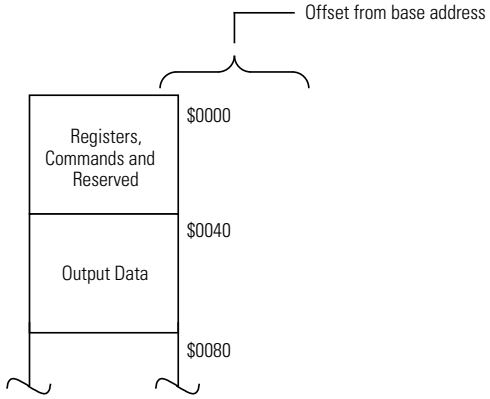
Board Address: The base VMEbus address is set by configuration of a jumper field. A jumper exists for each of the addresses A31 through A7; the address space occupied by this board is 128 consecutive bytes.

VMEbus Access: Address modifier bits are jumper selected and decoded to support nonprivileged, supervisory, and either nonprivileged or supervisory board accesses.

Output Data Transfer: Output data is stored in 32 16-bit registers. The board can be software configured to accept either two's complement or offset binary data.

Output change may be initiated by register access, however, outputs are double buffered which allows all channels to be synchronously updated by either a software or external trigger.

Address Map:



Electrical Characteristics

(At +25 °C and rated power supplies unless otherwise noted.)

Outputs: Thirty-two or sixteen single-ended; one DAC per channel

Full-Scale Output: ±10 V, ±5 V, ±2.5 V, 0 to +2.5 V, 0 to +5 V, 0 to +10 V (software selectable)

Output Code: Each 12-bit DAC accepts digital codes in offset binary or two's complement (software selectable)

Resolution: 12 bits

Output Impedance: < 0.8 Ω, online
> 10 MΩ, offline

Output Current: ±10 mA, over the entire output voltage range

Output Short Circuit Protection: Indefinite short-to-common; transient overvoltage protected to ±25 V (for one second)

Transfer Characteristics

Transfer Function:

$$E_{OUT} = E_{OUT\,MIN} + \left(\frac{N_{DATA}}{4{,}096} \times E_{SPAN}\right)$$

Where:

E_{OUT} = Channel output voltage

E_{OUTMIN} = Negative end of range

N_{DATA} = Channel data from VMEbus

E_{SPAN} = Positive end of range minus negative end of range

Example: for the ±5 V range:

$$E_{OUT} = -5\ V + \left(\frac{N_{DATA}}{4{,}096} \times 10\ V\right)$$

Differential Nonlinearity: 0.030 percent SPAN, maximum. Monotonic over the operating temperature range.

Integral Nonlinearity: 0.030 percent SPAN, maximum (referenced to best fit straight line)

Accuracy, Initial[1]**:** Maximum error at +25 °C:

±0.03 percent setting ±0.025 percent SPAN ±1.5 mV

Gain error — Offset error

Example: for a setting of +2.000 V on the ±5 V range:

Max Error = (±0.03% x 2.000 V) ± (0.025% x 10 V) ±1.5

= ±0.6 mV ± 2.5 mV ± 1.5

= ±4.6 mV

Accuracy Stability

Temperature Effect: ±35 ppm setting ±25 ppm SPAN ±30 µV, maximum drift per °C

Long Term: ±45 ppm setting ±30 ppm SPAN ±50 µV, maximum drift per 1,000 hr

Interchannel Crosstalk Rejection: 70 dB minimum, DC - 1 kHz

Output Noise[2]**:**

4 mV p-p maximum at 3σ (10 Hz to 10 kHz)

30 mV p-p maximum at 3σ (10 Hz to 20 MHz)

Transition Impulse: 5 µV-s, maximum spike during data transition

BIT Switch Impulse: 1 µV-s, maximum spike during channel change

Settling Time (0.01 Percent):

18 µs, step = 100 percent SPAN

12 µs, step = 50 percent SPAN

Access Time[3]

Write Access Time: 500 ns maximum at data transfer rates less than 200 kHz

Maximum Sustainable VMEbus Data Transfer Rate: 200 kHz, minimum

Physical/Environmental Specifications

External Trigger[4]**:**

Polarity	Programmable
Level	TTL, VIH = 2.0 V; VIL = 0.8 V
Pulse Width	1 µs, minimum

Dimensions: 6U single slot Eurocard form factor

Height	9.2 in. (233.4 mm)
Depth	6.3 in. (160 mm)
Thickness	0.8 in. (20.3 mm)

Weight (Mass): 0.7 kgm maximum

Temperature: 0 to +65 °C, operating

-25 to +85 °C, storage

Relative Humidity: 20% to 80%, noncondensing

Cooling: Normal VMEbus chassis forced air circulation

1 Initial accuracy is established when the board is channel-calibrated directly after reference calibration.

2 Output noise is specified at 3s standard deviations, which includes 99.7 percent of all noise peaks for a normal distribution. Glitch (transition) and BIT-switching noise is not included.

3 Access time is specified as the delay from active Data Strobes to DTACK.

4 May be accessed from a front panel BNC connector or from the VMEbus P2 connector.

Power Requirements: +5 VDC at 4.0 A maximum; outputs fully loaded

Altitude: Operation to 3,000 m

MTBF: 107,400 hours (217F)

Trademarks

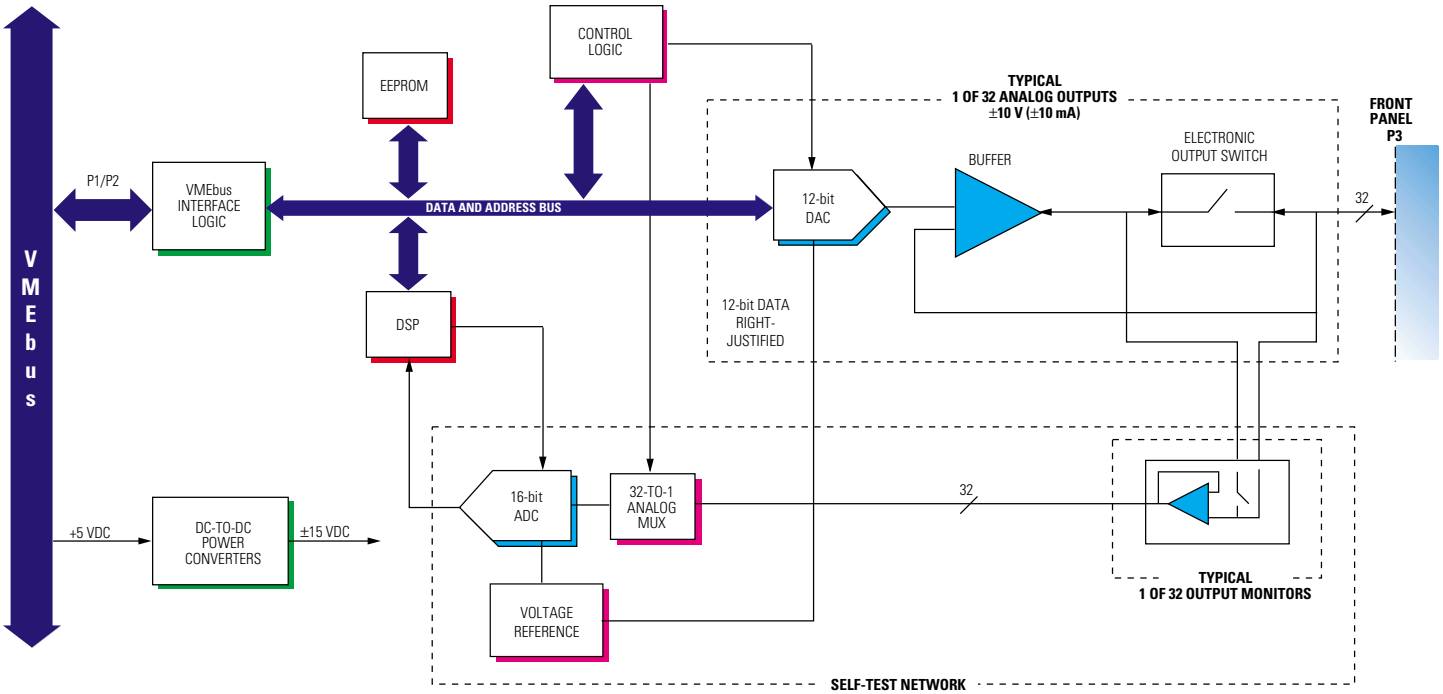


Figure 1. VMIVME-4140 Functional Block Diagram

GE Fanuc Embedded Systems Information Centers

USA and the Americas:

Huntsville, AL	*1 800 322-3616*
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Additional Resources

For more information, please visit the GE Fanuc Embedded Systems web site at:

www.gefanuc.com/embedded