

# **VMIVME-4150**

## **Isolated 12-Channel 12-bit Analog Output Board with Voltage or Current Loop Outputs**

### **Product Manual**



*A GE Fanuc Company*

12090 South Memorial Parkway  
Huntsville, Alabama 35803-3308, USA

(256) 880-0444 ♦ (800) 322-3616 ♦ Fax: (256) 882-0859

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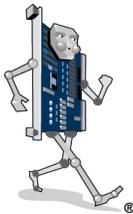
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# Table of Contents

<b>List of Figures</b> .....	7
<b>List of Tables</b> .....	9
<b>Overview</b> .....	11
Features .....	11
Functional Description .....	12
References .....	13
Physical Description and Specification .....	13
Safety Summary .....	14
Warnings, Cautions and Notes .....	15
<b>Chapter 1 - Theory of Operation</b> .....	17
Internal Functional Organization .....	18
VMEbus Interface .....	18
Channel Control .....	18
Analog Output Channels .....	21
Isolation .....	21
Digital/Analog Conversion .....	21
Voltage and Current Outputs .....	21
DC/DC Power Converters .....	23
<b>Chapter 2 - Configuration and Installation</b> .....	25
Unpacking Procedures .....	26
Before Applying Power: Checklist .....	26
Operational Configuration .....	27
Bipolar Voltage Outputs .....	30
Unipolar Voltage Outputs .....	31

Current Loop Output . . . . .	32
Address Modifiers . . . . .	33
Address Selection . . . . .	34
Calibration . . . . .	35
Equipment Required . . . . .	35
Analog Outputs Calibration Procedure . . . . .	36
Bipolar Voltage Outputs . . . . .	36
Unipolar Voltage Outputs . . . . .	37
Current Outputs. . . . .	37
I/O Cable and Front Panel Connector Configuration. . . . .	38
<b>Chapter 3 - PROGRAMMING . . . . .</b>	<b>41</b>
Board Identification Register . . . . .	42
Board Address and Access Privilege . . . . .	43
Control and Status Register (CSR) . . . . .	44
Reset Operations. . . . .	46
Control of Analog Outputs . . . . .	47
Output Registers and Data Format . . . . .	47
Scaling and Enabling . . . . .	47
Output Load Cycles. . . . .	47
<b>Chapter 4 - Maintenance . . . . .</b>	<b>49</b>
Maintenance . . . . .	49
Maintenance Prints . . . . .	50

# List of Figures

- Figure 1-1 VMEbus Interface and Control ..... 19
- Figure 1-2 Channel Control ..... 20
- Figure 1-3 VMIVME-4150 Output Timing (Typical Channel) ..... 20
- Figure 1-4 Isolated Output Channel ..... 22
- Figure 2-1 Location of Potentiometers and Jumpers ..... 29
- Figure 2-2 Address Modifier Jumper E15 Configuration ..... 33
- Figure 2-3 Base Address Select Jumpers E13, E14 and E16 ..... 34
- Figure 2-4 P3/P4 Connector Pin Layout ..... 38



# List of Tables

Table 2-1	VMIVME-4150 Jumper Locations and Functions .....	27
Table 2-2	Jumper Functions for Bipolar Voltage Outputs .....	30
Table 2-3	Unipolar Jumper Functions .....	31
Table 2-4	Current Loop Output Jumper Functions .....	32
Table 2-5	Bipolar Voltage Output Calibration Values .....	36
Table 2-6	Unipolar Voltage Output Calibration Values .....	37
Table 2-7	Current Output Calibration Values .....	37
Table 2-8	P3 Pin Assignments .....	39
Table 2-9	P4 Pin Assignments .....	40
Table 3-1	VMIVME-4150 Board Register Map .....	41
Table 3-2	VMIVME-4150 Control and Status Register (CSR) Bitmap .....	44
Table 3-3	Control/Status Register Functions .....	45



# Overview

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## Introduction

### Features

The VMIVME-4150 is a 12-bit Analog Output Board which provides 12 isolated high quality 12-bit analog output channels on a single 6U form factor VMEbus board. Each channel is electrically isolated from all other channels and from the VMEbus. Listed below are some features of the VMIVME-4150 :

- 12 fully isolated analog outputs
- 1,000 Vpk isolation, channel-to-channel and channel-to-bus
- 12-bit resolution
- Bipolar voltage output ranges selectable as  $\pm 2.5$ ,  $\pm 5$ , or  $\pm 10$  V
- Unipolar voltage output ranges selectable as 0 to 2.5 V, 0 to 5 V, or 0 to 10 V
- 10 mA load capacity for voltage outputs over full  $\pm 10$  V range
- Available with 4 to 20, 0 to 20, or 5 to 25 mA current loop outputs
- 0.05 percent accuracy for voltage outputs, 0.08 percent for current loop outputs
- 4, 8, or 12-channel configurations
- Optical data coupling provides full galvanic isolation
- Static readback data registers simplify program control
- Front panel access for field connections
- Program-controlled connect/disconnect operation of voltage outputs facilitates system testing

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## Functional Description

The VMIVME-4150 internal organization is illustrated in the functional block diagram shown in Figure 1.2-1. The board will operate with sustained isolation voltages as high as 1,000 Vpk. Bipolar output voltage ranges are selectable as  $\pm 2.5$ ,  $\pm 5$ , or  $\pm 10$  V. Unipolar output voltage ranges are selectable as 0 to 2.5 V, 0 to 5 V, or 0 to 10 V, and full 10 mA loading is supported throughout these ranges. 4, 8, or 12 channel configurations are available.

Voltage outputs may be disconnected under program control during system testing, and are disconnected automatically during reset. Optional current-mode outputs support applications that require standard 4 to 20, 0 to 20, or 5 to 25 mA analog current loops. Compliance of the current mode outputs is 9 V if the loop supply originates on the board, or 27 V with an external loop power supply. A front panel LED (Fail) is provided. The LED light is on during system reset and can be turned OFF under user software control.

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## References

For a detailed description and specification of the VMEbus, please refer to:

***VMEbus Specification Rev. C. and the VMEbus Handbook***

VMEbus International Trade Assoc. (VITA)

7825 East Gelding Dr.

Suite 104

Scottsdale, AZ 85260

(602) 951-8866

(602) 951-0720 (FAX)

[www.vita.com](http://www.vita.com)

## Physical Description and Specification

Refer to VMIC's Specification No. 800-004150-000 for detailed specifications.

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## Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

### Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

### Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

### Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

### Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

### Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

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**WARNING:** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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## **Warnings, Cautions and Notes**

**STOP** informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

**WARNING** denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION** denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE** denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.



# *Theory of Operation*

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## **Introduction**

Optical data coupling, serial data transfers, and isolated D/A converters are used to produce twelve galvanically isolated analog output channels. Each channel contains a serial 12-bit Digital-to-Analog (D/A) converter which generates a signal voltage in response to commands from the VMEbus. The D/A converter voltage then drives an output module which is factory configured for a specific voltage or current output option. Power for each channel is supplied as  $\pm 15$  VDC by an isolated DC/DC converter. A functional block diagram of the VMIVME-4150 board is shown in Figure 1-1 on page 19.

## Internal Functional Organization

The VMIVME-4150 board consists of the following functional elements, all of which are described in the following sections:

- VMEbus interface
- Channel control
- Isolated analog outputs
- DC/DC power converters.

### VMEbus Interface

Communications with the VMEbus is controlled with a single Electrically Programmable Logic Device (EPLD), as shown in Figure 1-1 on page 19. Data and control registers are distributed among three Channel-Control EPLD's. The control-logic EPLD responds to data transfer requests from the VMEbus, and directs the flow of data between the bus and the internal data and control registers. Data Transfer Acknowledge (DTACK\*) is generated when a transfer from the bus has been completed, or when data is ready to be transferred to the bus. Transfers proceed normally if address pipelining is present, but the board will respond only to the first address in the pipeline sequence. The VMEbus interface logic will not respond to transfer requests in which the BERR\*, DTACK\*, LWORD\*, or IACK\* control line is asserted.

### Channel Control

Control of data transfer to the output D/A converters is partitioned into three identical 4-channel groups, with a single EPLD assigned to each group. This method of partitioning permits the board to be populated with only those devices required to support the 4, 8, or 12-channel optional configuration.

As shown in Figure 1-1 on page 19, the EPLD which controls channels 00 through 03 also contains the Board Identification Register (BIR) and part of the Control/Status register (CSR). This EPLD detects the presence of one or both of the other two channel-control EPLD's, and adjusts the distribution of the CSR accordingly.

Each channel-control EPLD contains four data registers which receive the channel data words from the VMEbus, and provides an independent data serializer for each channel. Figure 1-2 on page 20 illustrates the movement of data within a single control channel. A data transfer to any 16-bit channel data register from the bus initiates the serializing process which moves the data to the serial output D/A converter. Data in each register is right-justified with 12 significant bits.

Only the 12 significant data bits in each channel are serialized for transfer to the associated D/A converter. The three digital signals required to produce the transfer are shown in Figure 1-3 on page 20. The board selection (BDSEL L) initiates the transfer sequence. The CLOCK line provides the primary timing, and clocks the information present on the DATA line into the serial D/A converter, MSB first through LSB last. The output of the converter does not change during the serial transfer. When the serial transfer has been completed, the LOAD signal performs a parallel transfer of data to an output latch in the converter, and the output voltage responds to the new data.

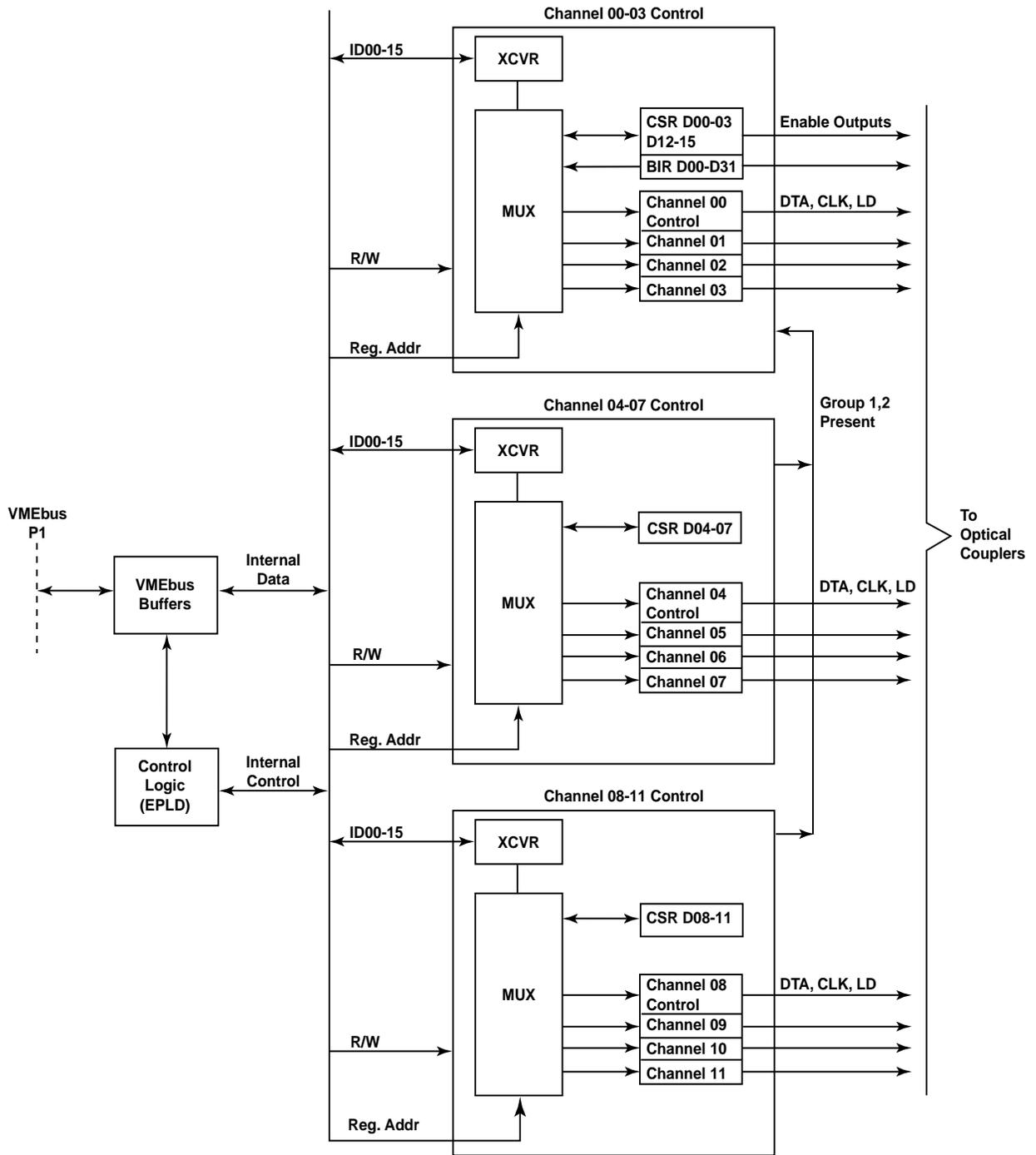


Figure 1-1 VMEbus Interface and Control

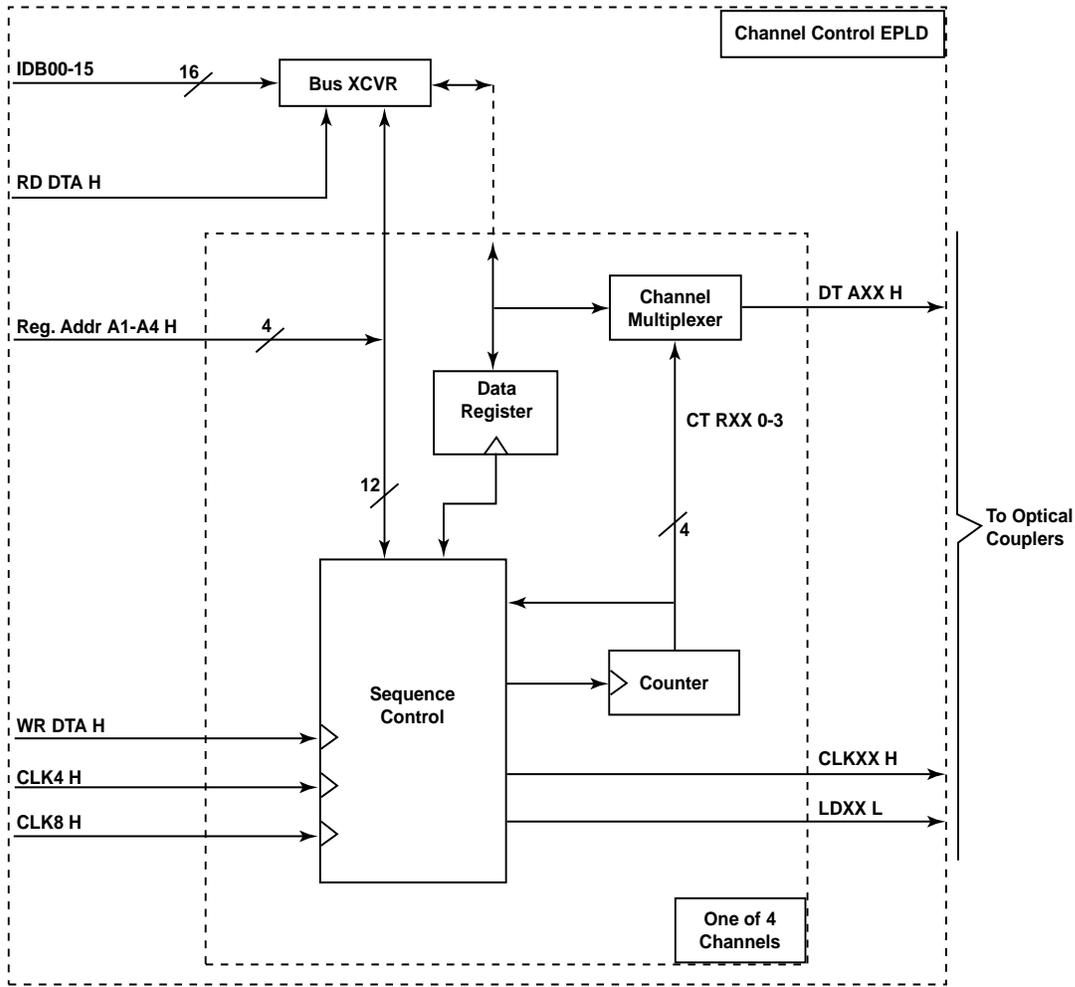


Figure 1-2 Channel Control

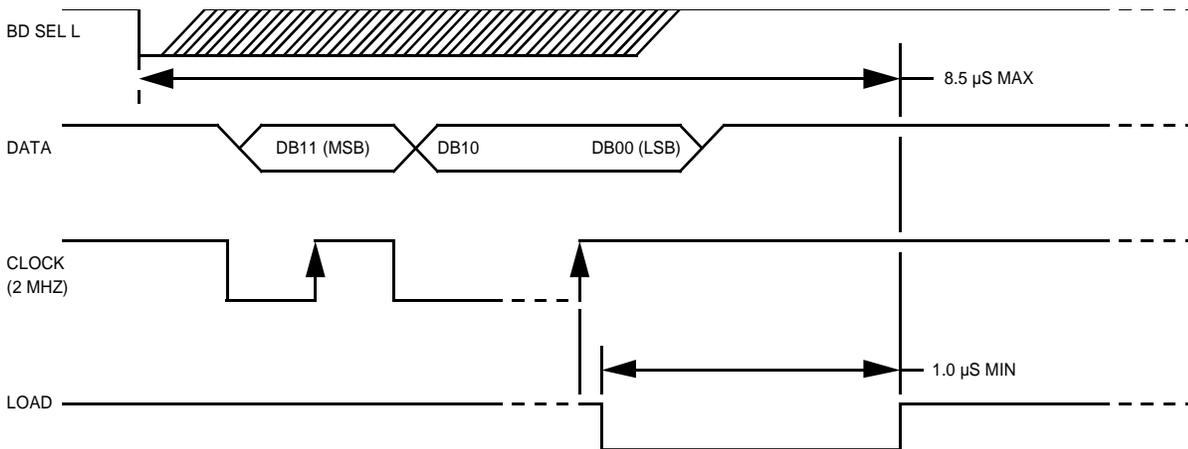


Figure 1-3 VMIVME-4150 Output Timing (Typical Channel)

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## Analog Output Channels

### Isolation

Each output channel is isolated from the VMEbus and from all other channels by an isolated DC/DC converter and by four optical couplers. The DC/DC converter provides isolated  $\pm 15$  VDC power for the channel, and the optical couplers isolate the digital control signals IDTA, ICLK, ILD, and IENA from EPLD signals DATA, CLOCK, LOAD, and ENAOUT (Figure 1-4 on page 22). Power for the optical couplers is supplied as +5 VDC, and is series regulated from the isolated +15 V rail.

### Digital/Analog Conversion

A serial Digital to Analog (D/A) converter receives the 12-bit data word from the channel control EPLD, and produces an output voltage range that is jumper controlled as zero to -2.5 V, -5 V, or -10 V. The D/A buffer converts these ranges into the output ranges specified in the output ordering option for voltage outputs, or to zero to +10 V for current outputs. Channel span is adjusted in the feedback loop of the D/A buffer.

The voltage reference level is selected as +2.5 V, +5 V, or +10 V by the output module. A current output module automatically selects a +10 V reference. A voltage output module passes the state of the module control jumpers directly to the reference, and permits any of the three voltages to be selected.

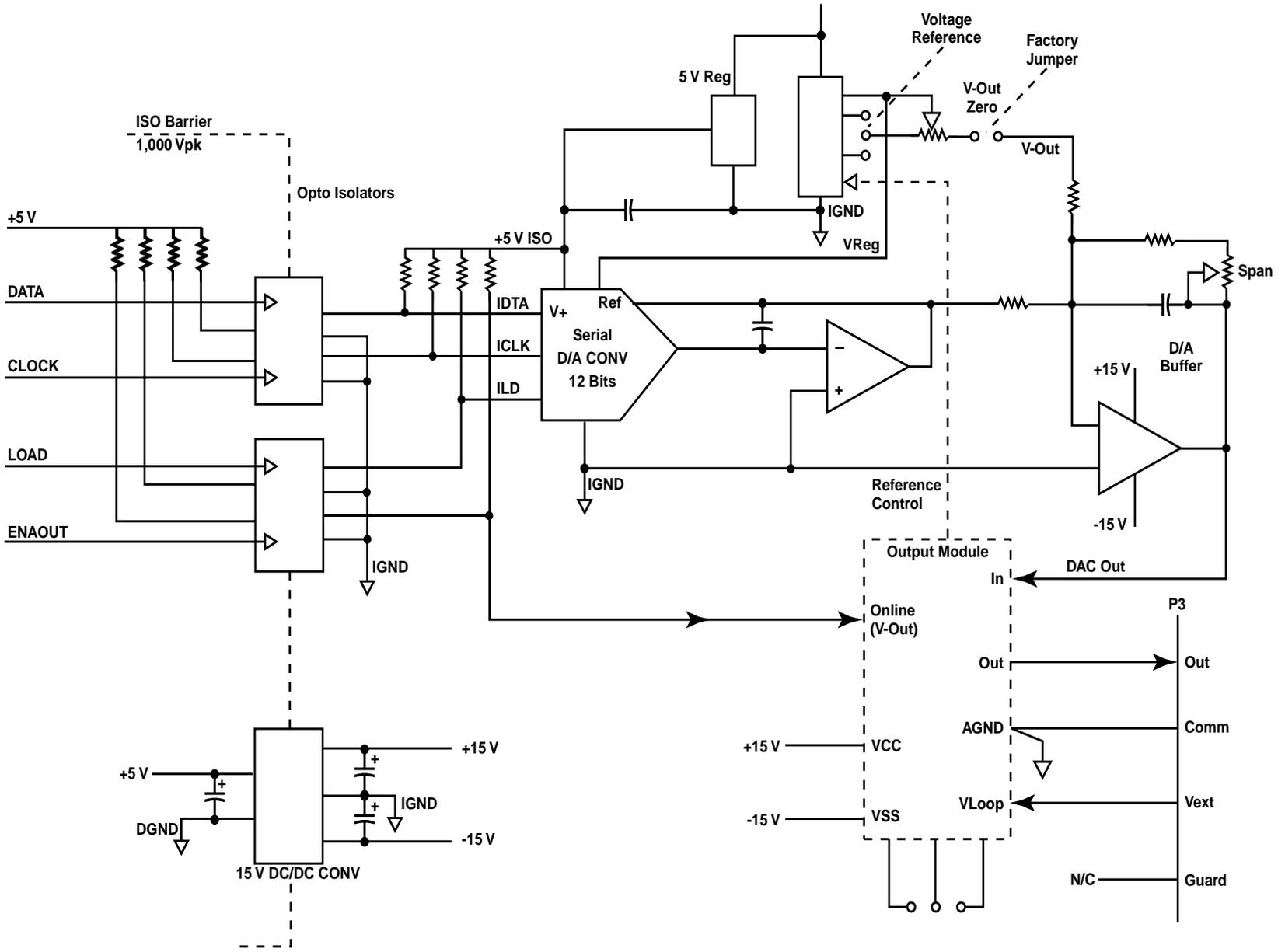
### Voltage and Current Outputs

All outputs are factory-configured for either unipolar voltage, bipolar voltage, or constant current. Each module contains an offset potentiometer to permit adjustment of the channel offset error to zero.

A voltage output module consists of a unity gain buffer and an output switch. The buffer provides the output drive capability necessary to support 10 mA loads over the maximum output range of  $\pm 10$  V. The switch provides the on-line/off-line field disconnect feature, and is controlled by the ENAOUT digital signal. The output switch is located in the feedback loop of the buffer, and consequently does not contribute significantly to the final output resistance of  $0.5 \Omega$ . Jumpers which are connected to the voltage module permit selection of any of the three available reference voltages.

The current output module contains a voltage-to-current converter and a pass transistor. The module is factory-jumpered to provide the specified output current range with a voltage range from the D/A converter of zero to +10 V. The pass transistor boosts the current output capability to the maximum level necessary to support the specified output current range. The jumpers which are connected to the module are used to select the source of loop power either as the internal isolated +15 V rail, or as an external supply which can provide a loop voltage up to +30 V.

Figure 1-4 Isolated Output Channel



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## **DC/DC Power Converters**

Each channel contains a single DC/DC converter (Figure 1-4 on page 22) which derives isolated  $\pm 15$  VDC power from the VMEbus +5 VDC power bus, and is packaged in a 24-pin dual-in-line module. The isolated  $\pm 15$  VDC outputs from the converter supply all power required for the isolated section of the channel, including the optical isolators, the DAC, and the output module.



# ***Configuration and Installation***

## **Contents**

Unpacking Procedures ..... 26  
Operational Configuration ..... 27  
Calibration ..... 35  
Analog Outputs Calibration Procedure ..... 36  
I/O Cable and Front Panel Connector Configuration ..... 38

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## Unpacking Procedures

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**CAUTION:** Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

---

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

## Physical Installation

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**NOTE:** Do not install or remove board while power is applied.

---

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

## Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming, Chapter 1 and 3, been reviewed and applied to system requirements.
2. Review *Operational Configuration* section on page 27 and Table 2-2 on page 30 to verify that all factory-installed jumpers are in place. To change the *board address* or *address modifier* response, refer to *Operational Configuration* section on page 27.
3. Have the I/O cables, with the proper mating connectors, been connected to the input/output connectors? Refer to *I/O Cable and Front Panel Connector Configuration* section on page 38 for connector descriptions.
4. Calibration has been performed at the factory. If recalibration is required, refer to *Analog Outputs Calibration Procedure* section on page 36.

After the checklist above has been completed, the board can be installed in a VMEbus system. This board can be installed in any slot position, with the exception of slot-one which is usually reserved for the master processing unit.

## Operational Configuration

Control of the VMIVME-4150 board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on-board performance. The locations and functions of all VMIVME-4150 jumpers are shown in Figure 2-1 on page 29 and are summarized in Table 2-2 on page 30. The function of the output range select jumpers are option dependent and will be discussed in detail in *Bipolar Voltage Outputs* section on page 30, *Unipolar Voltage Outputs* section on page 31 and *Current Loop Output* section on page 32.

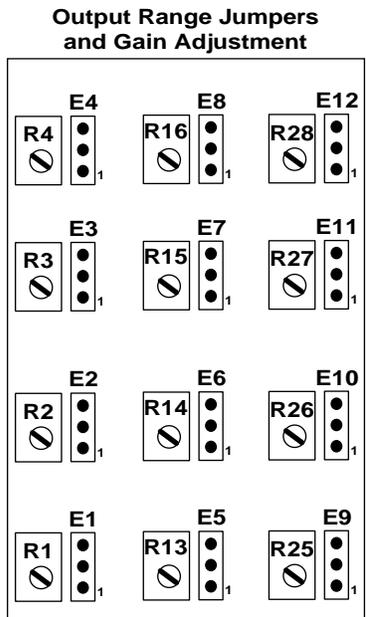
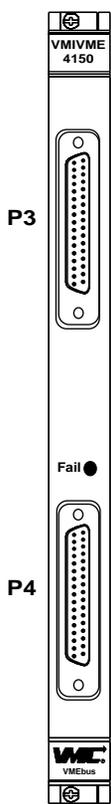
**Table 2-1** VMIVME-4150 Jumper Locations and Functions

Jumper ID	Function	Alterable	Factory Configuration
E15-1,2	Supervisory Only	Yes	Installed
E15-3,4	Nonprivileged Only	Yes	Omitted
E15-5,6	Short I/O	Yes	Installed
E16-1,2	Memory Address Bit A5=0	Yes	Installed
E16-3,4	Memory Address Bit A6=0	Yes	Installed
E16-5,6	Memory Address Bit A7=0	Yes	Installed
E13-1,2	Memory Address Bit A8=0	Yes	Installed
E13-3,4	Memory Address Bit A9=0	Yes	Installed
E13-5,6	Memory Address Bit A10=0	Yes	Installed
E13-7,8	Memory Address Bit A11=0	Yes	Installed
E13-9,10	Memory Address Bit A12=0	Yes	Installed
E13-11,12	Memory Address Bit A13=0	Yes	Installed
E13-13,14	Memory Address Bit A14=0	Yes	Installed
E13-15,16	Memory Address Bit A15=0	Yes	Installed
E14-1,2	Memory Address Bit A16=0	Yes	Installed
E14-3,4	Memory Address Bit A17=0	Yes	Installed
E14-5,6	Memory Address Bit A18=0	Yes	Installed
E14-7,8	Memory Address Bit A19=0	Yes	Installed
E14-9,10	Memory Address Bit A20=0	Yes	Installed
E14-11,12	Memory Address Bit A21=0	Yes	Installed
E14-13,14	Memory Address Bit A22=0	Yes	Installed
E14-15,16	Memory Address Bit A23=0	Yes	Installed
E1-1,2	Channel 9 Output Range Sel	Yes	*Installed
E1-2,3	Channel 9 Output Range Sel	Yes	Omitted
E2-1,2	Channel 6 Output Range Sel	Yes	*Installed
E2-2,3	Channel 6 Output Range Sel	Yes	Omitted
E3-1,2	Channel 3 Output Range Sel	Yes	*Installed
E3-2,3	Channel 3 Output Range Sel	Yes	Omitted
E4-1,2	Channel 0 Output Range Sel	Yes	*Installed

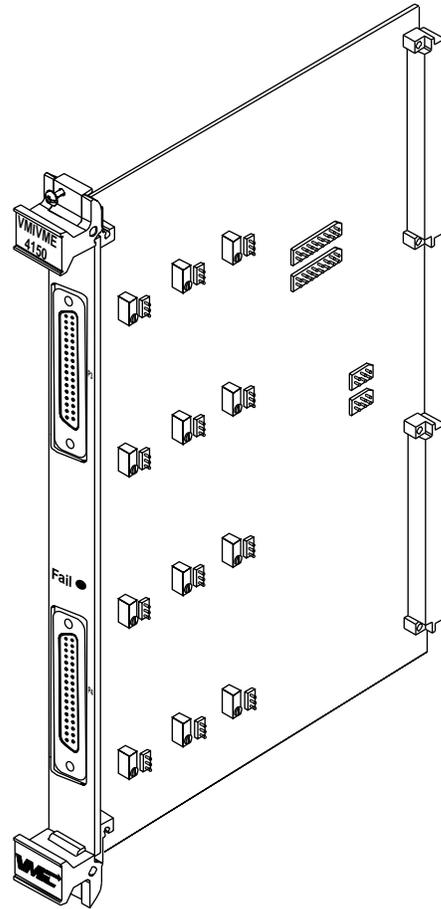
**Table 2-1** VMIVME-4150 Jumper Locations and Functions (Continued)

Jumper ID	Function	Alterable	Factory Configuration
E4-2,3	Channel 0 Output Range Sel	Yes	Omitted
E5-1,2	Channel 10 Output Range Sel	Yes	*Installed
E5-2,3	Channel 10 Output Range Sel	Yes	Omitted
E6-1,2	Channel 7 Output Range Sel	Yes	*Installed
E6-2,3	Channel 7 Output Range Sel	Yes	Omitted
E7-1,2	Channel 4 Output Range Sel	Yes	*Installed
E7-2,3	Channel 4 Output Range Sel	Yes	Omitted
E8-1,2	Channel 1 Output Range Sel	Yes	*Installed
E8-2,3	Channel 1 Output Range Sel	Yes	Omitted
E9-1,2	Channel 11 Output Range Sel	Yes	*Installed
E9-2,3	Channel 11 Output Range Sel	Yes	Omitted
E10-1,2	Channel 8 Output Range Sel	Yes	*Installed
E10-2,3	Channel 8 Output Range Sel	Yes	Omitted
E11-1,2	Channel 5 Output Range Sel	Yes	*Installed
E11-2,3	Channel 5 Output Range Sel	Yes	Omitted
E12-1,2	Channel 2 Output Range Sel	Yes	*Installed
E12-2,3	Channel 2 Output Range Sel	Yes	Omitted
<b>NOTE:</b> *Omitted for options 000, 100, 040, 140, and 240			

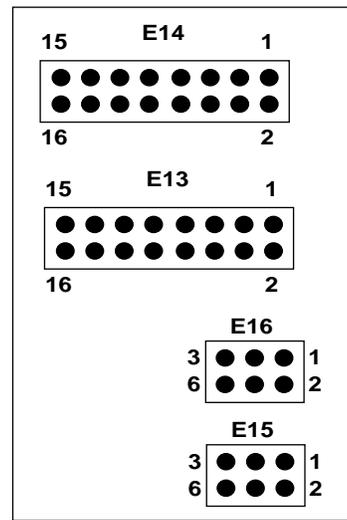
Figure 2-1 Location of Potentiometers and Jumpers



**VMIVME-4150 User Configurable Jumpers and Potentiometers**



E13, E14 and E16 are the Base Address Select Jumpers. E15 is the Address Modifier Jumper.



## Bipolar Voltage Outputs

The VMIVME-4150 provides (if option ordered) Bipolar Voltage Outputs for 4, 8, or 12 channels. The channel can be configured via user-installed jumpers for 2.5 V, 5 V, or 10 V. Table 2-2 below describes the jumper functions for this mode, along with the designators for the adjustment pots associated with each channel.

**Table 2-2** Jumper Functions for Bipolar Voltage Outputs

Channel**	Output Range Jumper	Voltage	Gain Adj	Zero Adj
0	E4-1,2	2.5 V	R4	U8 POT
0	E4-2,3	5 V	R4	U8 POT
0	E4- OPEN	10 V	R4	U8 POT
1	E8-1,2	2.5 V	R16	U36 POT
1	E8-2,3	5 V	R16	U36 POT
1	E8- OPEN	10 V	R16	U36 POT
2	E12-1,2	2.5 V	R28	U64 POT
2	E12-2,3	5 V	R28	U64 POT
2	E12- OPEN	10 V	R28	U64 POT
3	E3-1,2	2.5 V	R3	U7 POT
3	E3-2,3	5 V	R3	U7 POT
3	E3- OPEN	10 V	R3	U7 POT
4	E7-1,2	2.5 V	R15	U34 POT
4	E7-2,3	5 V	R15	U34 POT
4	E7- OPEN	10 V	R15	U34 POT
5	E11-1,2	2.5 V	R27	U62 POT
5	E11-2,3	5 V	R27	U62 POT
5	E11- OPEN	10 V	R27	U62 POT
6	E2-1,2	2.5 V	R2	U6 POT
6	E2-2,3	5 V	R2	U6 POT
6	E2- OPEN	10 V	R2	U6 POT
7	E6-1,2	2.5 V	R14	U32 POT
7	E6-2,3	5 V	R14	U32 POT
7	E6- OPEN	10 V	R14	U32 POT
8	E10-1,2	2.5 V	R26	U60 POT
8	E10-2,3	5 V	R26	U60 POT
8	E10- OPEN	10 V	R26	U60 POT
9	E1-1,2	2.5 V	R1	U5 POT
9	E1-2,3	5 V	R1	U5 POT
9	E1- OPEN	10 V	R1	U5 POT
10	E13-1,2	2.5 V	R13	U30 POT
10	E13-2,3	5 V	R13	U30 POT
10	E13- OPEN	10 V	R13	U30 POT
11	E9-1,2	2.5 V	R25	U58 POT
11	E9-2,3	5 V	R25	U58 POT
11	E9- OPEN	10 V	R25	U58 POT

**NOTE:** \*\* Channels 0 Through 3 = VMIVME-4150-000  
Channels 0 Through 6 = VMIVME-4150-100  
Channels 0 Through 11= VMIVME-4150-200

## Unipolar Voltage Outputs

The VMIVME-4150 provides (if option ordered) Unipolar Voltage outputs for 4, 8, or 12 channels. The channel can be configured via user-installed jumpers for 0 to 2.5 V, 0 to 5 V, or 0 to 10 V. The Table 2-3 below describes the jumper functions for this mode, along with the associated gain and zero adjustment designator for each channel.

**Table 2-3** Unipolar Jumper Functions

Channel**	Output Range Jumper	Voltage	Gain Adj	Zero Adj
0	E4-1,2	0 to 2.5 V	R4	U8 POT
0	E4-2,3	0 to 5 V	R4	U8 POT
0	E4- OPEN	0 to 10 V	R4	U8 POT
1	E8-1,2	0 to 2.5 V	R16	U36 POT
1	E8-2,3	0 to 5 V	R16	U36 POT
1	E8- OPEN	0 to 10 V	R16	U36 POT
2	E12-1,2	0 to 2.5 V	R28	U64 POT
2	E12-2,3	0 to 5 V	R28	U64 POT
2	E12- OPEN	0 to 10 V	R28	U64 POT
3	E3-1,2	0 to 2.5 V	R3	U7 POT
3	E3-2,3	0 to 5 V	R3	U7 POT
3	E3- OPEN	0 to 10 V	R3	U7 POT
4	E7-1,2	0 to 2.5 V	R15	U34 POT
4	E7-2,3	0 to 5 V	R15	U34 POT
4	E7- OPEN	0 to 10 V	R15	U34 POT
5	E11-1,2	0 to 2.5 V	R27	U62 POT
5	E11-2,3	0 to 5 V	R27	U62 POT
5	E11- OPEN	0 to 10 V	R27	U62 POT
6	E2-1,2	0 to 2.5 V	R2	U6 POT
6	E2-2,3	0 to 5 V	R2	U6 POT
6	E2- OPEN	0 to 10 V	R2	U6 POT
7	E6-1,2	0 to 2.5 V	R14	U32 POT
7	E6-2,3	0 to 5 V	R14	U32 POT
7	E6- OPEN	0 to 10 V	R14	U32 POT
8	E10-1,2	0 to 2.5 V	R26	U60 POT
8	E10-2,3	0 to 5 V	R26	U60 POT
8	E10- OPEN	0 to 10 V	R26	U60 POT
9	E1-1,2	0 to 2.5 V	R1	U5 POT
9	E1-2,3	0 to 5 V	R1	U5 POT
9	E1- OPEN	0 to 10 V	R1	U5 POT
10	E13-1,2	0 to 2.5 V	R13	U30 POT
10	E13-2,3	0 to 5 V	R13	U30 POT
10	E13- OPEN	0 to 10 V	R13	U30 POT
11	E9-1,2	0 to 2.5 V	R25	U58 POT
11	E9-2,3	0 to 5 V	R25	U58 POT
11	E9- OPEN	0 to 10 V	R25	U58 POT

**NOTE:** \*\* Channels 0 Through 3 = VMIVME-4150-040  
Channels 0 Through 6 = VMIVME-4150-140  
Channels 0 Through 11 = VMIVME-4150-240

## Current Loop Output

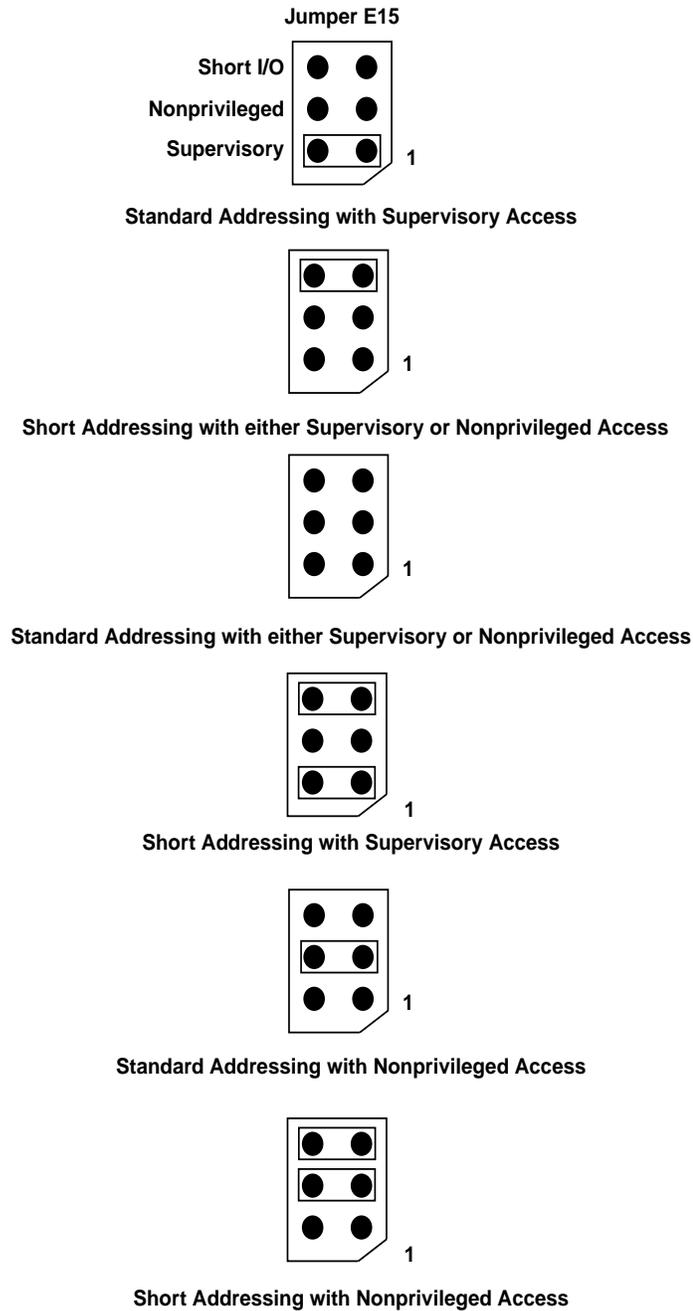
The VMIVME-4150 provides (if option ordered) a Current Loop Output for 4, 8, or 12 channels. A 15 V loop power supply is provided on the board. 30 volts can be supplied with an external loop power supply. A jumper is provided for each channel to configure the internal or external power supply as shown in Table 2-4 below.

**Table 2-4** Current Loop Output Jumper Functions

Channel**	Jumper	Loop Supply	Gain Adj	Zero Adj
0	E4-1,2	Internal	R4	U8 POT
0	E4-2,3	External	R4	U8 POT
1	E8-1,2	Internal	R16	U36 POT
1	E8-2,3	External	R16	U36 POT
2	E12-1,2	Internal	R28	U64 POT
2	E12-2,3	External	R28	U64 POT
3	E3-1,2	Internal	R3	U7 POT
3	E3-2,3	External	R3	U7 POT
4	E7-1,2	Internal	R15	U34 POT
4	E7-2,3	External	R15	U34 POT
5	E11-1,2	Internal	R27	U62 POT
5	E11-2,3	External	R27	U62 POT
6	E2-1,2	Internal	R2	U6 POT
6	E2-2,3	External	R2	U6 POT
7	E6-1,2	Internal	R14	U32 POT
7	E6-2,3	External	R14	U32 POT
8	E10-1,2	Internal	R26	U60 POT
8	E10-2,3	External	R26	U60 POT
9	E1-1,2	Internal	R1	U5 POT
9	E1-2,3	External	R1	U5 POT
10	E13-1,2	Internal	R13	U30 POT
10	E13-2,3	External	R13	U30 POT
11	E9-1,2	Internal	R25	U58 POT
11	E9-2,3	External	R25	U58 POT
NOTE: ** Channels 0 Through 3 = VMIVME-4150-010, 020 or 0304 Channels 0 Through 6 = VMIVME-4150-110, 120 or 130 Channels 0 Through 11= VMIVME-4150-210, 220 or 230				

## Address Modifiers

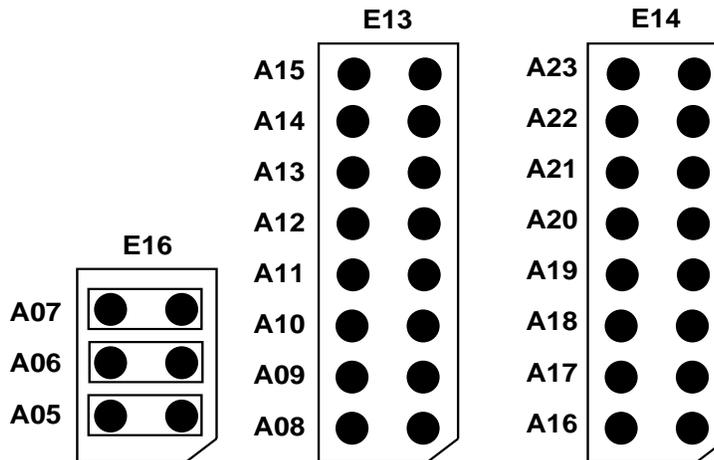
The VMIVME-4150 is factory configured to respond to either short supervisory or short nonprivileged access. Figure 2-2 below shows the configuration of the Address Modifier Jumper. The configuration can be changed by installing jumpers at the appropriate locations in the header as shown in the figure.



**Figure 2-2** Address Modifier Jumper E15 Configuration

## Address Selection

The VMIVME-4150 is designed with banks of Address Select Jumpers that specify the base address of the board. The Address Selection Jumpers are shown in Figure 2-3 below. The VMIVME-4150 is factory configured to respond to \$0000. An installed jumper causes the board to compare to a low address line, an omitted jumper causes the board to compare to a high address line.



The example shown is for a I/O base address of FF00 Hex (Short I/O Access) or FFFF00 (Standard I/O Access)

Figure 2-3 Base Address Select Jumpers E13, E14 and E16

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## Calibration

Before delivery from the factory, the VMIVME-4150 board is fully calibrated. Should recalibration be required however, refer to *Bipolar Voltage Outputs* section on page 30, *Unipolar Voltage Outputs* section on page 31 and *Current Loop Output* section on page 32 to perform the indicated calibration procedures in the order shown. Location of all adjustments are shown in Figure 2-1 on page 29. As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however all adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

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**NOTE:** The bipolar and unipolar voltage modules (option dependent) will be calibrated at FULLSCALE value for the maximum range, If the user configures the board for any range other than FULLSCALE (maximum range), calibration will be required.

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## Equipment Required

<b>Digital Multimeter:</b>	Voltage Measurements:  ±10 VDC range; 5 or more digits; ±0.005 percent of reading accuracy; 10 MΩ minimum input resistance.  Current Measurements:  0-100 mADC range; 5 or more digits; ±0.005 percent of reading accuracy; 100 Ω maximum input resistance.
<b>Cardcage:</b>	VMEbus 6U backplane or equivalent, with J1 and J2 connectors, 680x0-series controller, +5 ±0.2 VDC, 8 Amp (reserved current) power supply. One slot allocated for testing the VMIVME-4150 board.
<b>Extender Card:</b>	VMEbus 6U extender card
<b>Resistors:</b>	250 Ω ±5%, 1/4 watt (current outputs only) 1 kΩ ±5%, 1/4 watt

## Analog Outputs Calibration Procedure

1. See “Operational Configuration” on page 27, and configure the VMIVME-4150 board for the output configuration that is required for the application. For calibration of current outputs, configure the outputs for operation with the internal loop supply located on the board in a convenient location in the A16 or A24 system space.
2. Install the VMIVME-4150 board on an extender card in the VMEbus cardcage. Make provisions for connecting the DMM to each analog output channel, with the (+) common lead at the output pin and the (-) lead at the common pin. The channel output pins are defined in Table 2-8 on page 39 and Table 2-9 on page 40. Connect each common pin to the VMEbus digital ground through a 1.0 k $\Omega$  5% 1/4 watt resistor.
3. Apply power to the board. Write the value A000 (hex) to the CSR (refer to Table 3-1 on page 41 for the locations of all registers). All data transfers will be D16.
4. Allow a minimum warm-up interval of ten minutes before proceeding.
5. Proceed with *Bipolar Voltage Outputs* below, *Unipolar Voltage Outputs* section on page 31 or *Current Outputs* section on page 37. The locations of output modules and adjustment potentiometers are illustrated in Figure 2-1 on page 29.

### Bipolar Voltage Outputs

1. Connect the DMM to the Channel 00 output pins, with the (+) lead connected to the output pin and the (-) lead connected to the common pin.
2. Write the value \$0800 to the Channel 00 output data register. Adjust the ZERO potentiometer on the Channel 00 output module for a DMM indication that conforms to the MIDSCALE value contained in Table 2-5 below for the assigned output range.
3. Write the value \$0FFF to the Channel 00 output data register. Adjust the Channel 00 gain potentiometer for a DMM indication that conforms to the POSITIVE FULLSCALE value contained in Table 2-5 below for the assigned output range.
4. Write the value \$0000 to the Channel 00 output data register. If the DMM indication does not conform to the NEGATIVE FULLSCALE value contained in Table 2-5 below for the assigned output range, repeat steps (2), (3) and (4) until the measurements for all three steps are correct.
5. Repeat steps (1) through (4) for the remaining active output channels.
6. Bipolar calibration is completed. Remove power, remove all test connections.

**Table 2-5** Bipolar Voltage Output Calibration Values

Output Range	Output Value (VDC)		
	Midscale	Positive Fullscale	Negative Fullscale
$\pm 2.5$ VDC	0.0000 $\pm 0.0006$	+2.4988 $\pm 0.0006$	-2.5000 $\pm 0.008$
$\pm 5$ VDC	0.0000 $\pm 0.0010$	+4.9975 $\pm 0.0010$	-5.0000 $\pm 0.011$
$\pm 10$ VDC	0.0000 $\pm 0.0020$	+9.9951 $\pm 0.0020$	-10.0000 $\pm 0.018$

## Unipolar Voltage Outputs

1. Connect the DMM to the Channel 00 output pins, with the (+) lead connected to the output pin and the (-) lead connected to the common pin.
2. Write the value \$0000 to the Channel 00 output data register. Adjust the Channel 00 gain potentiometer for a DMM indication that conforms to the ZERO value contained in Table 2-6 below for the assigned output range.
3. Write the value \$0FFF to the Channel 00 output data register. If the DMM indication does not conform to the POSITIVE FULLSCALE value contained in Table 2-6 below for the assigned output range, repeat steps (2), (3), and (4) until the measurements for all three steps are correct.
4. Repeat steps (1) through (3) for the remaining active output channels.
5. Unipolar calibration is completed. Remove power, remove all test connections.

**Table 2-6** Unipolar Voltage Output Calibration Values

Output Range	Output Value (VDC)	
	Zero	Positive Fullscale
0 To +2.5 VDC	0.0000 ±0.0006	+2.4988 ±0.0015
0 To +5 VDC	0.0000 ±0.0010	+4.9975 ±0.0020
0 To +10 VDC	0.0000 ±0.0020	+9.9951 ±0.0040

## Current Outputs

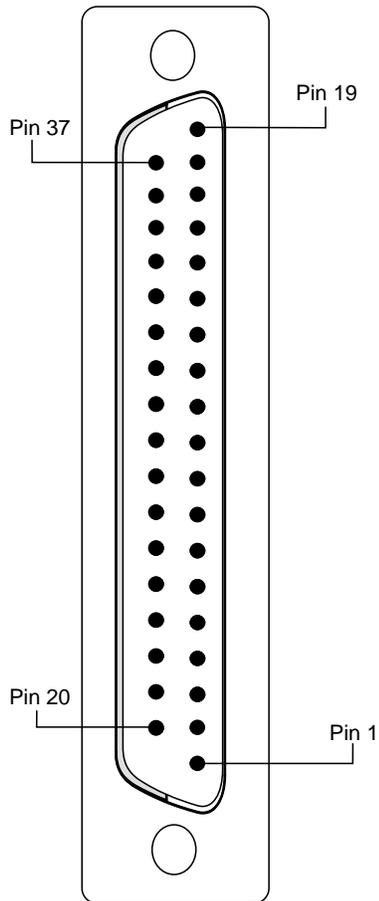
1. Connect the DMM to the Channel 00 output pins, with the (+) lead connected to the output pin through a series resistance of 250, and the (-) lead connected to the common pin. Leave the external loop supply pins (VEXT) disconnected.
2. Write the value \$0000 to the Channel 00 output data register. Adjust the ZERO potentiometer on the Channel-00 output module for a DMM indication that conforms to the ZERO SCALE value contained in Table 2-7 below for the assigned output range.
3. Write the value \$0FFF to the Channel 00 output data register. Adjust the Channel 00 gain potentiometer for a DMM indication that conforms to the FULLSCALE value contained in Table 2-7 below for the assigned output range.
4. Repeat steps (1) through (4) for the remaining active output channels.
5. Calibration is completed. Remove power, remove all test connections.

**Table 2-7** Current Output Calibration Values

Output Range (mADC)	Output Value (mADC)	
	Zero Scale	Fullscale
4 TO 20	4.000 ±0.004	20.000 ±0.008
0 TO 20	0.000 ±0.004	20.000 ±0.008
5 TO 25	5.000 ±0.004	25.000 ±0.008

## I/O Cable and Front Panel Connector Configuration

The front input connectors (P3 and P4) on the VMIVME-4150 are standard subminiature 37-pin female D-shell connectors. The P3/P4 connector pin layout is shown in Figure 2-4 below. The pin assignments for P3 and P4 are shown in Table 2-8 on page 39 and Table 2-9 on page 40.



**Figure 2-4** P3/P4 Connector Pin Layout

**Table 2-8** P3 Pin Assignments

<b>Pin</b>	<b>Data Bit</b>	<b>Pin</b>	<b>Data Bit</b>
19	OUT 0	37	COMM 0
18	VEXT 0	36	N/C
17	N/C	35	N/C
16	OUT 1	34	COMM 1
15	VEXT 1	33	N/C
14	N/C	32	N/C
13	OUT 2	31	COMM 2
12	VEXT 2	30	N/C
11	N/C	29	N/C
10	OUT 3	28	COMM 3
9	VEXT 3	27	N/C
8	N/C	26	N/C
7	OUT 4	25	COMM 4
6	VEXT 4	24	N/C
5	N/C	23	N/C
4	OUT 5	22	COMM 5
3	VEXT 5	21	N/C
2	N/C	20	N/C
1	N/C		

**Table 2-9** P4 Pin Assignments

<b>Pin</b>	<b>Data Bit</b>	<b>Pin</b>	<b>Data Bit</b>
19	OUT 6	37	COMM 6
18	VEXT 6	36	N/C
17	N/C	35	N/C
16	OUT 7	34	COMM 7
15	VEXT 7	33	N/C
14	N/C	32	N/C
13	OUT 8	31	COMM 8
12	VEXT 8	30	N/C
11	N/C	29	N/C
10	OUT 9	28	COMM 9
9	VEXT 9	27	N/C
8	N/C	26	N/C
7	OUT 10	25	COMM 10
6	VEXT 10	24	N/C
5	N/C	23	N/C
4	OUT 11	22	COMM 11
3	VEXT 11	21	N/C
2	N/C	20	N/C
1	N/C		

# PROGRAMMING

## Contents

Board Identification Register .....	42
Board Address and Access Privilege .....	43
Control and Status Register (CSR) .....	44
Reset Operations .....	46
Control of Analog Outputs .....	47

## Introduction

Communication with the VMIVME-4150 board is established through control, status, data and identification registers that are mapped into a 16-word block in either the A16 short I/O space or the standard A24 data space. All registers are listed in Table 3-1 below and described throughout this chapter.

Each of the twelve analog outputs is controlled through a dedicated 12-bit Output Data Register (ODR). Data is serialized and transferred to an output D/A converter when the associated ODR receives a data transfer from the bus. All channels operate independently.

**Table 3-1** VMIVME-4150 Board Register Map

Board Address (Hex)	Register Function	Designation	Access Mode
00	Board ID	BIR	Read Only
04	Control/Status	CSR	Read/Write
06	Reserved	...	
08	CH 00 Output Data	ODR 00	Read/Write
0A	CH 01 Output Data	ODR 01	Read/Write
0C	CH 02 Output Data	ODR 02	Read/Write
0E	CH 03 Output Data	ODR 03	Read/Write
10	CH 04 Output Data	ODR 04	Read/Write
12	CH 05 Output Data	ODR 05	Read/Write
14	CH 06 Output Data	ODR 06	Read/Write
16	CH 07 Output Data	ODR 07	Read/Write
18	CH 08 Output Data	ODR 08	Read/Write
1A	CH 09 Output Data	ODR 09	Read/Write
1C	CH 10 Output Data	ODR 10	Read/Write
1E	CH 11 Output Data	ODR 11	Read/Write

---

## **Board Identification Register**

The Board Identification register contains the board identification code (2200 0000 hex) for the VMIVME-4150 board, and occupies the first two words at the board base address.

---

## **Board Address and Access Privilege**

On-board programmable address jumpers permit the communication registers to be located on any 16-word boundary in either the A16 short I/O space or the A24 data space. Selection of A16 or A24 operation is jumper-controlled. Access privilege is jumper-selectable as supervisory mode, nonprivileged mode, or either mode.

## Control and Status Register (CSR)

Control and Status register functions and the bitmap are summarized in Table 3-2 below and Table 3-3 on page 45. Control register bits are mapped directly to the readback STATUS register at the same location. All CSR bits are cleared to zero (LOW) during a reset operation. The CSR provides control and monitoring of the following board functions:

- Output enabling (voltage outputs)
- Output load cycle status
- Data coding
- Self test LED.

**Table 3-2** VMIVME-4150 Control and Status Register (CSR) Bitmap

Relative Address \$04 Control/Status Register 0 (Read/Write)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
LED	Reserved	Output EN	Two's CMPL	CH 11 Busy	CH 10 Busy	CH 09 Busy	CH 08 Busy

Relative Address \$05 Control/Status Register 1 (Read/Write)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH 07 Busy	CH 06 Busy	CH 05 Busy	CH 04 Busy	CH 03 Busy	CH 02 Busy	CH 01 Busy	CH 00 Busy

Table 3-3 Control/Status Register Functions

Control/Status Register	Name	Function
D00	Channel 00 Busy	The Channel Busy flag is set when the associated channel output data register receives a data transfer from the bus, and remains set for approximately 8 $\mu$ s while the data word is transferred to the output D/A converter. A channel register should not be updated from the bus while the associated busy flag is set.
D01	Channel 01 Busy	
D02	Channel 02 Busy	
D03	Channel 03 Busy	
D04	Channel 04 Busy	
D05	Channel 05 Busy	
D06	Channel 06 Busy	
D07	Channel 07 Busy	
D08	Channel 08 Busy	
D09	Channel 09 Busy	
D10	Channel 10 Busy	
D11	Channel 11 Busy	
D12	Two's Complement	Channel data is processed in 12-bit offset binary if D12 is cleared (reset default) or in two's complement format with extended sign if D12 is set. (See text)
D13	Analog Outputs On	All outputs are connected to the output connectors if D13 is set, or disconnected if D13 is cleared. Note: For current output options, the outputs are placed in a minimal current output state when this bit is cleared to a zero. This bit must be set to a "1" to allow operation.
D14	Reserved	
D15	Fail LED L	The "FAIL" LED is OFF if D15 is set, or is ON if D15 is cleared.
<b>NOTE:</b>		
<b>Logic State Convention:</b> To avoid ambiguities in references to logic levels, this document uses the convention that a data bit or control line is "SET" when it is in the "1", or HIGH state, and is "CLEARED" when "0" or LOW.		

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## Reset Operations

All read/write registers are cleared to ZERO by a system reset operation. The reset operation places the board in the following state:

- Analog Output Level....Current outputs are minimal; voltage outputs are minus fullscale
- Analog Output State....All voltage channels are disconnected from the output connectors
- Data Coding .....Offset binary
- Front Panel LED .....Illuminated.

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## Control of Analog Outputs

### Output Registers and Data Format

The twelve independent analog outputs are controlled through output data registers ODR 00 through ODR 11. Readback capability is provided, and both D8 (even/odd) and D16 transfers are supported. Data is configured in right-justified 12-bit offset binary format or two's complement format. The data format is controlled by CSR bit D12, and is offset binary if D12 is cleared, or two's complement if D12 is set.

In the offset binary format (reset default), the upper four bits D12 to D15 are ignored during loading and are returned as zero during readback. In two's complement format, data is received and returned in two's complement with the sign extended through the most significant bit D15 during readback.

### Scaling and Enabling

Available output ranges are  $\pm 2.5$  V,  $\pm 5$  V, or  $\pm 10$  V for bipolar voltage outputs, 0 to +2.5 V, 0 to 5 V, or 0 to 10 V for unipolar voltage outputs, and 0 to 20 mA, 0 to 25 mA, or 5 to 25 mA for current outputs. The analog output range is determined independently for each output channel by on-board jumpers which are described in Section 5. All voltage outputs are disconnected from the output connectors if D13 in the CSR is cleared, or are connected to the output connectors if CSR D13 is set.

If the CSR D12 control bit is cleared, the output data is coded in offset binary. Each output level is scaled linearly from \$0000 for negative fullscale or lowest output level, to \$0FFF for positive fullscale, or highest output level.

For two's complement coding (CSR D12 set), the output data is scaled from \$F800 for negative fullscale to \$07FF for positive fullscale. Two's complement coding normally is used only for bipolar outputs.

### Output Load Cycles

Data from an output data register is transferred serially to the output D/A converter during an internal Output Load Cycle. A data transfer to a data register initiates a load cycle for the associated output channel. The load cycle is completed in approximately 8  $\mu$ s, and proceeds automatically after initiation without further intervention from the VMEbus. The level of the associated analog output channel is updated at the end of the load cycle. For D8 transfers, the load cycle is initiated by an odd-byte transfer.

Each Channel Busy Flag (D00 through D11) is set when the assigned channel output data register receives a data transfer from the bus, and remains set for approximately 8  $\mu$ s during the ensuing output load cycle. Data transfers to an output register should not take place while the associated busy flag is set. However, any register can be read at any time without affecting board performance. All output channels are controlled independently, and any output data register can be updated without affecting the other eleven channels.



# Maintenance

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## Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

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Contact VMIC Customer Service at 1-800-240-7782, or  
E-mail: [customer.service@vmic.com](mailto:customer.service@vmic.com)

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## **Maintenance Prints**

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.