VMIVME-4900

DIGITAL-TO-SYNCHRO/RESOLVER CONVERTER BOARD

INSTRUCTION MANUAL

DOCUMENT NO. 500-000101-000 P

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RECORD OF REVISIONS

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B	09/29/88	Appendix A	88-0184
C	09/29/88	Section 2	88-0246
D	02/23/89	Appendix A	88-0353
E	04/20/89	Cover, page ii, Appendix A	89-0013
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G	09/18/89	Entire Manual	89-0130
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P	02/25/97	Cover, pages ii, vi, vii, Section 6, and Deleted Appendix B	97-0222

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

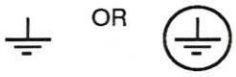
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

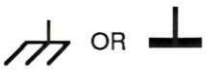
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-4900
DIGITAL-TO-SYNCHRO/RESOLVER CONVERTER BOARD

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SECTION 1

INTRODUCTION AND FUNCTIONAL DESCRIPTION

1.1 INTRODUCTION

The 4900 board is a VMEbus compatible Digital-to-Synchro/Resolver Converter (DSC/DRC) which utilizes either one or two DSC/DRC depending on the option chosen. Features of the board include the following:

a. Synchro or resolver outputs
b. One or two DSC/DRCs
c. 14-bit converter with an overall accuracy of ±4 arc minutes
d. Internal transformers
e. 8- or 16-bit VMEbus data transfer
f. Front panel Fail LED
g. 115 Vrms or 26 Vrms reference excitation voltage
h. Built-in-test feature

1.2 FUNCTIONAL DESCRIPTION

The DSC/DRC Board is based on Data Device Corporation's (DDC) converter modules (or an equivalent design). The board supports a wide variety of options which are supported by configuring jumpers on the basic printed circuit board and by installing option parts. These options are listed in the VMIVME-4900 product specification, document number 800-000101-000. The VMIVME-4900 board, with supporting Built-in-Test features both off-line and on-line fault detection and isolation. The Built-in-Test feature requires a VMIC single channel, Synchro-to-Digital Converter (SDC) board (VMIVME-4910), or a quad-channel SDC board (VMIVME-4911) and a standard synchro test backplane (SRTbus™) installed in the P2 position of a standard VME chassis, as shown in Figure 1.2-1. The board accepts a 14-bit digital output word (shaft angle) and a reference excitation voltage and produces a synchro or resolver output.

The DSC/DRC Board is provided with several options and is capable of interfacing with most standard synchro or resolver devices. The board is ideally suited for computer-based systems in which digital information is processed, such as simulators, robotics, and other control-oriented systems.

1.3 REFERENCE DOCUMENT LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

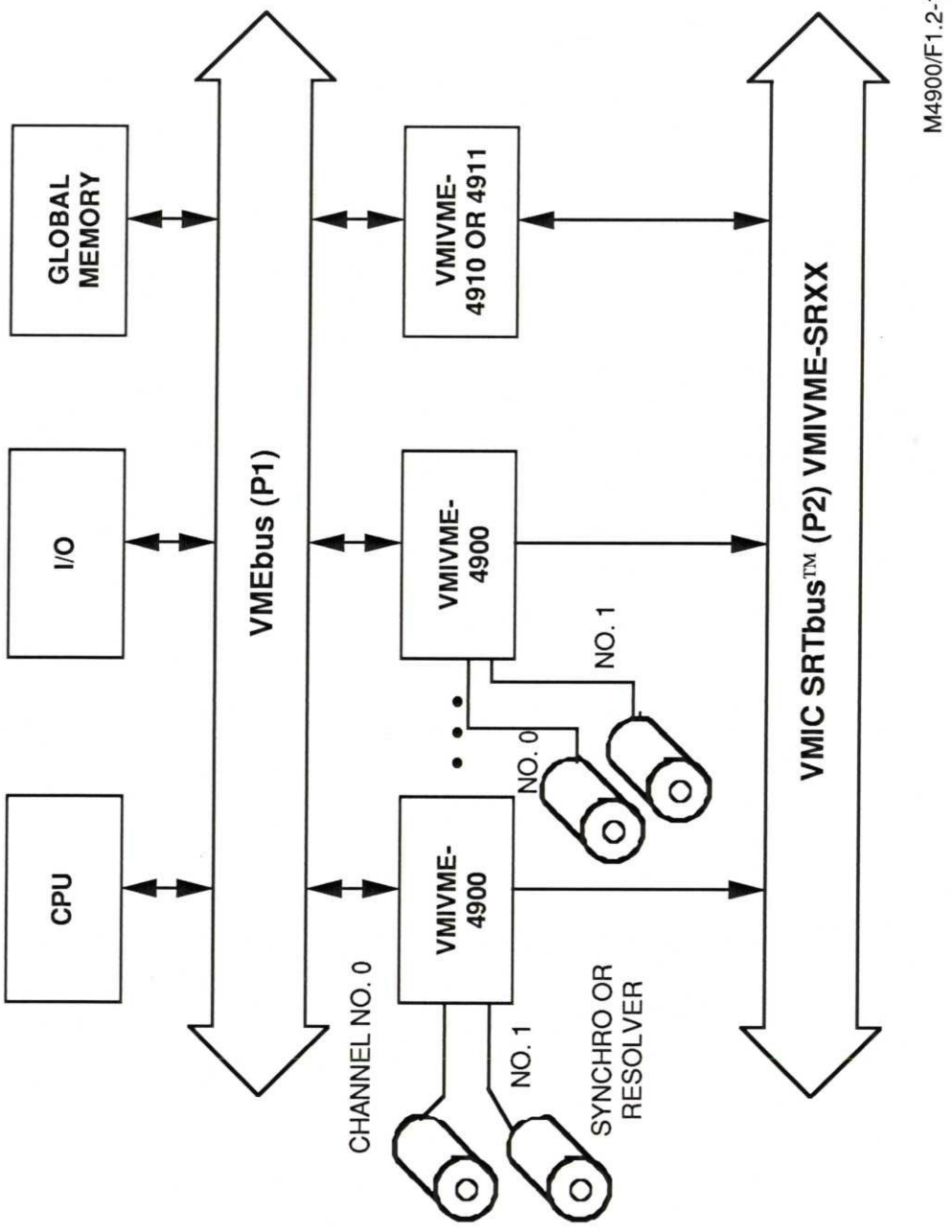


Figure 1.2-1. Synchro/Resolver Test Subsystem (On-line and Off-line Testing)

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

Additional data on Digital-to-Synchro Converters (DSCs) is available from the following sources:

Data Converters Product Catalog-(August 1984)
ILC Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716

Synchro Conversion Handbook
ILC Data Device Corporation
105 Wilbur Place
Bohemia, New York 11716

VME Microsystems International Corporation
Synchro/Resolver (Built-in-Test) Subsystem
Configuration Guide - Document No. 825-00000-004

This product is compatible with VMIC's 90XX family of IIOCs. These products were designed for high performance, real-time data acquisition and control such as that found in the simulation, training, and manufacturing industry. The IIOC is a multiprocessor controller that includes CPU(s), global memory(s), a wide variety of host computer interfaces and firmware that provides a "turnkey" total I/O solution. More information concerning this product may be obtained by requesting VMIC's Intelligent I/O Controller Family Instruction Manual, Document No. 500-009000-000.

NOTICE

FOR REAL-TIME FAULT DETECTION AND ISOLATION, THE IIOC REQUIRES THE USE OF VMIC'S VMIVME-4911. THE IIOC FIRMWARE IS NOT COMPATIBLE WITH THE VMIVME-4910.

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-000101-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual presents detailed information about the hardware operation of the VMIVME-4900 Digital-to-Synchro/Resolver Converter (DSC/DRC) Board. Information concerning programming is provided in Section 4.

3.2 FUNCTIONAL OPERATION

The VMIVME-4900 Board design may be functionally divided into seven primary sections, as shown in Figure 3.2-1, functional block diagram. These primary functional sections are listed below:

a. Address decode logic
b. VMEbus foundation logic
c. Output data and control registers
d. Digital-to-synchro/resolver modules
e. Built-in-test hardware operation
f. Output relay control
g. Power connections

3.3 ADDRESS DECODE LOGIC

A functional block diagram of the address decode logic is shown in Figure 3.3-1. Two eight position DIP switches are provided to enable the user to select from a wide range of short I/O memory addresses for the board address. The user may also select non-privileged or supervisory short I/O transfers. The board is configured at the factory to respond to short supervisory I/O transfers (jumper JW4 removed).

3.4. VMEbus FOUNDATION LOGIC

The VMIVME-4900 VMEbus foundation logic shown in Figure 3.4-1 consists primarily of a DTACK generator, control signal buffers, and data transceivers that buffer data to be transmitted to output registers and to the Control and Status Register (CSR) which controls the front panel Fail LED. The control logic is designed to support 8- and 16-bit transfers. Address bits A01 and A02 are

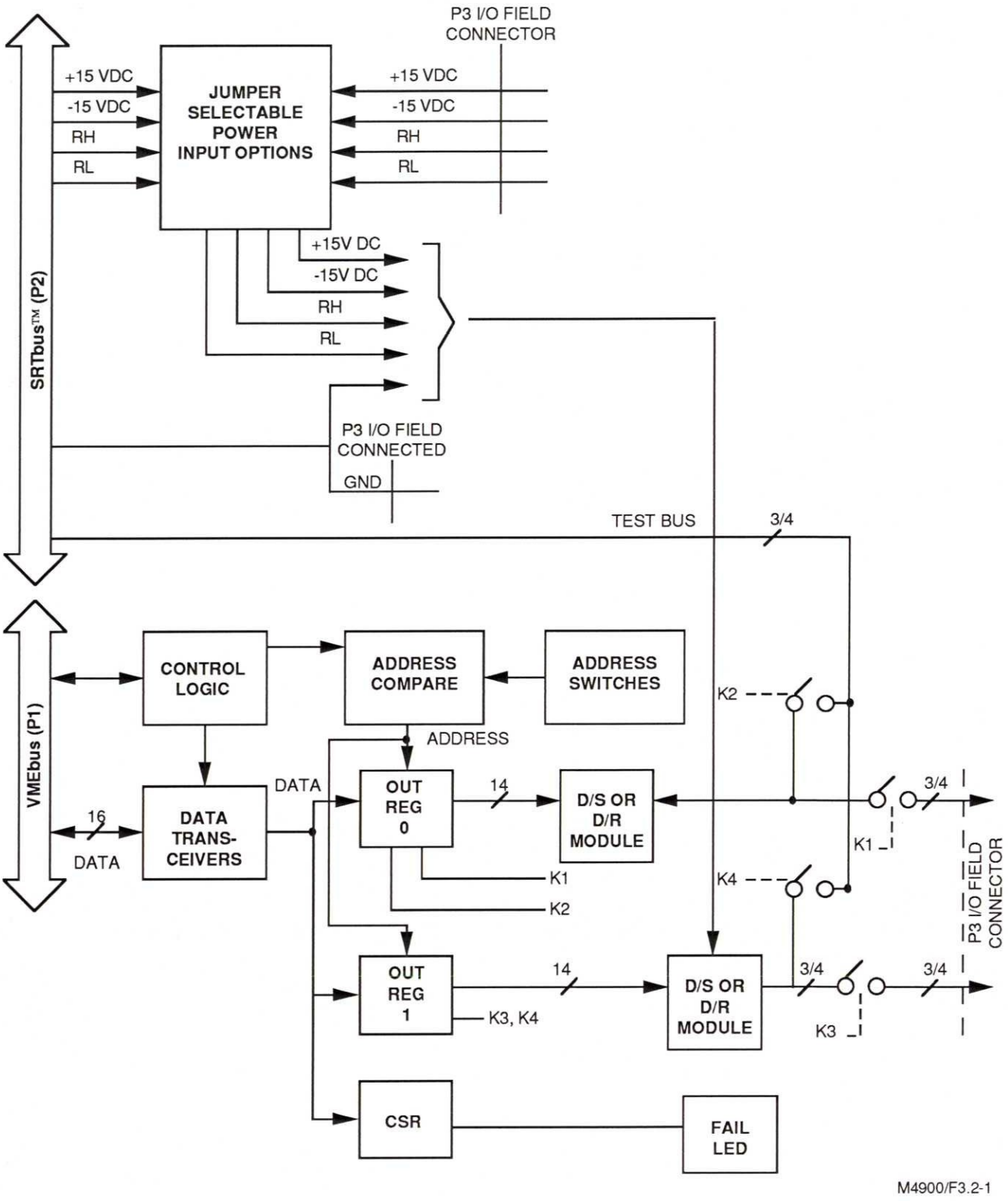


Figure 3.2-1. VMIVME-4900 Digital-to-Synchro/Resolver Converter Functional Block Diagram

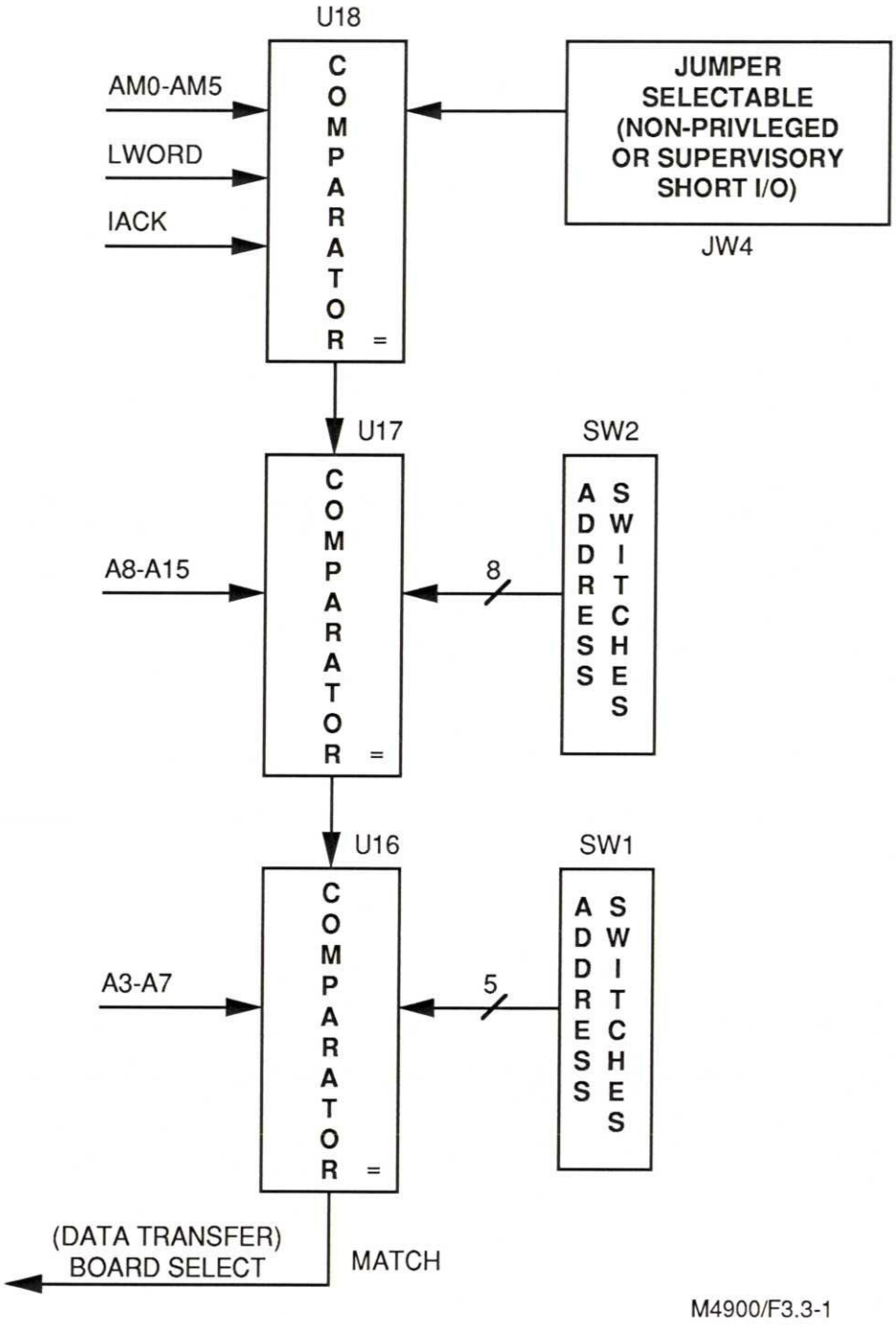


Figure 3.3-1. Address Decode Detailed Block Diagram

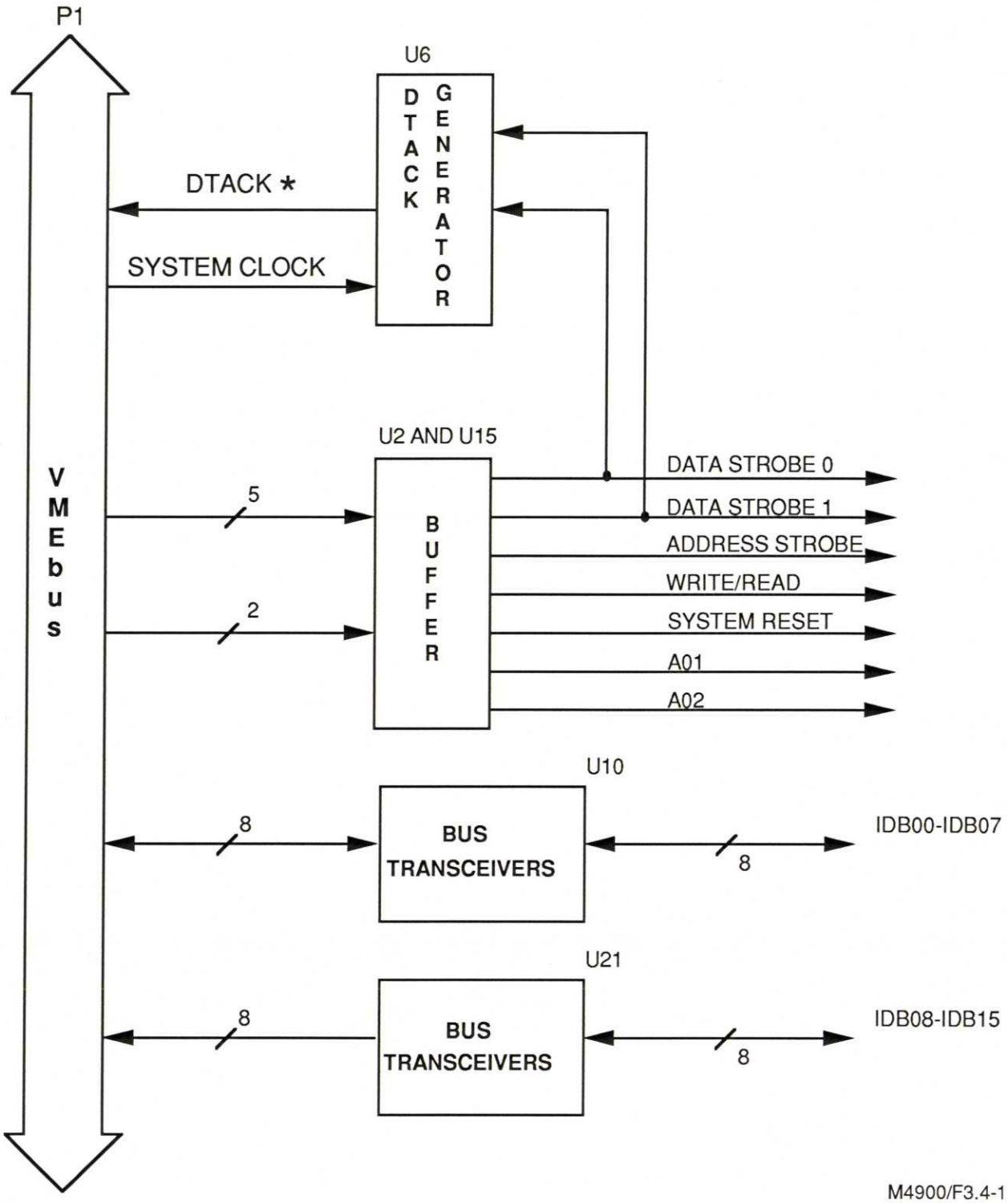


Figure 3.4-1. VMEbus Foundation Logic Detailed Block Diagram

decoded to select one of two output data registers and the CSR which controls the front panel Fail LED.

3.5 OUTPUT DATA AND CONTROL REGISTERS

The VMIVME-4900 is designed with four eight-bit output data and control registers and a one-bit CSR that controls the front panel Fail LED, as shown in Figure 3.5-1. All registers are cleared at power-up by the VMEbus SYSRESET signal; therefore, all synchro/resolver outputs are disconnected from their loads, and the front panel Fail LED is illuminated.

3.6 DIGITAL-TO-SYNCHRO/RESOLVER CONVERTER MODULE

A functional block diagram of the DSC/DRC module is shown in Figure 3.6-1. The digital data provided as inputs to each module is stored in holding registers, as described in Section 3.5. VMIC selects the specific synchro/resolver modules from a wide variety of vendors that meet manufacturing options as specified by the user. The reader should refer to Section 2 for a detailed explanation of available options.

3.7 BUILT-IN-TEST HARDWARE OPERATION WITH VMIVME-4910

The VMIVME-4900 supports fault detection and isolation when used with the VMIC SRTbus™ and VMIC's model VMIVME-4910 or VMIVME-4911. The SRTbus™ is a synchro/resolver test bus that utilizes the user I/O pins on the P2 VMEbus connector. Programming the proper control bits in each output word of the VMIVME-4900 allows field disconnect and/or real-time loopback testing, via the SRTbus™ and the VMIVME-4910 or 4911.

A typical VMIC Digital-to-Synchro Converter (DSC) subsystem may be configured such that a VMIC P2 Synchro Backplane (SRTbus™) is utilized for isolating failures to the board level. The DSC Built-in-Test subsystem is based on an individually switched DSC output to a shared Synchro-to-Digital Converter (SDC) board, as shown in Figure 3.7-1. This subsystem may be economically expanded by utilizing the VME repeater link as shown in Figure 3.7-2.

Each DSC board is designed to support both off-line and on-line fault detection and isolation by programming two Built-in-Test output control switches. During off-line testing, synchro/resolver outputs are physically disconnected from the loads. Connection to the test backplane is electrically interlocked, such that no two synchro outputs from a VMIVME-4900 can be connected to the backplane simultaneously.

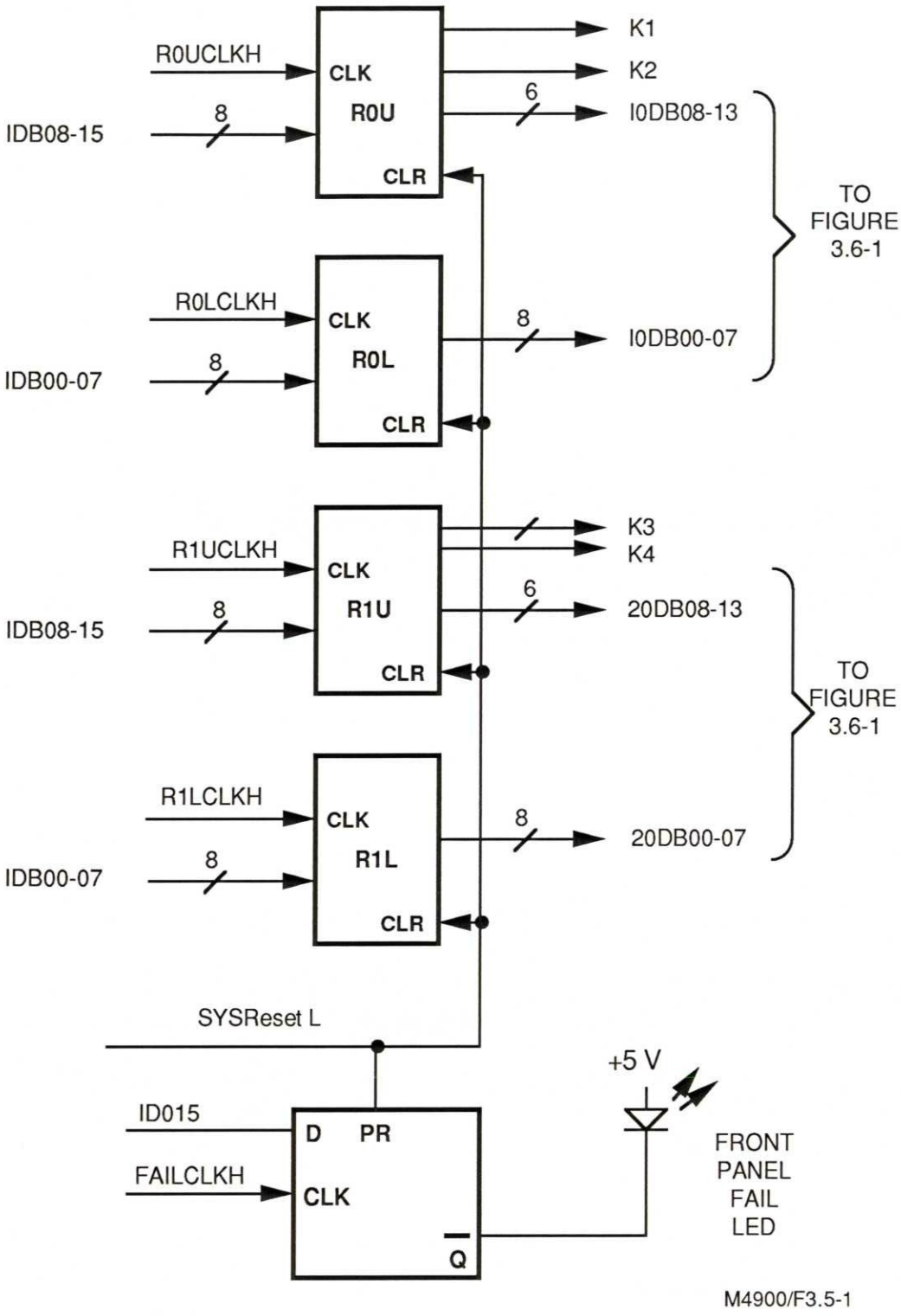


Figure 3.5-1. Output Data and Control Registers

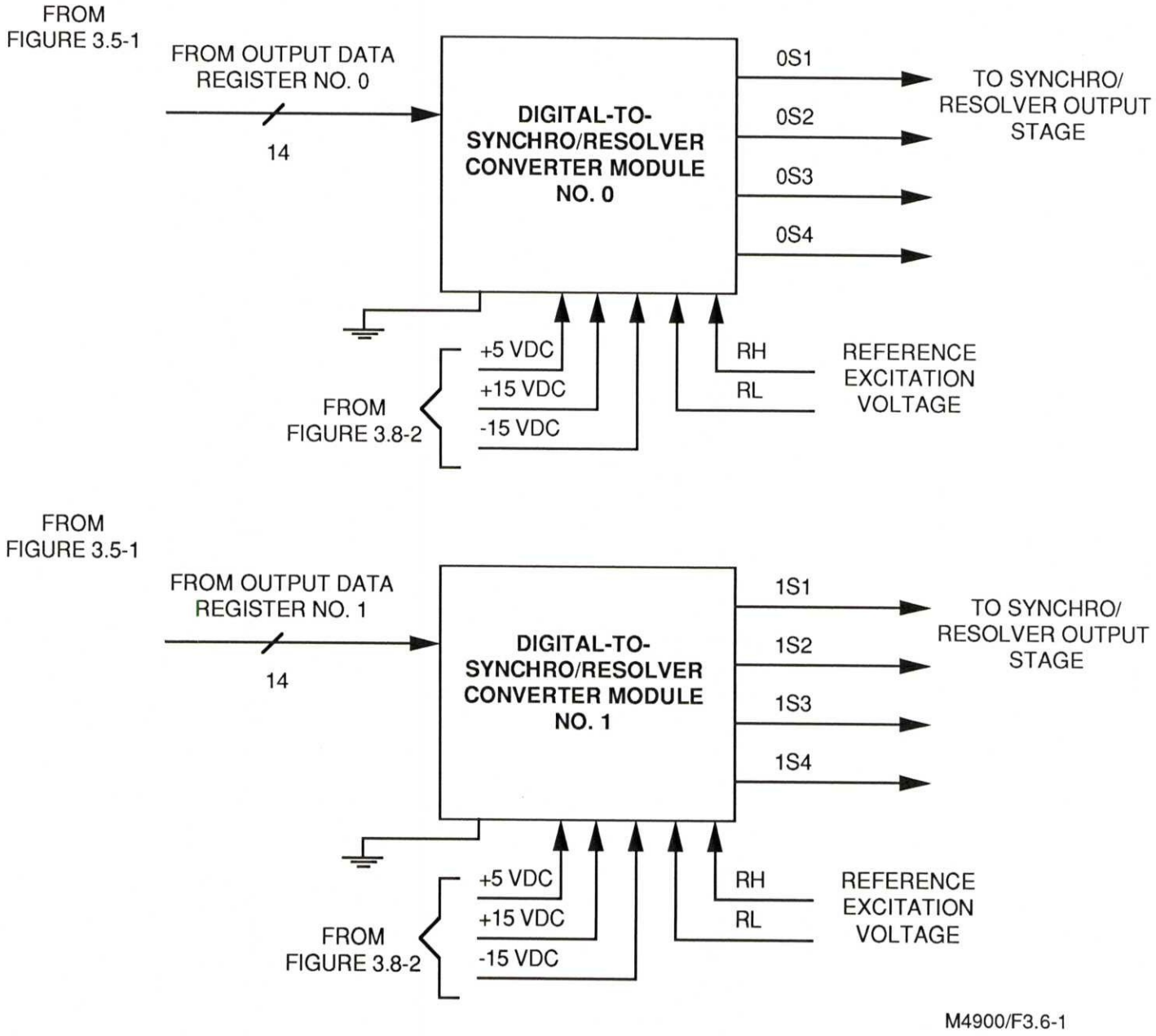


Figure 3.6-1. Digital-to-Synchro/Resolver Converter Detailed Block Diagram

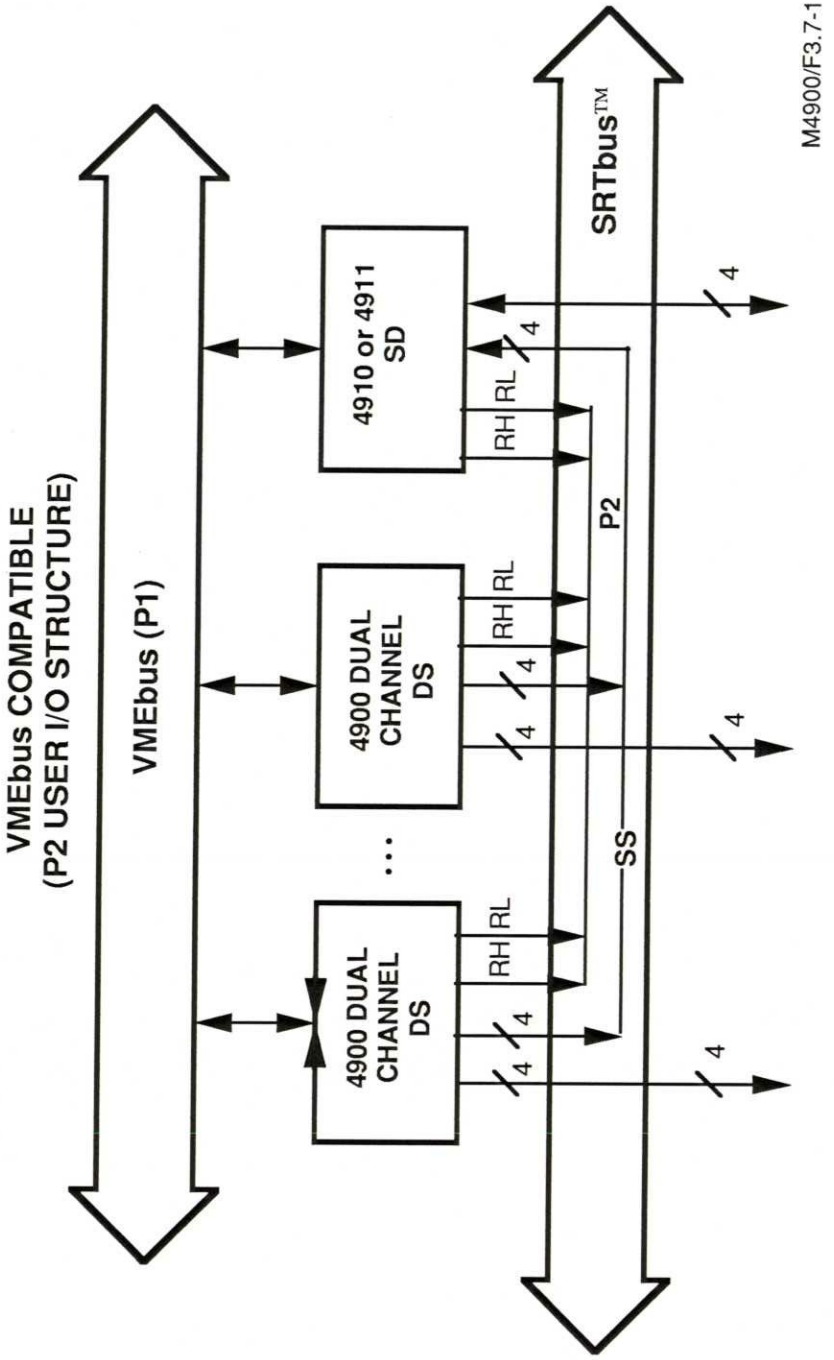


Figure 3.7-1. Typical Built-in-Test Configuration

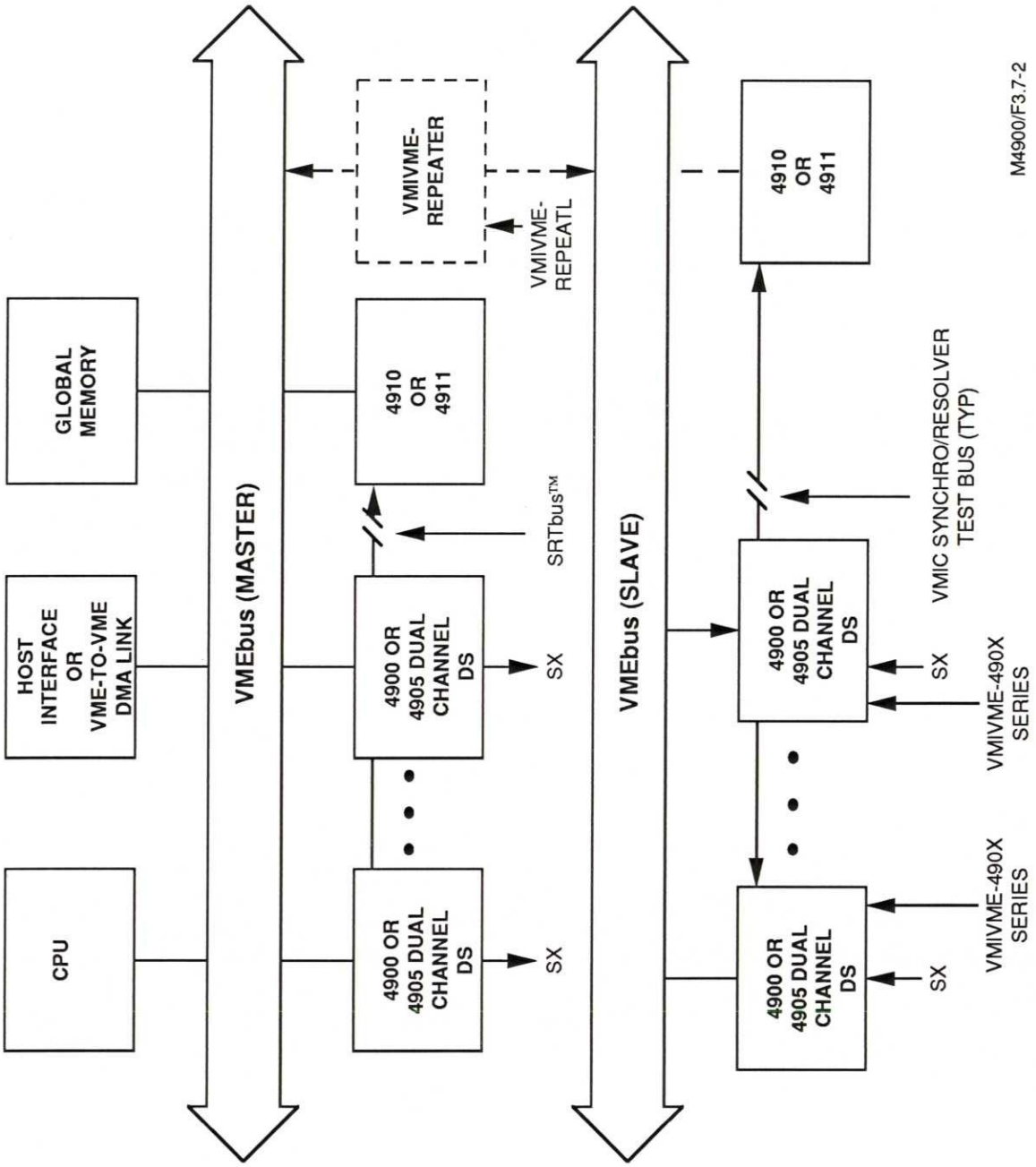


Figure 3.7-2. Expanded Synchro/Resolver Subsystem with Built-in-Test

VMIC's 4910 series SDC interface may be utilized for fault detection and isolation of DS boards (Figure 3.7-3) and is based on Data Device Corporation's (DDC) Model SDC 634. The VMIVME-4910 series is only available as a single channel, dual height board with front panel Fail LED.

The user can also elect to receive channel "A" synchro/resolver inputs from the VMIC synchro/resolver backplane via the P2 connector. This configuration lends itself for use with a DSC/DRC board, such as the VMIVME-4900, for test purposes or the user could supply field inputs directly to the P2 connector instead of using the P3 I/O connector (refer to Figure 3.7-4).

3.8 BUILT-IN-TEST HARDWARE OPERATION WITH VMIVME-4911

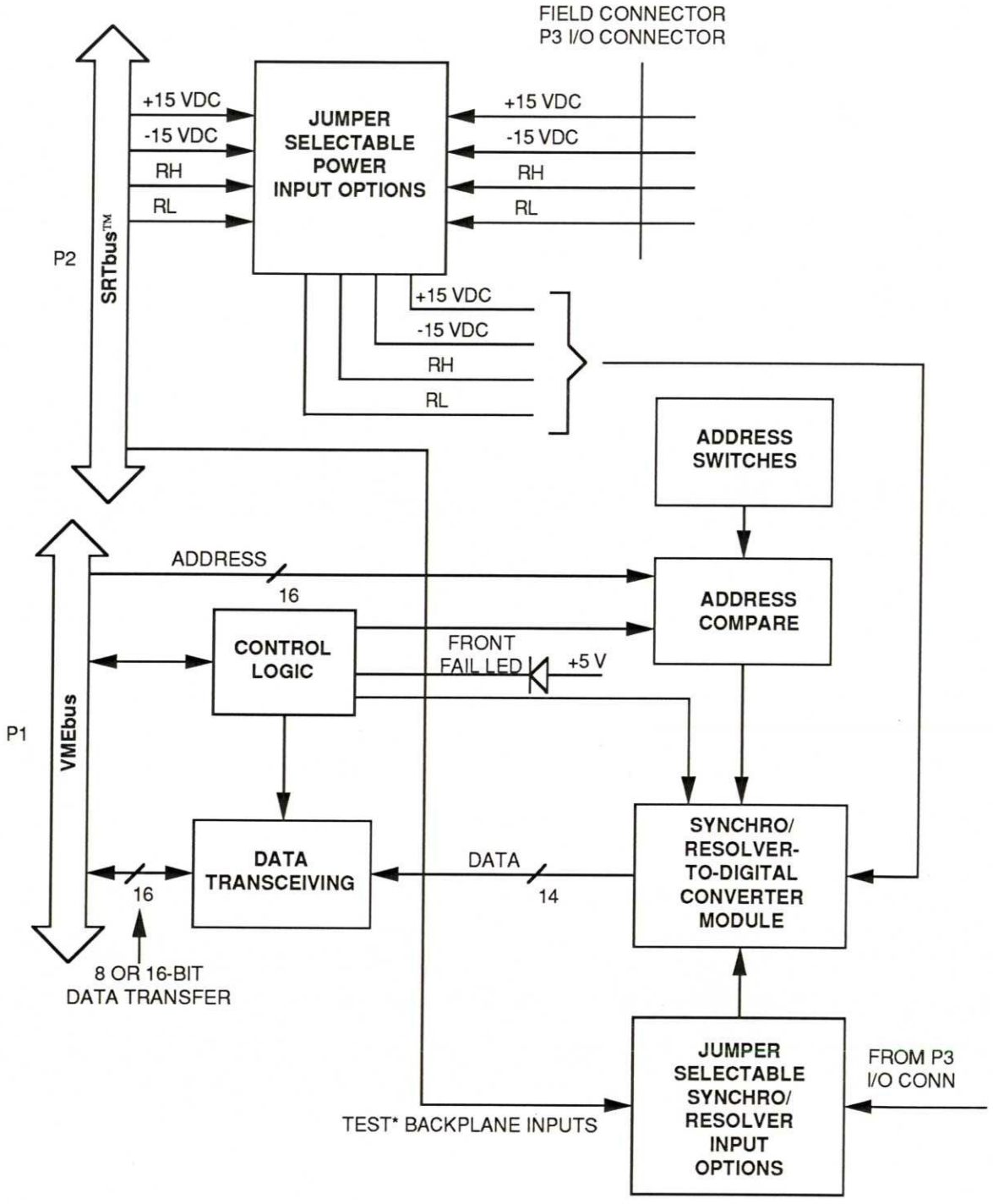
The VMIVME-4911 Quad Channel SDC (Figure 3.8-1) is designed so that channel "A" may be jumpered to the P2 backplane such that the board can be loop-tested via VMIC's SRTbus™ and DSC boards, as shown in Figure 3.8-2. This concept provides the user with the capability to design systems with off-line and on-line fault detection and isolation. The reader should refer to VMIC's Synchro/Resolver Subsystem Configuration Guide (Document No. 825-000000-004) for a thorough explanation of synchro/resolver Built-in-Test concepts.

3.9 OUTPUT RELAY CONTROL

Four relays are provided to allow programmed field disconnect and to support real-time and off-line fault detection and isolation, as shown in Figure 3.7-4. The relays are controlled by data bits in each holding register, as described in Section 3.5. Relays K1 and K3 provide the field disconnect functions, whereas relays K2 and K4 provide the wrapback testing hardware, as described in Section 3.7. Relay control logic for relays K2 and K4 is designed with a hardware interlock to preclude simultaneous energization. Each synchro/resolver output is fused at the immediate outputs of the synchro/resolver board for overcurrent protection.

3.10 POWER CONNECTIONS

The VMIVME-4911 Quad Channel SDC Board is designed to use three DC power supplies and one reference signal, as shown in Figure 3.8-2. Because of the high density VMIC design requirements, external ±15 VDC power supplies are required for most applications. The user should refer to the VMIVME-4900 product specification, document number 800-000101-000 for power requirements as a function of options ordered. Jumpers are provided, as shown in Figure 3.8-2, to allow the user the option to select front panel or rear panel 15 VDC and reference inputs.



*Used for fault isolation of VMIVME-49XX series DS, or DR boards.

Figure 3.7-3. VMIVME-4910 Functional Block Diagram

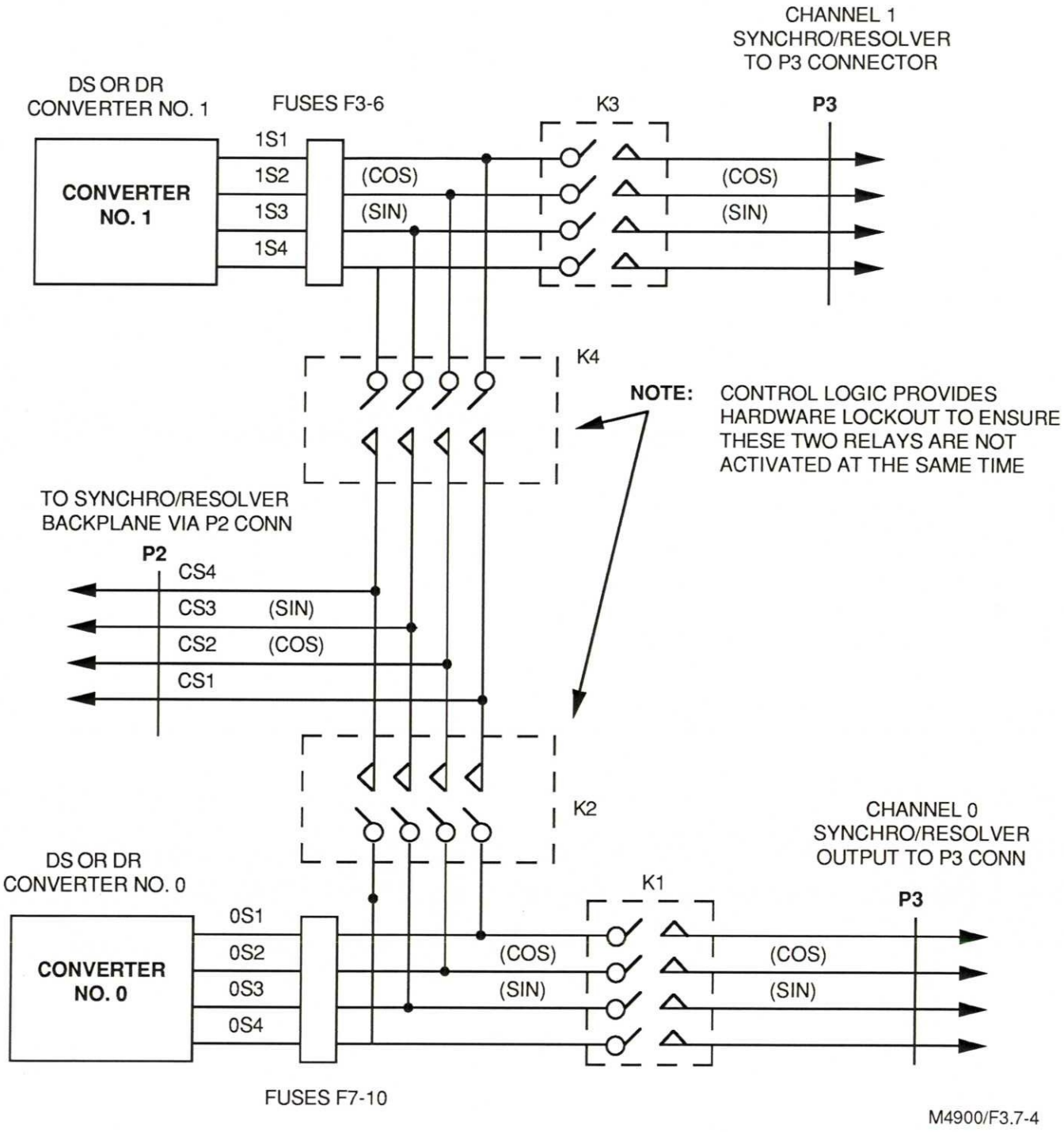


Figure 3.7-4. Synchro/Resolver Output Functional Block Diagram

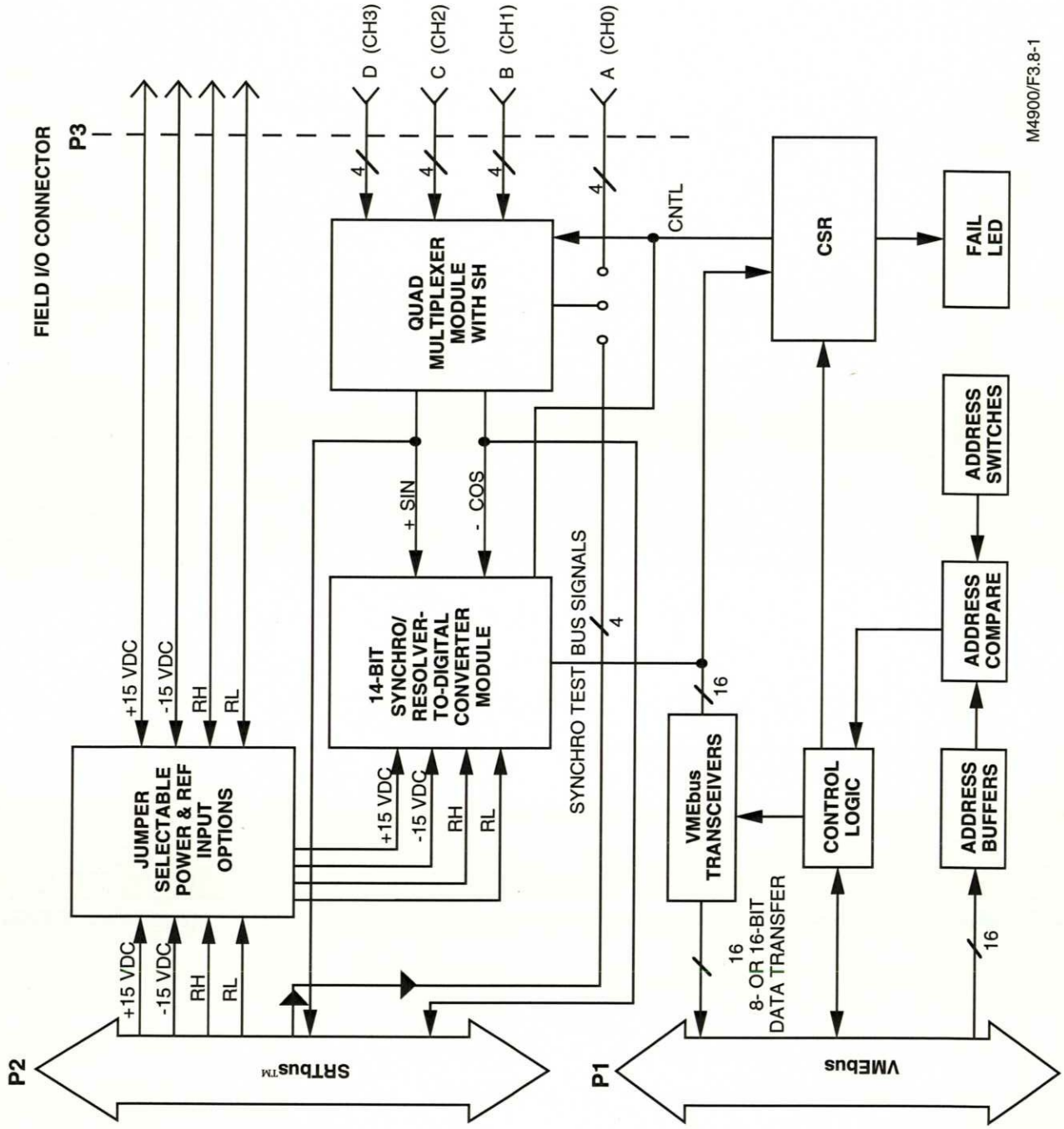


Figure 3.8-1. VMIVME-4911 Quad Channel Synchro/Resolver-to-Digital Converter Board Functional Block Diagram

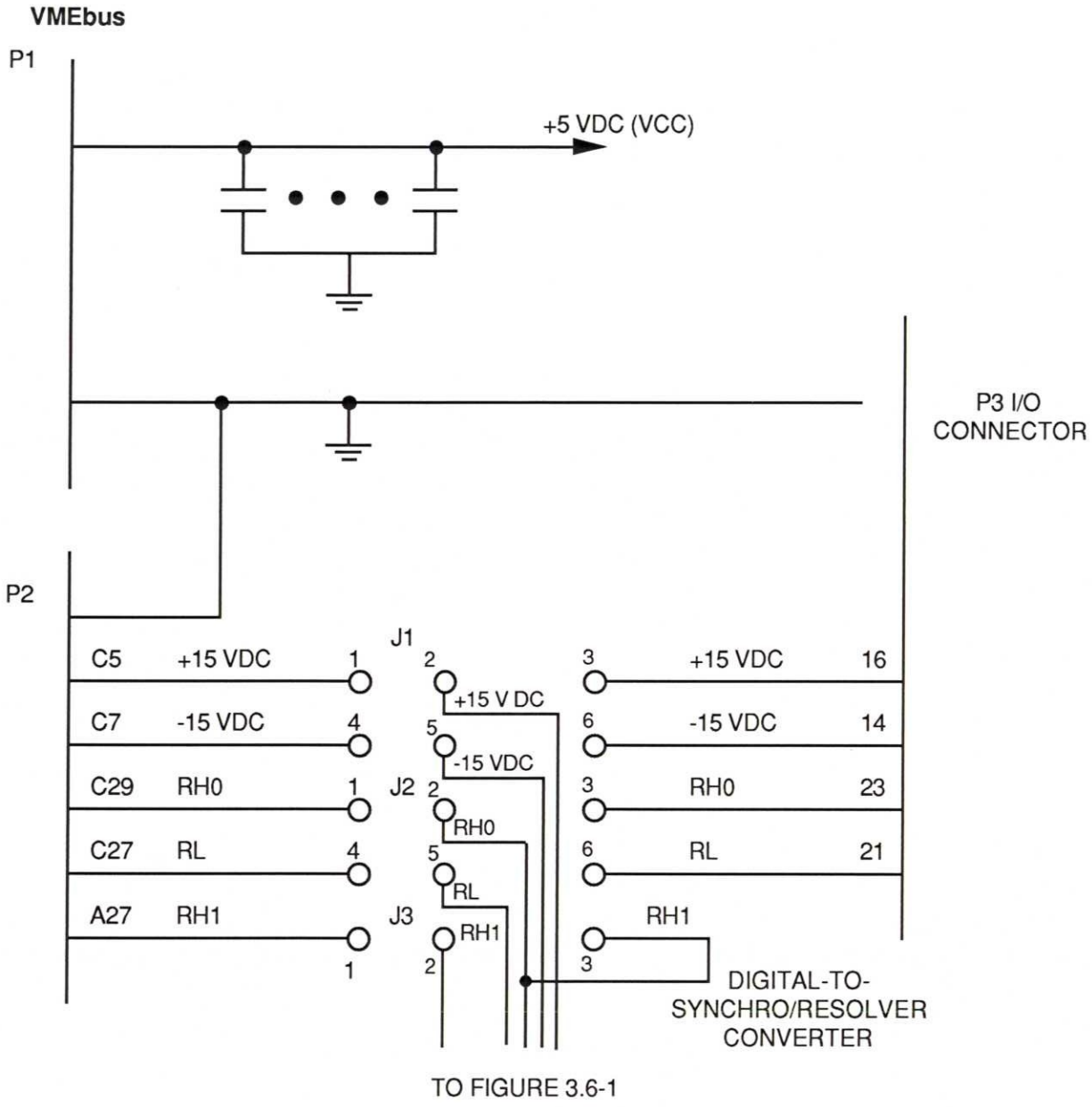


Figure 3.8-2. Power Connection Block Diagram

SECTION 4

PROGRAMMING

4.1 PROGRAMMING

An output operation is initiated by executing an output transfer instruction that loads one of two output registers. The execution of this instruction sends the VMEbus an address that causes selection of the Digital-to-Synchro/Resolver Converter (DSC/DRC) Board, if the board address switches match the address transmitted. The bit pattern of the data output word determines the position of the user's torque receiver(s). The bit-to-angle conversion (position) information is shown in Table 4.1-1.

The Control Processing Unit (CPU) should not initiate large shaft position changes that may result in overdriving the torque receiver(s). High current electrical transients and mechanical transients may damage the torque receiver and or the digital-to-synchro/resolver board.

The VMIVME-4900 DSC/DRC Board is initialized at power-up with the field (user torque receivers) disconnected and the front panel Fail LED illuminated.

WARNING

TWO TEST RELAYS (K2 AND K4) CONNECT THE SYNCHRO OUTPUT CHANNELS TO THE SYNCHRO BACKPLANE (SEE FIGURE 3.6-1); THEREFORE, ONLY ONE OF THESE RELAYS CAN BE ENERGIZED AT ONE TIME. THE PROGRAMMER MUST PROVIDE A ONE MILLISECOND (MINIMUM) DELAY FOR RELAYS TO DROP OUT BEFORE ANOTHER RELAY CAN BE ENERGIZED. TEST RELAYS ON OTHER BOARDS MUST ALSO BE DE-ENERGIZED BEFORE EITHER TEST RELAY IS ENERGIZED ON THIS BOARD. SIMULTANEOUS CONNECTION OF MORE THAN ONE SYNCHRO SIGNAL TO THE TEST BACKPLANE CAN RESULT IN STUCK RELAYS AND/OR BLOWN FUSES.

4.2 REGISTER MAP

The VMIVME-4900 contains four 8-bit data registers, and one 8-bit control register. Also included within the data registers are the relay control bits for test and output control, for specific relay control information refer to Tables 4.2-1 and 4.3-1. All registers are *write only* registers and can be written as bytes or words. All Synchro/Resolver (SR) data output registers are *write* only and can be written as bytes or words.

Table 4.1-1. Bit-to-Angle Conversion

BIT	DEG/BIT	MIN/BIT
DB13	180	10,800
DB12	90	5,400
DB11	45	2,700
DB10	22.5	1,350
DB9	11.25	675
DB8	5.625	337.50
DB7	2.183	168.75
DB6	1.406	84.30
DB5	0.7031	42.19
DB4	0.3516	21.09
DB3	0.1758	10.55
DB2	0.0875	5.27
DB1	0.0439	2.64
DB0	0.0220	1.32

DB refers to register bit definitions, as seen in Section 4-2, and not to the pin outs on the Data Device Corporation (DDC) converter modules.

M4900/T4.1-1

Table 4.2-1. Address Map and Register Bit Formats

HEX ADDRESS	BINARY ADDRESS				
A15 - A4	A3	A2	A1	A0	
X X X	X	0	0	0	**DS OR DR NO. 0 OUTPUT REGISTER UPPER BYTE**
					BIT 15 | **BIT 14** | **BIT 13** | **BIT 12** | **BIT 11** | **BIT 10** | **BIT 9** | **BIT 8**
					OUT CH0 "1" = OUT | TEST CH0 "1" = TEST | 0DB13 | 0DB12 | 0DB11 | 0DB10 | 0DB9 | 0DB8
X X X	X	0	0	1	**DS OR DR NO. 0 OUTPUT REGISTER LOWER BYTE**
					BIT 7 | **BIT 6** | **BIT 5** | **BIT 4** | **BIT 3** | **BIT 2** | **BIT 1** | **BIT 0**
					0DB7 | 0DB6 | 0DB5 | 0DB4 | 0DB3 | 0DB2 | 0DB1 | 0DB0
X X X	X	0	1	0	**DS OR DR NO. 1 OUTPUT REGISTER UPPER BYTE**
					BIT 15 | **BIT 14** | **BIT 13** | **BIT 12** | **BIT 11** | **BIT 10** | **BIT 9** | **BIT 8**
					OUT CH1 "1" = OUT | TEST CH1 "1" = TEST | 1DB13 | 1DB12 | 1DB11 | 1DB10 | 1DB9 | 1DB8
X X X	X	0	1	1	**DS OR DR NO. 1 OUTPUT REGISTER LOWER BYTE**
					BIT 7 | **BIT 6** | **BIT 5** | **BIT 4** | **BIT 3** | **BIT 2** | **BIT 1** | **BIT 0**
					1DB7 | 1DB6 | 1DB5 | 1DB4 | 1DB3 | 1DB2 | 1DB1 | 1DB0
X X X	X	1	0	0	**CONTROL STATUS REGISTER UPPER BYTE**
					BIT 15 | **BIT 14** | **BIT 13** | **BIT 12** | **BIT 11** | **BIT 10** | **BIT 9** | **BIT 8**
					FAIL LED "1" = ON | NOT USED
X X X	X	1	0	1	**CONTROL STATUS REGISTER LOWER BYTE**
					BIT 7 | **BIT 6** | **BIT 5** | **BIT 4** | **BIT 3** | **BIT 2** | **BIT 1** | **BIT 0**
					NOT USED

A15 ——— A3
Base address switch selectable

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Fail LED = Front panel Fail LED
1 = On
0 = Off
Fail LED is turned on at power-up or system reset.
All register bits are cleared at power-up or system reset, which de-energizes all relays.

4.3 BUILT-IN-TEST CONFIGURATION

Relays are provided on the 4900 to support off-line and real-time fault detection and isolation. The four relay functions are shown in Table 4.3-1.

Table 4.3-1. Relay Functions

DATA REG/BIT NO.	MNEMONIC RELAY CONTROL BIT	FUNCTION PERFORMED	RELAY NO.
DATA REG 0/BIT 15	OUT CH0	CONNECTS DS OR DR CHAN 0 TO P3 FRONT PANEL CONNECTOR	K1
DATA REG 0/BIT 14	TEST CH0	CONNECTS DS OR DR CHAN 0 TO P2 CONNECTOR/SRTbus™*	K2
DATA REG 1/BIT 15	OUT CH1	CONNECTS DS OR DR CHAN 1 TO P3 FRONT PANEL CONNECTOR	K3
DATA REG 1/BIT 14	TEST CH1	CONNECTS DS OR DR CHAN 1 TO P2 CONNECTOR/SRTbus™	K4

On power-up or on system reset, all relays are inactive.

M4900/T4.3-1

*SRTbus™ is a synchro/resolver test bus, VMIVME-SRXX.

4.4 BUILT-IN-TEST CONFIGURATION WITH SYNCHRO/ RESOLVER TEST BUS

VMIC's VMIVME-4911 Resolver/Synchro-to-Digital Converter (RDC/SDC) Board is utilized for fault detection and isolation of Digital-to-Synchro/Resolver Converter (DSC/DRC) boards and is based on an industry standard Quad-Multiplexing Synchro/Resolver-to-Digital Converter (SDC/RDC) module. This high performance, fast settling, 14-Bit SDC is required to support the real-time fault detection and isolation capabilities of the IIOC and the real-time synchro/resolver input data processing required in the simulation and training industry.

VMIC also produces a model VMIVME-4910 Tracking SDC/SRC board that supports fault detection and isolation. The VMIVME-4910 is a single-channel synchro/resolver input board that is designed with input data switching relays to support either inputs from field sources via the front panel connector or the P2 VMEbus connector. It is also designed to support loopback testing of VMIC's 49XX series DSC/DRC products. The worst-case settling time (after signal switching) of

the VMIVME-4910 may exceed 250 ms; therefore, it is not recommended for real-time data processing where switching rates are in excess of the worst-case settling time. VMIC recommends the VMIVME-4911 Quad SDC/RDC Board for real-time simulation and training applications. This high-speed converter features simultaneous sampling and random access with a resolution of 14 bits and 150 µs conversion time per channel.

The relay operation described in Section 5.4 provides the user with the information necessary to implement Built-in-Test functions.

SECTION 5
CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

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**********
*  CAUTION  *
**********
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SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

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**********
*  CAUTION  *
**********
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DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the board is properly aligned and oriented in the supporting card guides. Slide the board smoothly forward against the mating connector until firmly seated.

5.3 CONNECTOR AND JUMPER CONFIGURATION DETAILS

Pin functions for the P2 and P3 connectors are listed in Table 5.3-1. Jumper configurations for the ±15 VDC power and reference connection are shown in Figures 5.3-1, 5.3-2, and 5.3-3. The VMIVME-4900 is configured at the factory with the ±15 VDC and reference connected to the P2 connector.

Table 5.3-1. P2, P3 Pinout

SIGNAL	P 2	P3 JUMPER FOR CONNECTOR
GND	A3	
GND	A4	
GND	C1	25
+15 VDC	C5	
+15 VDC	C6	16
-15 VDC	C7	
-15 VDC	C8	14
RH	C29	23
RH 1	C29	23
RH1	A27	
RL	C27	21
0S1	C18	12
(COS) 0S2	C20	10
(SIN) 0S3	C22	7
0S4	C24	5
1S1	C18	3
(COS) 1S2	C20	1
(SIN) 1S3	C22	6
1S4	C24	4

M4900/T5.3-1

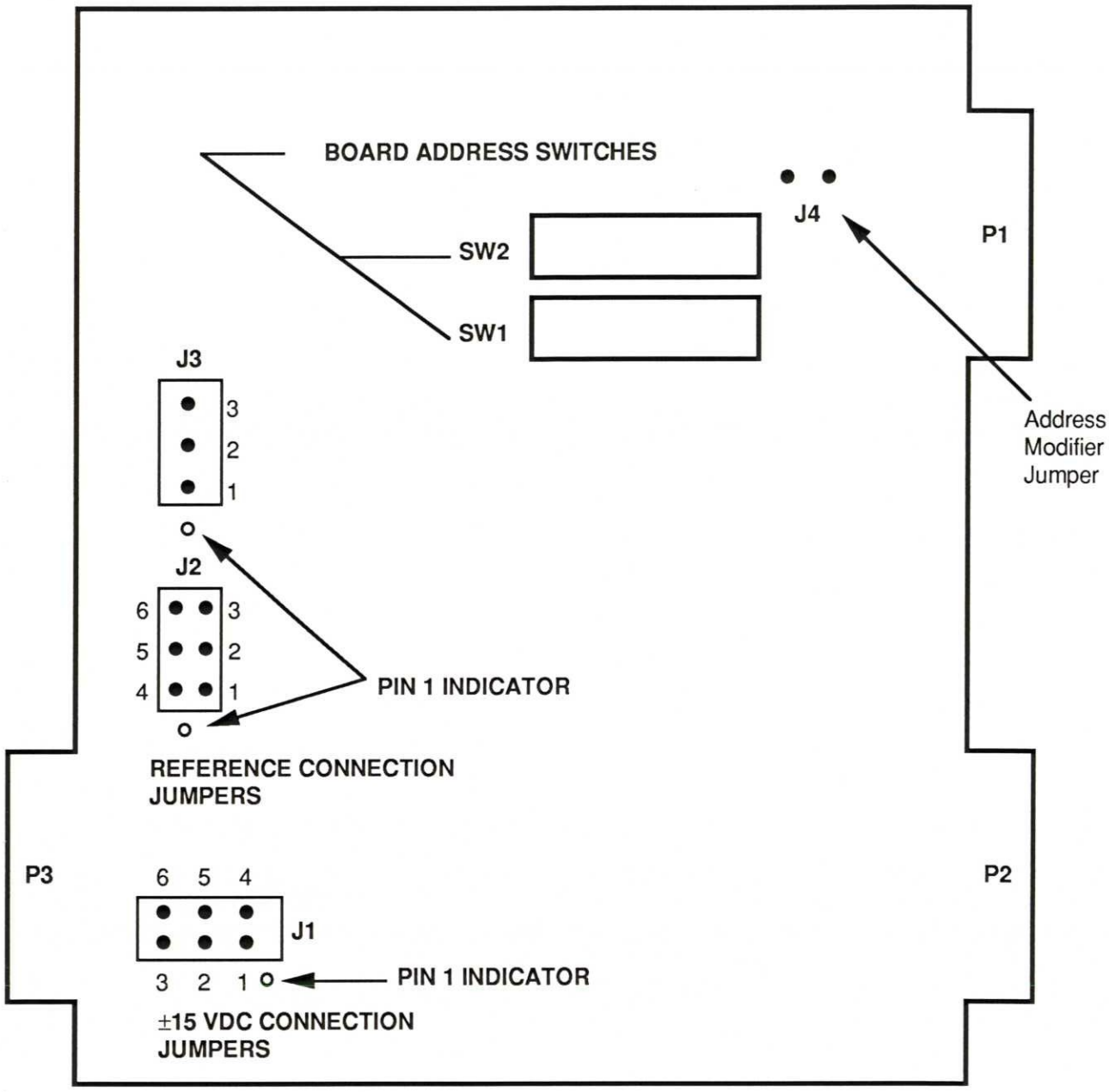
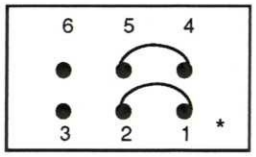


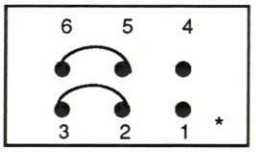
Figure 5.3-1. Switch and Jumper Locations



Factory Configuration

J1

JUMPERS INSTALLED FOR P2 CONNECTION OF ±15 V

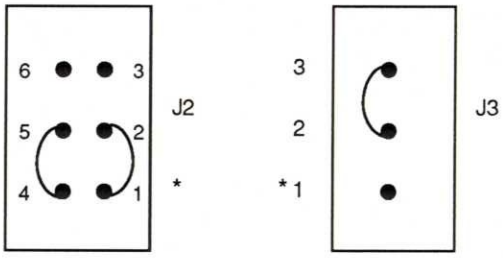


J1

JUMPERS INSTALLED FOR P3 CONNECTION OF ±15 V

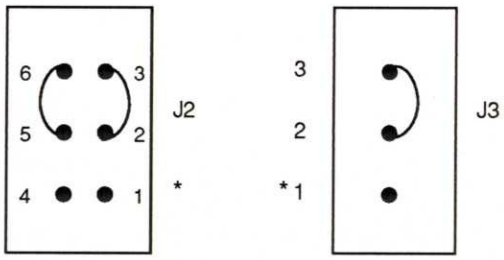
M4900/F5.3-2

Figure 5.3-2. Jumper Configuration ±15 VDC Power

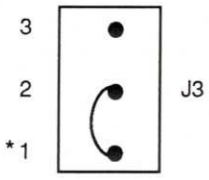


Factory Configuration

JUMPERS INSTALLED FOR P2 CONNECTION OF RH0 AND RL TO BOTH CHANNELS



JUMPERS INSTALLED FOR P3 CONNECTION OF RH0 AND RL TO BOTH CHANNELS



JUMPER INSTALLED FOR RH1 INPUT FROM P2 TO A27 TO CHANNEL 1

*Pin 1 is referenced by white dot on board.

M4900/F5.3-3

Figure 5.3-3. Jumper Configuration for RH and RL

5.4 BUILT-IN-TEST OUTPUT CONFIGURATION

Output relays on the VMIVME-4900 are used to configure the VMIVME-4900 for a variety of output configurations, including on-line and off-line test modes. Four relays, controlled by four relay control bits, allow the programmer to change the outputs at any time during operation. Table 5.4-1, in conjunction with Figure 3.6-1, explains each relay function in the output configuration control.

Table 5.4-1. Relay Functions

RELAY NO.	RELAY CONTROL BIT	OPERATION
K1	K1	CONNECTOR D/S OR D/R NO. 0 TO P3 FRONT PANEL CONNECTOR
K2	K2**	CONNECTS D/S OR D/R NO. 0 TO P2 CONNECTOR/SRTbus™
K3	K3	CONNECTS D/S OR D/R NO. 1 TO P3 FRONT PANEL CONNECTOR
K4	K4**	CONNECT D/S OR D/R NO. 1 TO P2 CONNECTOR/SRTbus™

On power-up or on system reset, all relays are inactive.

*SRTbus™ is a synchro/resolver test bus, VMIVME-SRXX.
**Control hardware prevents K2 and K4 bits from being asserted at the same time. The asserted relay must be de-energized prior to asserting the other relay. The first one set has priority.

M4900/T5.4-1

5.5 HARDWARE CONNECTOR TO SYNCHROS OR RESOLVERS

Depending on whether the board has Digital-to-Resolver Converter (DRC) or Digital-to-Synchro Converters (DSC) on board, the pinouts in Section 5.3 are directly applicable to the terminals labeled on the synchro or resolver load. When driving a synchro load with the board, the S4 pin for channel No. 0 and channel No. 1 will not be connected. The RH and RL signed pinouts connect directly to the rotor terminals labeled R1 and R2, respectively. RH and RL are common to both DRC and DSC channels.

5.6 BUILT-IN-TEST CONFIGURATION WITH SYNCHRO/RESOLVER TEST BUS

The VMIVME-4900 is designed to support both off-line and on-line fault detection and isolation when used in conjunction with the VMIVME-4910 or VMIVME-4911 Synchro/Resolver-to-Digital Converter (SDC/RDC) Board. Fault detection and isolation are accomplished by using multiple VMIVME-4900 boards and a single VMIVME-4910 or VMIVME-4911 in a wrapback configuration, via the VMIC Synchro/Resolver (SR) Test bus (SRTbus™).

Off-line testing is performed by disconnecting the DSC or DRC converters from the field, via relay K1 or K3, and by connecting the chosen DSC or DRC converter to the P2 connector, via relay K2 or K4, as shown in Figure 3.7-4. When the K2 or K4 relay connects a DRC or DSC to the test bus, the SR output can then be read by performing a read transfer from the 4910 or 4911 board.

On-line testing is similar to the off-line case, except that testing of the synchro/resolver converters can be accomplished while a load is being driven. This is accomplished by energizing relay K1 or K3, while relay K2 or K4 is used to connect the DSC/DRC under test to the SRTbus™ to be converted by the SDC board, as explained in Section 4.

NOTICE

FOR REAL-TIME FAULT DETECTION AND ISOLATION, THE IIOC REQUIRES THE USE OF VMIC'S VMIVME-4911. THE IIOC FIRMWARE IS NOT COMPATIBLE WITH THE VMIVME-4910.

CAUTION

WHEN USING MULTIPLE VMIVME-4900 BOARDS IN CONJUNCTION WITH THE SRTbus™, THE PROGRAMMER MUST NOT SWITCH MORE THAN ONE SYNCHRO/RESOLVER OUTPUT ONTO THE SRTBUS™ AT ANY ONE TIME. DOING SO MAY RESULT IN DAMAGE TO THE DSC OR DRC BOARDS, OR THE SRTBUS™ BACKPLANE OR TO BOTH. A ONE MILLISECOND MINIMUM DELAY MUST BE PROVIDED TO ALLOW A RELAY TO BECOME DE-ENERGIZED.

5.7 IIOC OPERATIONAL CONFIGURATIONS

A wide variety of S/R configurations are supported by the IIOC firmware. The firmware supports any number of SDC/RDC boards followed by any number of SDC/RDC boards, etc.

The IIOC firmware does not support configurations of DSC/DRC boards without a minimum of one SDC/RDC board. Also the IIOC firmware does not support configurations of SDC/RDC boards without a minimum of one DSC/DRC board.

The IIOC firmware supports off-line and on-line fault detection and isolation of SR boards by using a loop-test technique that requires a minimum of one SR input board and one SR output board in any system that requires either a SR input or SR output.

The IIOC test firmware operates (refer to Figure 5.7-1) by testing in a sequence (TS1) all VMIVME-4900 boards using the left most VMIVME-4911 board in the chassis. Test sequence three (TS2) depicts an example where two SDC/RDC boards are configured followed by six DSC/DRC boards. The test sequence (TS2) begins by testing the DSC/DRC boards (slots 7 through 12) by using the SDC/RDC board in slot 5. After TS2, TS3 begins by selecting the DSC/DRC board as the test board. This board is used to test the SDC/RDC boards in slots 5 and 6. Likewise, the configuration in slots 13 through 20 are tested in test sequence 4 and 5.

5.8 ADDRESS MODIFIERS

The VMIVME-4900 is configured at the factory to respond to short supervisory I/O access. The configuration can be changed by installing jumper J4 to enable the board to respond to short non-privileged I/O access.

5.9 ADDRESS SELECTION SWITCHES

The VMIVME-4900 occupies 16 bytes of the VMEbus short I/O address space. The upper 13 address bits are switch selectable, as shown in Figure 5.9-1.

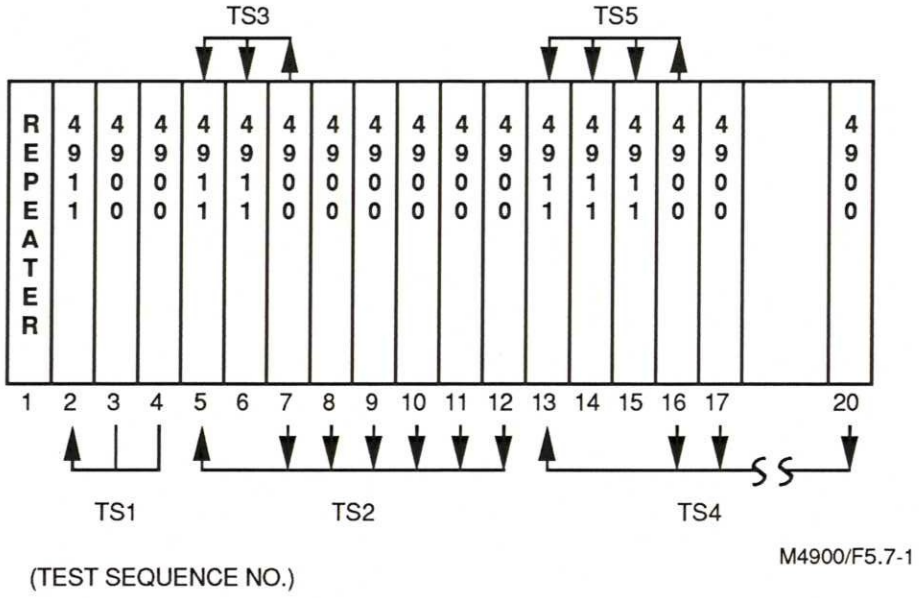


Figure 5.7-1. Sample Configuration and Test Sequences

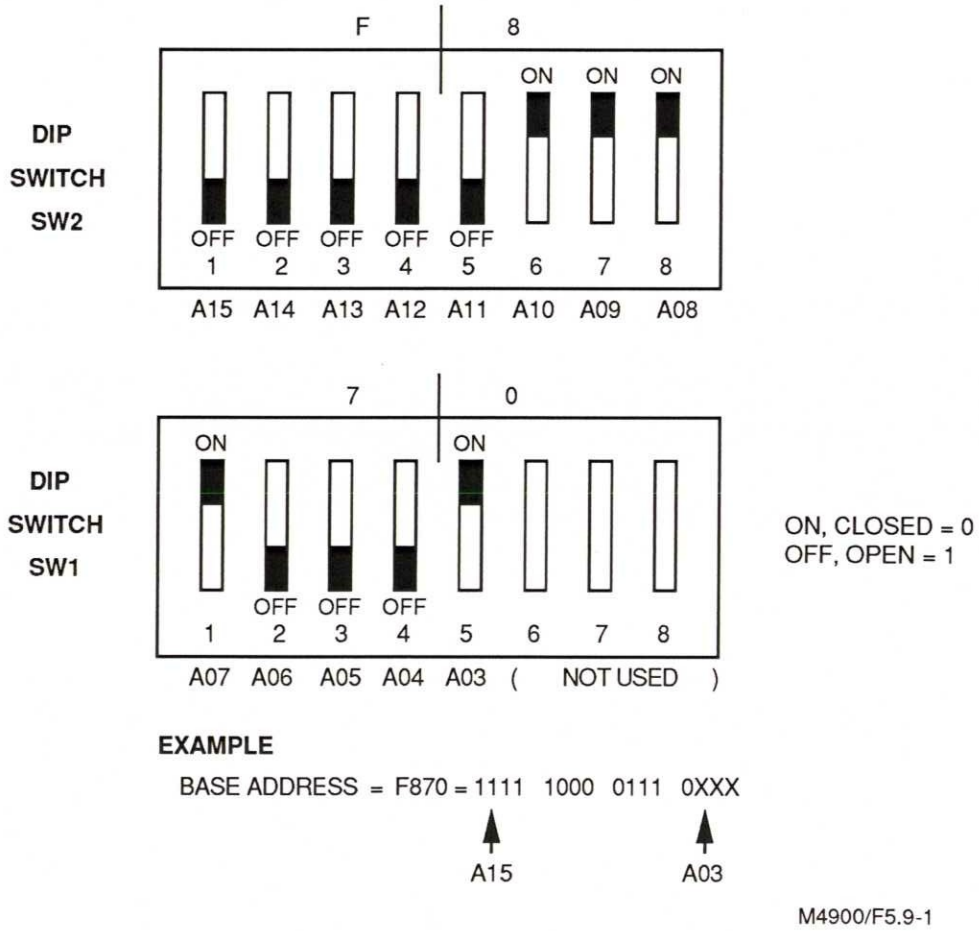


Figure 5.9-1. Base Address Switches

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC