VMIVME-1111

64-Bit Differential Digital Input Megamodule

Product Manual

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500-001111-000 Rev. V

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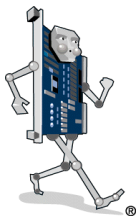

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Features

The VMIVME-1111 Differential Digital Input Board is designed to read a differential voltage from a variety of devices. The signals may originate from electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, Opto22 type signal conditioning modules or numerous other sources. The input signal conditioning circuits can also be configured by the user to accommodate high voltage current sink or voltage source options.

The VMIVME-1111 Differential Digital Input Megamodule™ has several unique features as specified below:

- 64 bits of differential or high voltage digital inputs
- Each group of 32 inputs are jumper selectable to monitor contact closure, voltage source, current sinking, or differential signals
- Open circuit provides logic "zero" or (jumper selectable) logic "one"
- Input filter option
- On-board Built-in-Test logic for fault detection and isolation
- Front panel with Fail LED
- User selectable input voltage thresholds (1.25 V to 66 V)
- RS422 / RS485 compatible differential line receivers provides ±7 V noise immunity
- VMEbus compatible
- 8-, 16-, 32-bit data transfers
- Double Eurocard form factor
- High reliability DIN type I / O connectors
- Compatible with the VMIVME-9016 Intelligent I / O Controller

Functional Description

The VMIVME-1111 is a member of VMIC's Megamodule™ family which is designed with common programming features such that subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these boards (VMIVME-1111, VMIVME-1110, VMIVME-2120, VMIVME-2130, VMIVME-2131 and VMIVME-2510B) is designed with two sets of board address switches or jumpers to provide an efficient memory address map for the Control Status Registers (CSRs) and I/O addresses. One set of these address switches or jumpers is for the CSR and may be set such that all CSRs among a variety of boards in a system may be mapped into contiguous memory locations. The other set of address switches or jumpers is for the I/O data registers, which can be mapped into their own contiguous but separate memory locations. The Megamodule™ product line is also designed to support 8-, 16-, and 32-bit data transfers. The board also features a front panel Fail LED that is illuminated at power-up reset and may be extinguished under program control upon successful completion of board level diagnostics. Specific hardware has been designed into the VMIVME-1111 to support Built-in-Test functions. The VMIVME-1111 supports both off-line and on-line fault detection and isolation.

Reference Material

For a detailed explanation of the VMEbus, refer to *The VMEbus Specification and Handbook* available from:

VMEbus Specification Rev. C1
and *The VMEbus Handbook*
VMEbus International Trade Association (VITA)
7825 Gelding Dr. Suite No. 104
Scottsdale, AZ 85620-3415
(602) 951-8866
Fax: (602) 951-0720
e-mail: info@vita.com
Internet: www.vita.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

Refer to VMIC Specification No. ***800-001111-000*** for a detailed explanation and physical description of the VMIVME-1111 64-Bit Differential Digital Input Megamodule. available from the following:

VMIC
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www.vmic.com

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

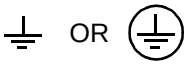
Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

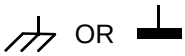
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



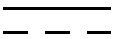
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, a practice or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER

1

Theory of Operation

Introduction

The VMIVME-1111 Differential Digital Input Board is designed to read a variety of signal inputs such as differential, electronic switching circuits, standard logic circuits, mechanical switch contacts, relay contacts, Opto 22 type signal conditioning modules, and numerous other sources, by letting the user change the configuration of the board's input circuits. The primary type of input signal conditioning electronics is differential. A typical input circuit design is shown in Figure 1-1 below. Input voltages up to 66 volts can be utilized.

The design of the VMIVME-1111 board, as shown in the functional block diagram (Figure 1-2 on page 18), consists primarily of the following four sections:

- VMEbus Compatibility Logic
- Device Addressing
- Input Signal Conditioning
- Built-in-Test Logic

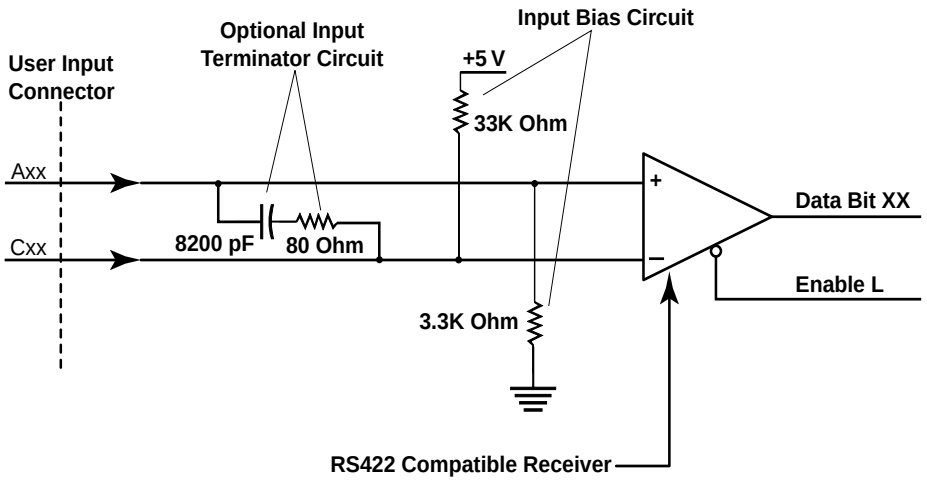


Figure 1-1 Differential Discrete Input Termination

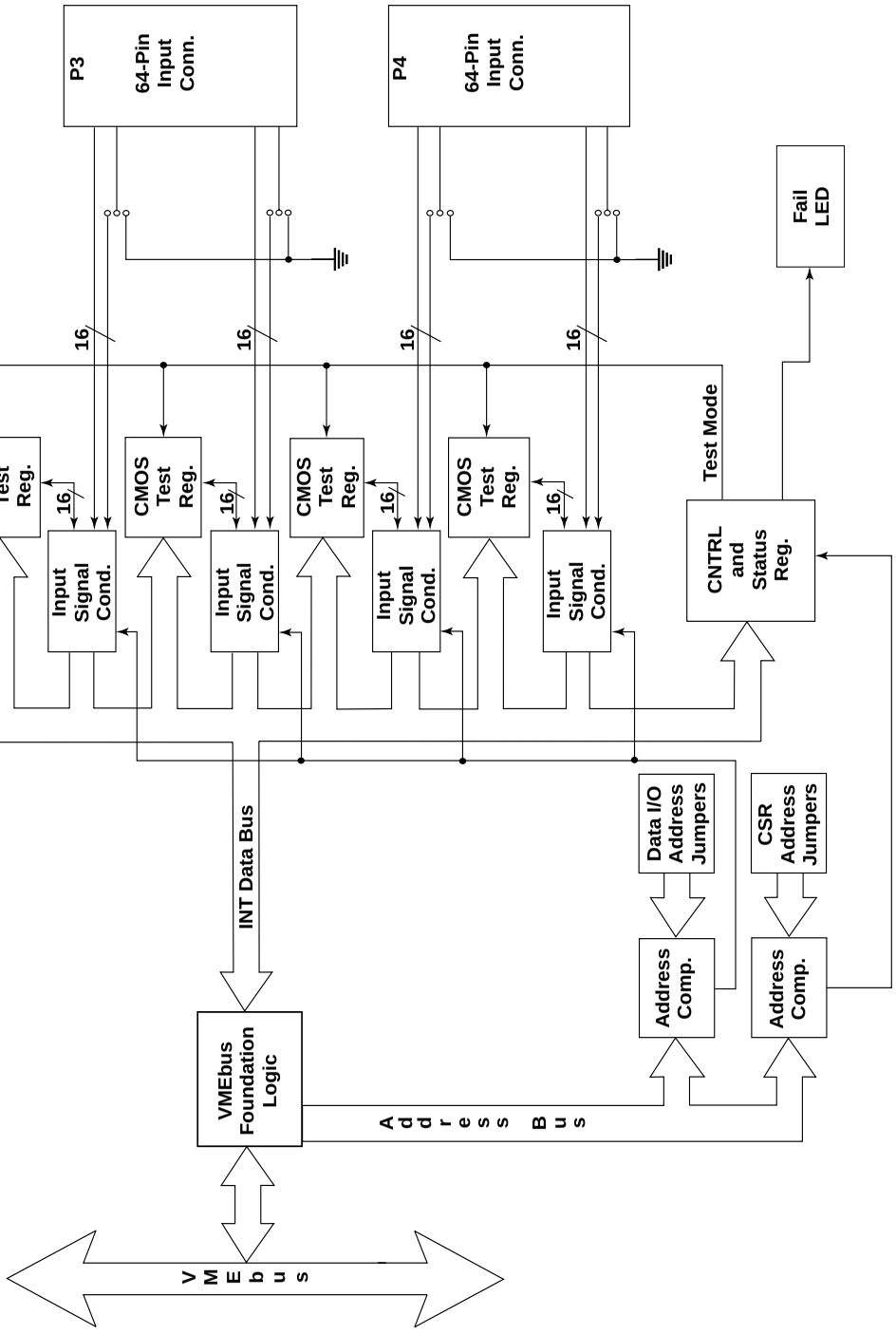


Figure 1-2 VMIVME-1111 Functional Block Diagram

Device Addressing

The VMIVME-1111 is designed to support data transfers in supervisory and/or non-privileged short I/O memory space. Two jumpers labeled AM2 are provided, as shown in Figure 1-3 (Address Selection Block Diagram), to allow user selection of either or both I/O access type for the Data Registers and the Control Status Register (CSR). The jumpers (AM2) are shown in Chapter 2 *"Configuration and Installation"*. The VMIVME-1111 is factory configured (jumpers AM2 not installed) to respond to short supervisory I/O access.

The VMIVME-1111 is designed with two sets of board select jumpers and decode logic, as shown in Figure 1-3, to provide an efficient memory address map for the CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into contiguous but separate memory locations when configuring subsystems that require more than one board.

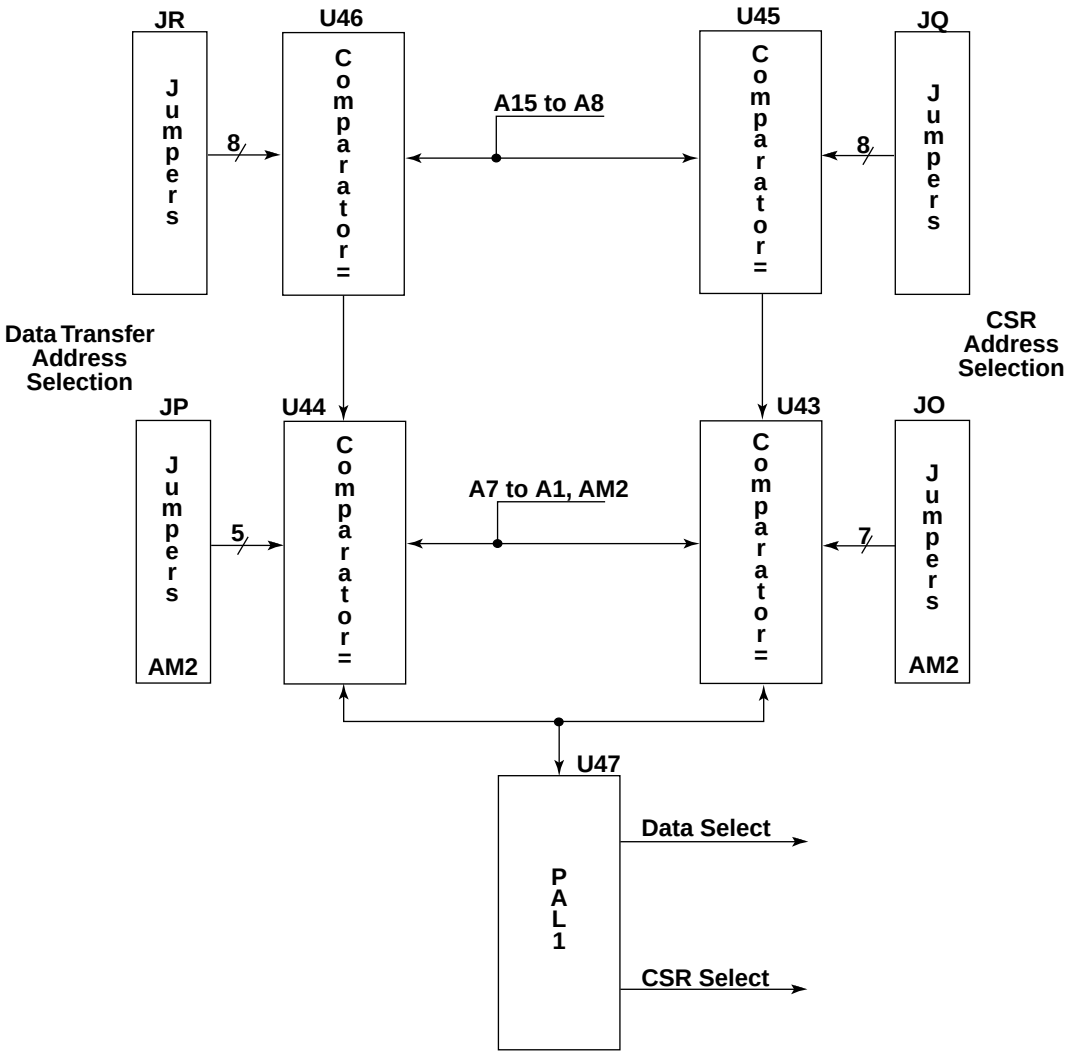


Figure 1-3 Device Address Selection Block Diagram

VMEbus Compatibility Logic

Typical VMEbus drivers, receivers, and control logic are shown in Figure 1-4 below and Figure 1-5 on page 21. Figure 1-4 shows the block diagram of the VMEbus control lines used by the VMIVME-1111. The DTACK generator is configured at the factory to provide the maximum data transfer rate possible with this board.

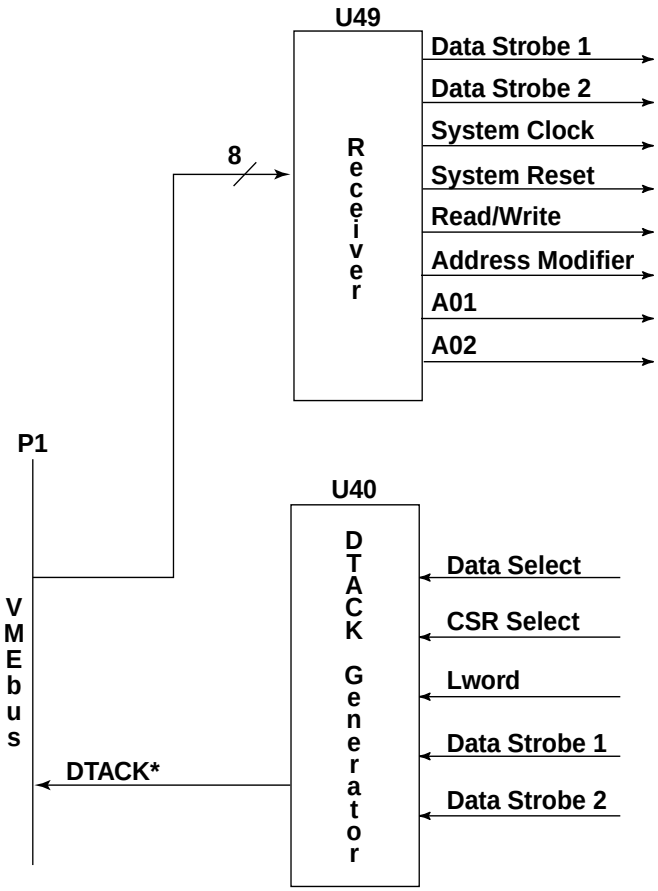


Figure 1-4 VMIVME-1111 Control Section Block Diagram

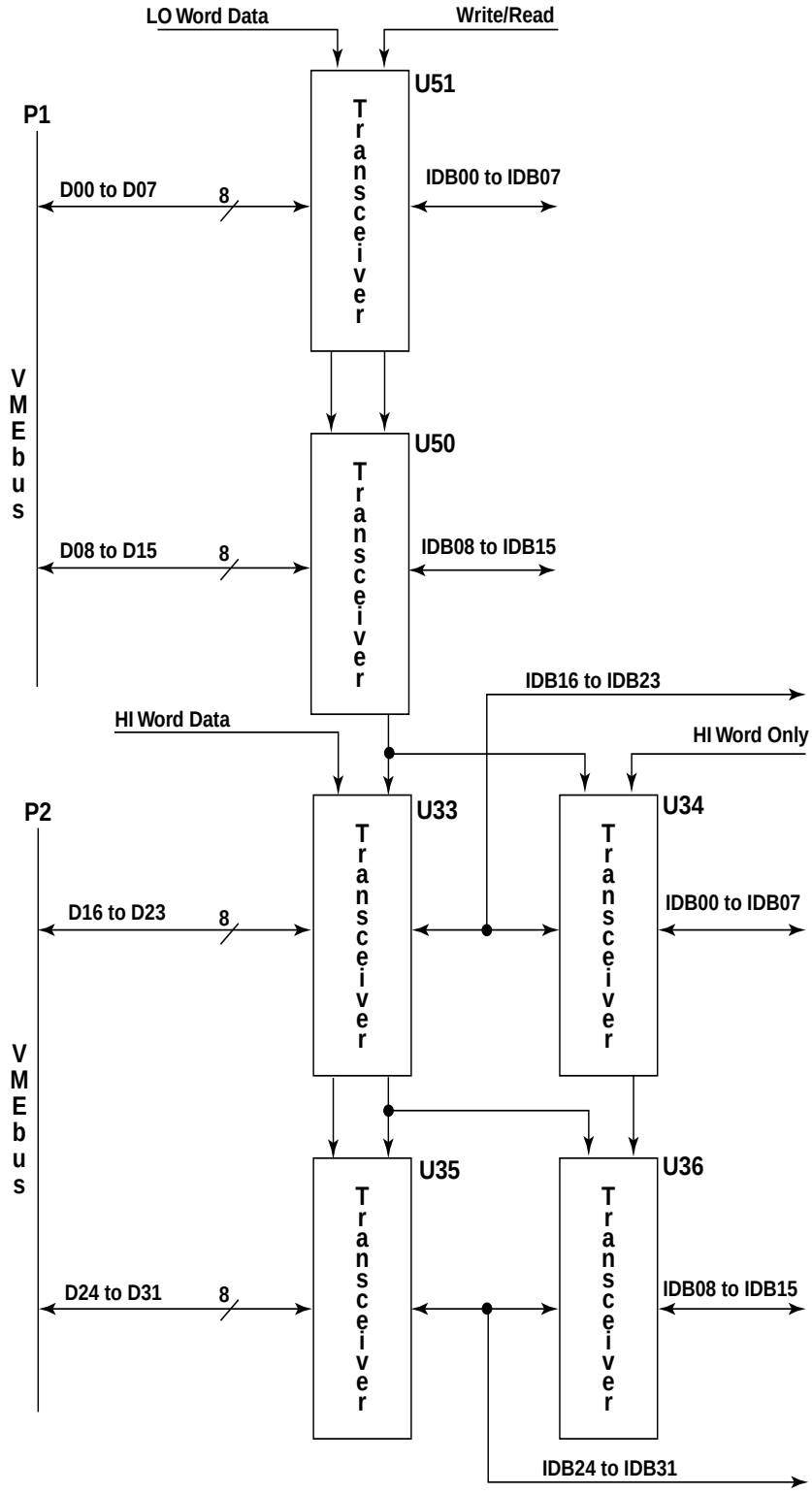


Figure 1-5 VMIVME-1111 Data Transfer Block Diagram

Data Transceivers

Data transfer transceivers are shown in Figure 1-5 on page 21. The VMIVME-1111 design supports 8-, 16-, and 32-bit data transfers.

Register Control Logic

The VMIVME-1111 board control is designed around four 16-bit read-only ports with signal conditioning and eight 8-bit CMOS test registers to support the Built-in-Test feature. The control logic shown in Figure 1-6 is separated into *read* and *write* control signals, which provides the capability to read or write 8-, 16- or 32-bits of data.

To perform input data transfers, data is transferred via transceivers, which are selected by address bit A1, DS0 and DS1. The 64 bits of differential voltage inputs may be addressed as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

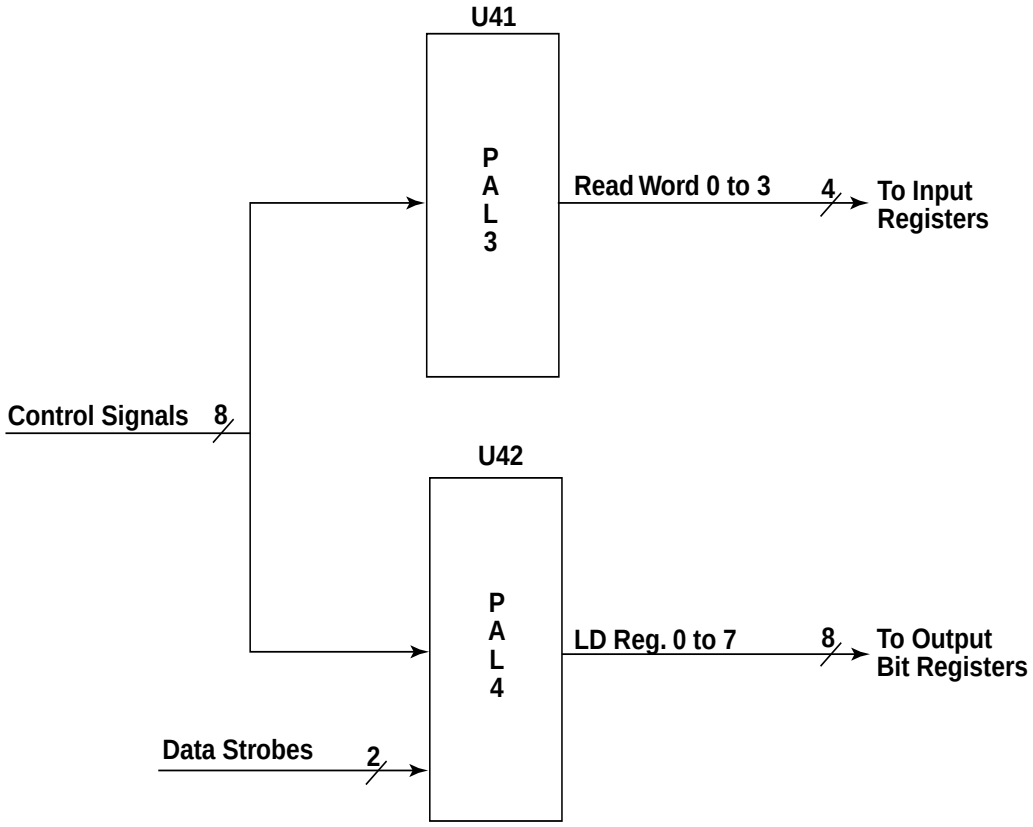


Figure 1-6 Register Control Logic Block Diagram

Control and Status Register (CSR)

The CSR is a *write only* register that controls the test mode bits and the Fail LED. The test mode bits enable the tri-state outputs of the CMOS test registers, allowing them to be used during Built-in-Test functions. The test mode has been split into two bits (Test Mode P3 and Test Mode P4) to allow half of the board to be active, while the other half is in test mode. Therefore, 32 inputs can be placed in test mode, while the other 32 inputs are not, and vice versa. A jumper (JS) is provided to maintain software compatibility with the VMIVME-1110, which only uses one test mode bit. If this board is to use only one test mode bit, then jumper JS goes to position 3 (as shown in Figure 1-7 below). If the board is to support two test mode bits, then jumper JS goes to position 1. The bit locations used by the VMIVME-1110 are valid here too. Bit 7 is used for test mode (VMIVME-1110 compatible) or for test mode P3 (split test mode). When the VMIVME-1111 is using split test mode, Bit 7 is used for test mode P3; bit 5 is used for test mode P4. In either case, bit 6 is always used to control the Fail LED. These signals are initialized active at power-up or after a system reset and are shown in Figure 1-7. While in the test mode, the effected inputs will not accept active user input data. To disable test mode and / or to turn off the Fail LED, a logical “one” must be written to the appropriate bit(s) of the CSR.

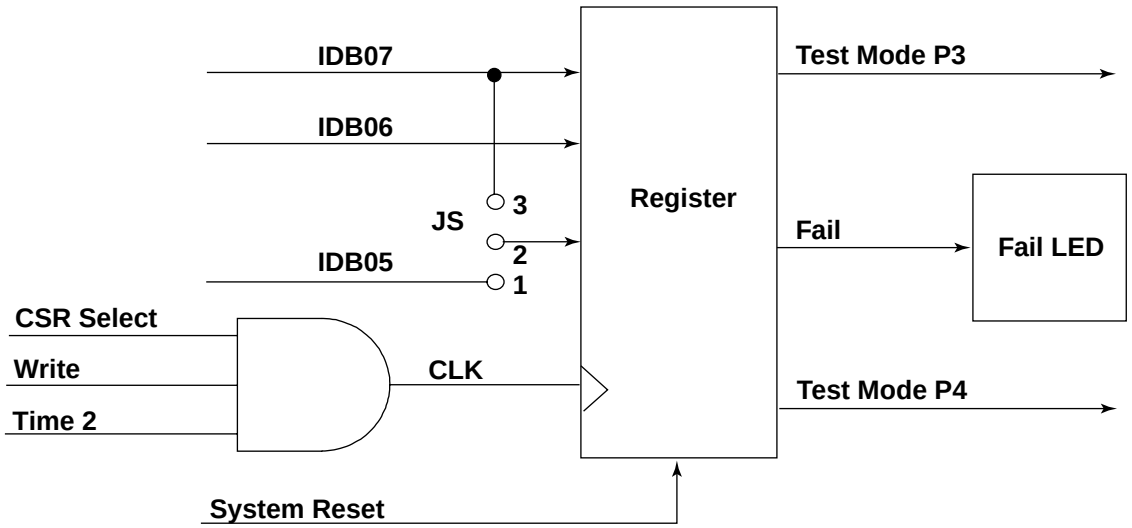


Figure 1-7 VMIVME-1111 CSR Control Logic Block Diagram

Board ID Code Register

The VMIVME-1111 is designed with a Board Identification (BD ID) register as part of the Control Status Register (CSR). The block diagram of this register is shown in Figure 1-8 below. The lower byte of the CSR is the control register, which contains the test mode bits, Fail LED bit and is a *write only* register. The upper byte of the CSR is used for the Board ID code of the VMIVME-1111. This is a *read only* register, and its value is 01 HEX.

The Board ID code register allows the VMIVME-9016 IIOC (Intelligent I/O Controller) to identify the boards it controls in the systems. This way the IIOC can set up its system configuration automatically, eliminating possible human error.

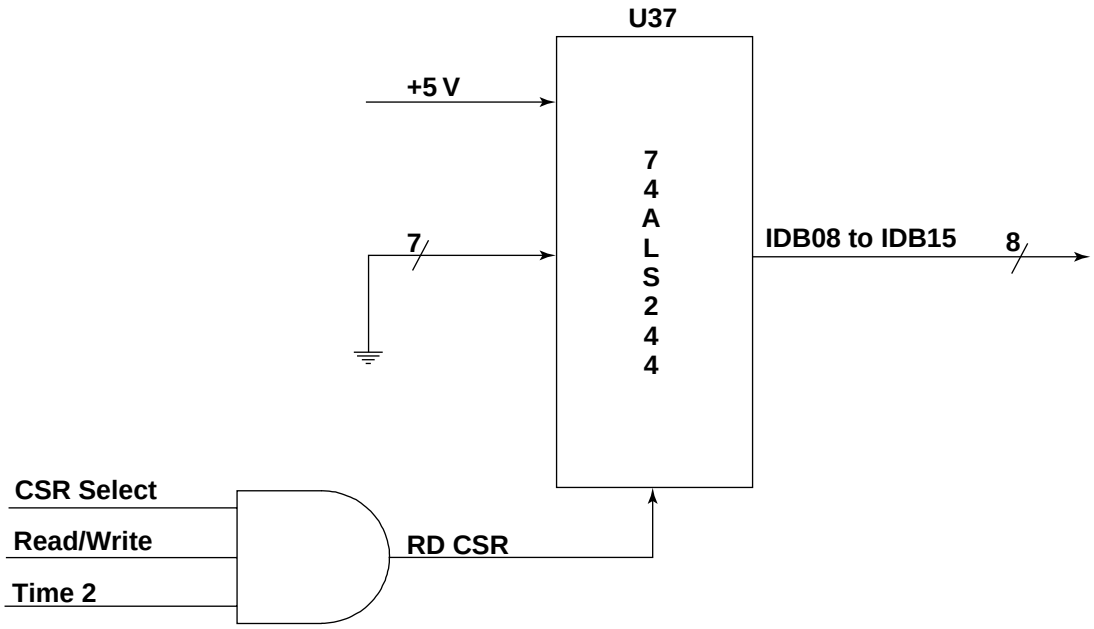


Figure 1-8 Board ID Register Logic Block Diagram

Test Registers

The VMIVME-1111 is designed utilizing eight 8-bit CMOS test registers to support the Built-in-Test features. The outputs of the test registers (labeled CIxx) are connected to the input comparators, as shown in Figure 1-9 on page 25. The test registers may be accessed on a byte by byte basis and they are labeled accordingly (R7 for register 7, etc.). The test registers use the non-inverting inputs of the comparators and the diagnostic software must assume positive true operations, even though the board may be configured for negative true inputs.

The comparator outputs (labeled COxx) go to the input data read registers (labeled DRx in Figure 1-11 on page 27). These registers are read as a word, as shown in Figure 1-11. From these data registers, data goes to the VMEbus foundation logic and then to the VMEbus. This configuration enables 100 percent testing of all the active devices on the board.

The Built-in-Test feature of the VMIVME-1111 is enabled by clearing the appropriate test mode bit to zero in the CSR. The VMIVME-1111 is built with two test mode bits. This allows half of the board to be in normal mode and accepting active data, while the other half is in test mode and processing test data. Please refer to the section titled “Control and Status Register (CSR)” on page 23 of this manual for a more detailed explanation of the use of the test mode bits.

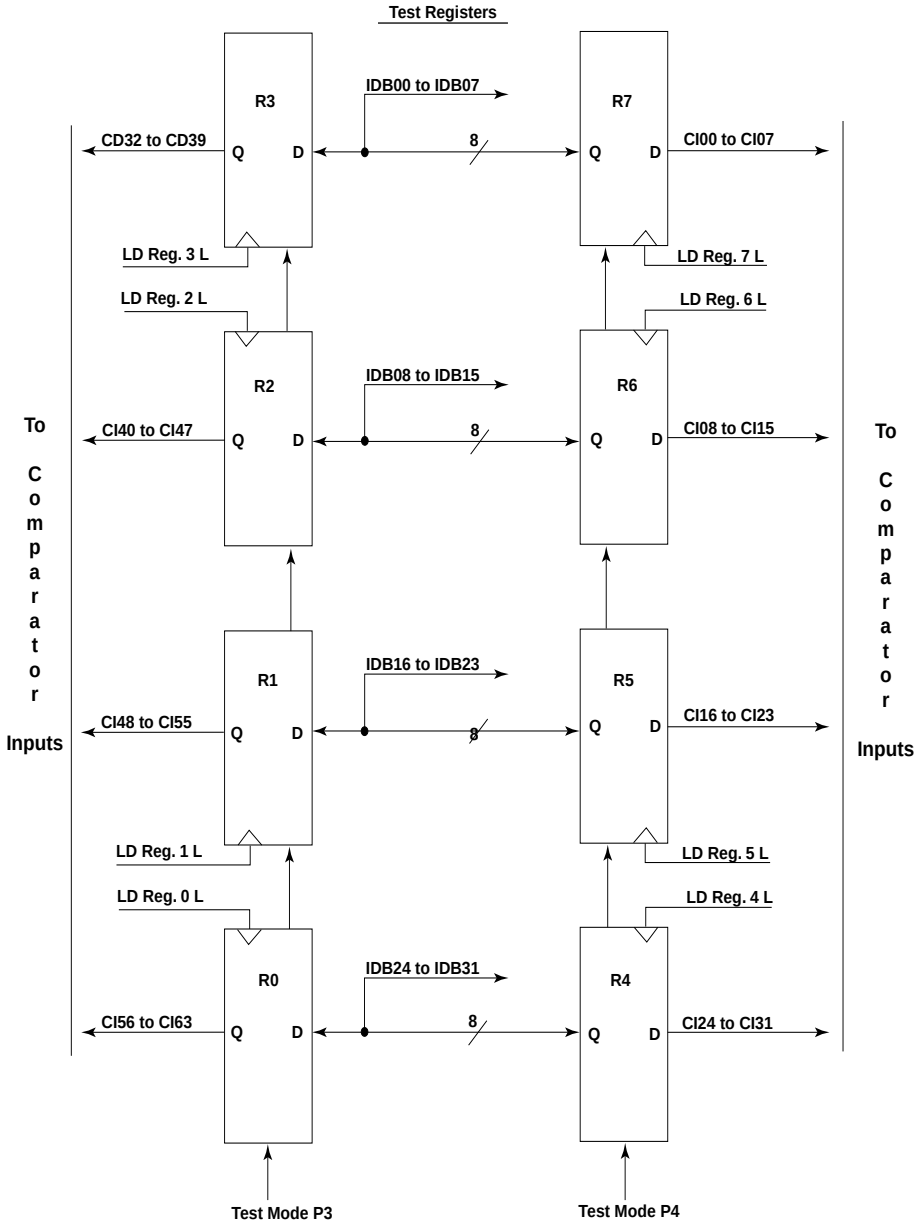


Figure 1-9 VMIVME-1111 Self-Test Logic (Test Data Registers) Block Diagram

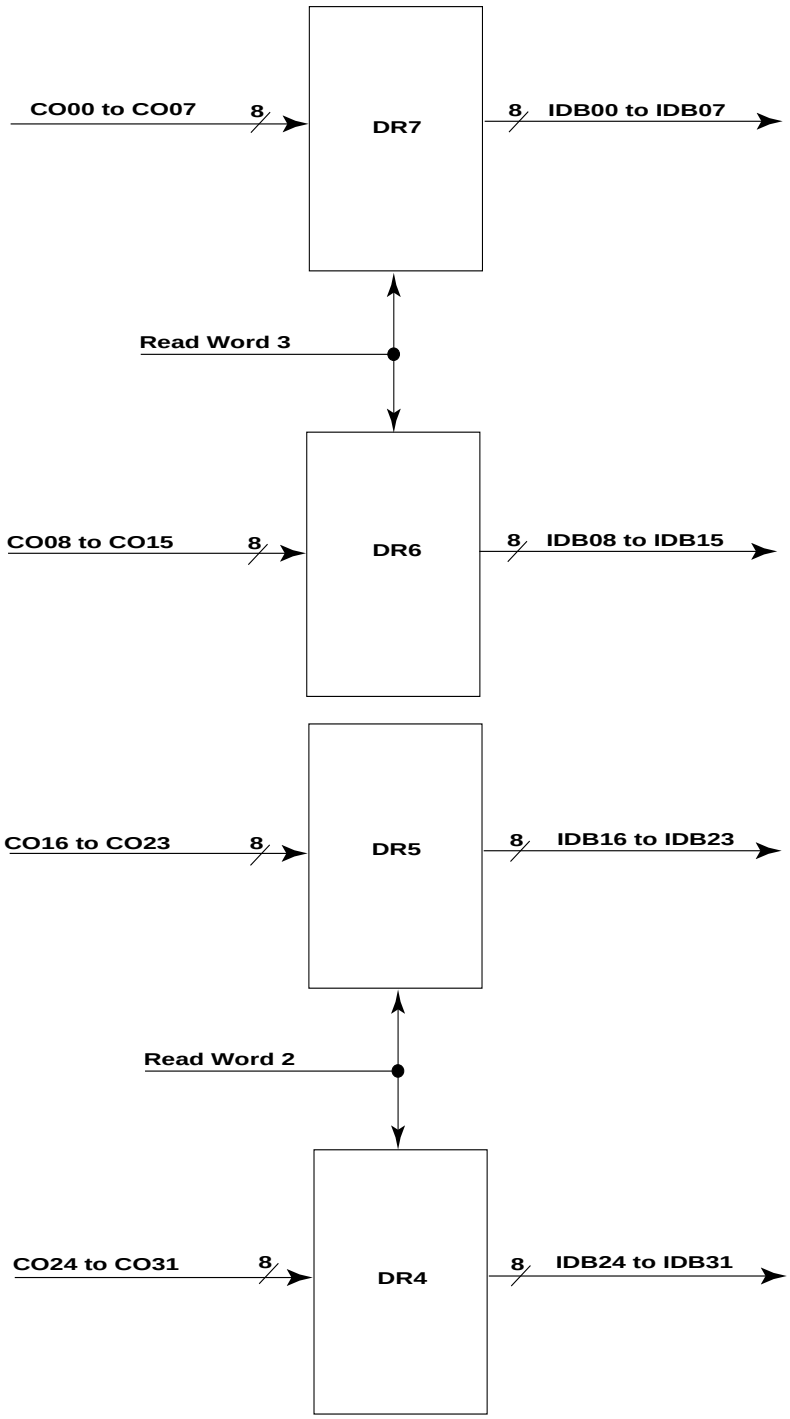


Figure 1-10 Input Data Registers Block Diagram (Sheet 1 of 2)

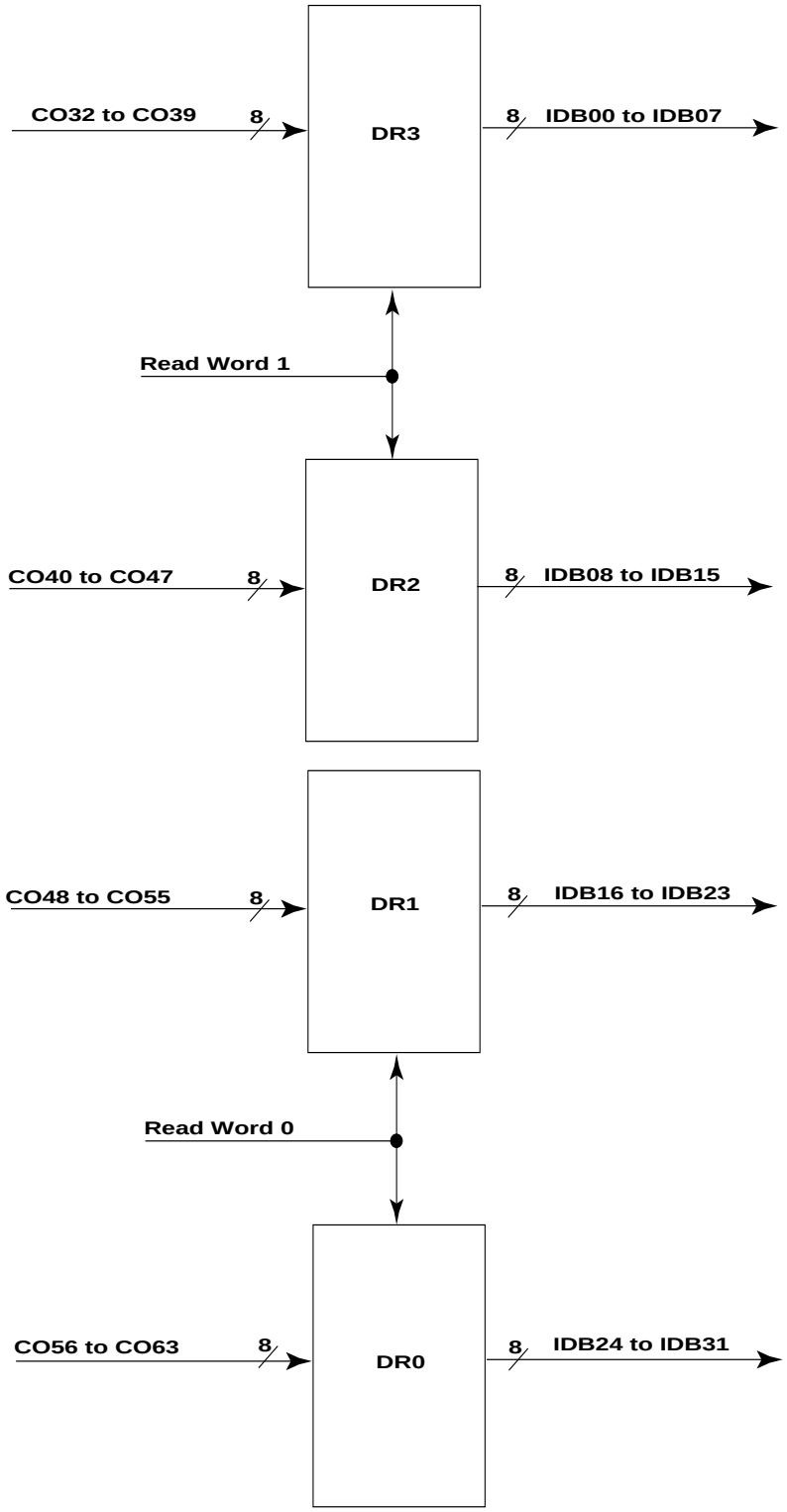


Figure 1-11 Input Data Registers Block Diagram (Sheet 2 of 2)

CHAPTER
2

Configuration and Installation

Contents

Introduction

This chapter leads you through the configuration and installation of the VMIVME-1111 64-Bit Differential Digital Input Megamodule.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. This board can be installed in any slot position, except slot one which is reserved for the system controller.

WARNING: Do not install or remove the board while power is applied.

Installation

This section describes the various input configurations that the VMIVME-1111 can utilize. The VMIVME-1111 can have half of its inputs set up for one type of input, or voltage level, while the other half is set up for some other type of input. The VMIVME-1111 splits the inputs by the input connector with which it is associated. Input channels CH00 to CH31 go with P4 configurations, and input channels CH32 to CH63 go with P3 configurations. Thus, the user can set up the inputs coming from connector P3 differently from the inputs coming from connector P4. A particular configuration can also handle a wide range of voltages.

The location of factory configurable jumpers and interchangeable SIPs on the VMIVME-1111 are shown in Figure 2-1 on page 32. The usage of the jumpers are listed in Table 2-1 below. The configuration of these jumpers is discussed in the following sections.

Table 2-1 Jumper Usage

Jumper Reference	Usage
JE → JD	P4's Row C Pins
JE → JH	P3's Row C Pins
J1	External Reference Voltages
JK	P4's Input Bias
JL	P3's Input Bias
JM	P4's Comparator Bias
JN	P3's Comparator Bias
JO, JQ	CSR Address Selection
JP, JR	Data Registers Bse Address Selection
JS	Split Test Mode

Before Applying Power: Checklist

Before installing the board in a VMEbus system, perform the following checklist to verify that the board is ready for the intended operation:

1. Have Sections 1 and 3 on Theory and Programming of the VMIVME-1111 been read and applied to system requirements?_____
2. Review this chapter to verify factory installation of the jumpers. _____
   —To change the address jumpers refer to"Address Selection Jumpers" on page 35.
   —To change address modifier response, refer to "Address Modifiers" on page 36.
3. The VMIVME-1111 is designed to accommodate a wide variety of input signals. The types of inputs available are listed in Table 2-2 on page 34, as well as a figure which shows a typical input jumper configuration and a typical input circuit. Set up the necessary jumpers and resistor SIPS to make the circuit indicated in Table 2-2 on page 34, record the pull up and pull down resistor values in Table 2-3 on page 58, and be sure the desired circuit is properly configured._____

4. Have the cables, with proper mating connectors, been connected to the input connectors? Refer to “I/O Cable and Card-Edge Connector Configuration” on page 62. _____

After completing the check list, the VMIVME-1111 Board may be installed. (Do not install or remove the board with power ON unless the extended ground pin option is ordered.) Generally the VMIVME-1111 may be installed in any slot position except slot one, which is usually reserved for the system controller processing unit.

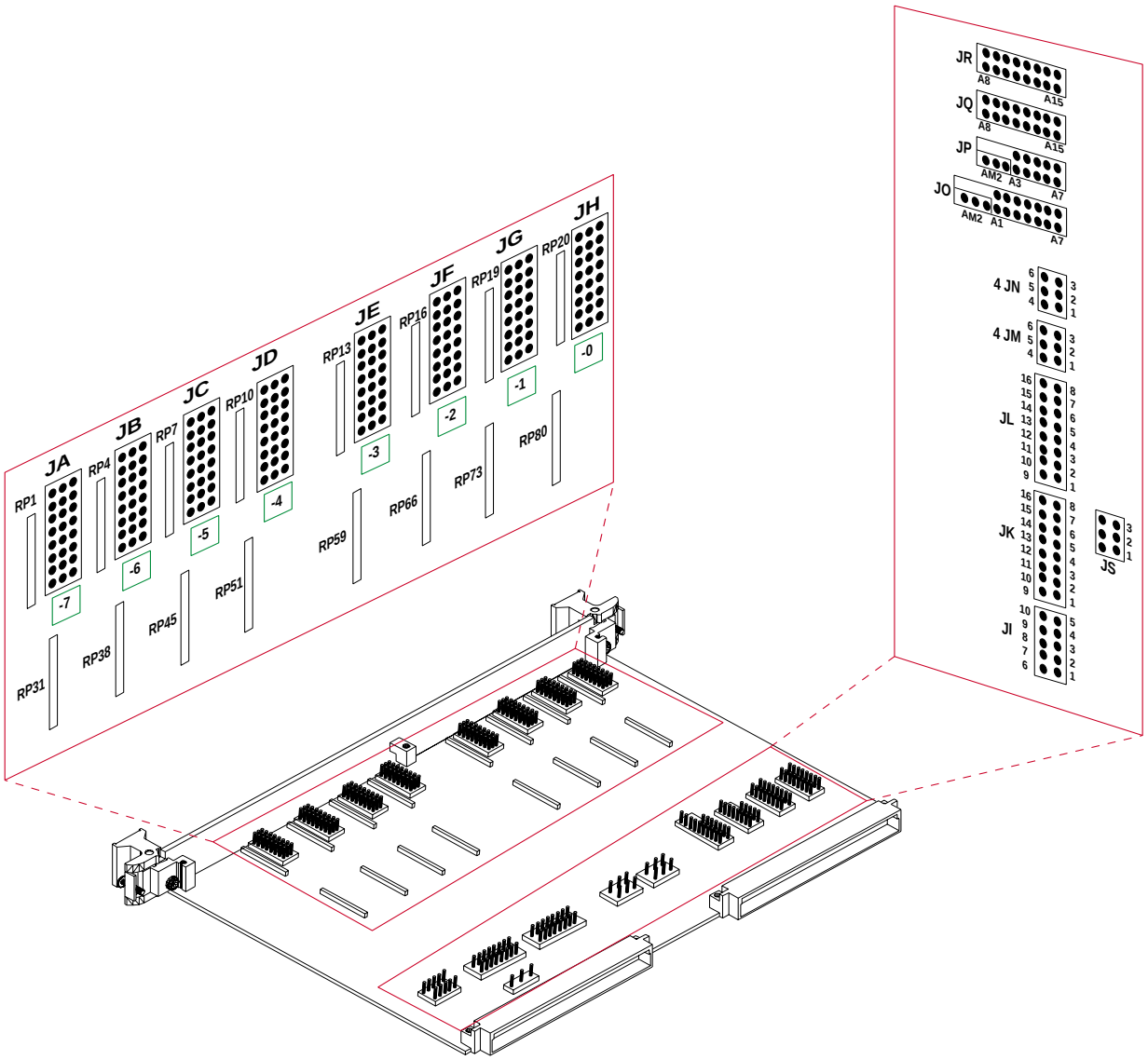


Figure 2-1 Location of Factory Configurable Jumpers and SIPs

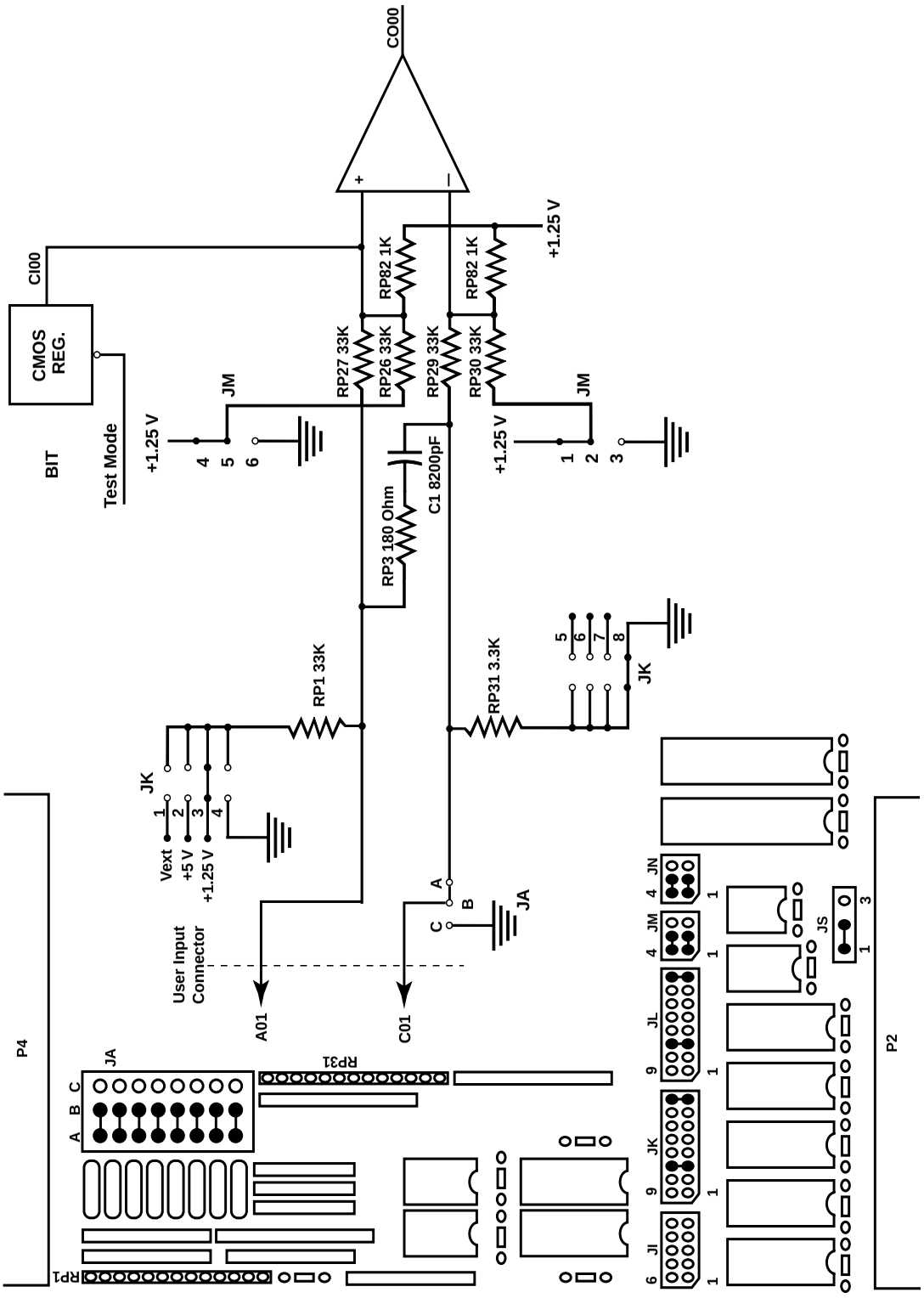


Figure 2-2 Jumper Configuration and Input Circuit for Factory Configuration

Table 2-2 Input Circuit Configuration

TYPE OF INPUT CIRCUIT	FIGURE NUMBER
a. Differential Inputs	Figure 2-6
b. Current Sinking; positive true	Figure 2-8
c. Current Sink; negative true	Figure 2-10
d. Contact Closure; positive true	Figure 2-12
e. Contact Closure; negative true	Figure 2-14
f. Voltage Sourcing; positive true	Figure 2-16
g. Voltage Sourcing; negative true	Figure 2-18
h. Voltage sourcing; TTL compatible positive true	Figure 2-20
i. Voltage sourcing; TTL compatible negative true	Figure 2-22

The process of configuring the board is as follows:

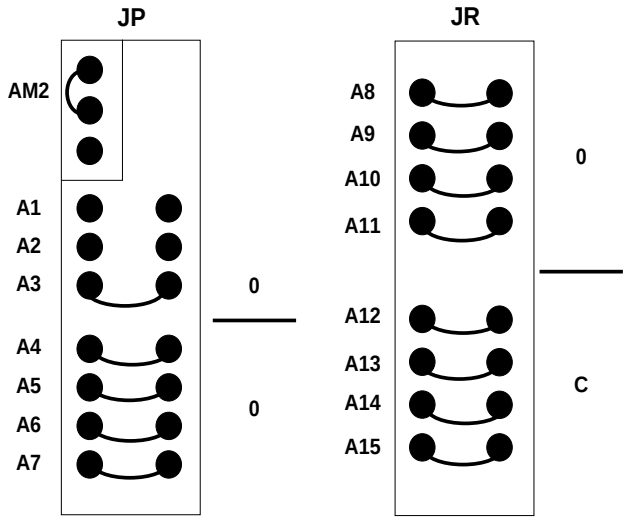
- First, determine the type of input circuit desired. Then, using the figure indicated in Table 2-2 configure the input bytes as needed. Remember that these figures will show the configuration for byte 7 of P4 (in other words, input channel 00). These figures are here as a guide only. They are meant to help the user in choosing the proper circuit and in configuring the jumpers for the associated input connector. Also remember that all bytes associated with an input connector should be configured the same. Copies of Figure 2-25 on page 57 should be used to document the final configuration chosen for the particular application of this board.

Before Applying External Power

Before applying external power to P3-ROWC-Pin 32, verify that jumper JH8 has been removed. Likewise, before applying external power to P4-ROWC-Pin 32, verify that Jumper JD-8 has been removed. Applying external power to these pins with these jumpers installed B to C will short external power to ground and destroy the VMIVME-1111.

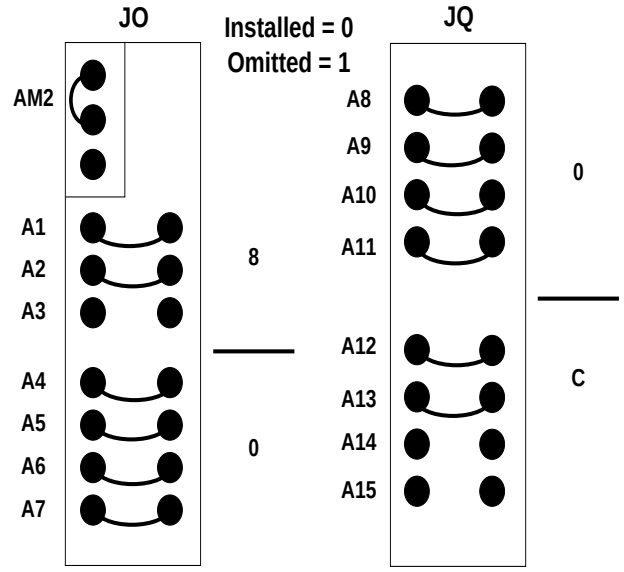
Address Selection Jumpers

Address selection jumpers are provided on the VMIVME-1111 to select the input port base address and the CSR address. See Figure 2-1 on page 32 for the jumper locations. The Input Port Device Address may be selected as shown in Figure 2-3 below. The CSR base address may be selected by positioning jumpers as shown in Figure 2-4 below. The jumper selections shown represent the factory configuration of the board.



The example shown is for a base address of C000.

Figure 2-3 Input Port Address Select Jumpers



The example shown is for a base address of C008.

Figure 2-4 CSR Select Jumpers

Address Modifiers

The VMIVME-1111 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumpers JP-AM2 and/or JO-AM2. These jumpers are the address modifier jumpers (AM2). The jumper JP-AM2 is used by the input data registers, and JO-AM2 is used by the CSR. They can be configured such that the board will respond to short supervisory (AM2 not installed), to short non-privileged (AM2 installed low), or to either I/O access (AM2 installed high). The jumper positions are shown in Figure 2-5 below.

Figure 2-5 Address Modifier Selections

Input Signal Conditioning Selection

The input circuitry of the VMIVME-1111 allows the user to select the kind of input conditioning he wishes to have without specifying it when ordering. The input circuits can be changed to meet changing needs. Table 2-2 on page 34, Figure 2-6 through Figure 2-24, and Table 2-3 on page 58 are guides to help in the configuration of this board. A work sheet for user jumper configuration of the board is shown in Figure 2-25 on page 57.

The figures show only one typical input circuit for connector P4, but they are applicable to all inputs for both connectors (P3 and P4). Headers JA, JB, JC and JD set up the input return pins (Row C) of connector P4, while headers JE, JF, JG and JH perform the same function for connector P3. Each header is associated with an input byte.

The figures also show the jumper headers for input bias (JK) and comparator bias (JM). These headers are used by all 32 input circuits associated with input connector P4. Jumpers JL and JN are the P3 counterparts of JK and JM. With this arrangement, inputs from P4 can be set up in one configuration and the inputs from P3 in another way.

Once an input circuit configuration is decided upon, refer to Table 2-2 on page 34 for the figures showing a typical input circuit and the jumper SIP configuration for that circuit. Then using Figure 2-2 on page 33, configure the rest of the jumpers and the input bias SIPS used by the corresponding input connector. The user can document this configuration by using copies of Figure 2-25 on page 57.

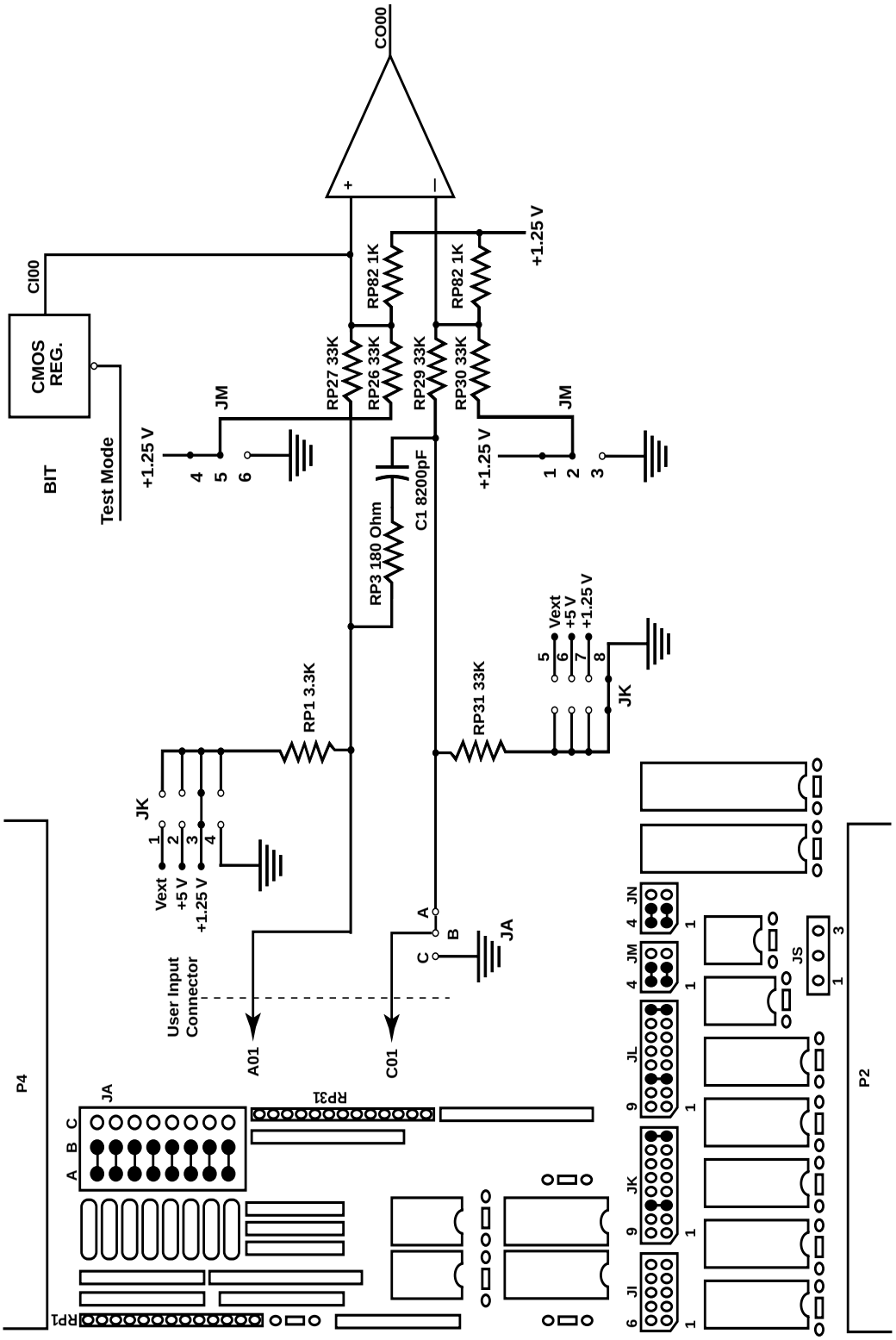
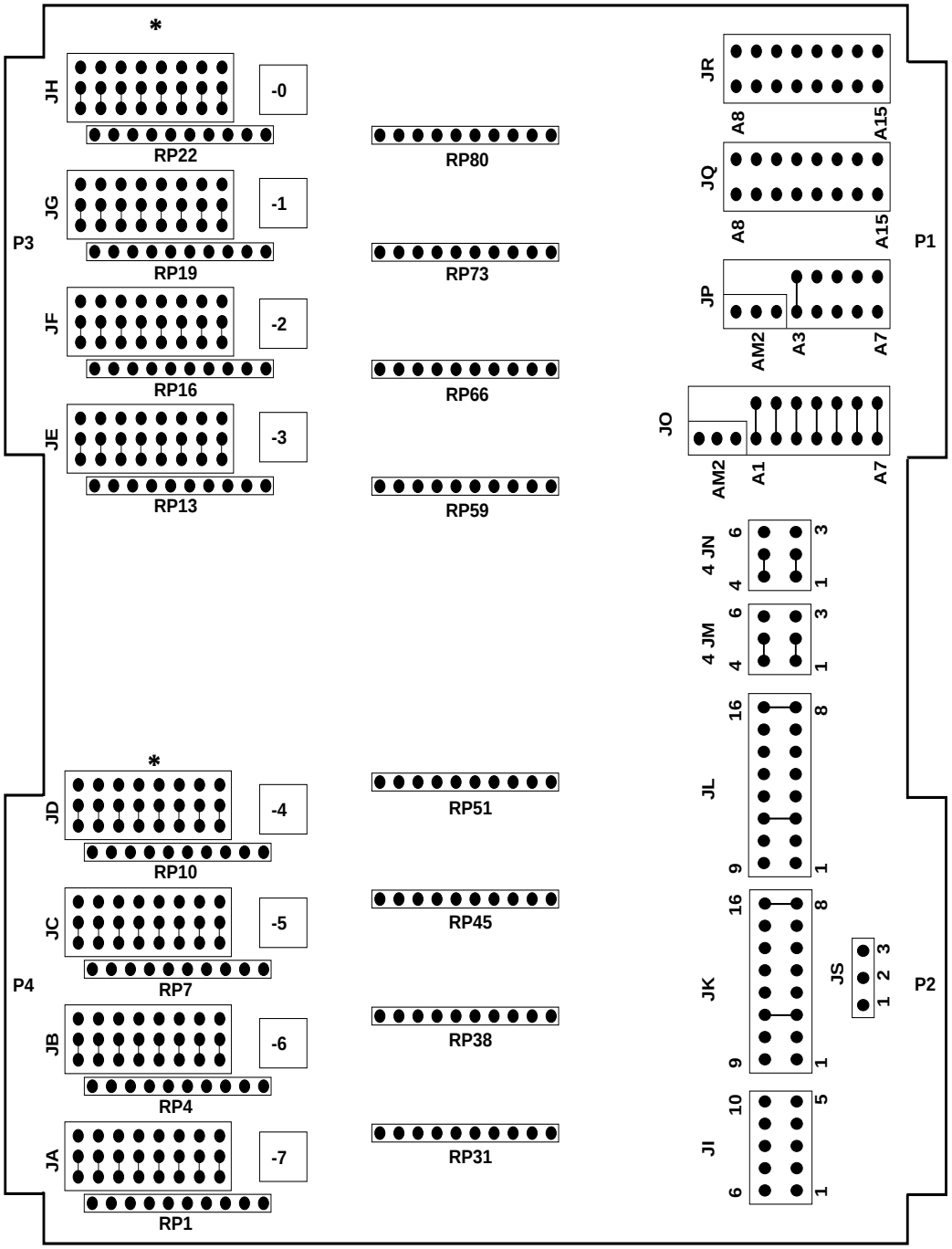


Figure 2-6 Jumper Configuration and Typical Input Circuit for Differential Inputs



NOTE: *These jumpers **MUST** be removed to route external voltages to the P3/P4 front panel connectors. Please refer to <TBD> for a thorough explanation of this option.

Figure 2-7 Jumper Configuration for Differential Inputs

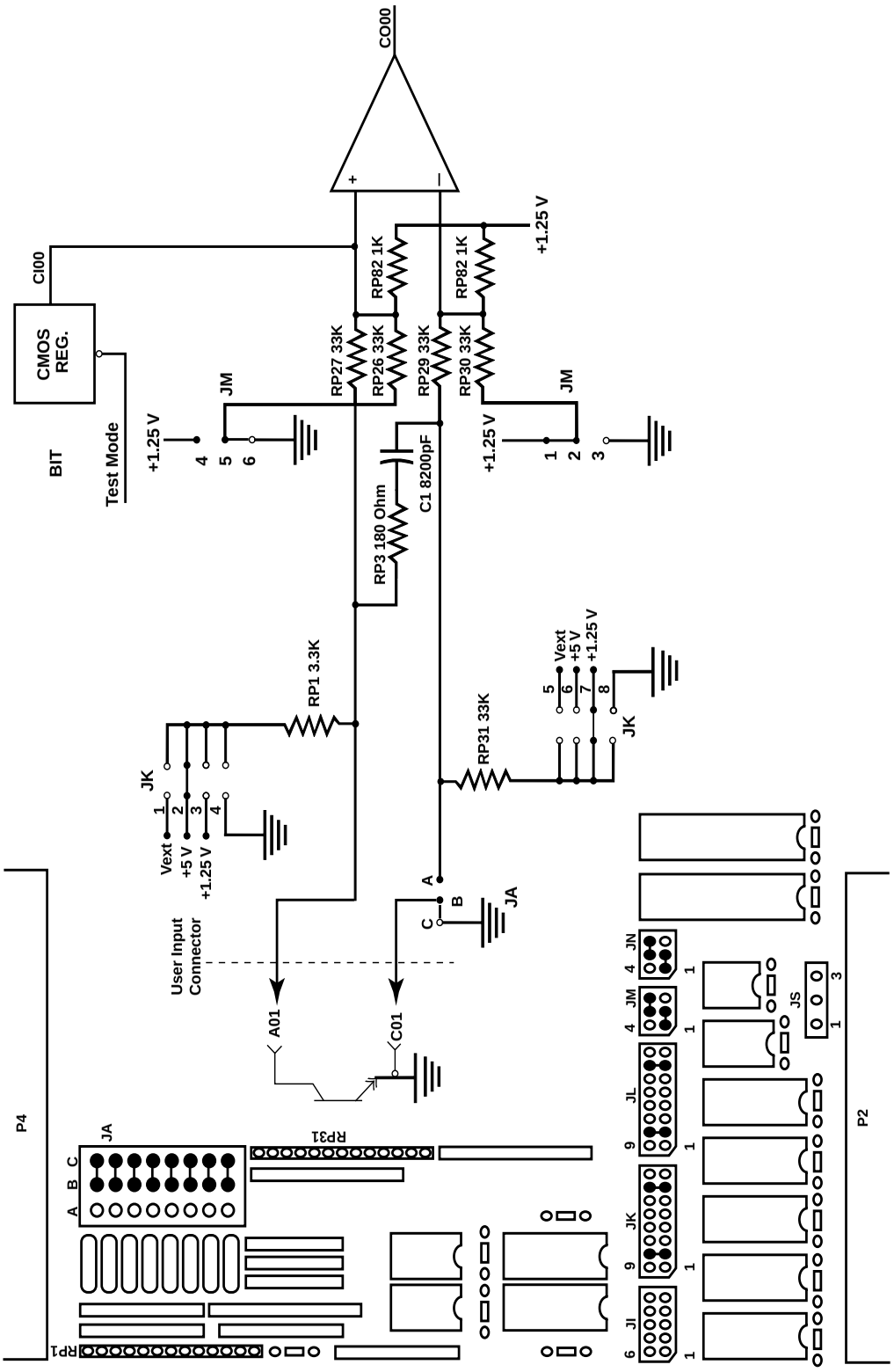
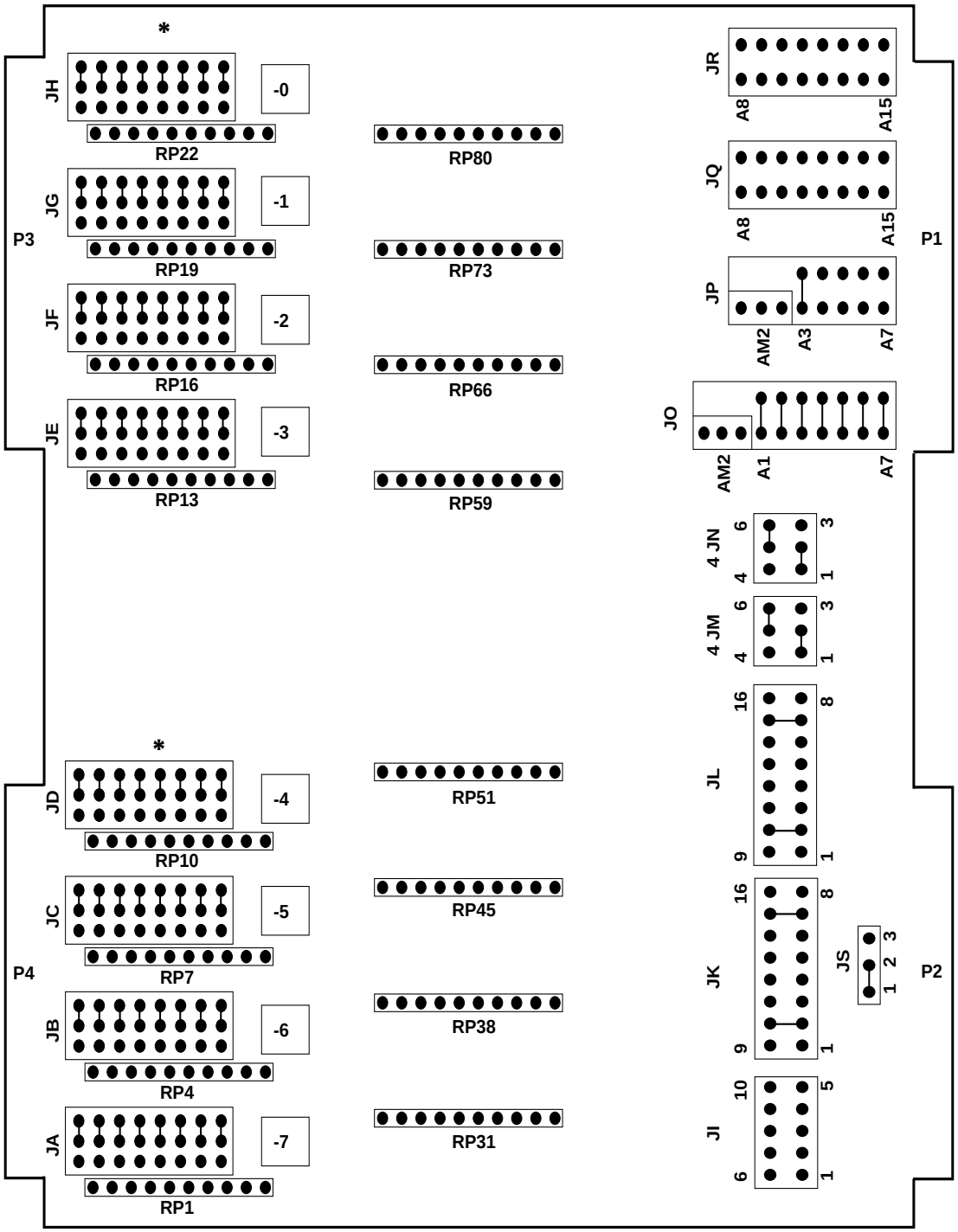


Figure 2-8 Jumper Configuration and Typical Input Circuit for Current Sink, Pos True



NOTE: *These jumpers **MUST** be removed to route external voltages onto the board using the P3/P4 front panel connectors.

Figure 2-9 Jumper Configuration for Current Sink, Pos True

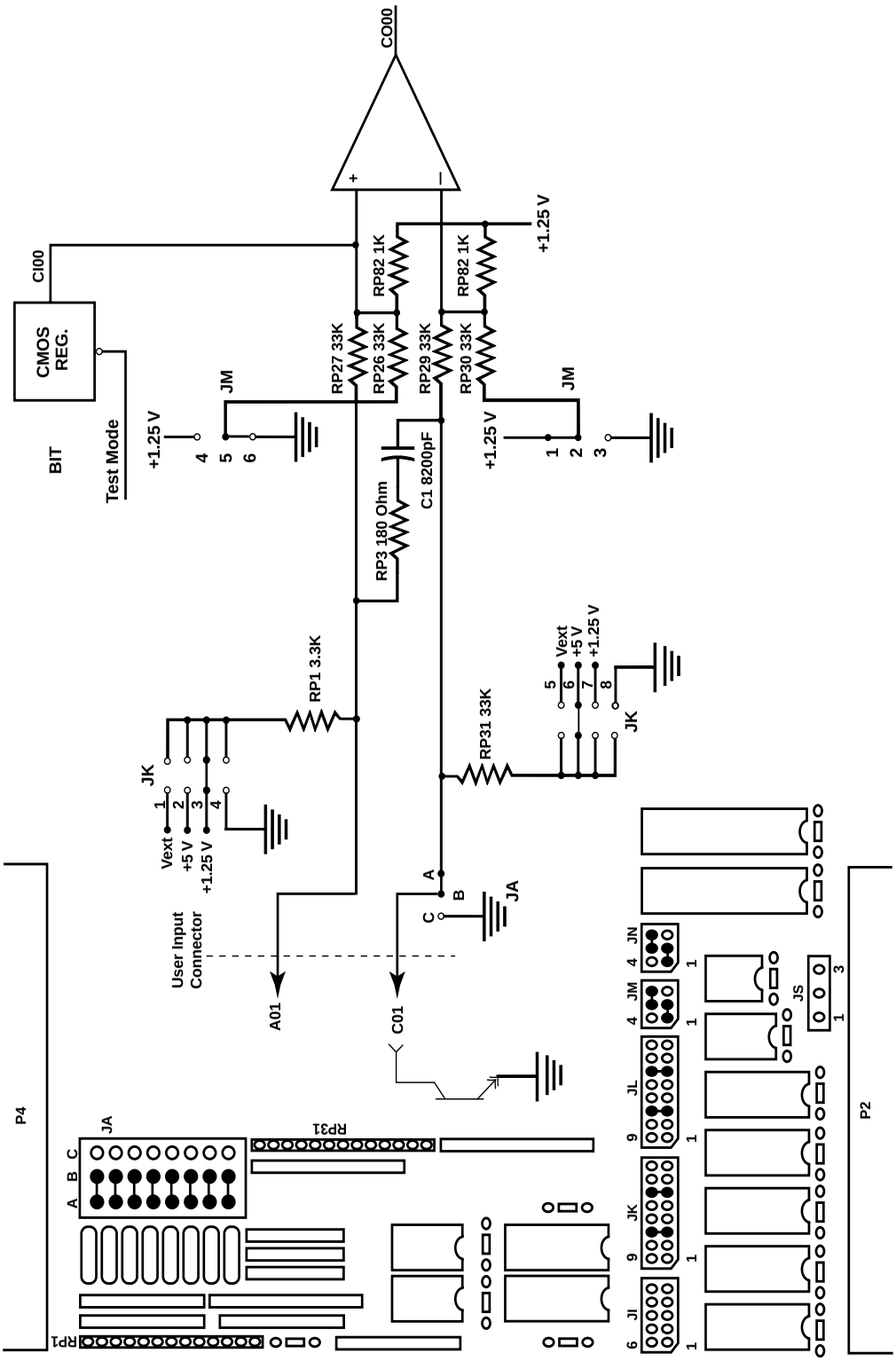
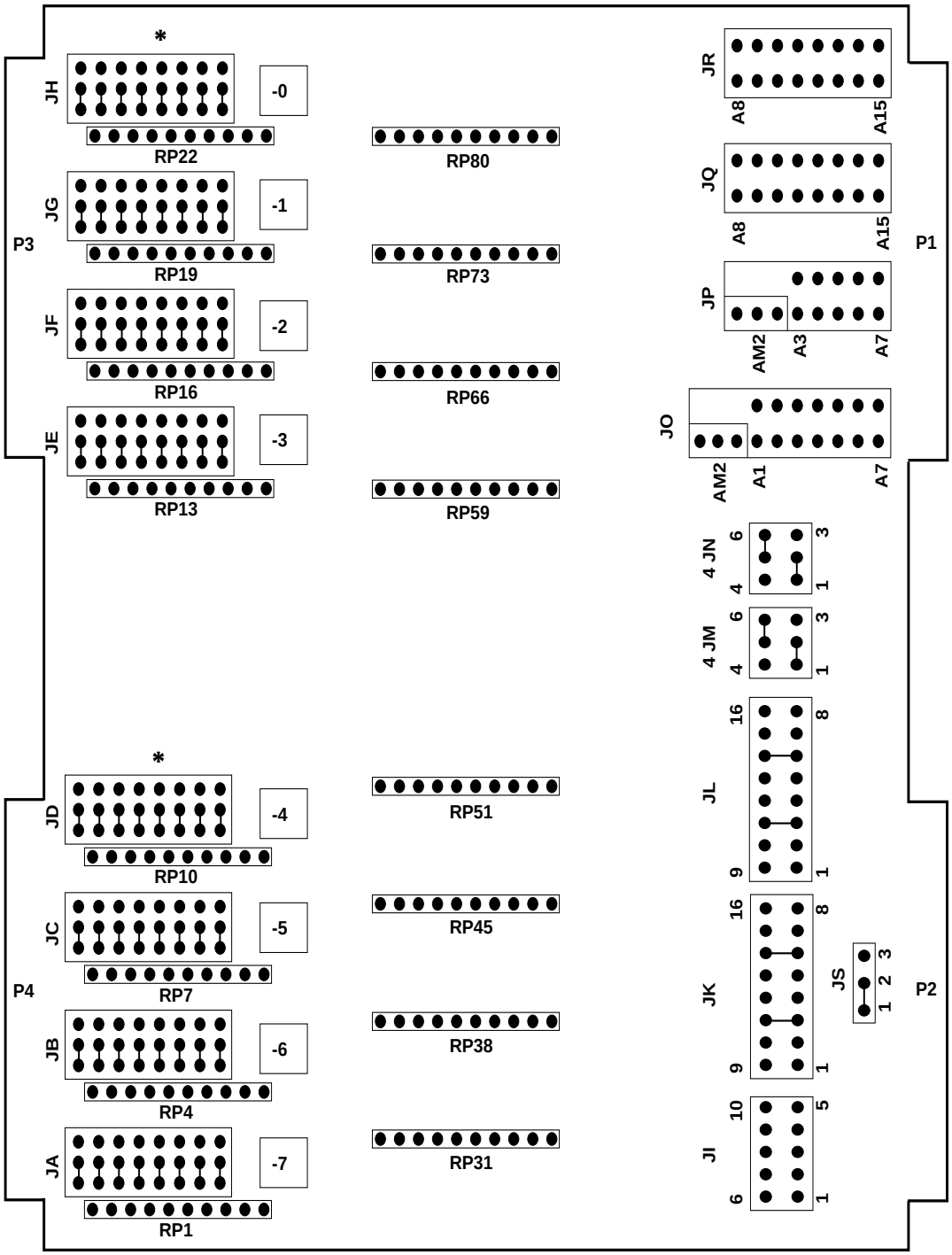


Figure 2-10 Jumper Configuration and Typical Input Circuit for Current Sink, Negative True



NOTE: *These jumpers **MUST** be removed to route external voltages onto the board using the P3/P4 front panel connectors.

Figure 2-11 Jumper Configuration for Current Sink, Negative True

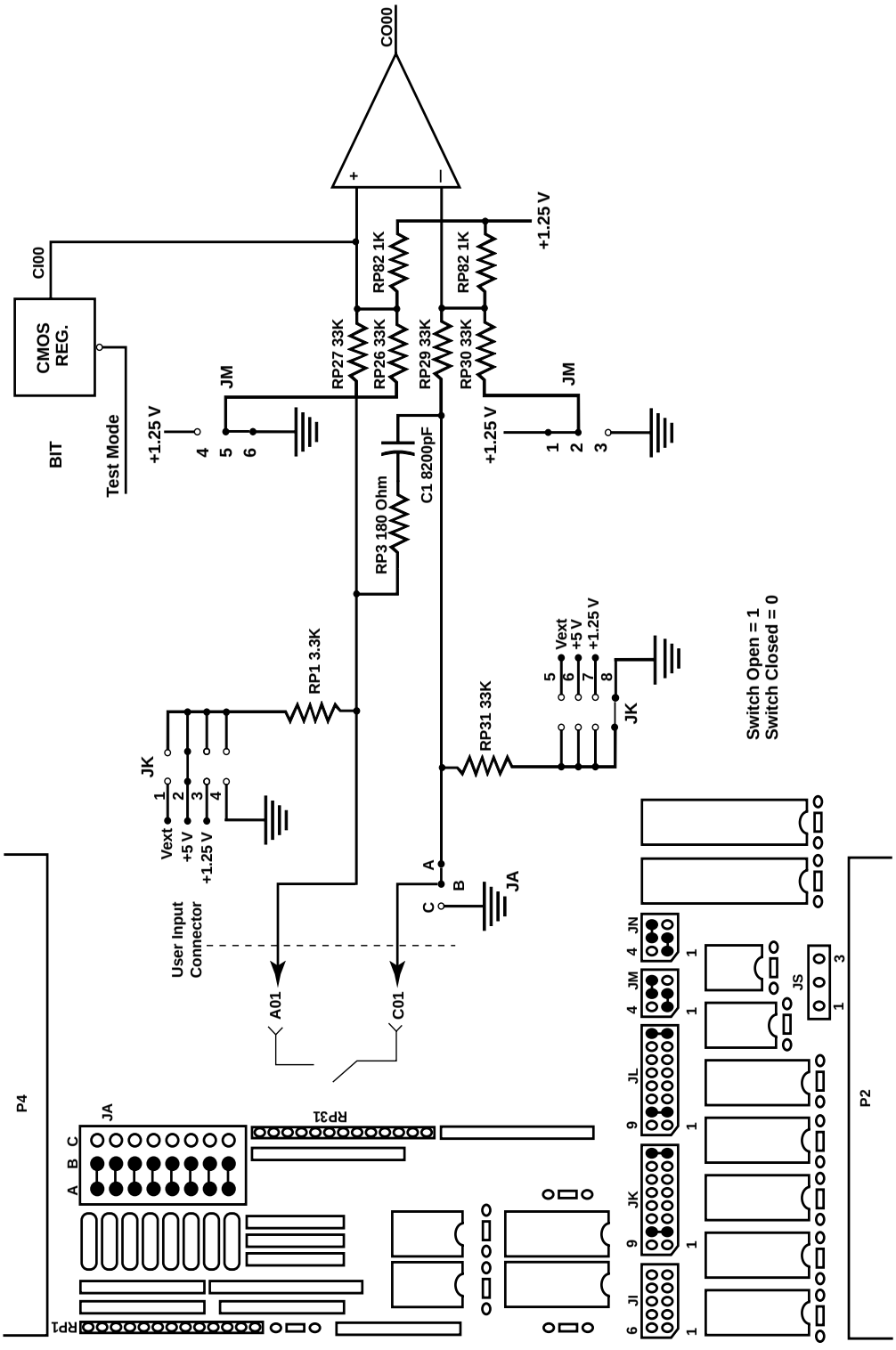
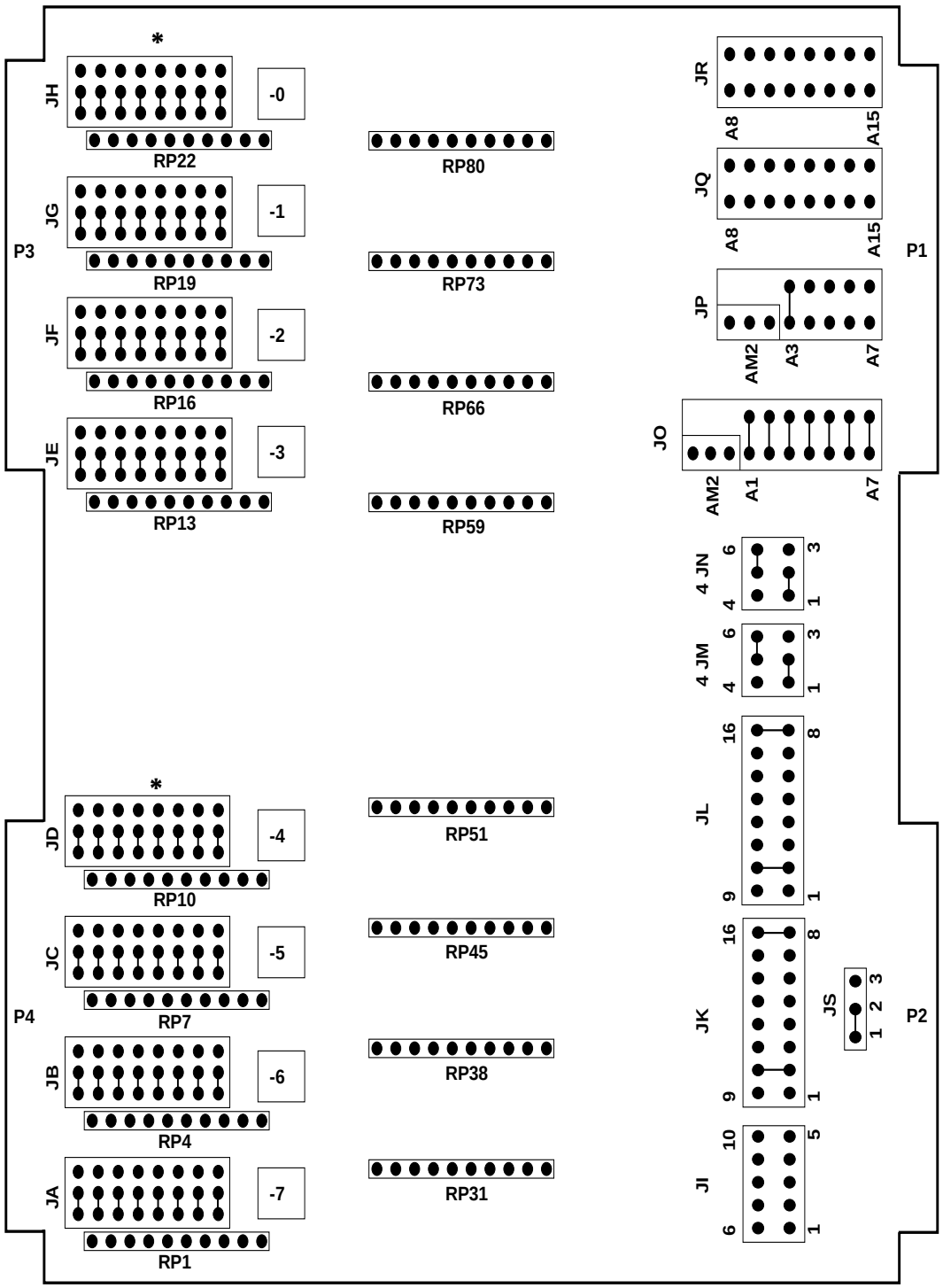


Figure 2-12 Jumper Configuration and Typical Input Circuit for Contact Closure, Pos True



NOTE: *These jumpers **MUST** be removed to route external voltages onto the board using the P3/P4 front panel Connectors.

Figure 2-13 Jumper Configuration for Contact Closure, Pos True

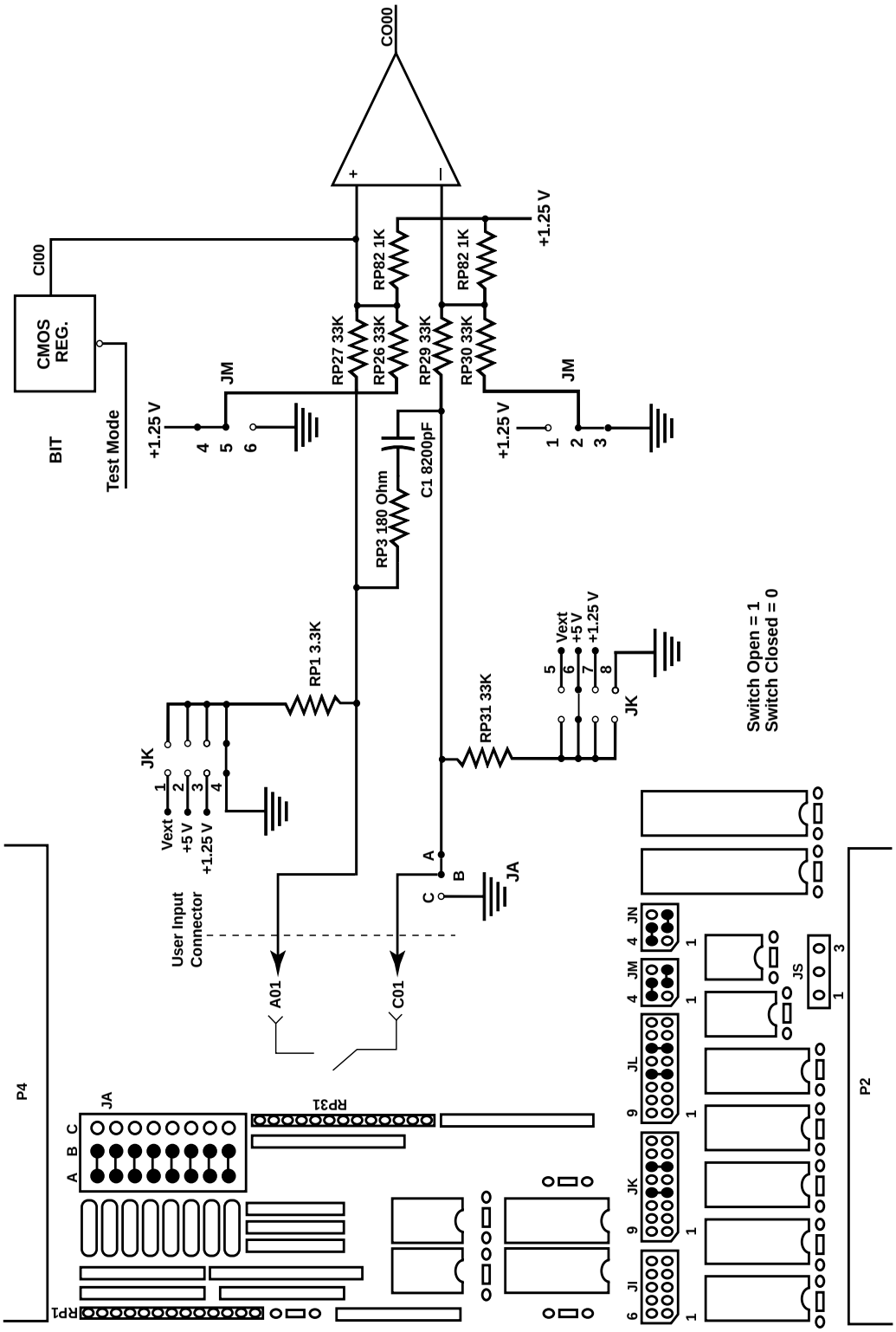
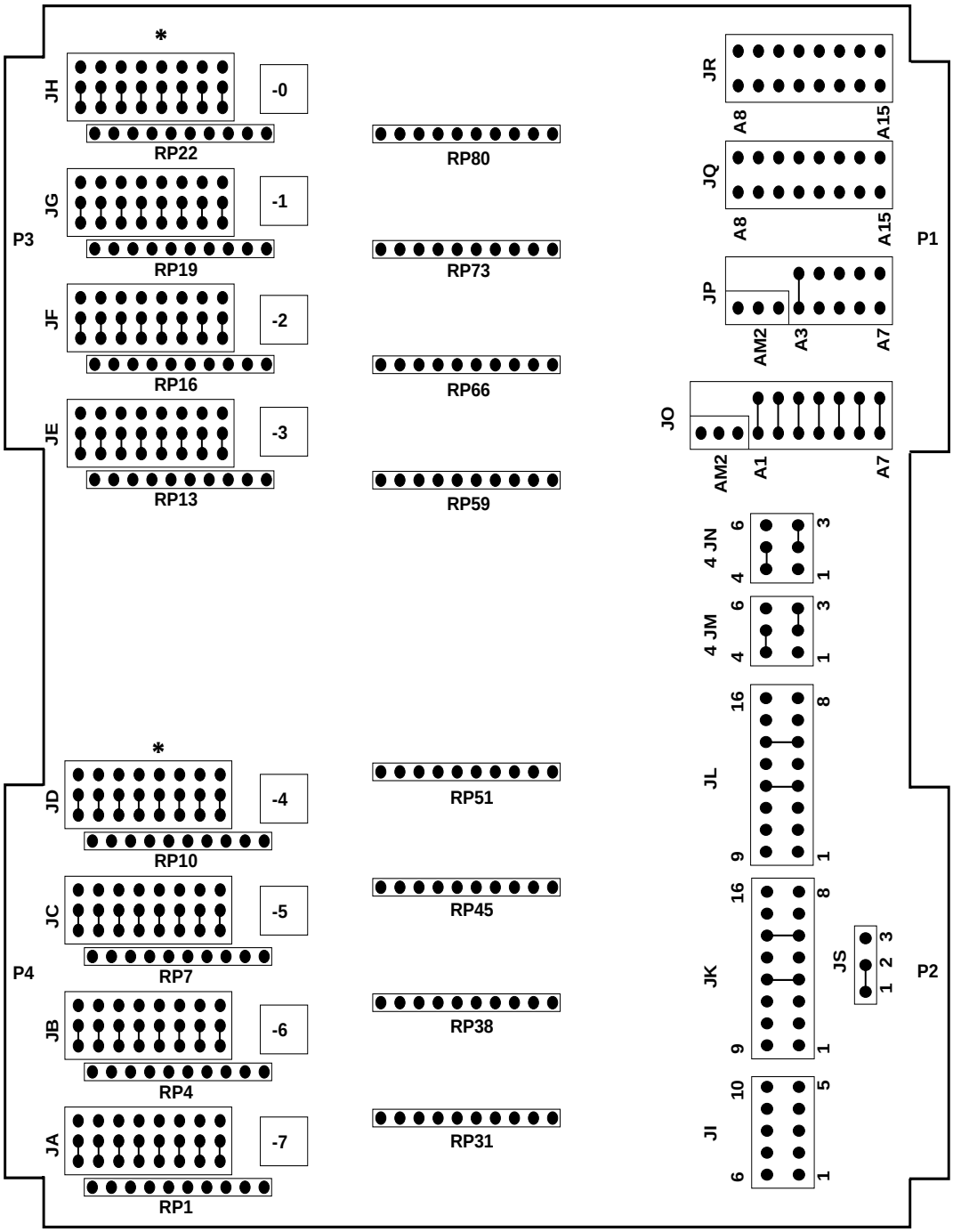


Figure 2-14 Jumper Configuration and Typical Input Circuit for Contact Closure, Neg True



NOTE: *These jumpers **MUST** be removed to route external voltages onto the board using the P3/P4 front panel connectors.

Figure 2-15 Jumper Configuration for Contact Closure, Neg True

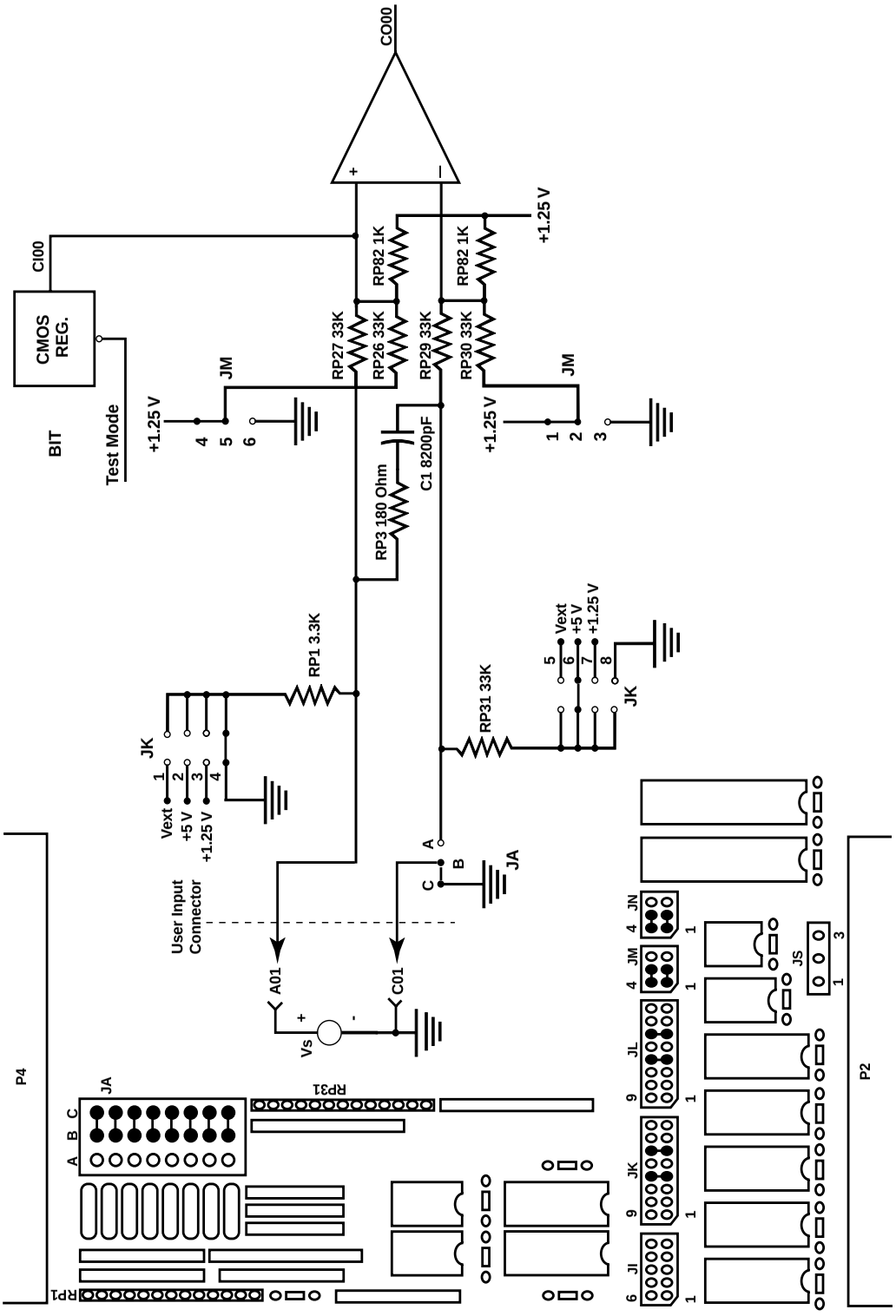
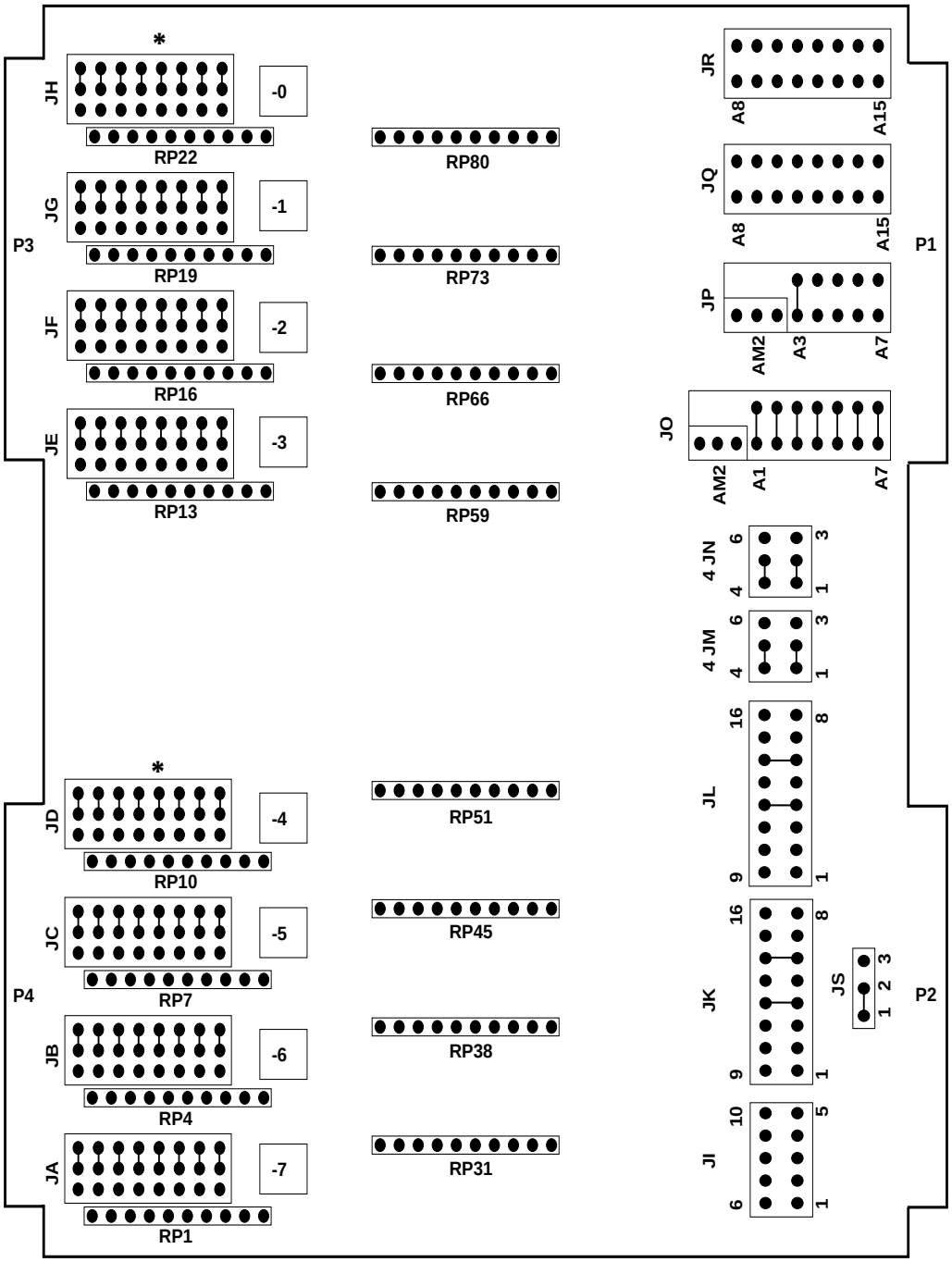
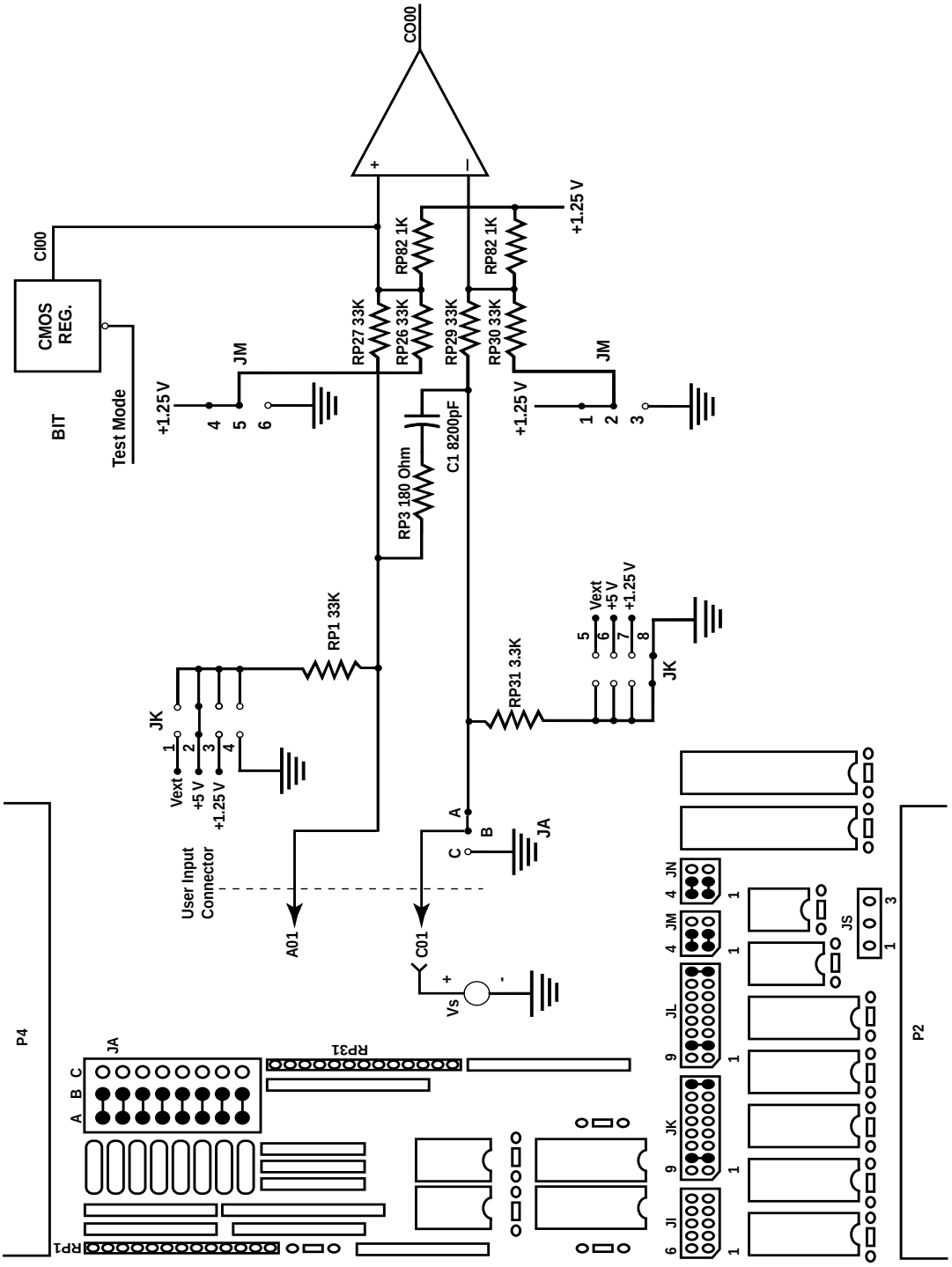


Figure 2-16 Jumper Configuration and Typical Input Circuit for Voltage Sourcing, Pos True



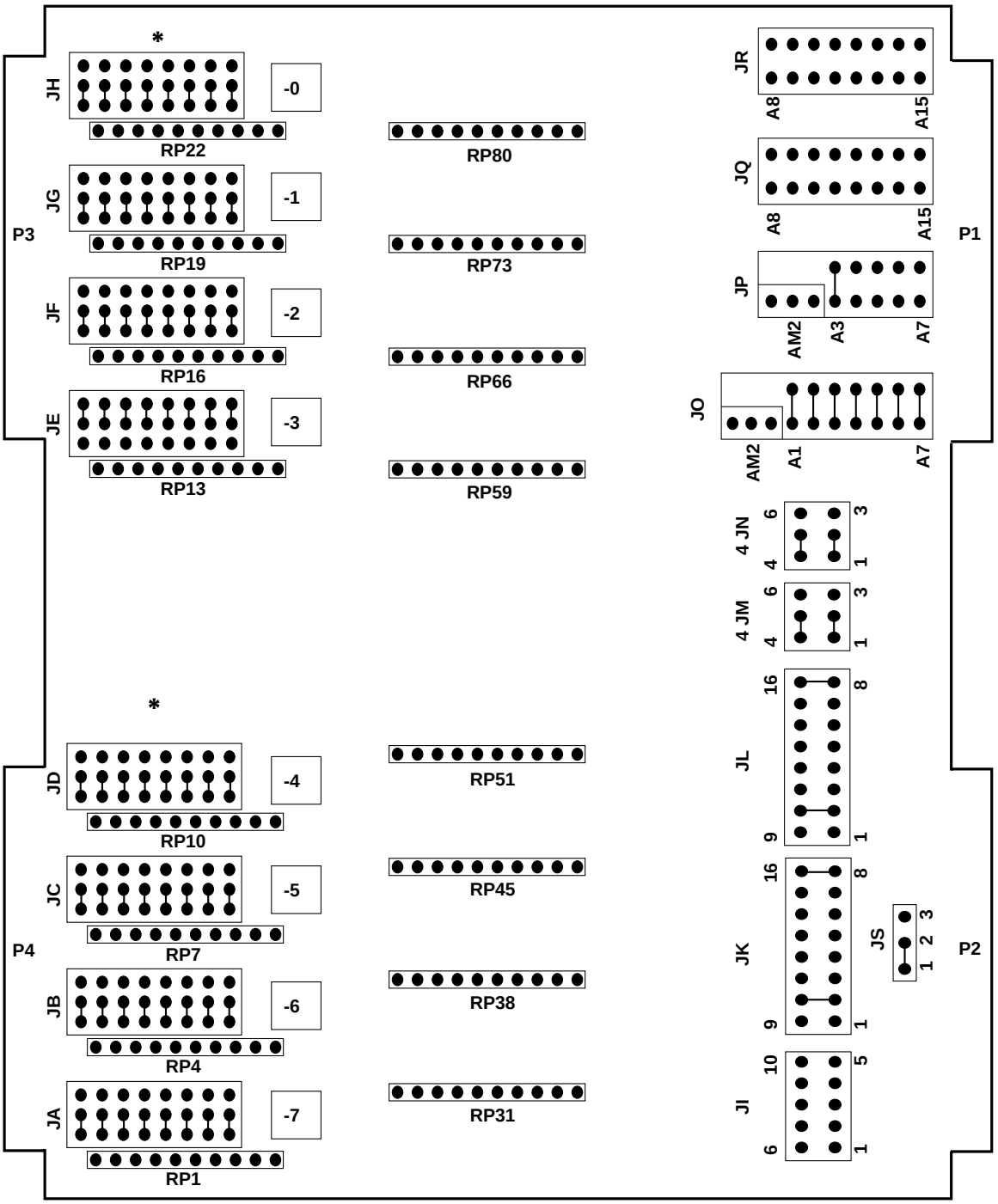
NOTE: *These jumpers **MUST** be removed to route external voltages onto the board using the P3/P4 front panel connectors.

Figure 2-17 Jumper Configuration for Voltage Sourcing, Pos True



NOTE: It is recommended that no connection be made to the Axx inputs for proper circuit operation.

Figure 2-18 Jumper Configuration and Typical Input Circuit for Voltage Sourcing, Neg True



NOTE: *These jumpers **MUST** be removed to route external voltages to the board using the P3/P4 front panel connectors.

Figure 2-19 Jumper Configuration for Voltage Sourcing, Neg True

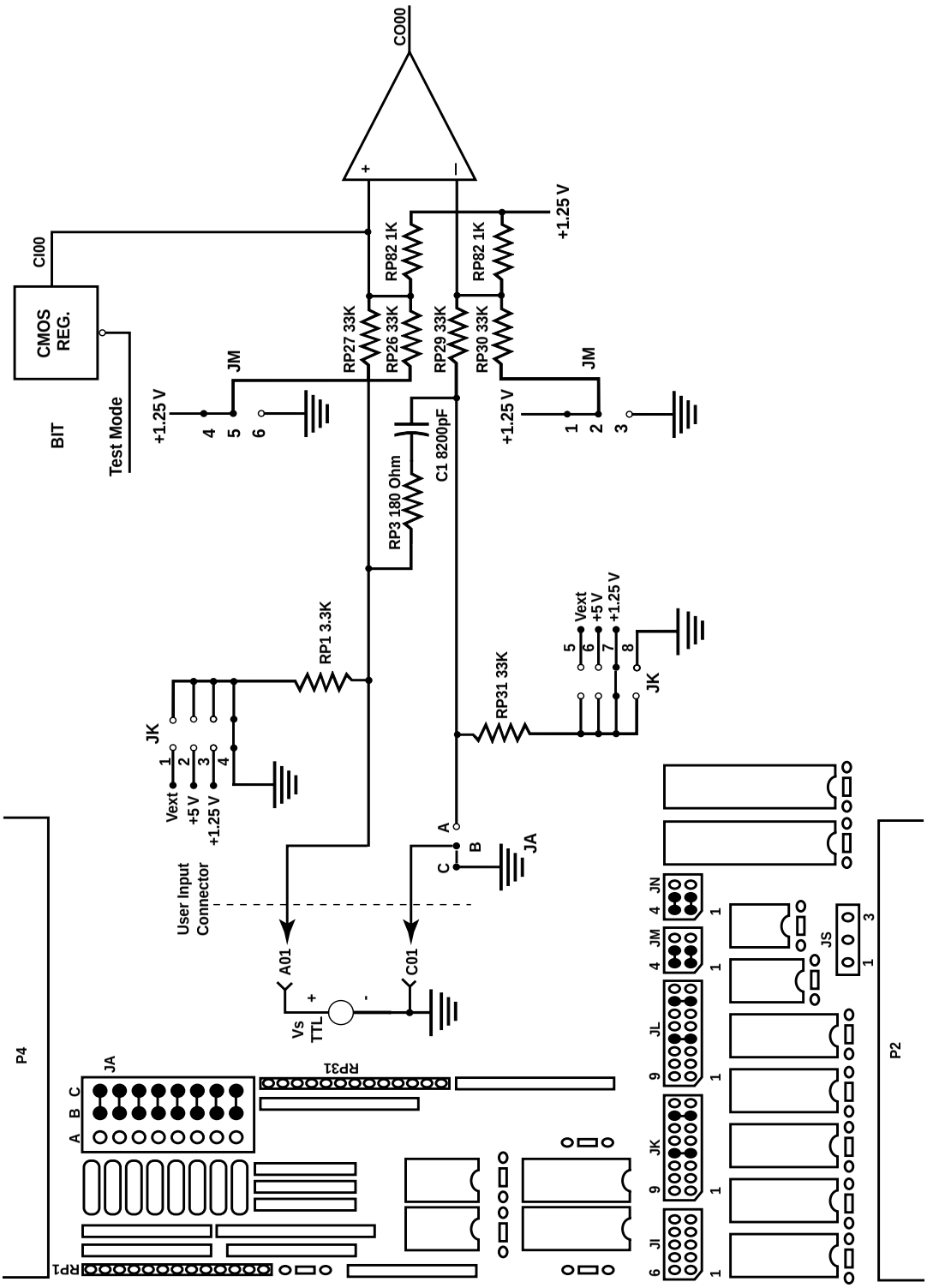
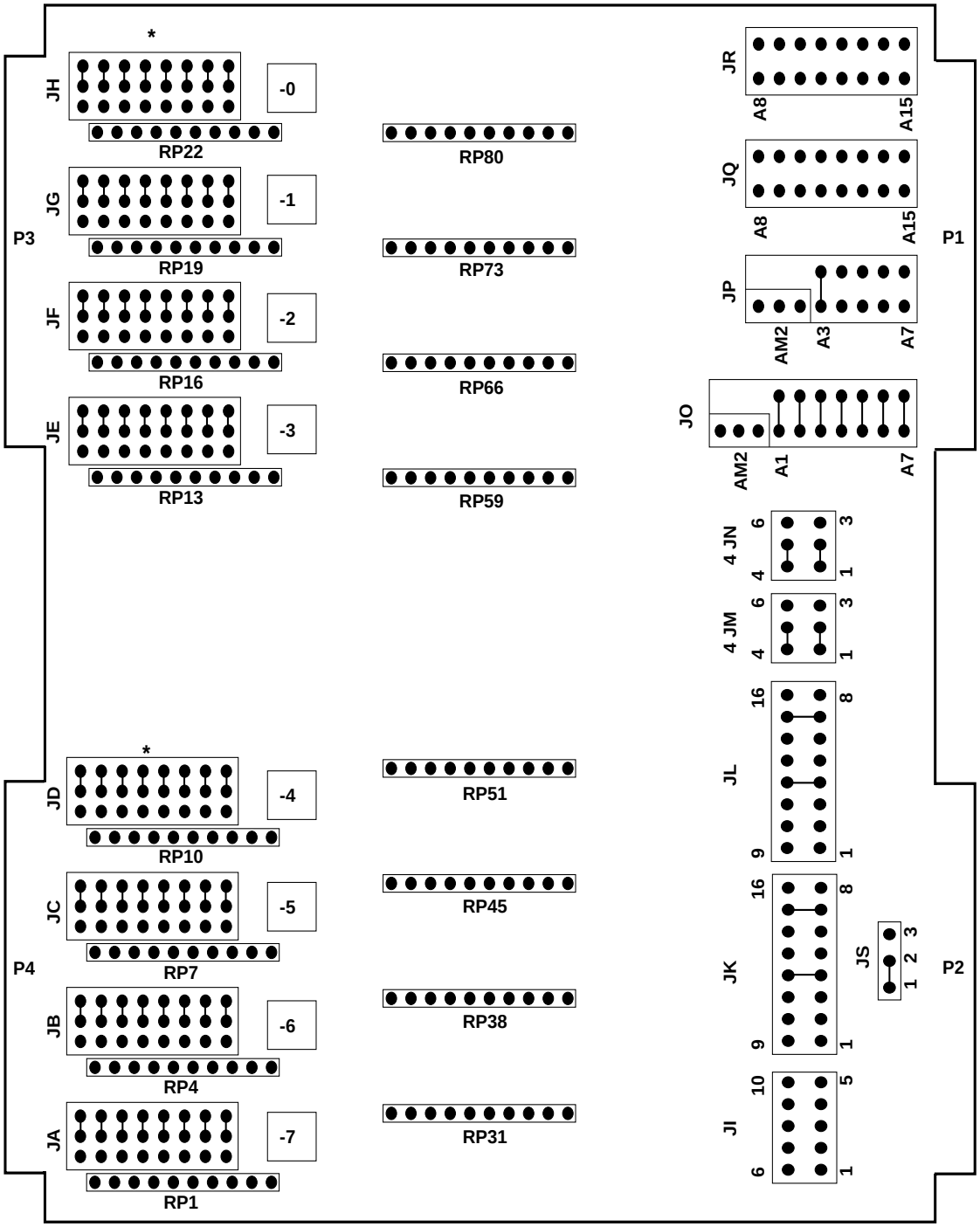
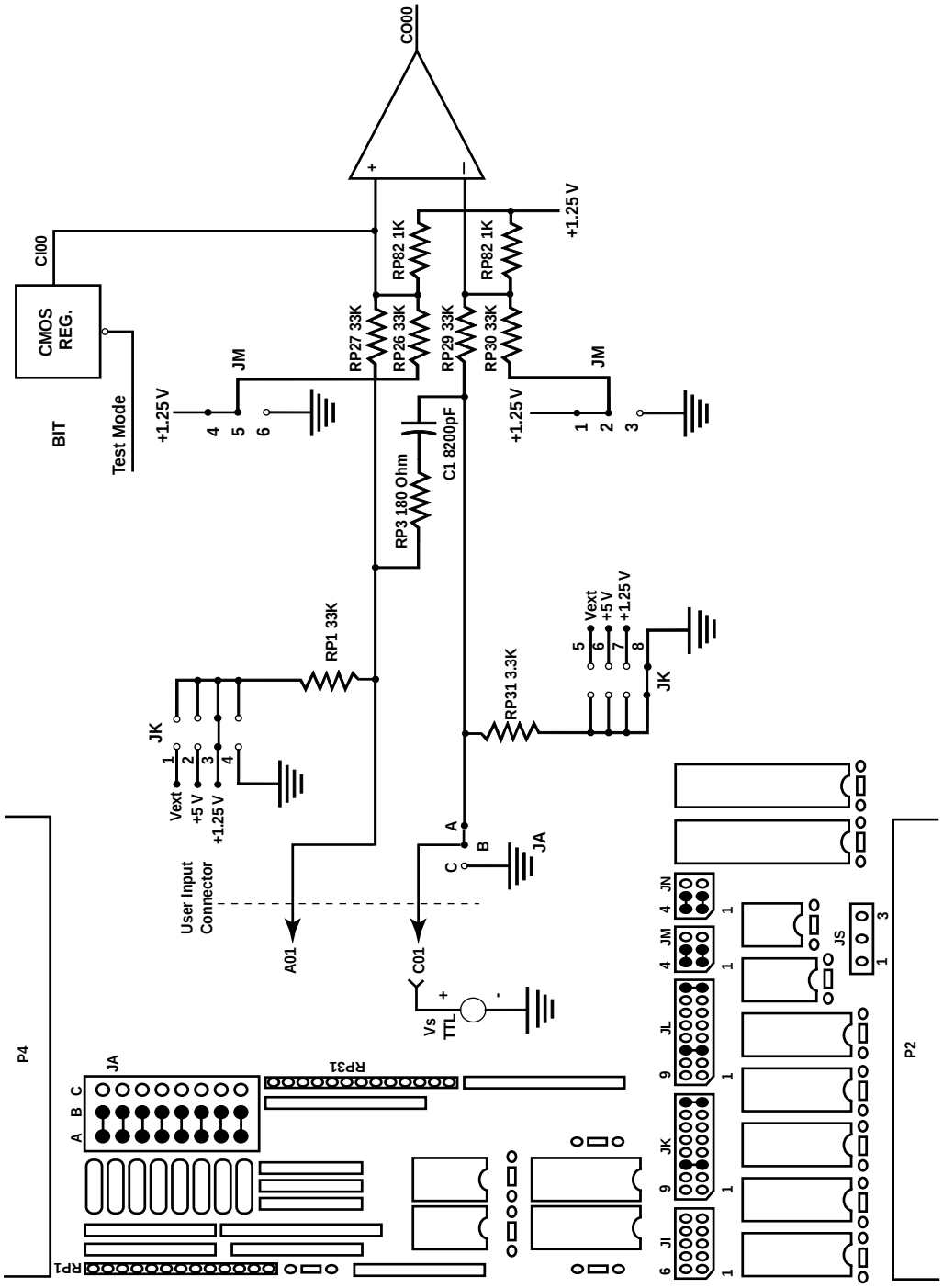


Figure 2-20 Jumper Configuration and Typical Input Circuit for Voltage Sourcing, TTL Pos True



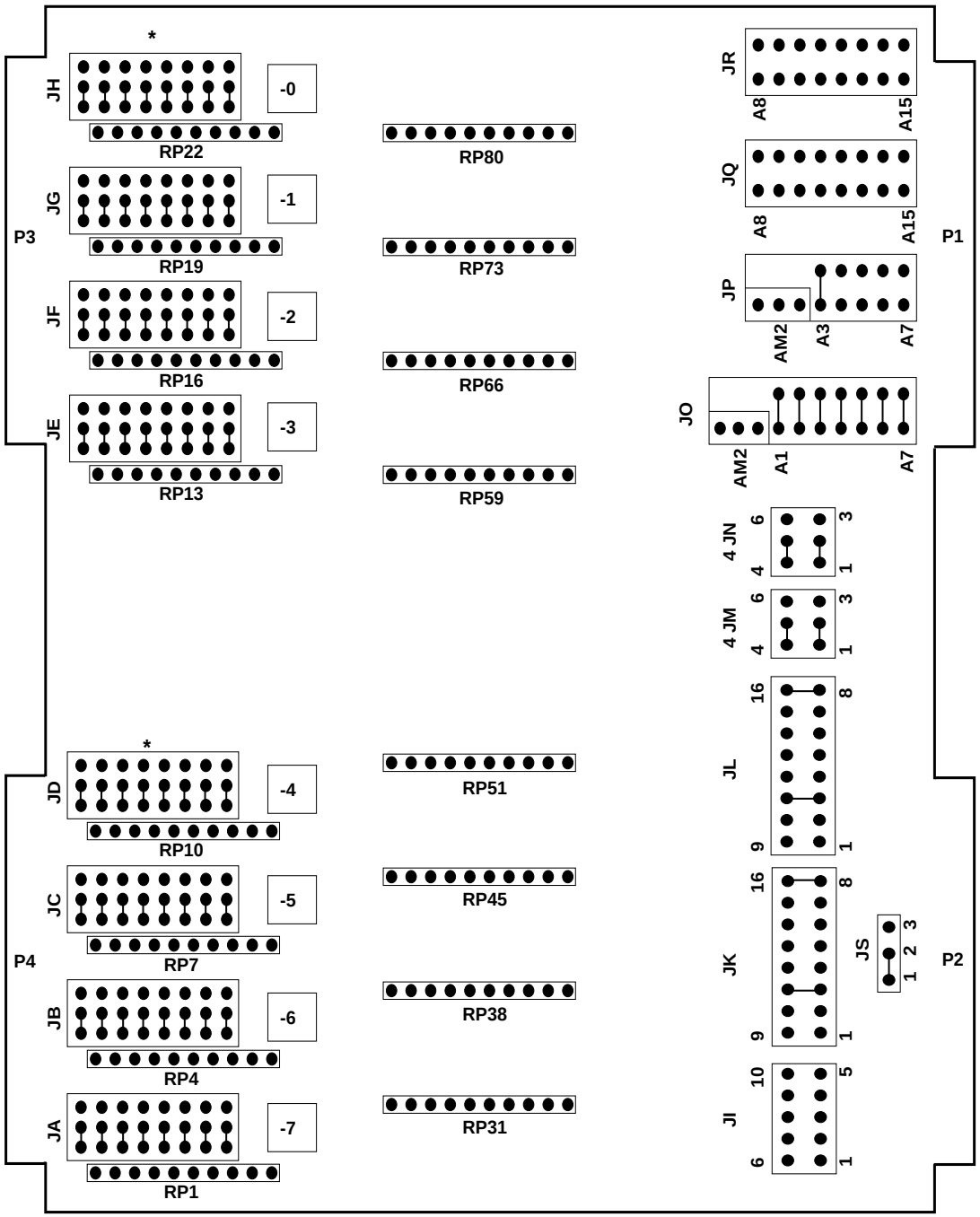
NOTE: *These jumpers MUST be removed to route external voltages to the board using the P3/P4 front panel connectors.

Figure 2-21 Jumper Configuration for Voltage Sourcing, TTL Pos True



NOTE: It is recommended that no connection be made to the Axx inputs for proper circuit operation.

Figure 2-22 Jumper Configuration and Typical Input Circuit for Voltage Sourcing, TTL Neg True



NOTE: *These jumpers MUST be removed to route external voltages to the board using the P3/P4 front panel connectors.

Figure 2-23 Jumper Configuration for Voltage Sourcing, TTL Neg True

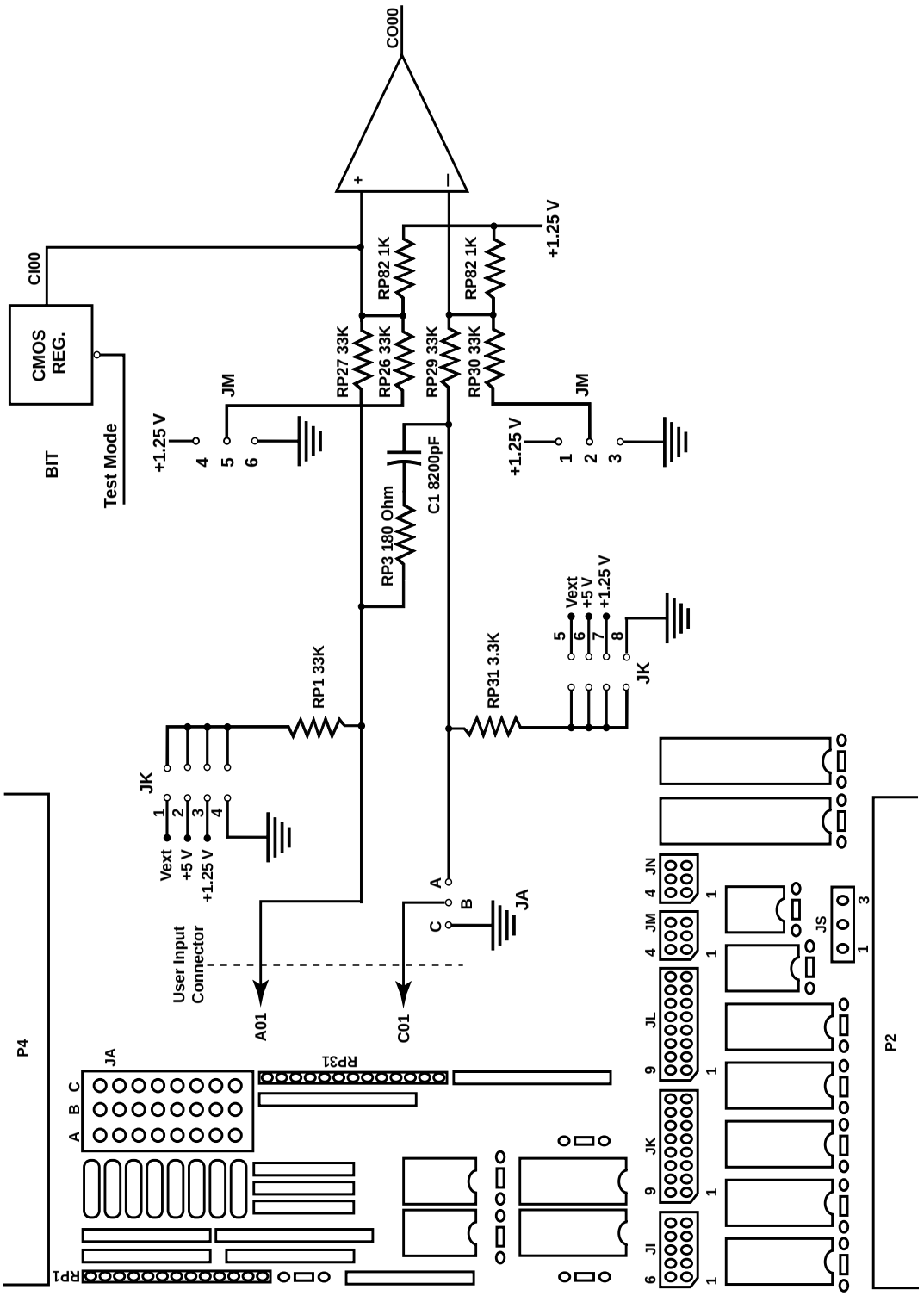
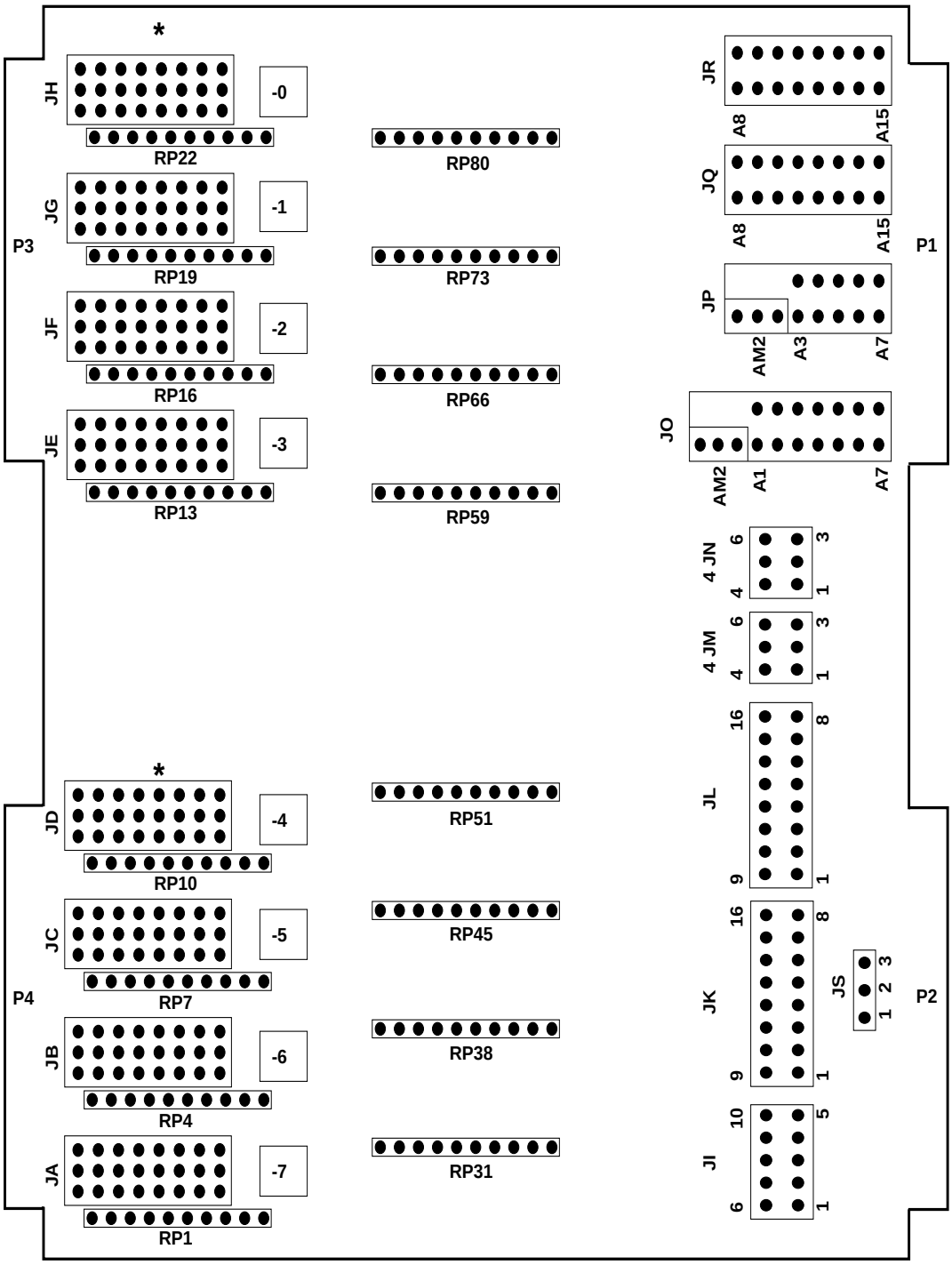


Figure 2-24 User Jumper Configuration and Input Circuit



NOTE: *These jumpers MUST be removed to route external voltages onto the board using the P3/P4 front panel connectors.

Figure 2-25 Worksheet for User Jumper Configuration of the Board

Table 2-3 Pull-up/Pull-Down Resistor Installation Sheet

Input Channels	Pull-Up Resistors	Pull-Down Resistors
0 to 7	RP1: Value = 3.3K* Value =	RP31: Value = 33K* Value =
8 to 15	RP4: Value = 3.3K* Value =	RP38: Value = 33K* Value =
16 to 23	RP7: Value = 3.3K* Value =	RP45: Value = 33K* Value =
24 to 31	RP10: Value = 3.3K* Value =	RP52: Value = 33K* Value =
32 to 39	RP13: Value = 3.3K* Value =	RP59: Value = 33K* Value =
40 to 47	RP16: Value = 3.3K* Value =	RP66: Value = 33K* Value =
48 to 55	RP19: Value = 3.3K* Value =	RP73: Value = 33K* Value =
56 to 63	RP22: Value = 3.3K* Value =	RP80: Value = 33K* Value =
* Factory Installation.		

External Pull-Up/Threshold Voltage

External voltage to the VMIVME-1111 is selected by jumper JI. External voltage can be brought to the board via the P2 connector on the backplane or via a front panel input connector pin. Refer to Figure 2-26.

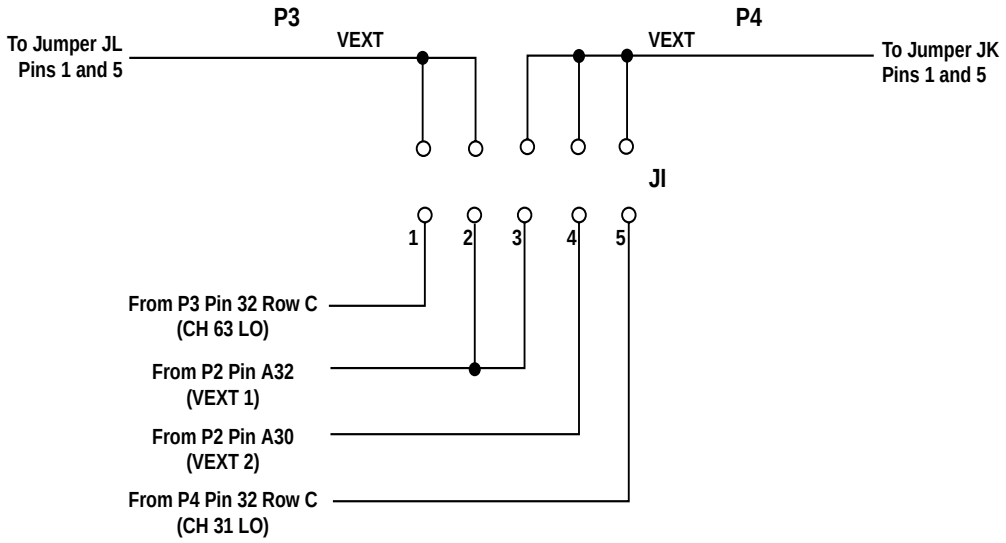


Figure 2-26 External Voltage Jumper Definitions

The external voltage can be different for each front panel user input connector. Jumper JI selects the different functions. The voltage can be supplied from the VMEbus backplane via P2 pin A32 to maintain compatibility with the VMIVME-1110 Board. If a single external voltage is needed, use positions 2 and 3 of JI. However, by using connector P2 pin A30 and P2 pin A32, Jumper JI can configure connector P4 user inputs to use the voltage from pin A30 (install position 4 of JI) and the P3 inputs to work with the voltage from P2 pin A32 (install position 2 of JI). Therefore, two different external voltages can be used by the VMIVME-1111's input circuits via jumper JI.

Jumper JI can also select an input channel to provide the external voltage by installing positions 1 and 5. The input pins used are P4 - pin 32 Row C (CH 31 LOW) and P3 - pin 32 Row C (CH 63 LOW). Caution: if this option is chosen, the input cannot be used for data transfer, the current drawn by the boardcannot exceed 1A (to prevent damage to the connector pin), and the associated jumpers for Row C (JD-8 and / or JH-8) must not be installed. Connecting these voltages with JD-8 or JH-8 installed B to C will short external power to ground and destroy the VMIVME-1111. An example of how the jumpers would be placed for a differential input board with external voltage provided via the P3 and P4 connectors is shown in Figure 2-7 on page 39. Please note the missing jumpers from headers JD and JH.

No matter how JI is configured, the configuration of jumpers JK and JL will determine whether the external voltage is used for input bias. Care must be taken to prevent the voltage across the 3.3 K SIPs from exceeding 20 V. Excessive power dissipated (in excess of 0.12 W) by the 3.3 K SIP resistor will damage the SIP. These SIPs are called

RP1 and RP31 in the previous figures. The logic diagram in Appendix A of this manual shows all of these SIPs. Their reference designators can be obtained by leafing through the schematic and noting them. Table 2-3 on page 58 has space available to document the values chosen.

The threshold voltage is set by the choice of the threshold resistor, and the voltage across it. Figure 2-28 on page 61, Table 2-4 on page 61 and Table 2-5 on page 61 show the threshold circuit and a table of values. The listed values are for some commonly used voltages. The equation used to determine the associated threshold voltage is also given in the tables. This way the user can calculate the threshold for the particular voltage to be used.

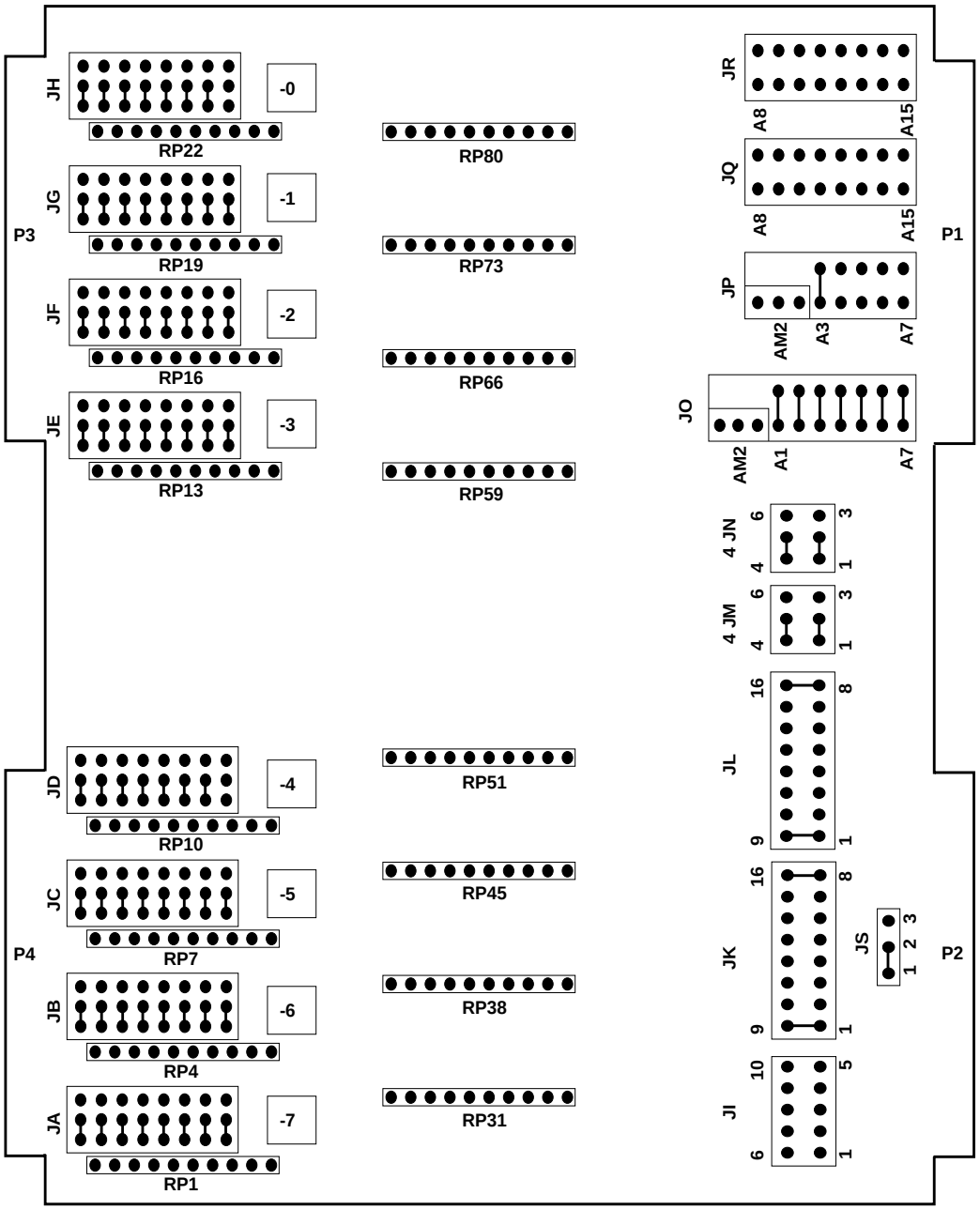


Figure 2-27 Jumper Locations for Differential Inputs with External Voltage

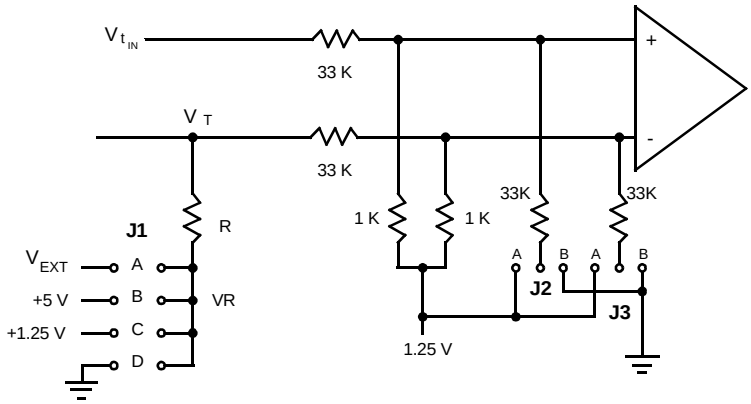


Figure 2-28 Threshold Voltage (V_t) Diagram

Case 1..... $V_t = 0.911\ VR + 0.11$
Case 2..... $V_t = V_t$ for Case 1 - 1.25
Case 3..... $V_t = V_t$ for Case 1 + 1.25

Table 2-4 Threshold Voltages (V_t) for R = 3.3K ohms

J1 Position	VR	V_t Case 1 J2 at A J3 at A	V_t Case 2 J2 at A J3 at B	V_t Case 3 J2 at B J3 at A
D	0 V	.11 V	-1.14 V	1.36 V
C	1.25 V	1.25 V	0 V	2.50 V
B	5.0 V	4.7 V	3.45 V	5.95 V
A	12.0 V	11 V	9.75 V	12.25 V
A	24.0 V	22 V	20.75 V	23.25 V
A	28.0 V	25.6 V	24.35 V	26.85 V
A	48.0 V	43.8 V	42.55 V	45.05 V
A	66.0 V	60.2 V	58.95 V	61.45 V

Case 1..... $V_t = 0.507\ VR + 0.6159$
Case 2..... $V_t = V_t$ for Case 1 - 1.25
Case 3..... $V_t = V_t$ for Case 1 + 1.25

Table 2-5 Threshold Voltages (V_t) for R=33K ohms

J1 Position	VR	V_t Case 1 J2 at A J3 at A	V_t Case 2 J2 at A J3 at B	V_t Case 3 J2 at B J3 at A
D	0 V	.616 V	-.634 V	1.866 V
C	1.25 V	1.25 V	0 V	2.50 V
B	5.0 V	3.15 V	1.90 V	4.40 V
A	12.0 V	6.7 V	5.45 V	7.95 V
A	24.0 V	12.8 V	11.55 V	14.05 V
A	28.0 V	14.82 V	13.57 V	16.07 V
A	48.0 V	24.96 V	23.71 V	26.21 V
A	66.0 V	34.10 V	32.85 V	35.35 V

I/O Cable and Card-Edge Connector Configuration

The input connectors (P3 and P4) on the VMIVME-1111 are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's connector and I/O Cable Application Guide (VMIC Publication 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Input cable connections to the VMIVME-1111 are shown in Figure 2-29 below. Note that Figure Figure 2-29 shows conductor no. 1 at the bottom of the connectors. Figure 2-30 on page 63 shows the pin layout of the P3 and P4 connectors. Table 2-6 on page 64 and Table 2-7 on page 65 detail the connector pin assignments. P1/P2 connector pin layouts are shown in Figure 2-31 on page 66, while the pin assignments are listed in Table 2-8 on page 67.

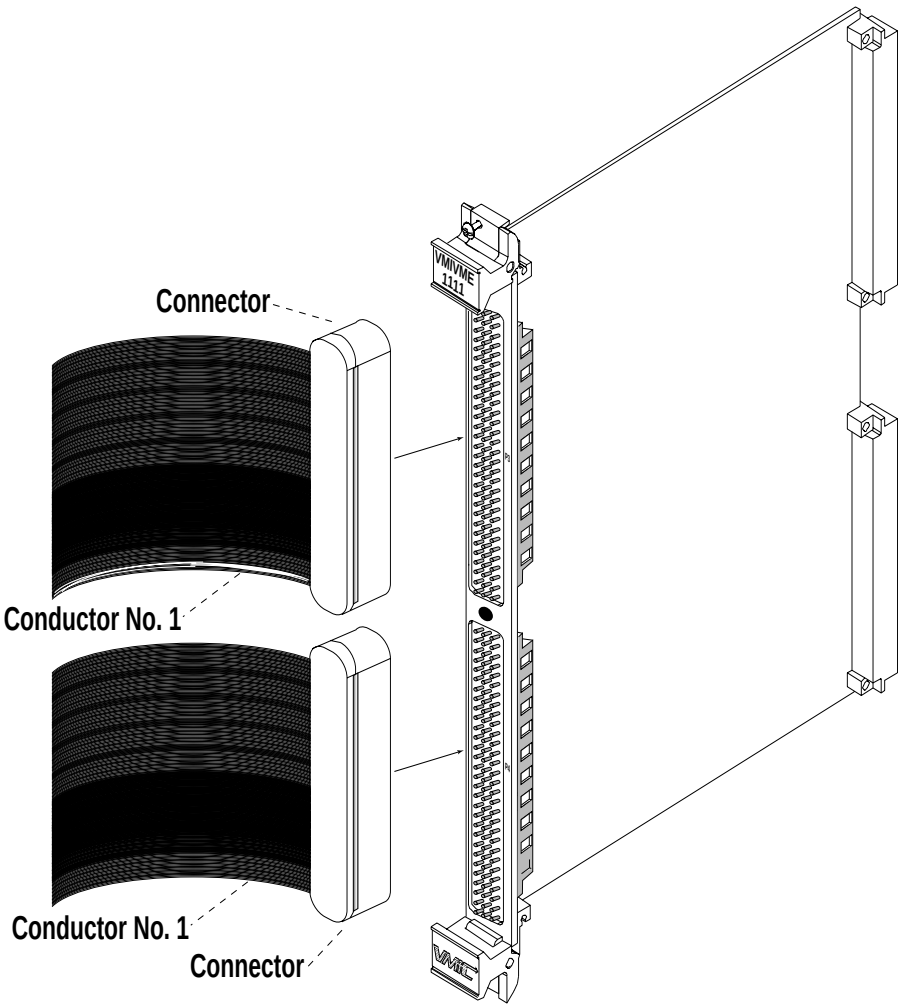


Figure 2-29 Cable Connector Configuration

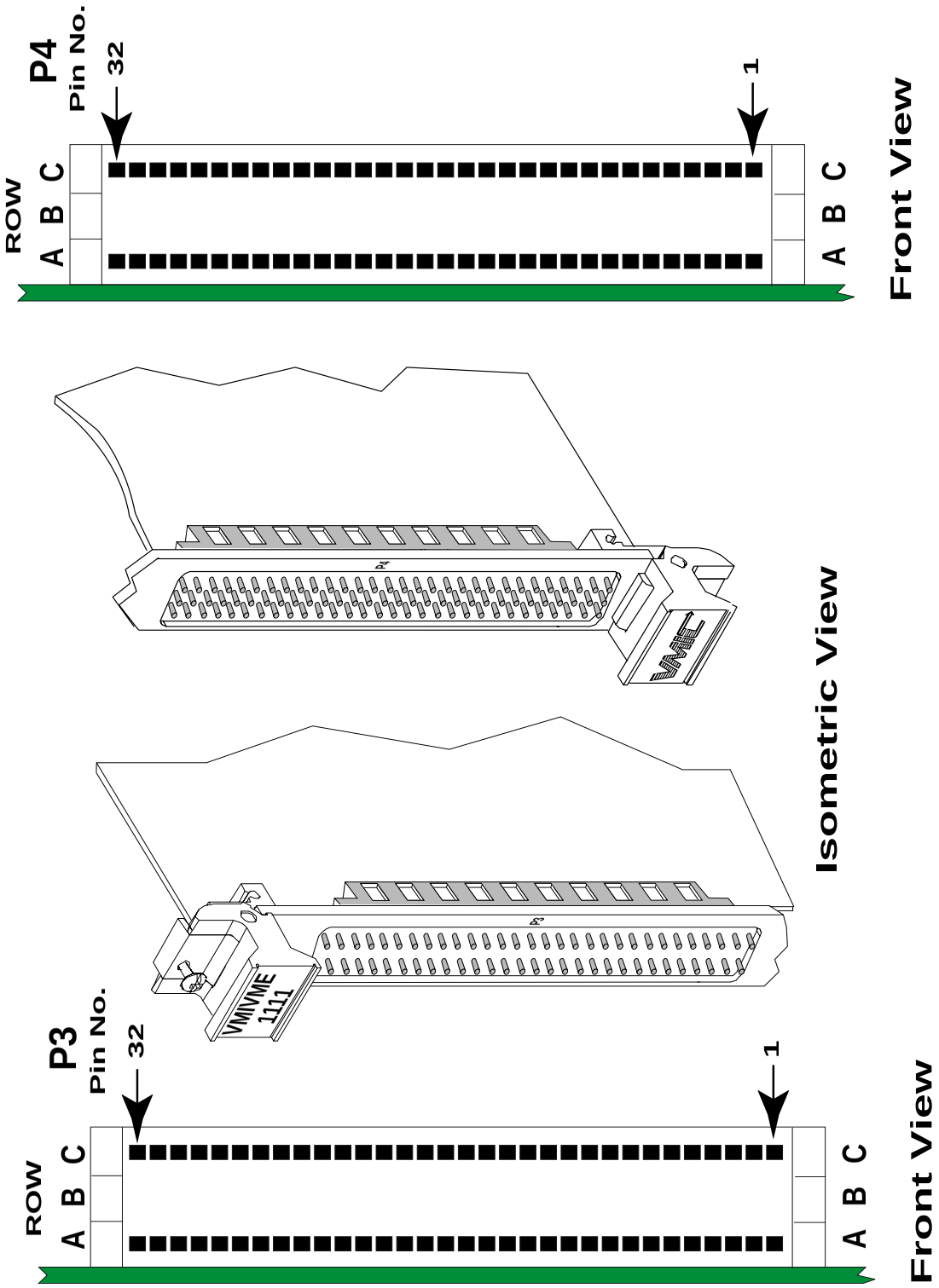


Figure 2-30 P3/P4 Connector Pin Layout

Table 2-6 P3 Connector Pin Assignments

Row A Pin No.	Channel No.	Row C Pin No.	Row A Pin No.	Channel No.	Row C Pin No.
32	63	JH-8*	16	47	JF-8
31	62	JH-7	15	46	JF-7
30	61	JH-6	14	45	JF-6
29	60	JH-5	13	44	JF-5
28	59	JH-4	12	43	JF-4
27	58	JH-3	11	42	JF-3
26	57	JH-2	10	41	JF-2
25	56	JH-1	09	40	JF-1
24	55	JG-8	08	39	JE-8
23	54	JG-7	07	38	JE-7
22	53	JG-6	06	37	JE-6
21	52	JG-5	05	36	JE-5
20	51	JG-4	04	35	JE-4
19	50	JG-3	03	34	JE-3
18	49	JG-2	02	33	JE-2
17	48	JG-1	01	32	JE-1

NOTE: Row C pins are set up by the stated jumper as described earlier.

CAUTION: *This pin can be used to bring in an external voltage. Before connecting an external voltage to P3 Row C Pin 32, verify that all jumpers are removed from JH-8. Applying an external voltage to P3 Row C Pin 32 with JH-8 connected B to C will short external power to ground and ***DESTROY*** the board.

Table 2-7 P4 Connector Pin Assignments

Row A Pin No.	Channel No.	Row C Pin No.	Row A Pin No.	Channel No.	Row C Pin No.
32	31	JD-8*	16	15	JB-8
31	30	JD-7	15	14	JB-7
30	29	JD-6	14	13	JB-6
29	28	JD-5	13	12	JB-5
28	27	JD-4	12	11	JB-4
27	26	JD-3	11	10	JB-3
26	25	JD-2	10	09	JB-2
25	24	JD-1	09	08	JB-1
24	23	JC-8	08	07	JA-8
23	22	JC-7	07	06	JA-7
22	21	JC-6	06	05	JA-6
21	20	JC-5	05	04	JA-5
20	19	JC-4	04	03	JA-4
19	18	JC-3	03	02	JA-3
18	17	JC-2	02	01	JA-2
17	16	JC-1	01	00	JA-1

NOTE: Row C pins are set up by the stated jumper as described earlier.

CAUTION: *This pin can be used to bring in an external voltage. Before connecting an external voltage to P4 Row C Pin 32, verify that all jumpers are removed from JD-8. Applying an external voltage to P4 Row C Pin 32 with JD-8 connected B to C will short external power to ground and ***DESTROY*** the board.

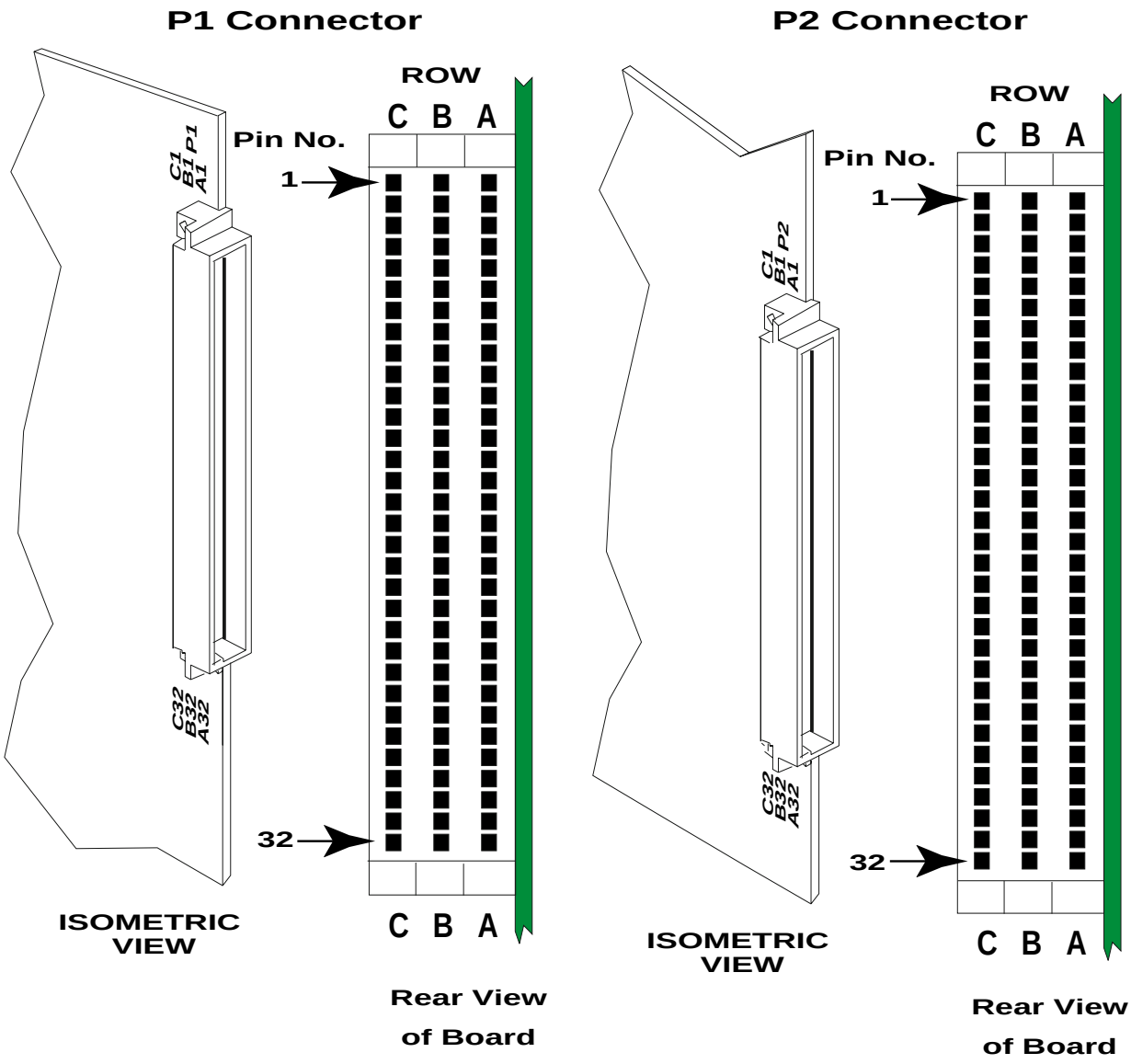


Figure 2-31 P1/P2 Connector Pin Layout

Table 2-8 P2 Connector Pin Assignments

Pin No.	Row A (1)	Row B (2)	Row C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30	Vext P4		
31		GND	
32	Vext P3	+5 V	

Test Mode Selection

Jumper (JS) is used to configure the VMIVME-1111 for single or split test mode. With pins 2 and 3 jumpered, the board has a single test mode bit (bit 7 of the CSR) and is software compatible with the VMIVME-1110 board. When pins 1 and 2 are jumpered, the VMIVME-1111 can split its inputs such that the inputs associated with the user connector P3 (controlled by bit 7 of the CSR) can be in test mode, while the inputs associated with the user connector P4 (controlled by bit 5 of the CSR) are in normal mode, and vice versa. The VMIVME-1111 is shipped with jumper (JS) configured for single bit test mode.

CHAPTER 3

Programming

Introduction

The VMIVME-1111 is designed to enable the user to read eight 8-bit input ports and to read or write to a Control Status Register (CSR) that controls the test mode and front panel LED. The input port and CSR address maps are shown below. The VMIVME-1111 supports a Built-in-Test function by writing to the eight 8-bit CMOS registers whose outputs are connected to the input port signal conditioning logic. The test registers may be written to using the same address as each input port, as shown in Table 3-1 below.

Table 3-1 Input Ports

Relative Address	Mnemonic	Name/Function
$XXX0	DR0	Input Port / Test Register 0
$XXX1	DR1	Input Port / Test Register1
$XXX2	DR2	Input Port / Test Register2
$XXX3	DR3	Input Port / Test Register3
$XXX4	DR4	Input Port / Test Register 4
$XXX5	DR5	Input Port / Test Register5
$XXX6	DR6	Input Port / Test Register6
$XXX7	DR7	Input Port / Test Register7

NOTE: XXX of an address is determined by input port address select jumpers JP and JR. See *"Input Signal Conditioning Selection"* in Chapter 2.

Table 3-2 Control and Status Register (CSR)

Relative Address	Mnemonic	Name/Function
$YYY0	BDID	Board ID Code (Read-Only)
$YYY1	CSRL	CSR Lower Byte (Write-Only)

NOTE: XXX of an address is determined by input port address select jumpers JP and JR. See *"Input Signal Conditioning Selection"* in Chapter 2

Register Bit Definitions Input Ports

The CSR bit definitions are listed in Table 3-3 below and described in the following paragraphs. For the Input Ports bit definitions see Table 3-4 starting below.

Control and Status Register (CSR)

Table 3-3 Control and Status Register Bit Map

Control and Status Register Upper Bits (CSRU): Offset $YYY0 (Write-Only)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	1
Board ID Code							

Control and Status Register Lower Bits (CSRL): Offset $YYY1 (Write-Only)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TM P3	FL	TM P4	Reserved				

Control and Status Register Bit Definitions

Bit 07: **Test Mode (TM P3)** - When Bit 7 is cleared to a logic "zero", the inputs associated with input connector P3 into test mode. This bit is the only test mode bit to be used if the board is configured to be software compatable with the VMIVME-1110 (Jumper JS in position 3).

Bit 06: **Fail LED (FL)** - This bit controls the state of the front panel Fail LED. Bit 06 is cleared to a logic "zero" to turn the LED ON.

Bit 05: **Test Mode (TM P4)** - When bit 5 is cleared to a Logic "zero", the inputs associated with input connector P4 into test mode. This bit is not used when the board is configured to be software compatable with the VMIVME-1110 (Jumper JS in position 3).

Bits 04 through 00: **Reserved** - These bits are reserved.

Input Data Registers (DR0 - DR7)

Table 3-4 Input Ports Register Bit Definitions

Input Port/Test Register 0 (DR0): Offset Address = $XXX0							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH63	CH62	CH61	CH60	CH59	CH58	CH57	CH56

Table 3-4 Inport Ports Register Bit Definitions (Continued)

Input Port/Test Register 1 (DR1): Offset Address = $XXX1							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH55	CH54	CH53	CH52	CH51	CH50	CHB49	CH48

Input Port/Test Register 2 (DR2): Offset Address = $XXX2							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH47	CH46	CH45	CH44	CH43	CH42	CH41	CH40

Input Port/Test Register 3 (DR3): Offset Address = $XXX3							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH39	CH38	CH37	CH36	CH35	CH34	CH33	CH32

Input Port/Test Register 4 (DR4): Offset Address = $XXX4							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24

Input Port/Test Register 5 (DR5): Offset Address = $XXX5							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16

Input Port/Test Register 6 (DR6): Offset $XXX6							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8

Input Port/Test Register 7 (DR7): Offset Address = $XXX7							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Detailed Data Access

Input Data Access

As seen in the register map, DR0-DR7 corresponds to input channels 63-0. Therefore, to access input data, the corresponding input port is read, provided the corresponding TM bit in the CSR is set to a "one". The programming sequence for normal operation is shown in Figure 3-1 below.

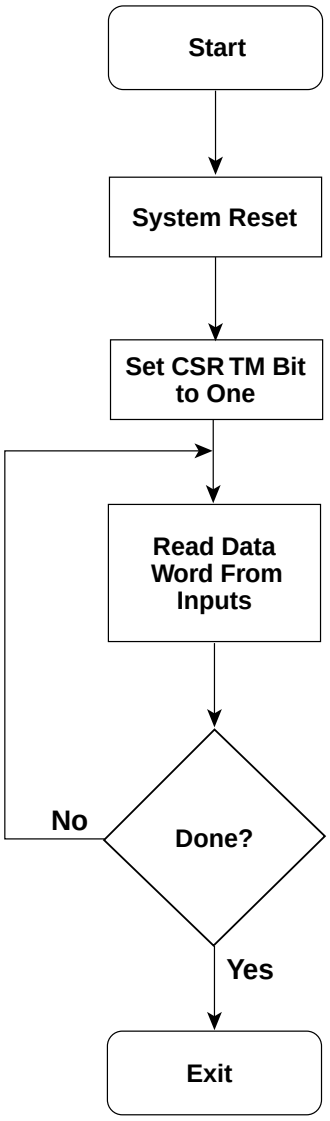


Figure 3-1 VMIVME-1111 Normal Programming Flow Chart

Built-in-Test

The Built-in-Test feature is activated by clearing the TM bit in the CSR to a zero (0). Test data is then written to the selected test register and may be read back on a read transfer from the same port address. The programming sequence for test mode operation is shown in Figure 3-2 below.

Whenever one or both of the test mode bits are cleared, the CMOS test register outputs are activated. The user can then execute loopback diagnostics on each port. Both test mode bits and the Fail LED bit are initialized active (logic "zero") by a system reset or at power-up. Isolation resistors are provided on each input to support real-time data test patterns for fault detection and isolation. During test mode the inputs will not respond to field input data.

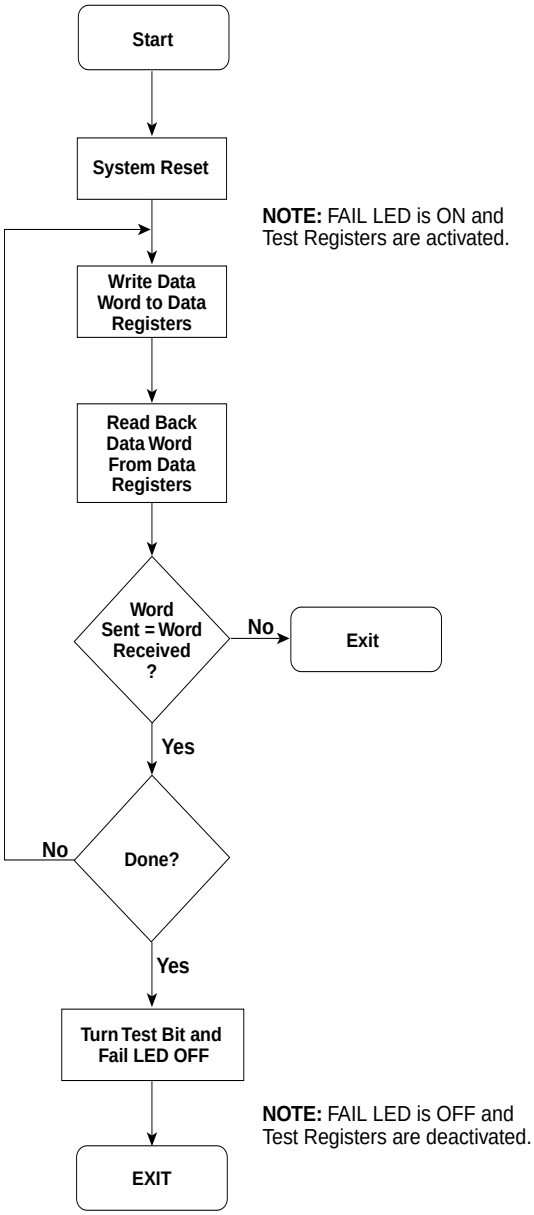


Figure 3-2 VMIVME-1111 Test Programming Flow Chart

Power-Up/System Reset

Upon power-up or when a system reset is performed, all bits will be set to "zero" in the CSR; therefore, the test mode is enabled and the Fail LED is ON.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.