# VMIVME-1150 64-bit Optically Coupled Digital Input Board

**Product Manual** 





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# **Overview**

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# Introduction

#### **Features**

The VMIVME-1150 is a VMEbus compatible 64-bit optically coupled digital input board. Its features include:

- 64 bits of optically isolated digital inputs
- 8- or 16-bit data transfers
- Inverting or non-inverting control options
- Debounce delay time specified by user
- Voltage source or current sink options
- 5 to 48 VDC operation (option dependent)

## **Functional Description**

The VMIVME-1150 Optically Coupled Digital Input Board consists of VMEbus compatibility logic, data input control logic, eight 8-bit input registers, and 64 bits of optically isolated inputs.

The VMEbus compatibility logic contains address decoding logic and data transfer control logic allowing 8- or 16-bit data transfers.

The data input control logic, in conjunction with eight 8-bit registers, selects bytes or words from 64 optically isolated input channels for data transfer onto the VMEbus.

Sixty-four optically coupled input channels convert high voltage digital inputs to TTL levels for data transfer. Each channel is debounced by an R-C filter that is user specified before shipment.

### **Reference Material List**

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

**VITA** 

VMEbus International Trade Association 7825 East Gelding Dr. Suite 104 Scottsdale, AZ 85260 (602) 951-8866 FAX: (602) 951-0720

FAX: (602) 951-0720 Internet: www.vita.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products:

### **Application and Configuration Guides:**

<u>Title</u>	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006
Data Acquisition Noise Reduction in Industrial Environments	825-000000-026

### **Physical Description and Specifications**

Refer to VMIC Specification No. **800-001150-000** for a detailed explanation and physical description of the VMIVME-1150 64-bit Optically Coupled Digital Input Board, available from the following:

VMIC 12090 South Memorial Pkwy. Huntsville, AL 35803-3308, USA (256) 880-0444 (800) 322-3616 FAX: (256) 882-0859 www.vmic.com

### **Safety Summary**

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

### **Ground the System**

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

#### Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

### **Keep Away from Live Circuits**

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

### Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

### Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

### **Dangerous Procedure Warnings**

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**WARNING:** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

## Safety Symbols Used in This Manual



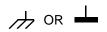
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

**STOP** informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

**WARNING** denotes a hazard. It calls attention to a procedure, a practice or condition which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION** denotes a hazard. It calls attention to an operating procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE** denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.



CHAPTER

# Theory of Operation

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# **Block Diagrams**

The VMIVME-1150 general architecture is shown in Figure 1-1 on page 21. Subsystems relevant to understanding the board's operation are shown in Figure 1-2 on page 22 and Figure 1-3 on page 23.

# Operational Overview

To perform data transfers with the VMIVME-1150, data is read from input data registers labeled R0 through R3. The appropriate inputs are selected via address bits A01 and A02. These bits are used to select between four banks of 16-bits for data inputs. The two data strobes DS0 and DS1 allow the 16-bit banks to be accessed as words or as bytes.

# **Data Transfer Description**

The data transfer/board select signal, shown in Figure 1-3 on page 23, is logically gated with DS0 and DS1 to produce active signals for data transfer. These gated signals activate data transceivers which drive input data from the input-data registers onto the VMEbus.

The read signal, READH, is also gated with the board select signal from the address comparators to form a read signal used to activate the decoder in the data input control subsystem. The decoder outputs, in turn, enable one of four groups of input data registers.

### **Optical Isolators**

Sixty-four optical isolators convert high voltage digital signals to TTL levels for transfer onto the VMEbus. Depending on the option selected, the input channels can be configured for 5, 12, 24, or 48 VDC operation. This voltage must be supplied via the VMEbus backplane on connector P2, if the current sink option is selected, with the positive side of the voltage going to Pin C30 (VPOS) and the negative side going to Pin C31 (VNEG). Please refer to the appropriate table in Section 2 for the power requirements the supply must handle. Each channel may be debounced with an R-C filter. Voltage source or current sink options are available. See "Configuration and Installation" on page 25 for application information.

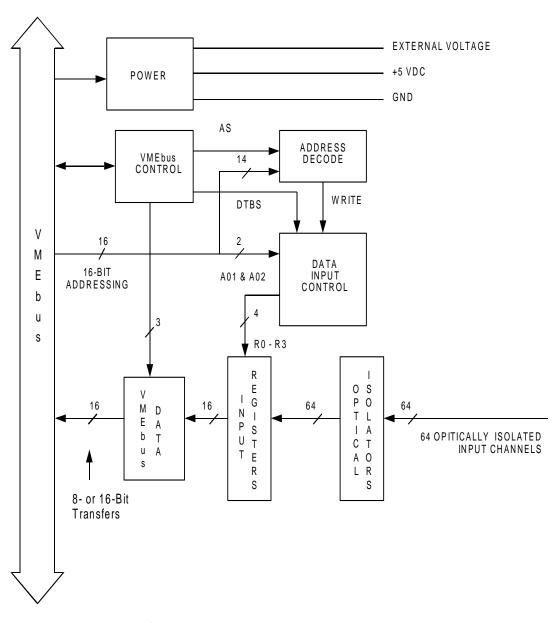


Figure 1-1 VMIVME-1150 Functional Block Diagram

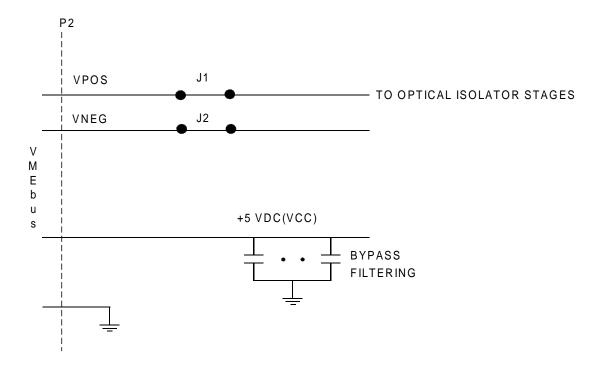


Figure 1-2 VMIVME-1150 Power Subsystem Block Diagram

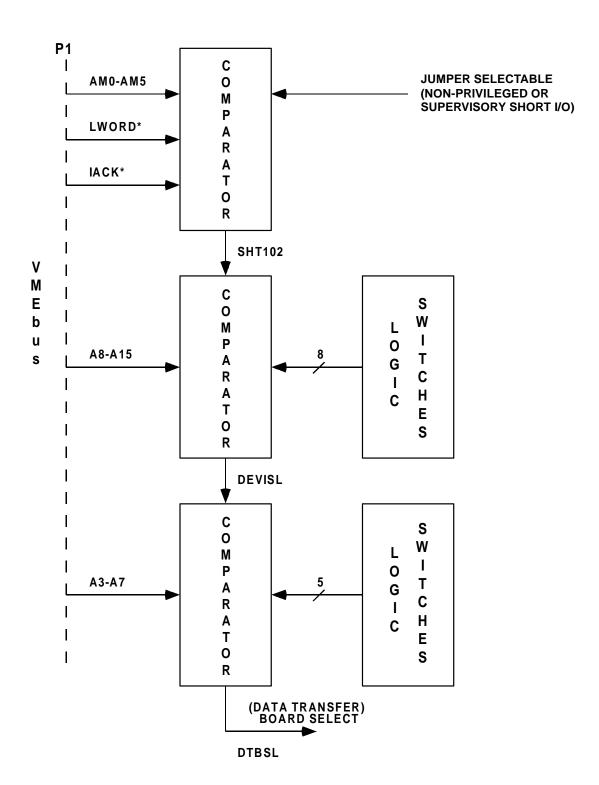


Figure 1-3 VMIVME-1150 Address Decode Subsystem Block Diagram



# Configuration and Installation

## **Contents**

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## **Unpacking Procedures**

**CAUTION:** Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning the disposition of the damaged item(s).

### **Physical Installation**

**CAUTION:** Do not install or remove the board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the card is properly aligned and oriented in the supporting card guides, slide the card smoothly forward against the mating connector until firmly seated.

## **Jumper and Switch Locations**

Refer to Figure 2-1 for the locations of the jumpers and switches described in this section. The input option of the VMIVME-1150 determines which jumper posts are installed on the board.

**NOTE:** For the voltage source option, the jumper terminals at J1-J2, J4-J18, J20-J36, J70-J86, and J88-J102 are not installed at the factory. For the contact sense option, the jumper terminals at J1-J2, J37-J51, J53-J69, J103-J119, and J121-J135 are not installed at the factory. It is not necessary to install the jumpers at J1 or J2. This connection has been made in the PC board.

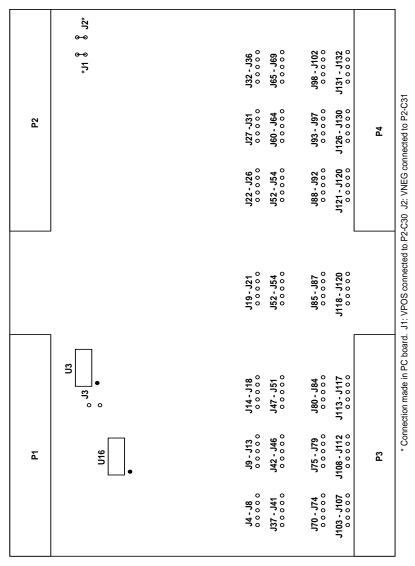


Figure 2-1 Jumper and Switch Locations

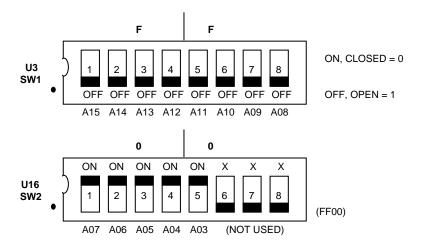
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#### **Address Modifiers**

The VMIVME-1150 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper J3. This makes the board respond to short non-privileged I/O accesses.

#### **Board Base Address**

Figure 2-2 shows the address Dual In-Line Package (DIP) switches on board the VMIVME-1150 and their use in the addressing scheme.



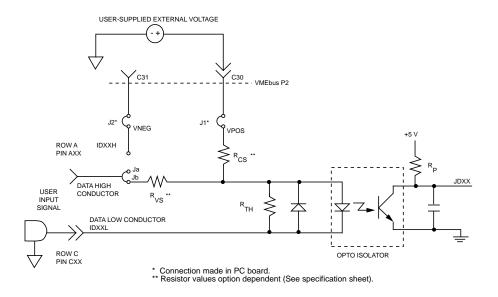
Example: For the VMIVME-1150 to respond to a base address of (FF00), the SW1 and SW2 switches should be set as shown above. X is an immaterial switch position.

Figure 2-2 Address Select Switches, SW1 and SW2

## **Application Notes**

There are three optional types of inputs available on the VMIVME-1150. They are logic source (not directly TTL compatible), voltage source, and contact sense. See Figure 2-3 and Figure 2-4 on page 30 and Figure 2-5 on page 30 for examples of the different input types. All three examples use the non-inverting option.

The different types of input, input voltages, and other options must be specified when placing an order.



**NOTE:** Connect the input such that it is across IDXXH and IDXXL (XX = channel number).

Figure 2-3 Logic Source Operation (Not Directly TTL Compatible)

# 2

# I/O Cable and Connector Configuration

The VMIVME-1150 is designed to receive inputs via two flat-ribbon cables connected to connectors P3 and P4 as shown in Figure 2-6 on page 31. This figure has conductor No. 1 shown at the bottom of the connector as it plugs into the header, due to pin No. 1 of P3 and P4 being mounted as shown.

Table 2-1 and Table 2-2 on page 32 show the P3 and P4 connector pin assignments for the 64 input channels of the VMIVME-1150. Table 2-3 on page 33 shows the pin assignments for the P2 connector.

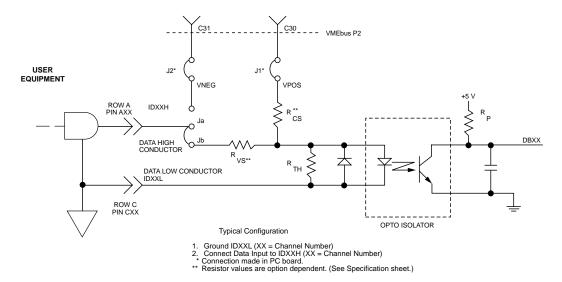


Figure 2-4 Voltage Source Operation

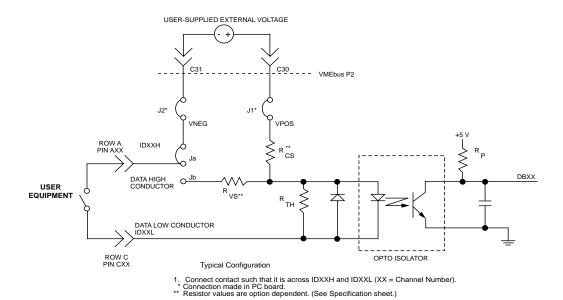
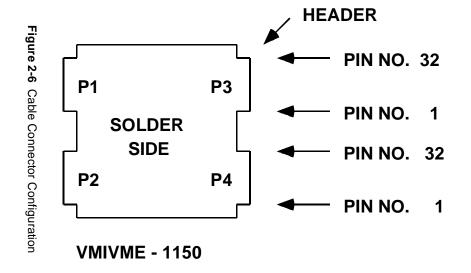


Figure 2-5 Contact Sense Operation



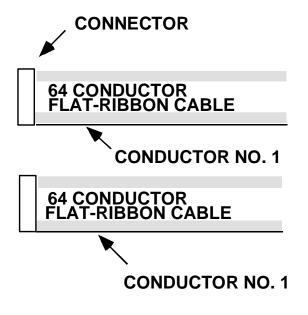


Table 2-1 P3 Pin/Channel Assignments

ROW A PIN	CHANNEL NO.	ROW C PIN	CHANNEL NO.	ROW A PIN	CHANNEL NO.	ROW C PIN	CHANNEL NO.
32	ID63H	32	ID63L	16	ID47H	16	ID47L
31	ID62H	31	ID62L	15	ID46H	15	ID46L
30	ID61H	30	ID61L	14	ID45H	14	ID45L
29	ID60H	29	ID60L	13	ID44H	13	ID44L
28	ID59H	28	ID59L	12	ID43H	12	ID43L
27	ID58H	27	ID58L	11	ID42H	11	ID42L
26	ID57H	26	ID57L	10	ID41H	10	ID41L
25	ID56H	25	ID56L	09	ID40H	09	ID40L
24	ID55H	24	ID55L	08	ID39H	08	ID39L
23	ID54H	23	ID54L	07	ID38H	07	ID38L
22	ID53H	22	ID53L	06	ID37H	06	ID37L
21	ID52H	21	ID52L	05	ID36H	05	ID36L
20	ID51H	20	ID51L	04	ID35H	04	ID35L
19	ID50H	19	ID50L	03	ID34H	03	ID34L
18	ID49H	18	ID49L	02	ID33H	02	ID33L
17	ID48H	17	ID48L	01	ID32H	01	ID32L

Table 2-2 P4 Pin/Channel Assignments

Table 2-3 P2 Connector Pin Assignments

PIN NO.	ROW A	ROW B <sup>2</sup>	ROW C <sup>1</sup>
1		+5 VOLTS	
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 VOLTS	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30		GND	Vpos
31		+5 VOLTS	Vneg
32			

1. External Reference Voltage is supplied by the user.

NOTES: 2. Inputs to Board - not required.

# **Programming**

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### Introduction

The eight 8-bit input data registers are accessed as four 16-bit registers or as eight 8-bit registers. These registers are accessed by address bits A1 and A2, when the board has been selected for a data transfer.

Thirteen address bits, A3-A15, are used for address decoding to generate a board select signal, which activates the board for a data transfer.

The VMIVME-1150 supports only 8- or 16-bit data transfers. If a Longword is attempted, the VMIVME-1150 will simply not respond and a bus error will occur.

# Register Map

Address bits A15-A3 are selected by the board base address selection switches (see "Board Base Address" on page 28 for further information). Therefore, XXX in the relative address represents the part of the address that is switch selectable.

RELATIVE ADDRESS	<b>MNEMONIC</b>	NAME/FUNCTION
\$XXX0	DR0	DATA REGISTER 0
\$XXX1	DR1	DATA REGISTER 1
\$XXX2	DR2	DATA REGISTER 2
\$XXX3	DR3	DATA REGISTER 3
\$XXX4	DR4	DATA REGISTER 4
\$XXX5	DR5	DATA REGISTER 5
\$XXX6	DR6	DATA REGISTER 6
\$XXX7	DR7	DATA REGISTER 7

# Register Bit Definitions

For Register Bit Definitions see Table 3-1 through Table 3-8.

Table 3-1 \$XXX0 Data Register 0							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
			INPUT	DATA			
ID63	ID62	ID61	ID60	ID59	ID58	ID57	ID56
		Tab	le 3-2 \$XXX1	Data Regist	er 1		
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
			INPUT	DATA			
ID55	ID54	ID53	ID52	ID51	ID50	ID49	ID48
Table 3-3 \$XXX2 Data Register 2							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
			INPUT	DATA			
ID47	ID46	ID45	ID44	ID43	ID42	ID41	ID40
Table 3-4   \$XXX3   Data Register 3							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID39	ID38	ID37	ID36	ID35	ID34	ID33	ID32
Table 3-5   \$XXX4   Data Register 4							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
			INPUT	DATA			
ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24

Table 3-6	\$XXX5	Data Register (	5
-----------	--------	-----------------	---

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16

# **Register Bit Definitions (Continued)**

Table 3-7\$XXX6Data Register 6

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
INPUT DATA							
ID15	ID14	ID13	ID12	ID11	ID10	ID 9	ID 8

Table 3-8\$XXX7Data Register 7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID 7	ID 6	ID 5	ID 4	ID 3	ID 2	ID 1	ID 0

Example: Bit 15 of Data Register 0 (1D63) corresponds to Connector P3 Pin A32 (ID63H) and Pin C32 (ID63L) as indicated in Table 2-1 on page 32.

# Maintenance

#### **Maintenance**

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

Contact VMIC customer Service at 1-800-240-7782, or E-mail: customer.service@vmic.com.

# **Maintenance Prints**

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.