VMIVME-2120
64-bit High-Voltage Digital Output Megamodule™

Product Manual

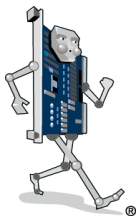
A GE Fanuc Company

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

500-002120-000 Rev. AC

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

COPYRIGHT AND TRADEMARKS



(I/O man figure)

(IOWorks man figure)

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

Table of Contents

List of Figures 7

List of Tables 9

Overview 11
Features 11
Functional Description 12
Reference Material List 13
Safety Summary 14
Ground the System 14
Do Not Operate in an Explosive Atmosphere 14
Keep Away from Live Circuits 14
Do Not Service or Adjust Alone 14
Do Not Substitute Parts or Modify System 14
Dangerous Procedure Warnings 14
Safety Symbols Used in This Manual 15

Chapter 1 - Theory of Operation 17
Operational Overview 17
Device Addressing 19
VMEbus Foundation Logic 21
Data Transfers 23
Register Control Logic 24
Control and Status Register (CSR) 25
Built-in-Test 26
Octal Registers and Output Drivers 27
Signal Function Description 30

Chapter 2 - Configuration and Installation 31
Unpacking Procedures 32
Physical Installation. 32
Jumper and Switch Locations 33
External Pull-Up Voltage/Suppressor Diode Connections. 34
Address Modifiers 35
DTACK Delay Jumper. 35
Address Selection Switches 35
I/O Cable and Card-Edge Connector Configuration 37

Chapter 3 - Programming 43
Output Data Registers Bit Maps 45
Control and Status Register Bit Definitions. 46
Detailed Programming. 47
Output Data Transfers. 47
Built-in-Test. 47

Maintenance 51
Maintenance 51
Maintenance Prints 52

List of Figures

Figure 1-1 Functional Block Diagram 19
Figure 1-2 Address Selection Block Diagram 20
Figure 1-3 Control Section Block Diagram 21
Figure 1-4 Address Section Block Diagram 22
Figure 1-5 Data Transfer Block Diagram 23
Figure 1-6 I/O Register Control Logic Block Diagram 24
Figure 1-7 CSR Control Logic Block Diagram 25
Figure 1-8 I/O Registers Block Diagram 28
Figure 1-9 I/O Registers Bank B Block Diagram 29
Figure 2-1 Switch and Jumper Locations 33
Figure 2-2 Connection for Inductive Loads or Long Cable Length 34
Figure 2-3 Jumper Installation for Pull-Up Voltage 35
Figure 2-4 Data Register Base Address Select Switches, S1 and S3 36
Figure 2-5 CSR Base Address Select Switches, S4 and S2 36
Figure 2-6 P3/P4 Front Panel Connectors 38
Figure 2-7 P2 Connector 40
Figure 2-8 Cable Connector Configuration 42
Figure 3-1 Programming Flowchart (Built-in-Test Active) 48
Figure 3-2 Programming Flowchart (Built-in-Test not Active) 49

List of Tables

Table 2-1 P3/P4 Connector Pin Assignments 39
Table 2-2 P2 Connector Pin Assignments 41
Table 3-1 Data Register Address Map 43
Table 3-2 CSR Address Map 44
Table 3-3 Output Data Register Bit Map 45
Table 3-4 CSR Bit Definitions 46

Overview

Introduction

Features

The VMIVME-2120 is capable of delivering 64 channels of high voltage and / or high current sink outputs. The VMIVME-2120 open collector output drivers are capable of supporting output voltages from 5 VDC to 48 VDC. A unique feature of the VMIVME-2120 Board is the Built-in-Test (BIT) logic, which allows the user, under software control, to verify the operation of each channel.

A brief overview of the VMIVME-2120's features include the following:

- 64 channels of high voltage digital outputs (5 to 48 VDC)
- 8-, 16- or 32-bit VMEbus data transfers
- High current open collector drivers (600 mA sink) with built-in suppressor diodes
- Outputs may be paralleled for higher drive capability
- Open collector pull-up resistors (optional)
- Optional fault protection for the outputs (outputs shutdown when current exceeds 1.0 A) may or may not be ordered
- Built-in-Test logic
- Front Panel software controlled Fail LED (for Built-in-Test)
- Separate user configurable address switches for the Control Status Register (CSR) and the data registers allow for contiguous addressing when more than one board is used in a VMEbus system

Functional Description

The VMIVME-2120 is a member of VMIC's Megamodule™ family which is designed with common programming features such that subsystems may be configured with contiguous I/O addresses to conserve memory. Each of these boards (VMIVME-1110, -1111, -2130, -2131, -2120, and -2510B) is designed with two sets of board address switches or jumpers to provide an efficient memory address map for the Control Status Registers (CSR) and the data I/O registers. CSR address switches may be set such that all CSRs among a variety of boards in the system are mapped into contiguous memory locations, while the data I/O addresses are mapped into another contiguous region of memory.

The Megamodule™ product line is designed to support 8-, 16-, and 32-bit data transfers and also features a front panel Fail LED that is illuminated at power-up or system reset and which may be extinguished under program control upon successful completion of board level diagnostics. The VMIVME-2120 has been designed with specific hardware to support Built-in-Test functions. These functions support both off-line and on-line fault detection and isolation.

Reference Material List

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VMEbus Specification Rev. C. and the VMEbus Handbook

VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

Physical Description and Specification

Refer to Specification 800-002120-000 available from:
VMIC
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308, USA
(256) 880-0444
(800) 322-3616
FAX: (256) 882-0859
www.vmic.com

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

Safety Symbols Used in This Manual

STOP: informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

CHAPTER 1

Theory of Operation

Contents

Device Addressing 19
VMEbus Foundation Logic 21
Data Transfers 23
Register Control Logic 24
Control and Status Register (CSR) 25
Built-in-Test 26
Octal Registers and Output Drivers 27
Signal Function Description 30

Introduction

Operational Overview

The VMIVME-2120 is designed for a variety of applications such as:

- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high-voltage drivers, and
- Fiber-optic LED drivers

The design of the VMIVME-2120 board as shown in the functional block diagram in Figure 1-1 on page 19 consists primarily of four sections which are:

- VMEbus Foundation Logic
- Device Addressing
- Output Drivers
- Built-in-Test Logic

The VMIVME-2120 board is designed using eight 8-bit bidirectional registers, a Control Status Register (CSR), high-performance output drivers, typical VMEbus foundation logic, and two device address switch banks. The two switch banks provide the user with the capability and flexibility to map I/O registers and CSRs into separate contiguous memory locations.

Device Addressing

The VMIVME-2120 is designed to support data transfers in supervisory or nonprivileged short I/O memory space. A jumper is provided as shown in Figure 1-1 (Address Selection Block Diagram) to allow user selection of either I/O access type. The jumper (JA) is shown on logic diagram 141-002120-000 in Appendix A. The VMIVME-2120 is factory configured (jumper JA not installed) to respond to short supervisory I/O access.

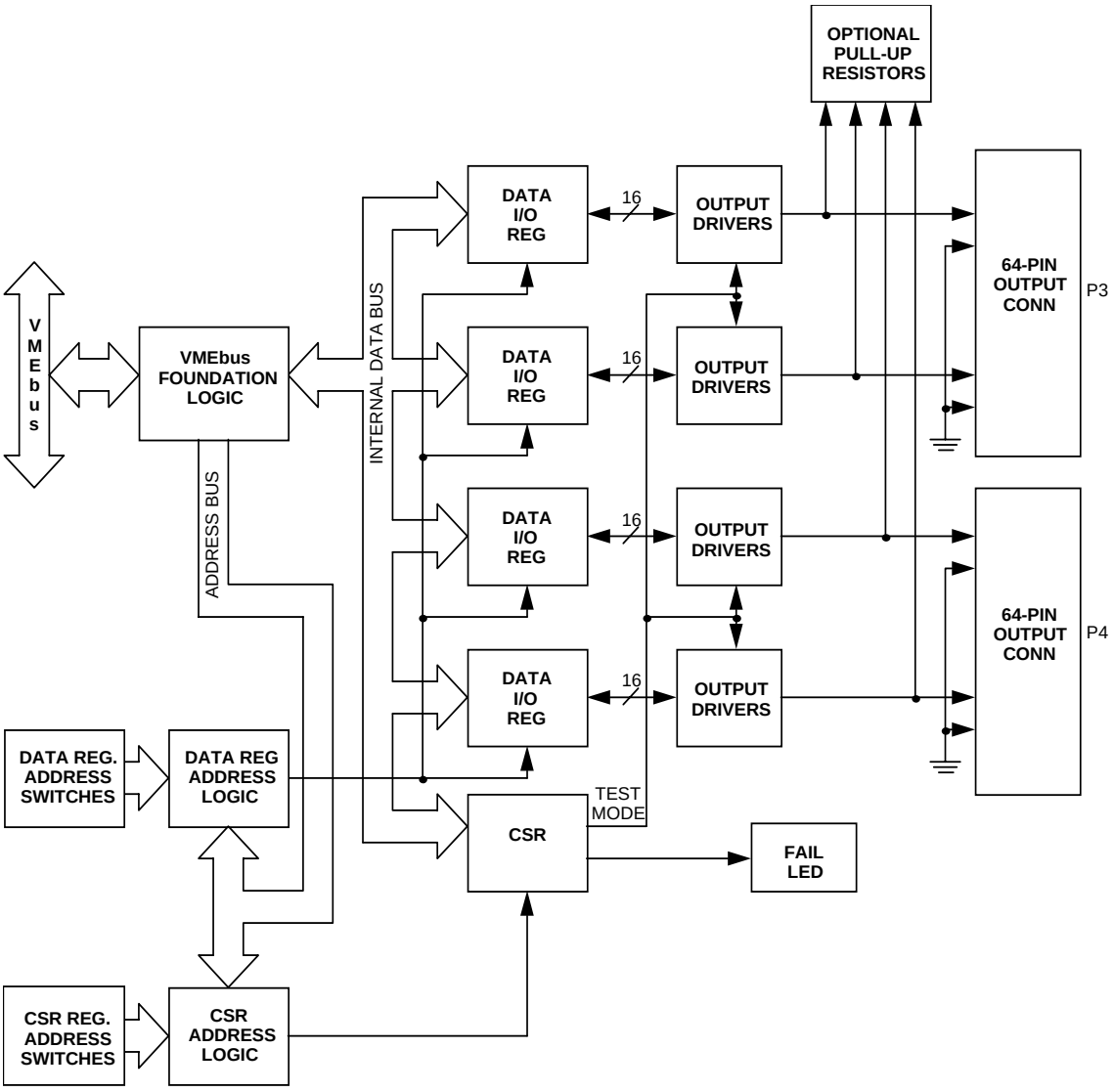


Figure 1-1 Functional Block Diagram

The VMIVME-2120 is designed with two sets of board select switches and decode logic as shown in Figure 1-2 to provide an efficient memory address map for CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into separate contiguous memory locations when configuring subsystems that require more than one board.

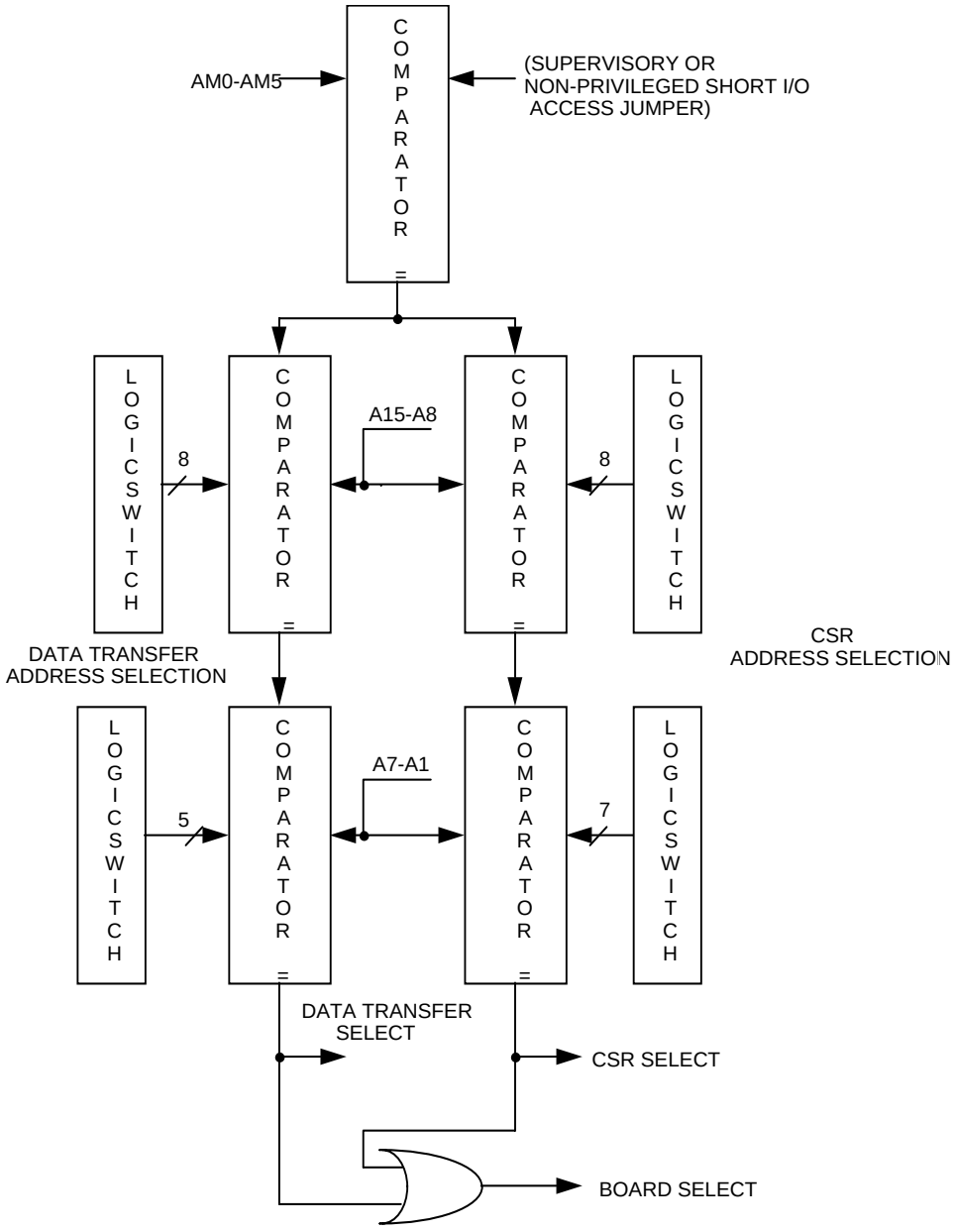


Figure 1-2 Address Selection Block Diagram

VMEbus Foundation Logic

Typical VMEbus drivers, receivers, and control logic are shown in Figure 1-3 and Figure 1-4. The DTACK generator shown in Figure 1-4 is designed with a jumper installed at the factory to provide the maximum data transfer rate.

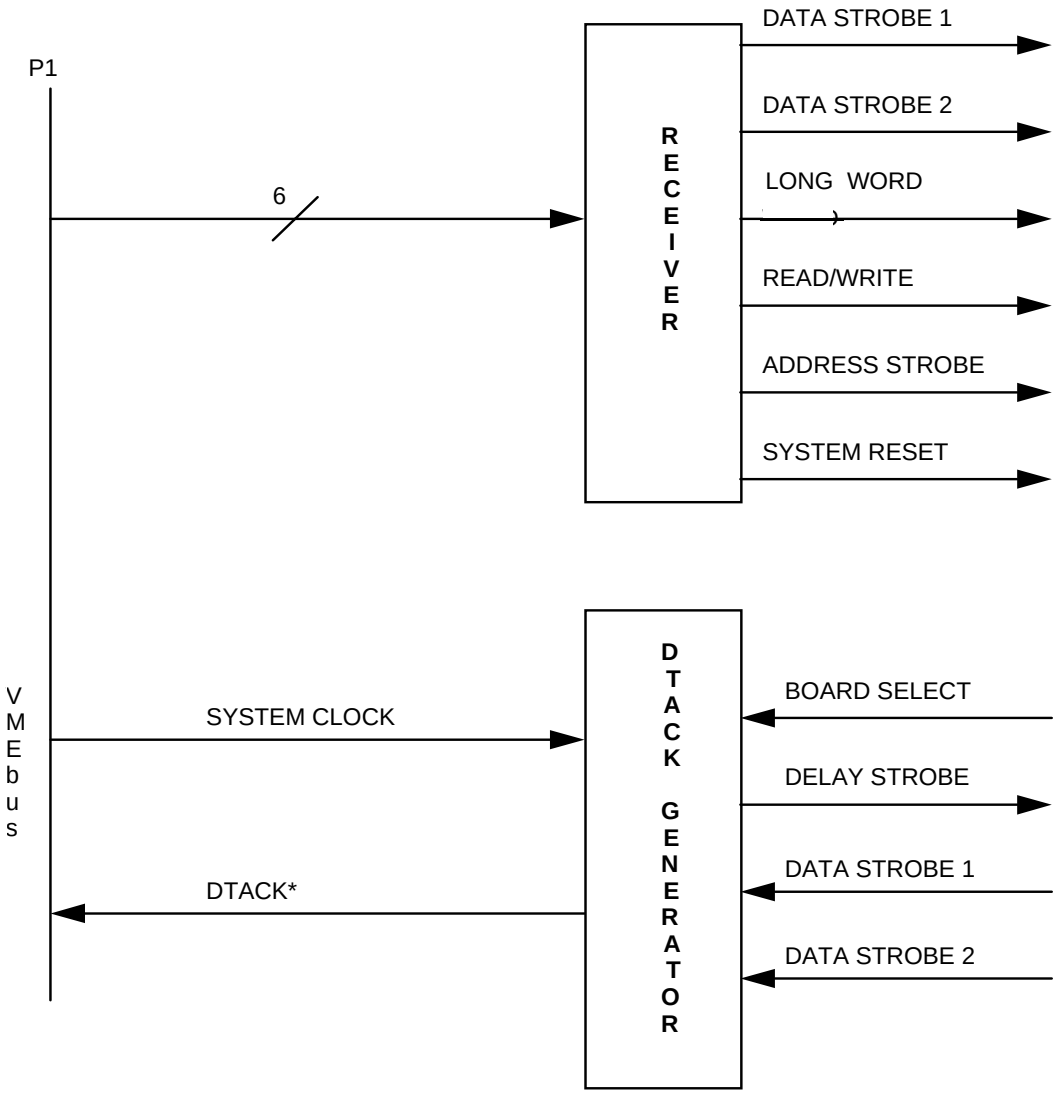


Figure 1-3 Control Section Block Diagram

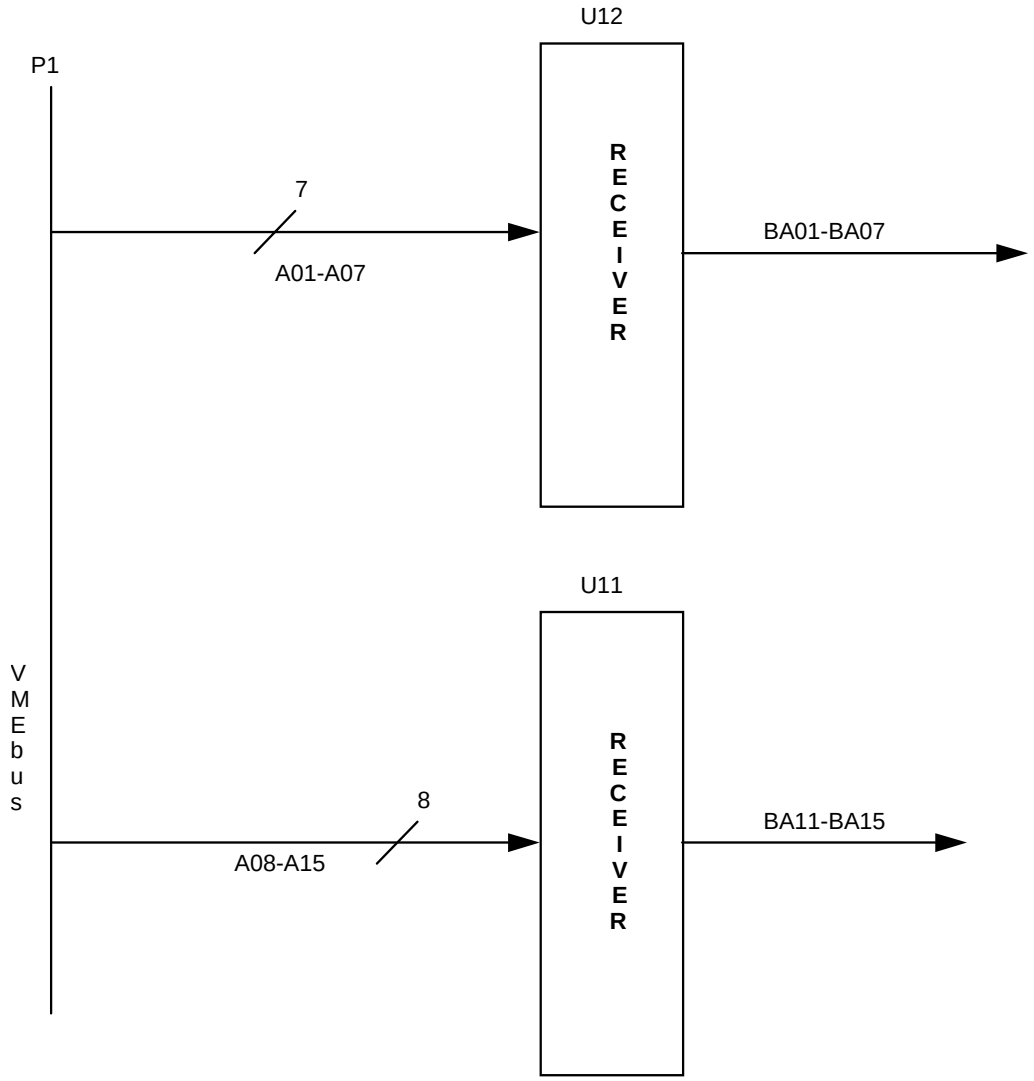


Figure 1-4 Address Section Block Diagram

Data Transfers

Data transfer transceivers are shown in Figure 1-5. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries.

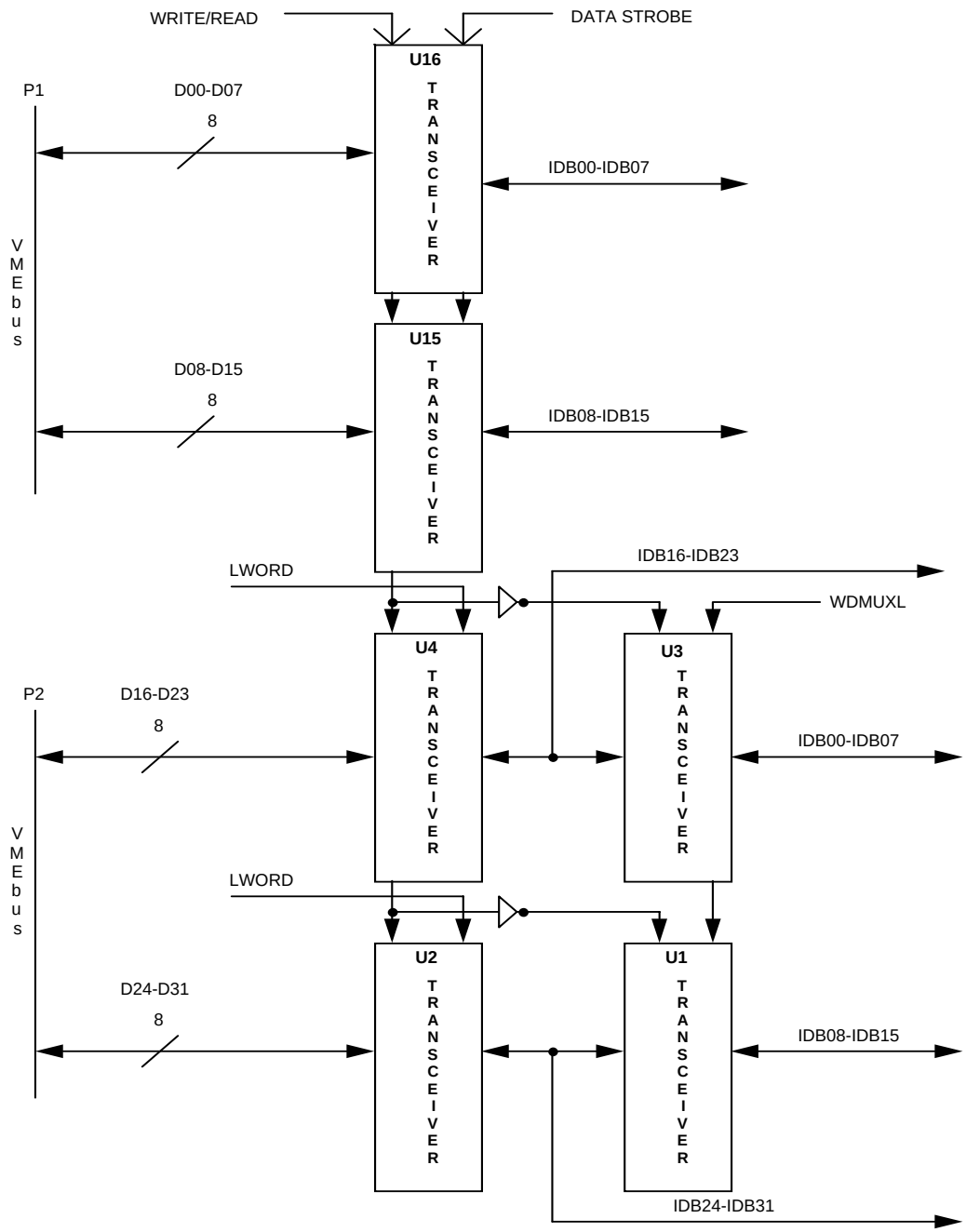


Figure 1-5 Data Transfer Block Diagram

Register Control Logic

The VMIVME-2120 board register control logic is designed to support *write* and *read* operations to and from eight 8-bit bi-directional dual port latches and write transfers to a CSR register that controls the test mode and front panel LED. The control logic shown in Figure 1-6 is separated into *read* and *write* control signals and provides the capability to *read* or *write* 8, 16, or 32 bits of data. To perform output data transfers, data is transferred via transceivers, which are selected by address bits A2, A1, and the data strobes. The 64 bits of high voltage outputs are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

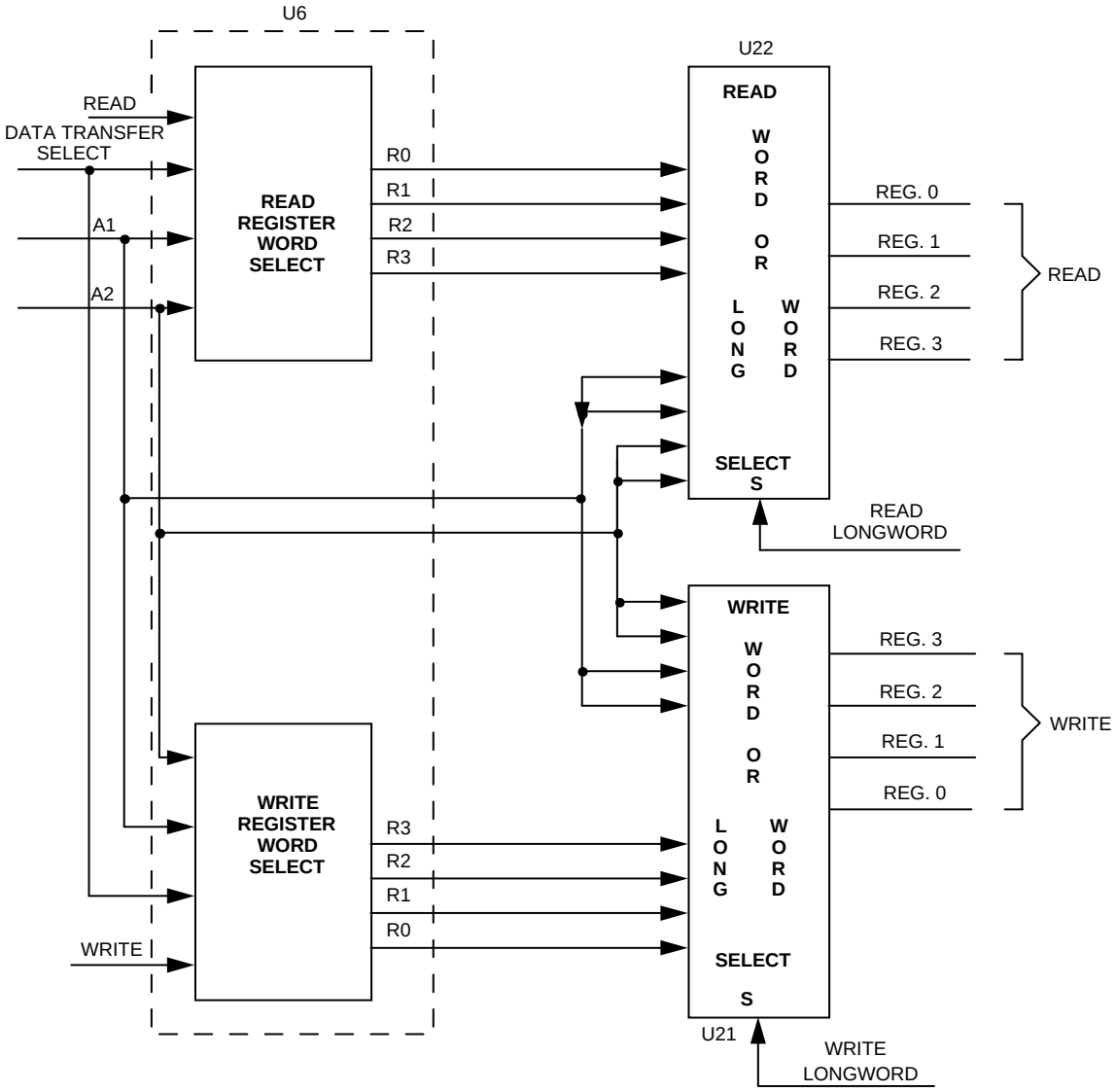


Figure 1-6 I/O Register Control Logic Block Diagram

Control and Status Register (CSR)

The CSR is a *write only* register that controls the Test Mode (TM) bit (bit 7) and the front panel Fail LED (bit 6) as shown in Figure 1-7. The TM bit disables the output drivers to perform Built-in-Test functions. Both bits of the CSR are initialized active upon system reset such that the register outputs are disabled and the front panel LED is illuminated. Writing a "zero" to these bits will turn the LED OFF and enable the output drivers.

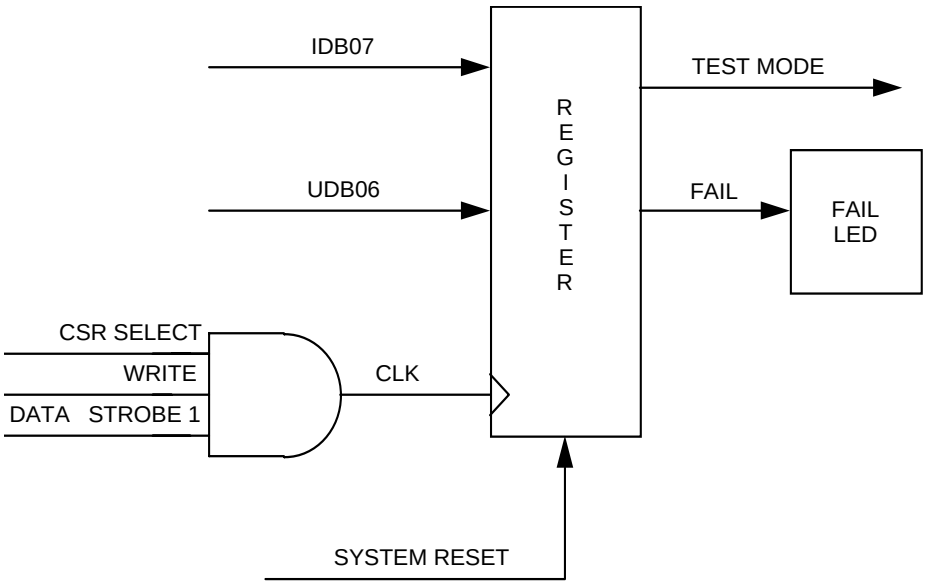


Figure 1-7 CSR Control Logic Block Diagram

Built-in-Test

The Built-in-Test feature of the VMIVME-2120 is enabled by asserting the test mode bit in the CSR. While in test mode, test data may be written to any Output Data Register (ODR), and read back on a *read* operation. While in test mode, accessing an ODR does not affect the user equipment since the output drivers are disabled by the test mode bit.

The Built-in-Test features of this product provide the user with the capability of performing real-time loopback testing with the output drivers connected, and off-line diagnostic testing with the output drivers disconnected from the field devices.

A front panel Fail LED is provided for quick fault isolation to the board level. The Fail LED is illuminated at power-up or system reset and may be extinguished by the user upon successful diagnostic execution.

Octal Registers and Output Drivers

A block diagram of the eight 8-bit I/O registers is shown in Figure 1-8 and Figure 1-9 on page 29. The AM295X I/O registers were selected as the primary building block because of their read back features, which allow the design to perform the Built-in-Test functions. An AM2952 is used for positive true boards, while the AM2953 is used on negative true boards.

The VMIVME-2120 is designed to support a wide range of output options. A jumper selectable option is provided that allows the selection of the 5 volt VMEbus power or an external power source for the open collector output drivers. If an external connection is required, it is supplied on pin A1 of connector P2. The VMIVME-2120 is factory configured with the pull-up voltage jumpered to the 5 volt VMEbus power.

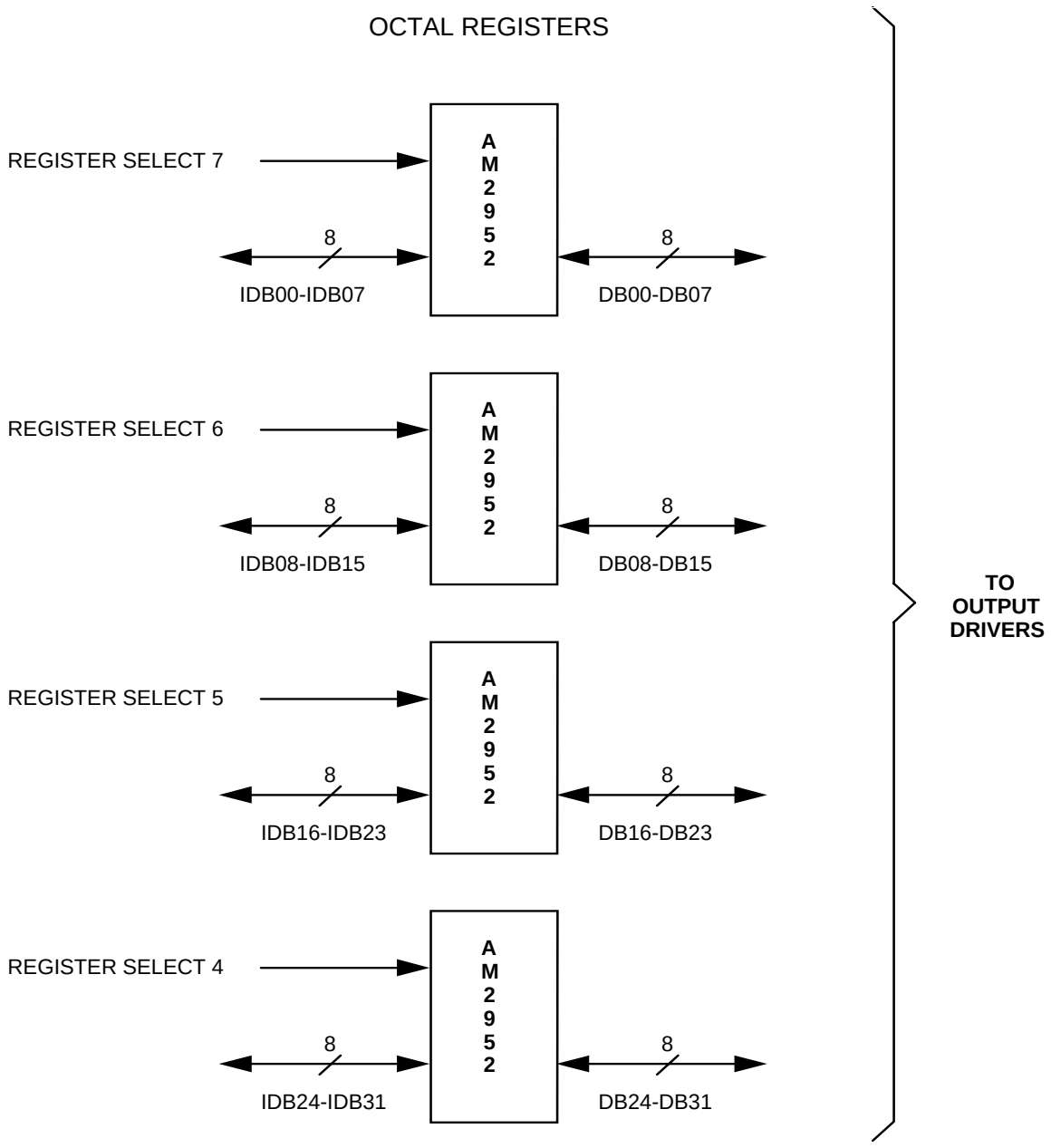


Figure 1-8 I/O Registers Block Diagram

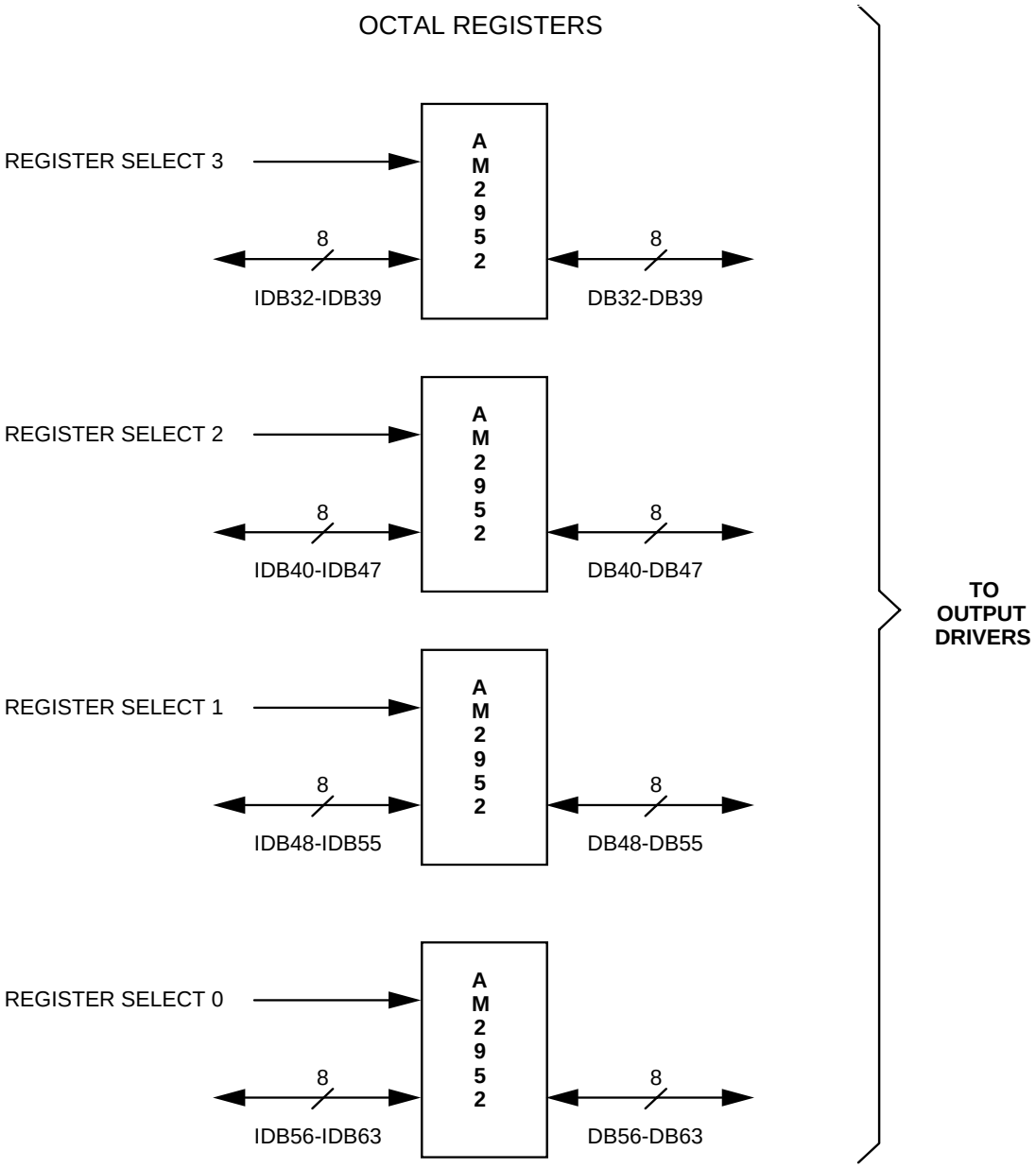


Figure 1-9 I/O Registers Bank B Block Diagram

Signal Function Description

The following paragraphs describe some of the key signals used on the VMIVME-2120.

1. DTBSL: DATA TRANSFER - Board Select, active low. This signal is active when an I/O data register address matches the VMEbus address.
2. CSRBSL: CONTROL STATUS REGISTER - BOARD SELECT, active low. This signal is active when the CSR address matches the VMEbus address.
3. BSL: BOARD SELECT, active low. The signal is active when either DTBSL or CSRBSL is active, and is used to gate control signals onto the board.
4. GDS0L: GATED DS0, active low. This is the gated data strobe 0.
5. GDS1L: GATED DS1, active low. This is the gated data strobe 1.
6. GLWORDL: GATED LWORD, active low. This signal is used for transceiver control and I/O data register selection.
7. GDS0DL: GATED DS0 DELAYED, active low.
8. GDS1DL: GATED DS1 DELAYED, active low. These delayed signals allow setup time through the data transceivers before clocking the data into the I/O data registers.
9. TML: TEST MODE, active low.
10. FAILH: FAIL MODE, active high.
11. WDMUXL: WORD MULTIPLEXER, active low. This signal allows the IDB16-IDB31 data bits to be transferred onto data lines D00 to D15 of the VMEbus or vise-versa.

CHAPTER
2

Configuration and Installation

Contents

Unpacking Procedures 32
Jumper and Switch Locations 33
External Pull-Up Voltage / Suppressor Diode Connections 34
I / O Cable and Card-Edge Connector Configuration 37

Introduction

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

NOTE: Do not install or remove board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

Jumper and Switch Locations

The physical locations of the jumpers and switches described in this section are shown in Figure 2-1.

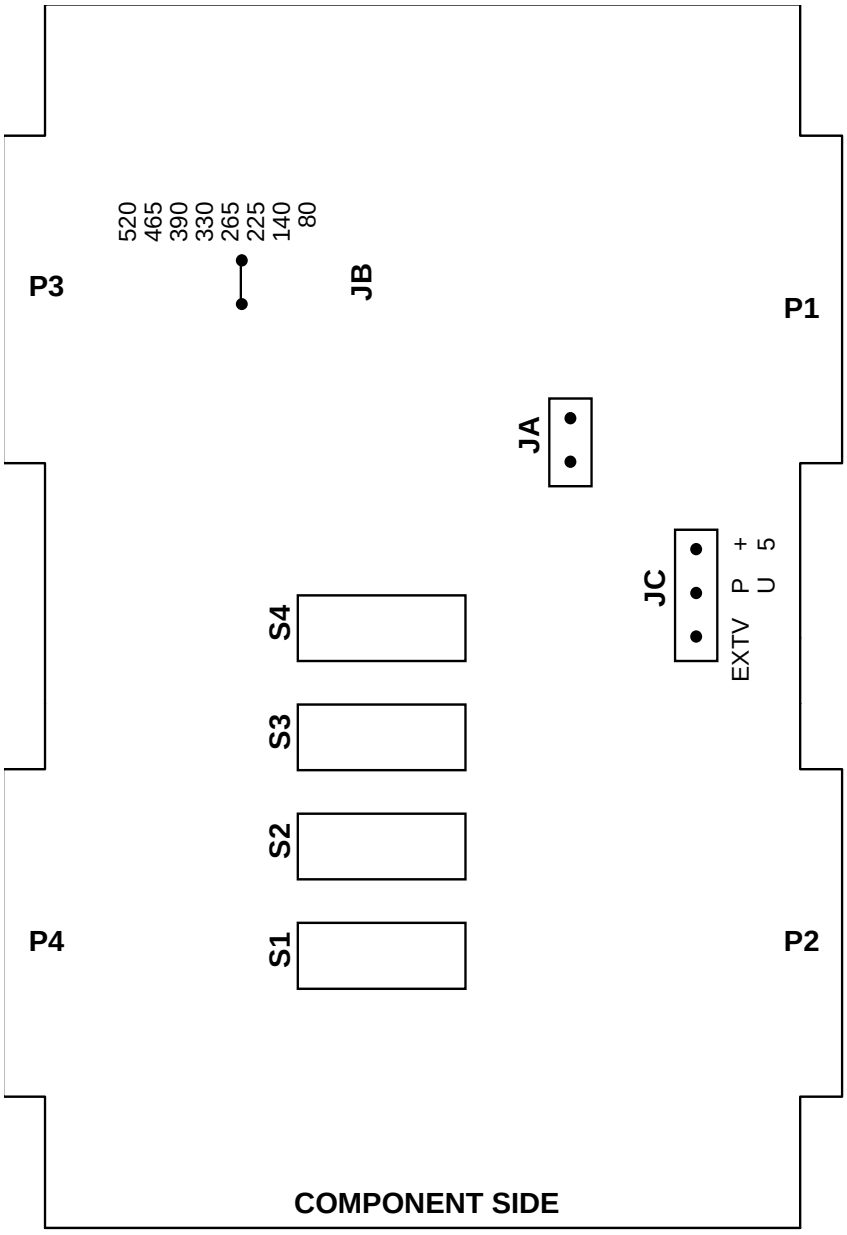


Figure 2-1 Switch and Jumper Locations

External Pull-Up Voltage/Suppressor Diode Connections

The output drivers of the VMIVME-2120 have built-in suppressor diodes for protection while driving inductive loads. If the user requires operation for a relay driver or a similar application, the coil voltage must be connected to the VMIVME-2120 External Voltage (EXTV) signal via connector P2 pin A1. User ground should be connected to P3/P4 Row C pins. The configuration and the required external voltage connection are shown in Figure 2-2 below and Figure 2-3 on page 35. The EXTV signal is routed to all 64 output channel circuits. In addition to suppressing inductive flyback the EXTV signal supplies a voltage to the optional pull-up resistors for electronic switch applications. The on-board 5 VDC power can be jumpered to the EXTV signal if +5 VDC is to be used for the pull-up voltage or the relay coil voltage as shown in Figure 2-3 on page 35.

WARNING: When driving **INDUCTIVE LOADS** or long cables, Jumper JC **MUST BE** connected to EXTV and P2-A1 **MUST BE** connected to the **USERS** relay coil voltage. If this is not done **SEVERE DAMAGE** may result from Inductive flyback voltage spikes that exceed maximum allowable levels. User ground must be connected to P3/P4 Row C pins. Failure to connect user ground may result in excess currents on the VME Backplane.

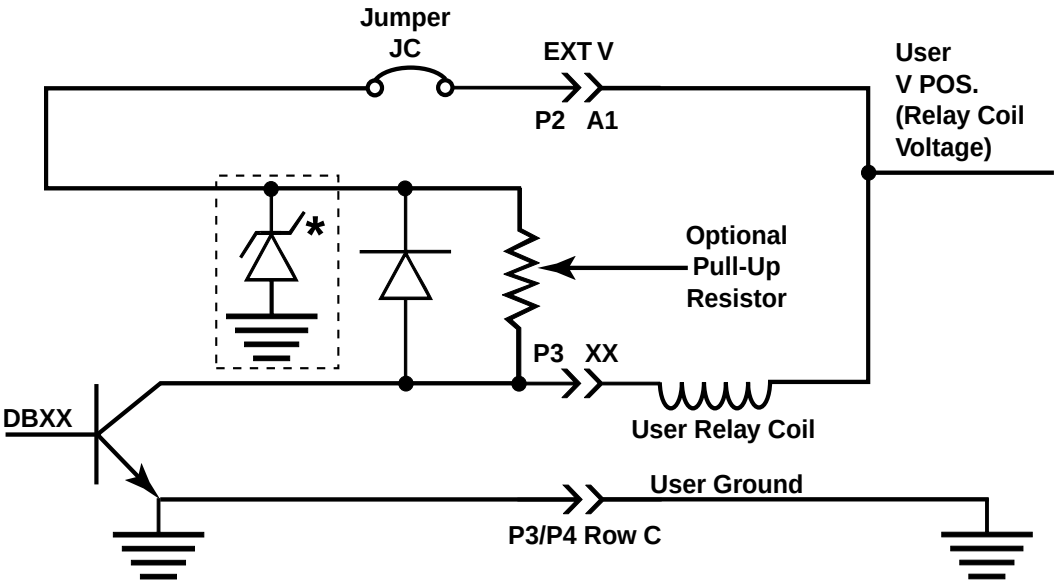


Figure 2-2 Connection for Inductive Loads or Long Cable Length

NOTE: * The Zener diode is supported on assembled board No. 332-002120-K and later. For support on assembled board No. 332-002120-000-J and earlier, refer to Document No. 132-002120-000 (Assembly Drawing).

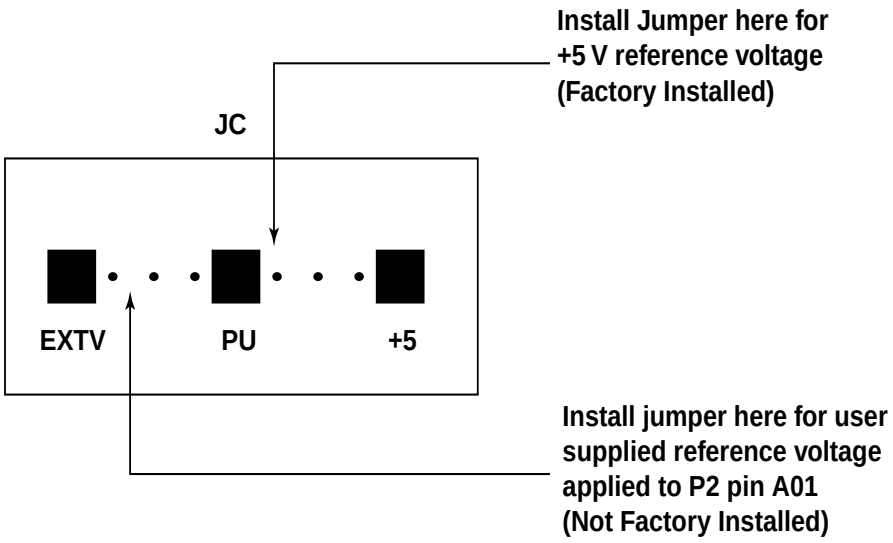


Figure 2-3 Jumper Installation for Pull-Up Voltage

Address Modifiers

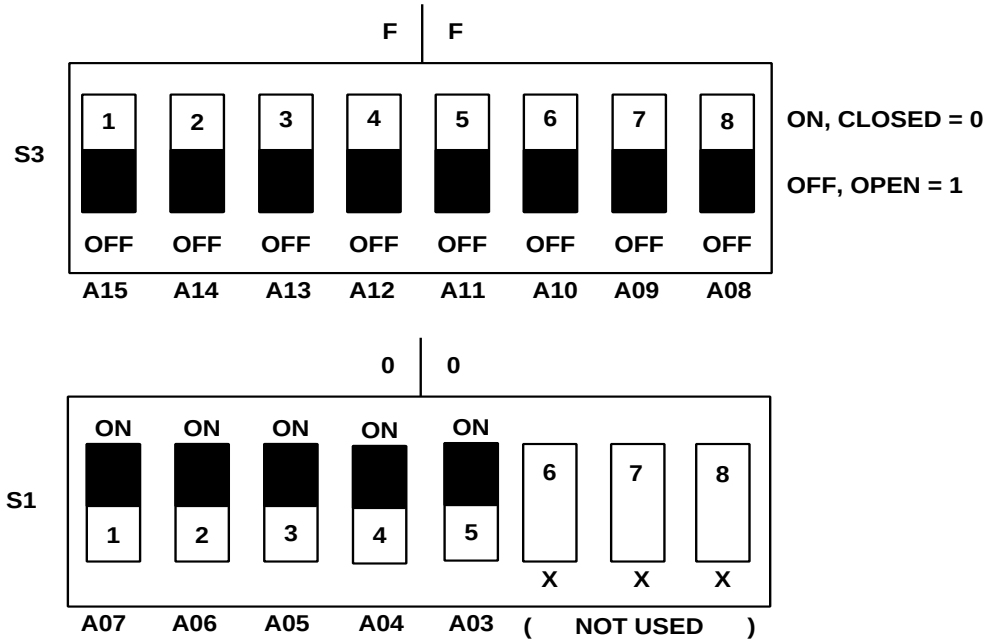
The VMIVME-2120 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed, by installing the jumper "JA". This will make the board respond to short non-privileged I/O access.

DTACK Delay Jumper

The VMIVME-2120 DTACK delay jumper is configured at the factory and should not be changed. It is set for the maximum data transfer rate.

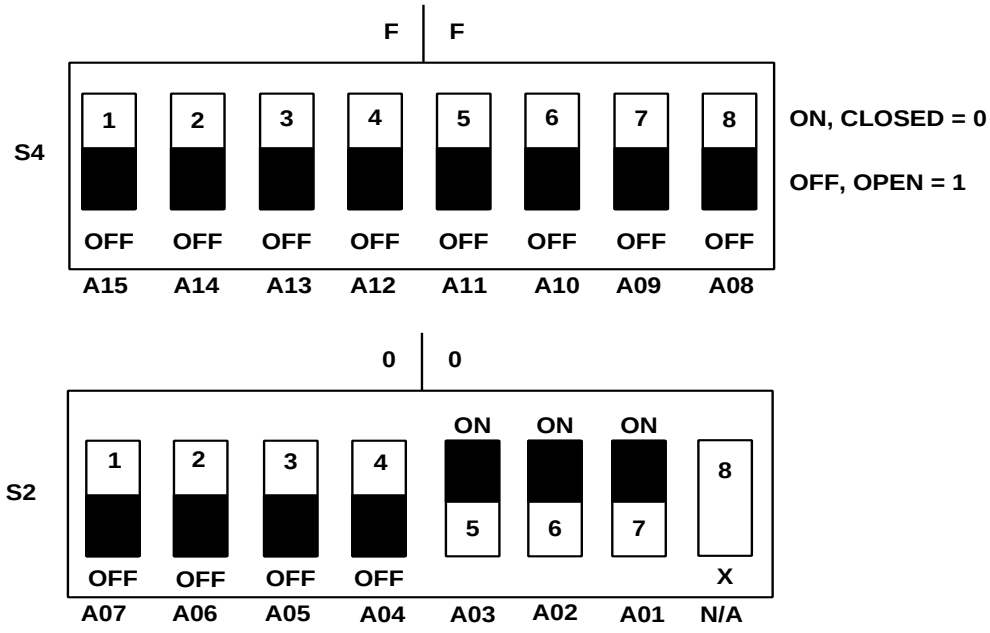
Address Selection Switches

The VMIVME-2120 is designed with two banks of address select switches that specify the beginning board address for data transfers and the address of the Control Status Register (CSR). The address selection switches are shown in Figure 2-2 on page 34 and Figure 2-3 above. The VMIVME-2120 is factory configured to respond to FF00 HEX for the data registers and to FFF0 HEX for the CSR.



The example shown is for a Base Address of $FF00 (Hex)

Figure 2-4 Data Register Base Address Select Switches, S1 and S3



The example shown is for a Base Address of $FFF0 (Hex)

Figure 2-5 CSR Base Address Select Switches, S4 and S2

I/O Cable and Card-Edge Connector Configuration

The output connectors (P3 and P4) on the VMIVME-2120 are 64 pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's connector and I/O Cable Application Guide (VMIC Document 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Output connector pin configurations for P3 and P4 are shown in Table 2-1 on page 39. Figure 2-6 on page 38 below illustrates the P3/P4 connectors. Details concerning connector P2 user I/O pins and the use of the external voltage input is shown in Table 2-2 on page 41 and Figure 2-7 on page 40.

The VMIVME-2120 board is designed with a high quality ground plane that is connected to VMEbus ground and to Row C I/O pins on connectors P3 and P4 to provide enhanced noise immunity and more reliable operation. Details concerning ouput cabling is shown in Figure 2-8 on page 42. This figure has conductor No.1 shown at the bottom of the cable as it plugs into the header. Connector pin assignments for the 64 output channels are shown in Table 2-1 on page 39. A compatible flat-ribbon cable connector is Panduit No.120-964-435E. A compatible strain relief is Panduit No.100-000-032.

CAUTION: If the total load current (transient and steady state) exceeds 1 AMP, it is important that the grounded conductors (P3/P4 Row C) be connected to the power supply (GND return (P3/P4 Row C) associated with these signal loads. This ground connection will prevent excessive currents (DC or noise) from flowing through the VMEbus backplane.

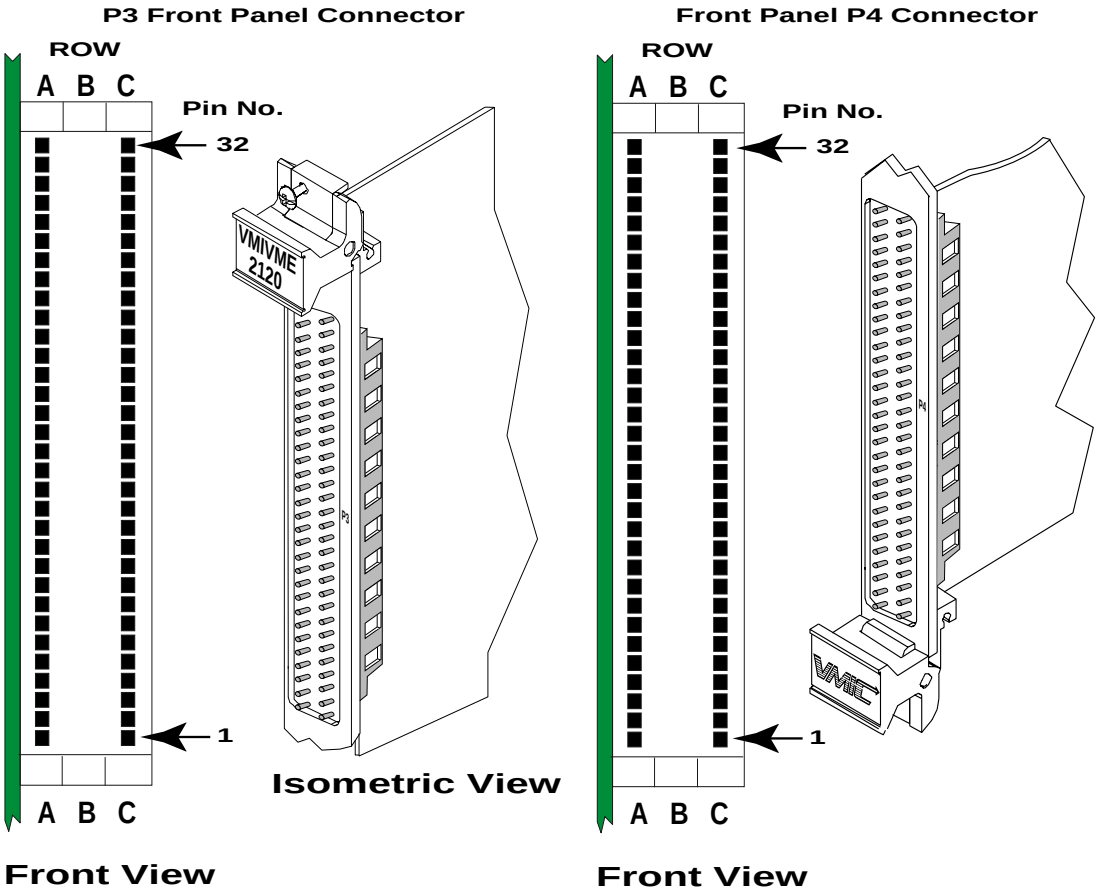


Figure 2-6 P3/P4 Front Panel Connectors

Table 2-1 P3/P4 Connector Pin Assignments

P3			P4		
Pin	**Row A**	**Row C**	**Pin**	**Row A**	**Row C**
32	63	GND	32	31	GND
31	62	GND	31	30	GND
30	61	GND	30	29	GND
29	60	GND	29	28	GND
28	59	GND	28	27	GND
27	58	GND	27	26	GND
26	57	GND	26	25	GND
25	56	GND	25	24	GND
24	55	GND	24	23	GND
23	54	GND	23	22	GND
22	53	GND	22	21	GND
21	52	GND	21	20	GND
20	51	GND	20	19	GND
19	50	GND	19	18	GND
18	49	GND	18	17	GND
17	48	GND	17	16	GND
16	47	GND	16	15	GND
15	46	GND	15	14	GND
14	45	GND	14	13	GND
13	44	GND	13	12	GND
12	43	GND	12	11	GND
11	42	GND	11	10	GND
10	41	GND	10	09	GND
09	40	GND	09	08	GND
08	39	GND	08	07	GND
07	38	GND	07	06	GND
06	37	GND	06	05	GND
05	36	GND	05	04	GND
04	35	GND	04	03	GND
03	34	GND	03	02	GND
02	33	GND	02	01	GND
01	32	GND	01	00	GND

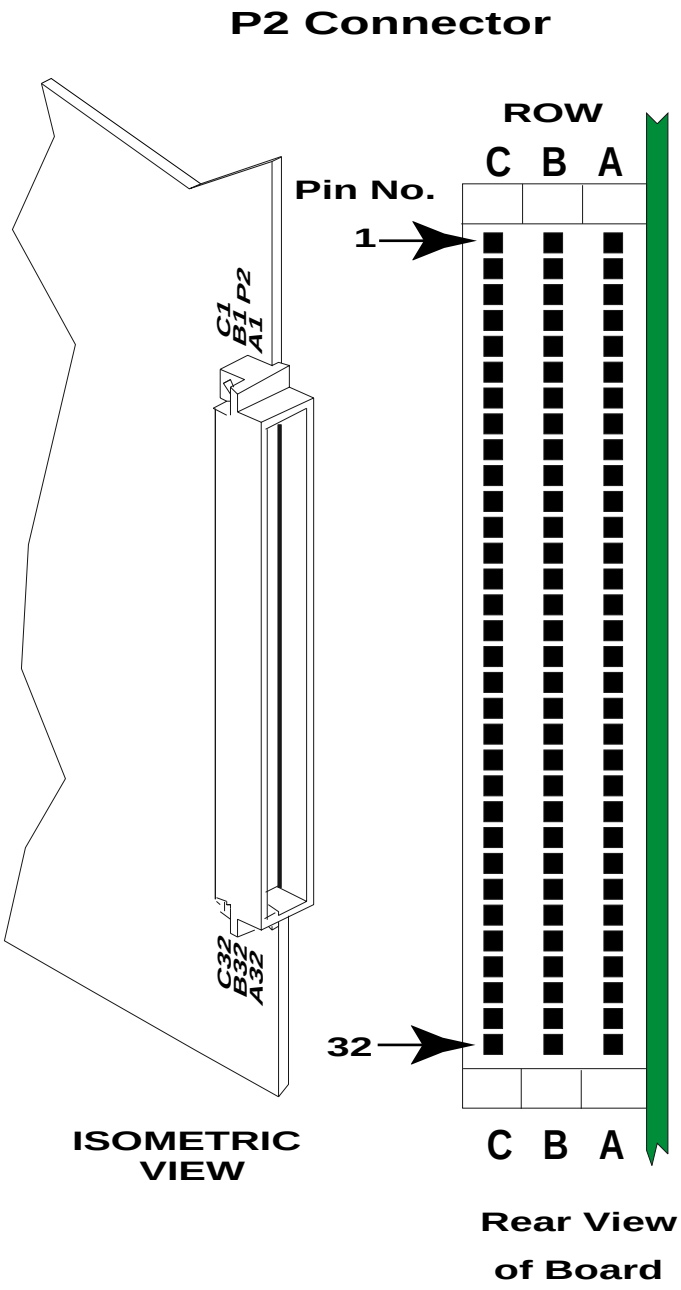


Figure 2-7 P2 Connector

Table 2-2 P2 Connector Pin Assignments

Pin	Row B[2]	Row C
1	+5 V	EXTV[1]
2	GND	
3		
4		
5		
6		
7		
8		
9		
10		
11		
12	GND	
13	+5V	
14		
15		
16		
17		
18		
19		
20		
21		
22	GND	
23		
24		
25		
26		
27		
28		
29		
30		
31	GND	
32	+5V	

NOTES:

[1] External reference voltage is supplied by the user.

[2] Inputs to the board - not required.

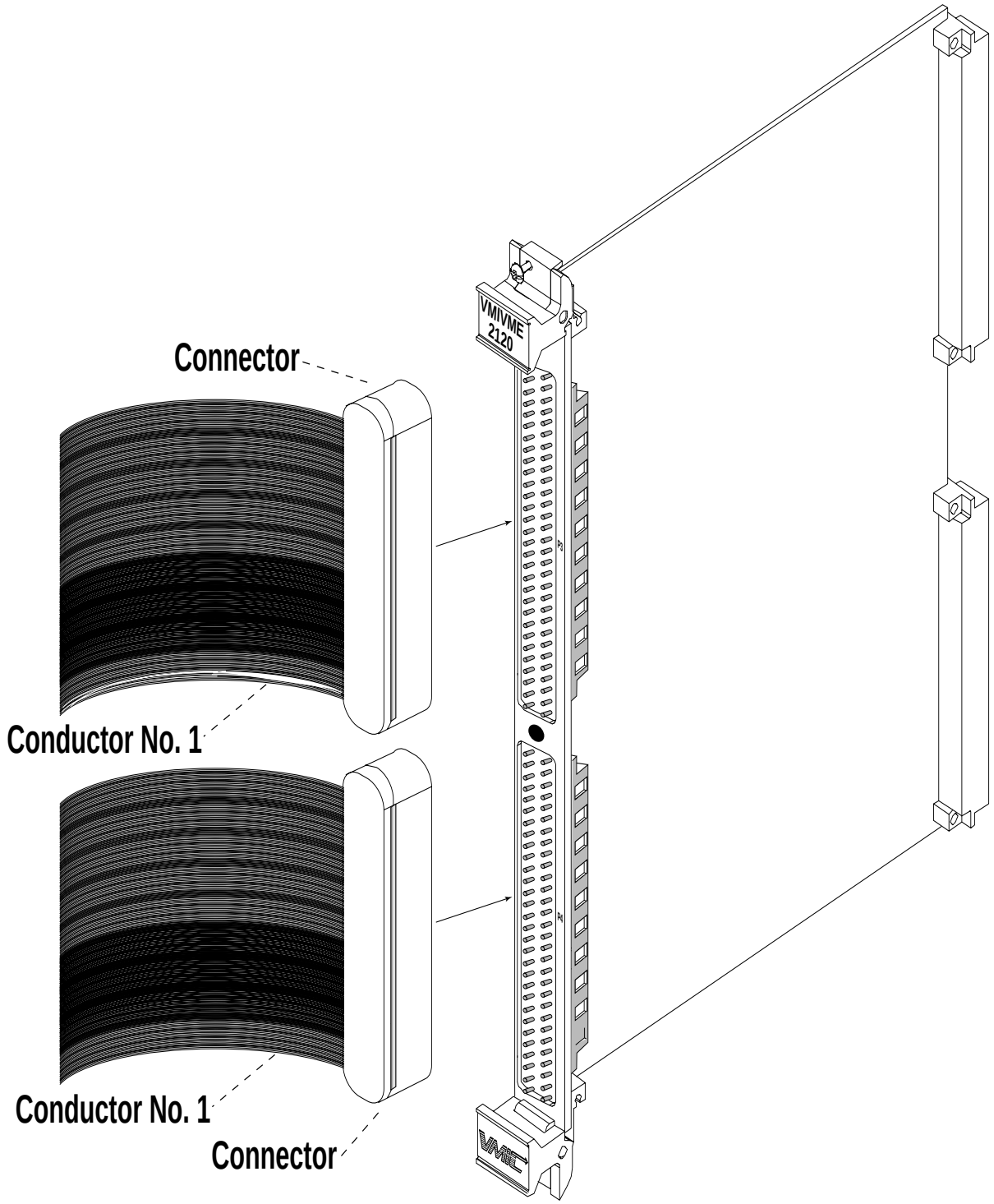


Figure 2-8 Cable Connector Configuration

CHAPTER 3

Programming

Contents

Output Data Registers Bit Maps 45
Detailed Programming 47

Register Map

The VMIVME-2120 contains eight 8-bit Output Data Registers (ODR) and a 16-bit Control Status Register (CSR). Register address maps are shown in Table 3-1 below and Table 3-2 on page 44. The ODR allows control of 64 high voltage, digital output channels and are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes. The ODR can be read under program control for data validation or diagnostic testing. The CSR is a *write only* register addressable as a 16-bit word or as two 8-bit bytes.

Table 3-1 Data Register Address Map

RELATIVE ADDRESS*	MNEMONIC	NAME/FUNCTION
$XXX0	DR0	DATA REGISTER 0
$XXX1	DR1	DATA REGISTER 1
$XXX2	DR2	DATA REGISTER 2
$XXX3	DR3	DATA REGISTER 3
$XXX4	DR4	DATA REGISTER 4
$XXX5	DR5	DATA REGISTER 5
$XXX6	DR6	DATA REGISTER 6
$XXX7	DR7	DATA REGISTER 7

NOTE: DR0-DR7 are *read/write* registers.
*XXX of address is determined by data register address select switches S3 and S1 as shown in Chapter 2.

Table 3-2 CSR Address Map

RELATIVE ADDRESS**	MNEMONIC	NAME/FUNCTION
$YYY0	CSRU	CSR UPPER BYTE
$YYY1	CSRL	CSR LOWER BYTE

NOTE: The CSR is a *write only* register.
**YYY of address is determined by CSR address select switches S4 and S2 as shown in Chapter 2.

Output Data Registers Bit Maps

The ODR bit map is shown in Table 3-3 below, and the CSR bit definitions are shown in Table 3-4 on page 46.

Table 3-3 Output Data Register Bit Map

Output Data Register: $XXX0 Data Register 0							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD63	OD62	OD61	OD60	OD59	OD58	OD57	OD56

Output Data Register: $XXX1 Data Register 1							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD55	OD54	OD53	OD52	OD51	OD50	OD49	OD48

Output Data Register: $XXX2 Data Register 2							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40

Output Data Register: $XXX3 Data Register 3							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD39	OD38	OD37	OD36	OD35	OD34	OD33	OD32

Output Data Register: $XXX4 Data Register 4							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
OD31	OD30	OD29	OD28	OD27	OD26	OD25	OD24

Output Data Register: $XXX5 Data Register 5							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
OD23	OD22	OD21	OD20	OD19	OD18	OD17	OD16

Output Data Register: $XXX6 Data Register 6							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OD15	OD14	OD13	OD12	OD11	OD10	OD9	OD8

Output Data Register: $XXX7 Data Register 7							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OD7	OD6	OD5	OD4	OD3	OD2	OD1	OD0

Control and Status Register Bit Definitions

Table 3-4 CSR Bit Definitions

Control and Status Register: $YYY0 CSRU							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Not Used							

Control and Status Register: $YYY1 CSRL							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TM=1	FL=1	Not Used					

Detailed Programming

Output Data Transfers

The register bit map in *Output Data Registers Bit Maps* on page 45 shows the correspondence between the ODRs (DR0 to DR7) and the output data channels 63 to 0.

Built-in-Test

The Built-in-Test features of the VMIVME-2120 provides the user with the capability of real-time loopback data verification and off-line diagnostic execution. The off-line Built-in-Test feature is initiated by setting the Test Mode (TM) bit in the CSR to a logic "one". When the TM bit is set, all of the output drivers are tristated, and test data can be written to the selected data register and read back on a *read* transfer without affecting the user's equipment. Data can also be read back when Test Mode is OFF. This permits on-line testing of the board.

The test mode bit and the Fail LED control bit are initialized ACTIVE at power-up or upon system reset. Thus, the Fail LED is ON and the output drivers are DISABLED. Simplified programming flow charts are shown in Figure 3-1 on page 48 and Figure 3-2 on page 49.

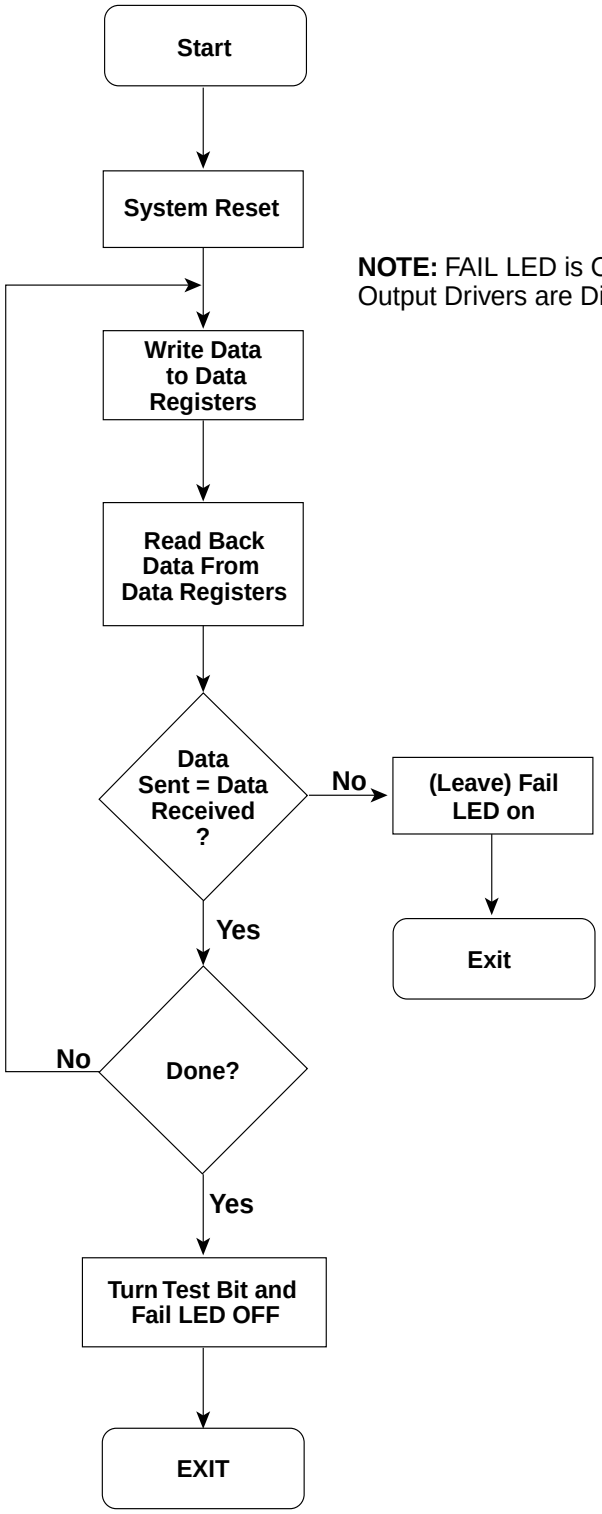
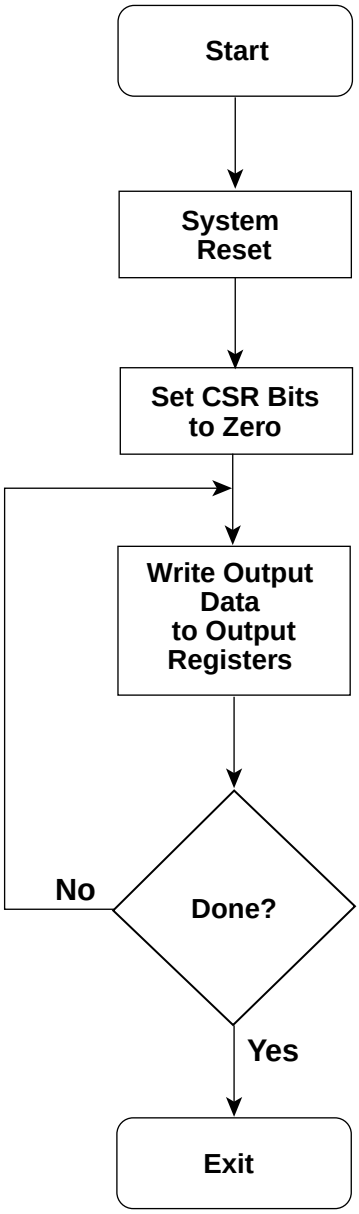


Figure 3-1 Programming Flowchart (Built-in-Test Active)



NOTE: At system reset, output drivers are disconnected and the Fail LED is illuminated

Figure 3-2 Programming Flowchart (Built-in-Test not Active)

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.