VMIVME-2232

32-CHANNEL RELAY OUTPUT BOARD WITH BUILT-IN-TEST

INSTRUCTION MANUAL

DOCUMENT NO. 500-002232-000 N

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VME Microsystems International Corporation

RECORD OF REVISIONS

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N	07/14/95	Cover, pages ii, and 5-3	95-0441

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SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

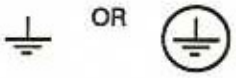
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

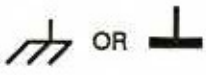
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-2232
32-CHANNEL RELAY OUTPUT BOARD WITH BUILT-IN-TEST

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SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-2232 is a VMEbus compatible 32-bit relay board. Its features include:

a. 32 Form C single-pole double-throw (SPDT) relays
b. Contact ratings:

   (1) 60 W, 125 VA maximum switching power
   (2) 220 VDC, 250 VAC maximum switching voltage
   (3) 2 Amp maximum switching current
   (4) 3 Amp maximum carry current

c. Optional contact protection electronics
d. 8-, 16-, or 32-bit data transfers
e. Built-in-Test
f. Front Panel Fail LED
g. Software compatible with VMIVME-2532A and VMIVME-2533

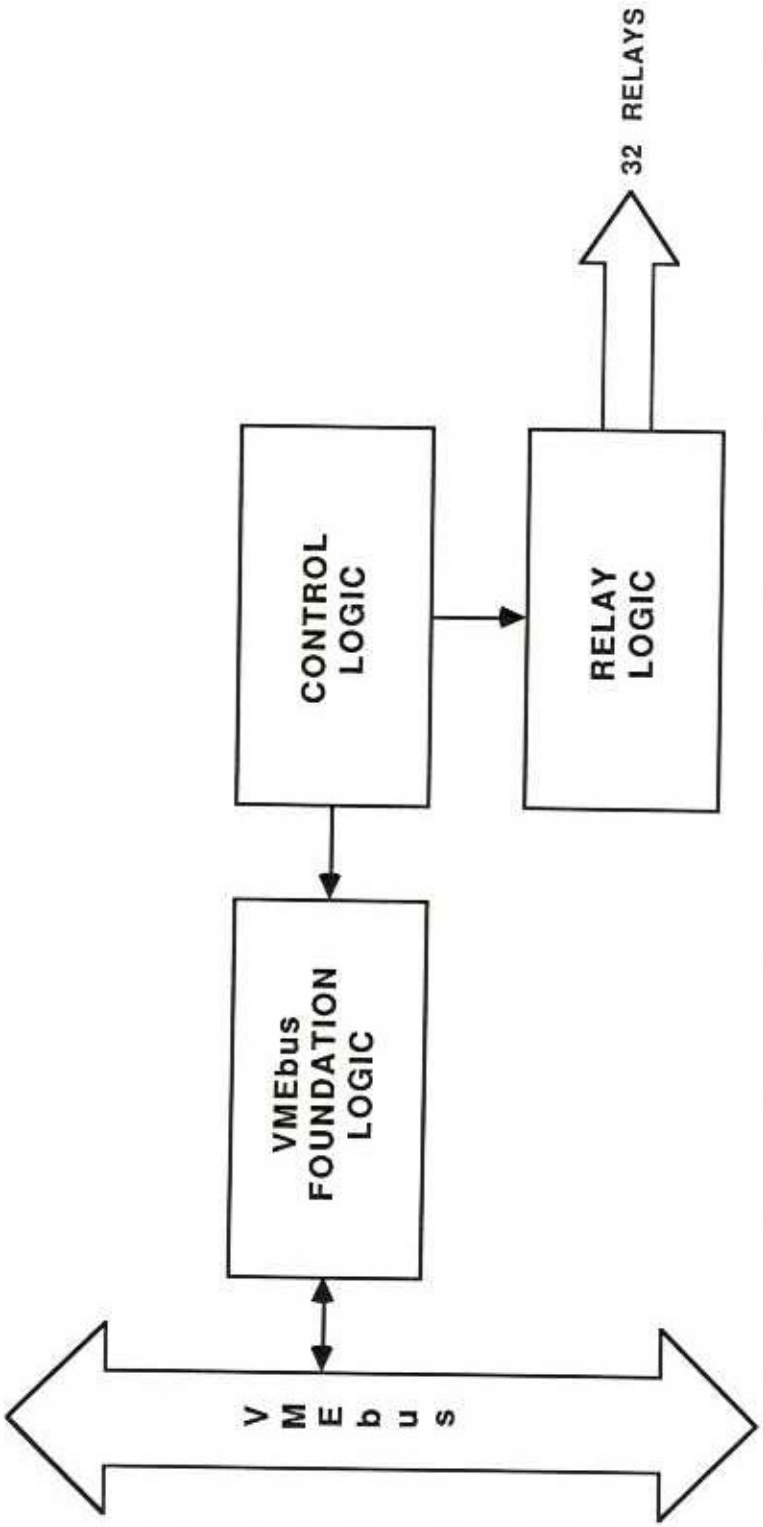
1.2 FUNCTIONAL DESCRIPTION

The VMIVME-2232 Relay Board consists of four 8-bit data registers used to control 32 relays. The board will support byte, word, and longword data transfers. Figure 1.2-1 illustrates a simplified block diagram of the board.

The VMIVME-2232 is designed with Built-in-Test electronics that enable the user to test all of the electronic circuitry on the board. Data written to the data registers and Control and Status Register (CSR) can be read back to verify proper operation. A simplified block diagram of the Built-in-Test features of the 2232 board is shown in Figure 1.2-2.

1.3 FUNCTIONAL BLOCK DIAGRAM

The VMIVME-2232 consists of VMEbus foundation logic, four 8-bit data registers, eight 4-bit relay drivers, a CSR, and 32 form C relays. Figure 1.3-1 is a block diagram showing these sections.



M2232/F1.2-1

Figure 1.2-1. Basic Relay Board Functions

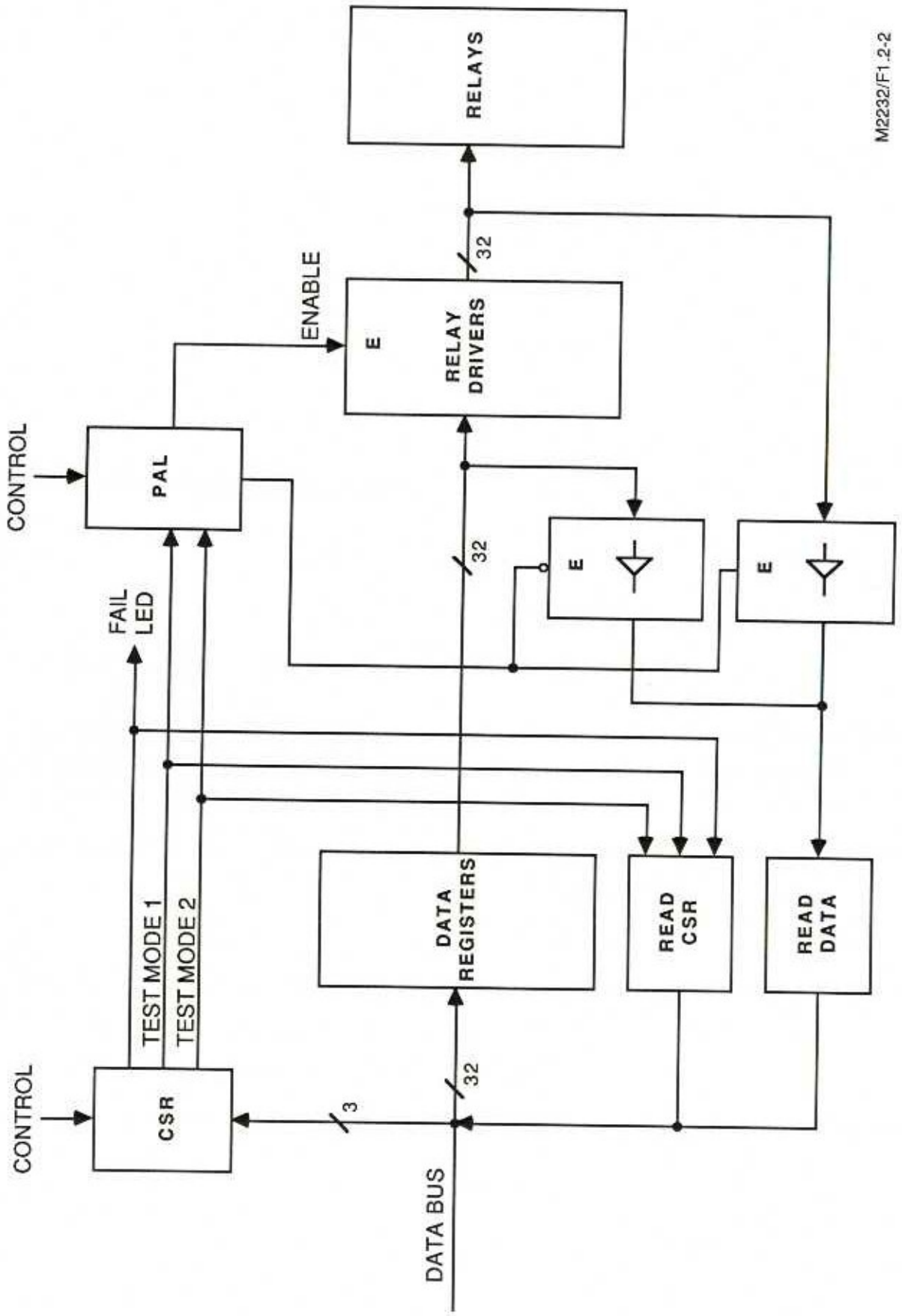


Figure 1.2-2. Simplified Built-in-Test Functional Block Diagram

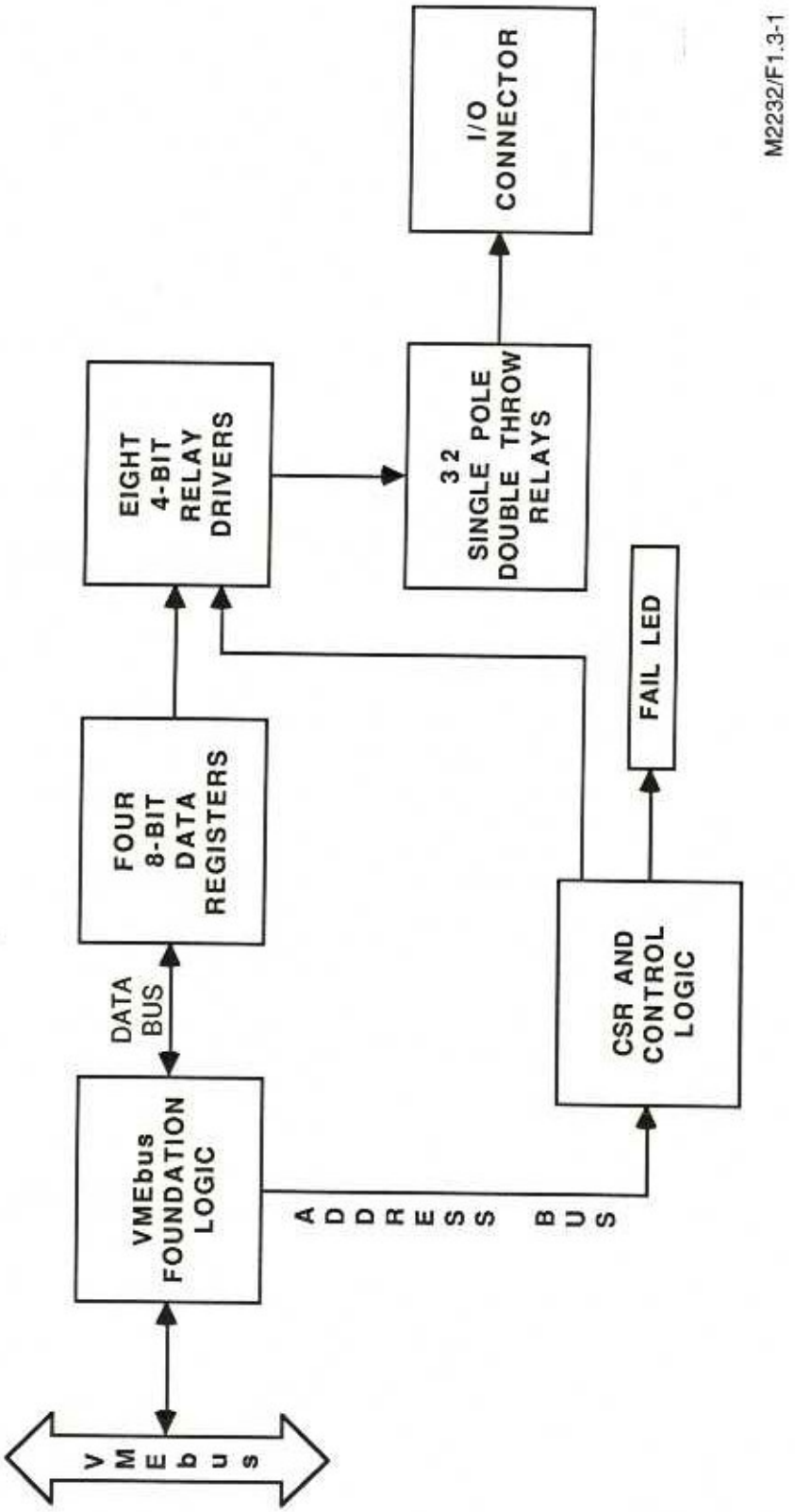


Figure 1.3-1. VMIVME-2232 Functional Block Diagram

The VMEbus foundation logic controls data transfers allowing 8-, 16-, or 32-bit data transfers. The four 8-bit data registers latch 32 bits of data. This data, along with the CSR, is used to control the relay drivers which operate the relays. The CSR contains three control bits. One bit controls the on-board Fail LED, while the other two bits are used for enabling the relay drivers and controlling the Built-in-Test circuitry.

1.4 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following application and configuration guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006

In addition, the "Engineer's Relay Handbook" is available from:

NARM Headquarters
P.O. Box 1505
Elkhart, IN 46515

NARM is the National Association of Relay Manufacturers and the handbook describes relay selection and operation.

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-002232-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual presents detailed information concerning the hardware operation of the board. The VMIVME-2232 consists primarily of five sections:

a. VMEbus Foundation Logic
b. Device Addressing
c. Control and Status Register (CSR)
d. Data Registers and Relay Drivers
e. 32 Form C Relays (SPDT)

Appendix A contains the logic diagram of the VMIVME-2232 board and should be referred to while studying this section of the manual.

3.2 VMEbus FOUNDATION LOGIC

Typical VMEbus drivers, receivers, and control logic are shown in Figure 3.2-1. The DTACK generator shown in Figure 3.2-2 is designed to select the maximum data transfer speed.

3.3 DEVICE ADDRESSING

The VMIVME-2232 is designed to support data transfers in supervisory and/or non-privileged I/O memory space. A jumper (AM02) is provided, as shown in Figure 3.3-1, (Address Decode Block Diagram) to allow these selections. AM02 is factory-configured (no jumper installed) to respond to short supervisory I/O access. Refer to section 5.4 for a detailed explanation of the address modifier jumper.

The VMIVME-2232 is designed with two sets of board select jumpers and decode logic, as shown in Figure 3.3-1, to provide an efficient memory address map for the CSR and data register addresses. This hardware permits configuring the data registers and CSRs into contiguous, but separate, memory locations. This can improve software's efficiency when working with more than one board in a system. The board is also designed to handle 8-, 16-, or 32-bit data transfers. Figure 3.3-2 shows the block diagram of this circuitry.

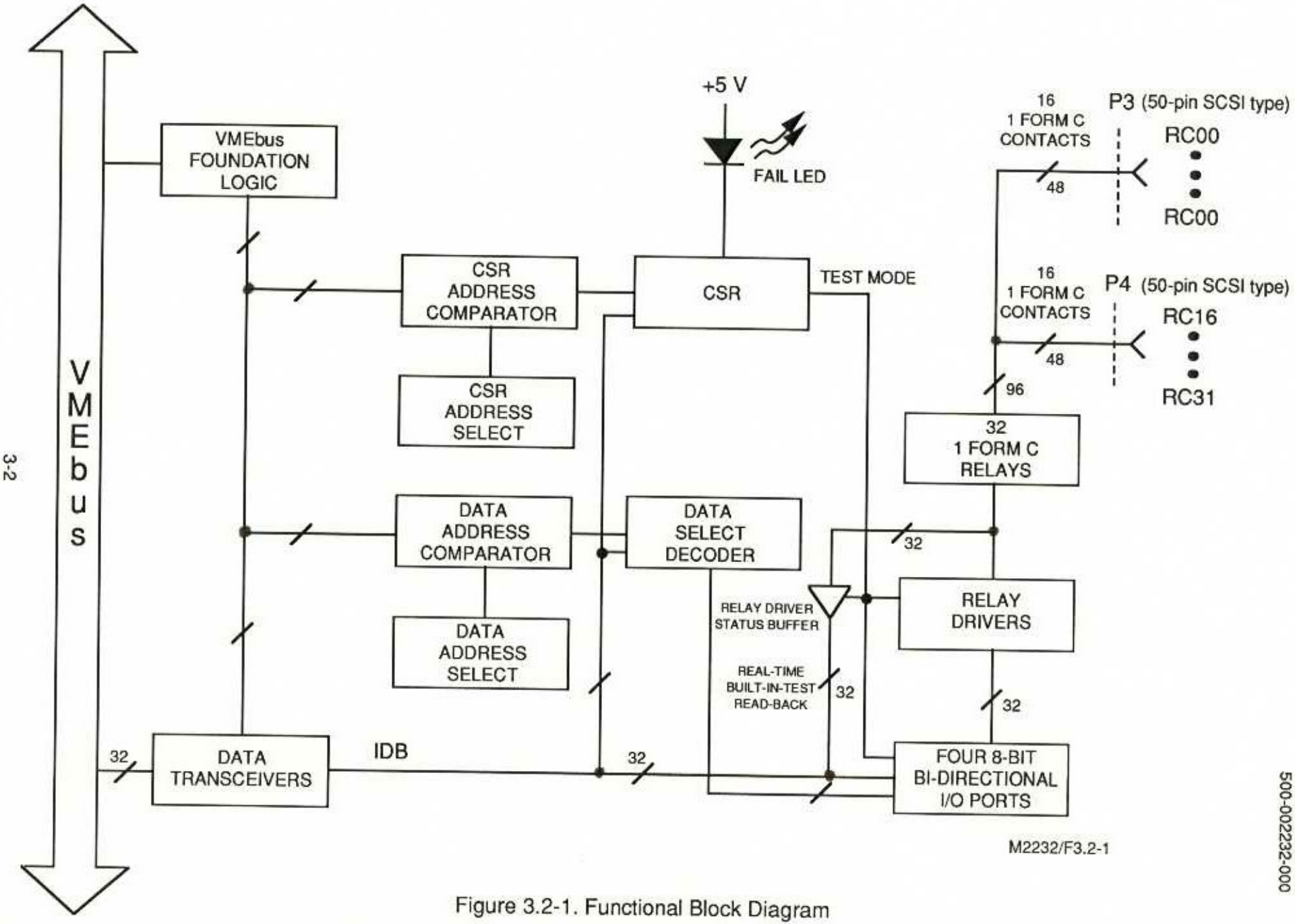


Figure 3.2-1. Functional Block Diagram

500-002232-000

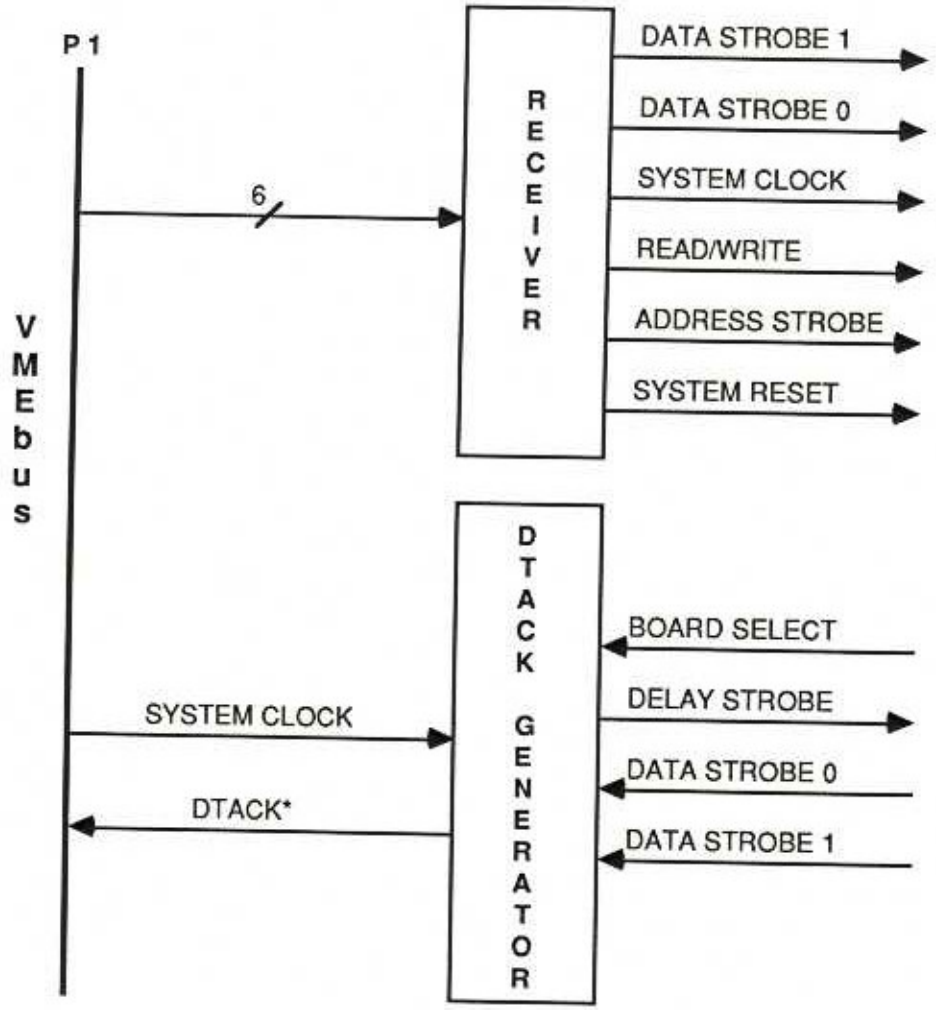


Figure 3.2-2. VMEbus Foundation Logic

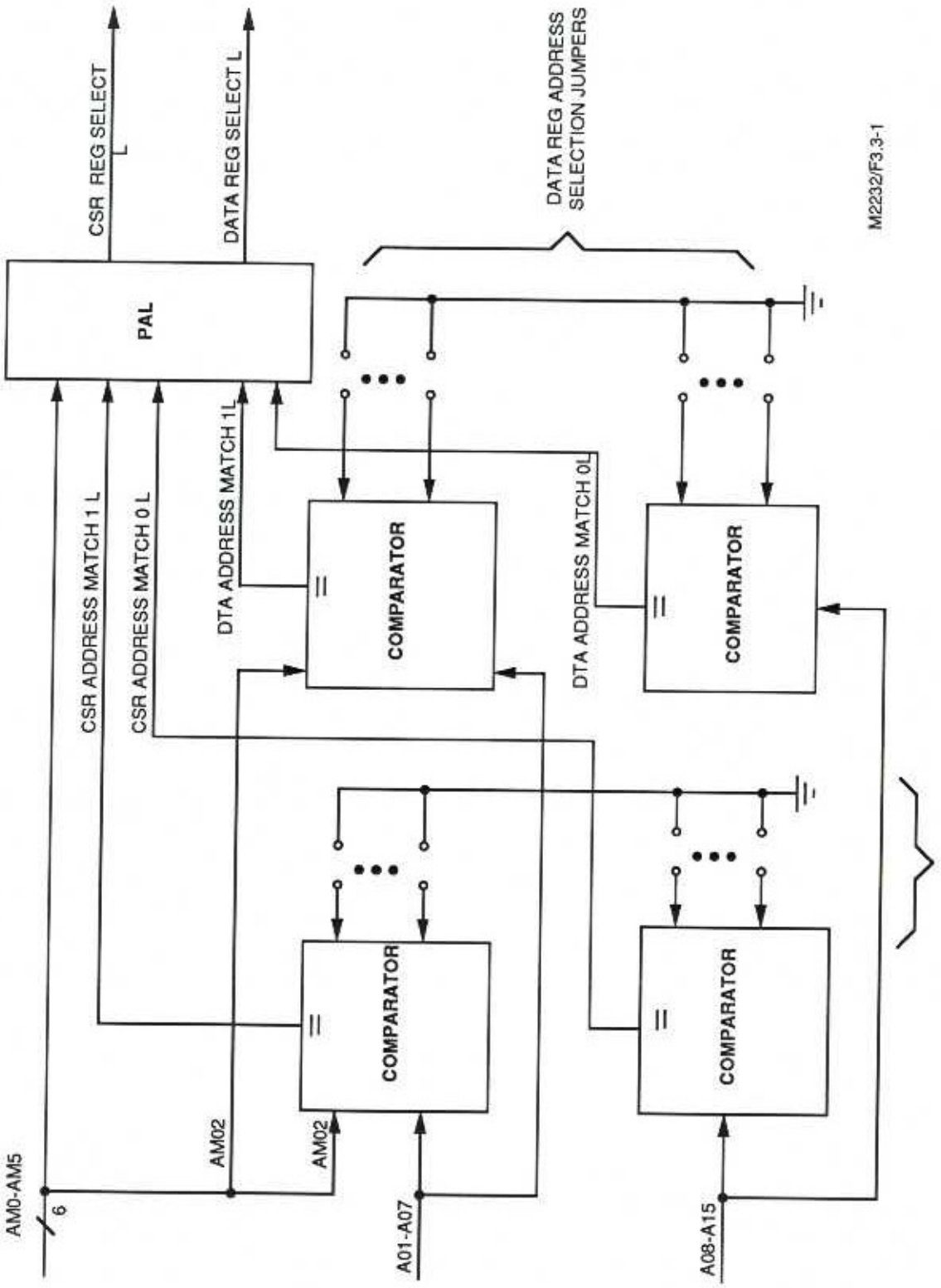


Figure 3.3-1. Address Decode Block Diagram

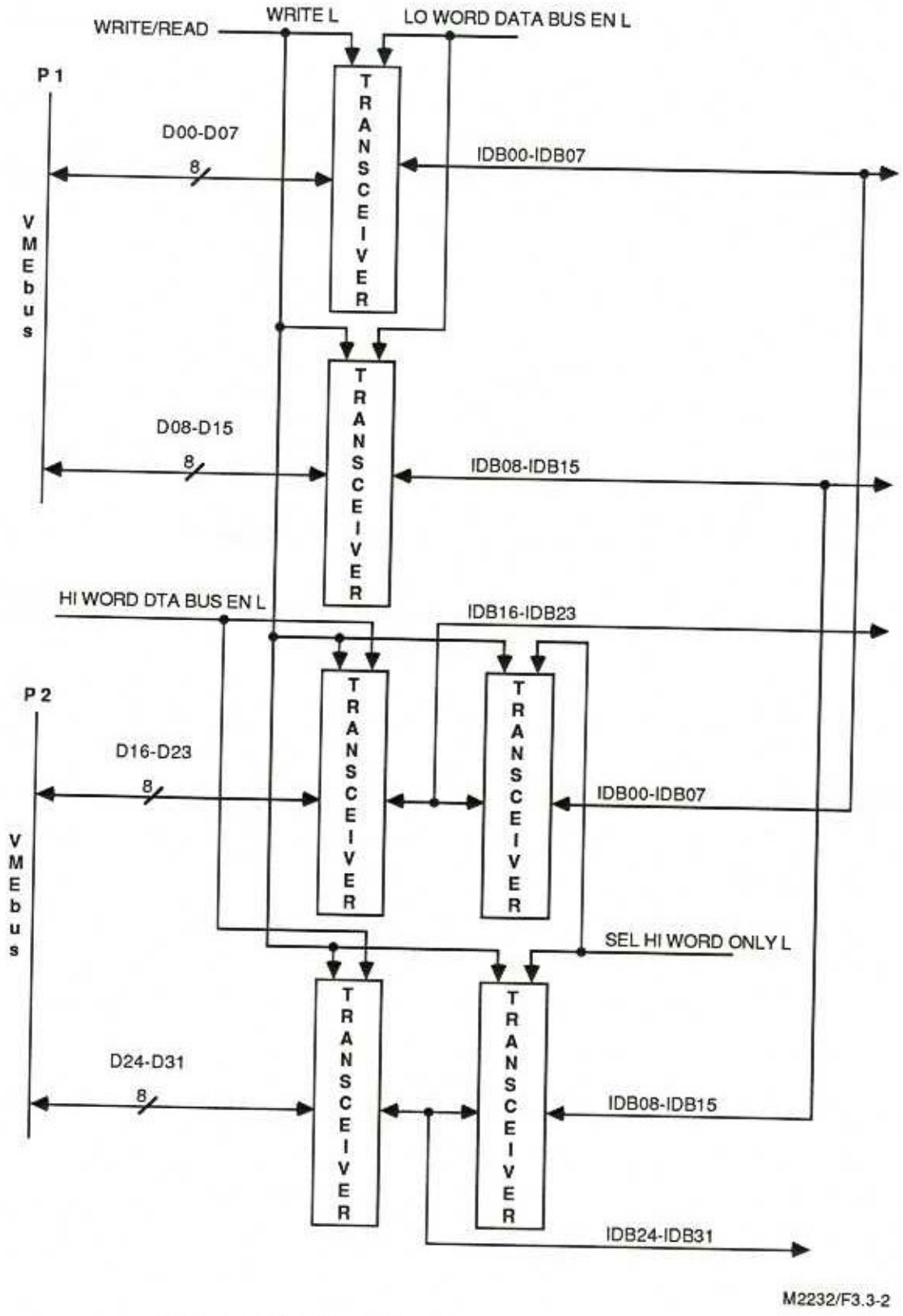


Figure 3.3-2. Data Transfer Block Diagram

3.4 CONTROL AND STATUS REGISTER (CSR)

The CSR controls the Test Mode (TM) Bits and the front panel Fail LED as shown in Figure 3.4-1. The TM bits are used for relay enabling and diagnostic testing. TM1 is used to enable/disable the relay drivers which operate the relays. TM2 is used to control data register read-back functions. When reading a data register, TM2 is used to select either the data registers or the relay drivers as the data source for read-back. The I/O mode bit is reserved for possible future enhancements to this product and is not used at this time. The user should write a zero to this I/O mode bit.

The CSR is initialized ***active*** upon system reset such that the drivers are disabled and the front panel Fail LED is illuminated. Only the upper nibble (bits 4 to 7) is used for controlling the board; this upper nibble is *read/writeable*. The lower nibble (bits 0 to 3) can be set up by the user via jumper JH, it is a *read only* nibble. These bits can define some function (such as board ID extension) for the user to test in software. The CSR also contains a board ID code register in the upper byte. This register can be used by system software to do automatic system configuration. The board ID code read from this register is fixed at 04 HEX; it is a *read only* register.

3.5 BUILT-IN-TEST DESCRIPTION

The 2232 test logic provides for three different modes of testing: off-line, on-line, and dedicated on-line. These modes are software compatible with the VMIVME-2532 and VMIVME-2533. Jumper JA is provided to accommodate future enhancements, and should not be removed from the ground position in which it was shipped.

Upon system reset, the CSR is cleared to all zeros, initializing the board in the off-line test mode (TM1 = 0, TM2 = 0). This mode of test disables the relay drivers and enables direct reading (loopback testing) of the data registers.

The on-line test mode is used to read the relay driver outputs while the relay drivers are enabled (TM1 = 1, TM2 = 1). A read of the data registers will actually read the relay driver lines (which control the relays). This feature can be used to verify relay driver operation when the relay drivers are enabled. This relay driver data is inverted from what was written to maintain software compatibility with the VMIVME-2532A.

3.6 OUTPUT RELAYS

A typical output relay (Aromat DS1E-M-DC5V or Omron G6E-134P-ST-US-DC5) is shown in Figure 3.6-1. Optional contact protection electronics is also shown. Each of the 32 relays is driven from the output logic as shown in Figure 3.6-2. The relay contacts are routed to two front panel SCSI-type connectors whose pin arrangements and assignments are specified in Section 5.

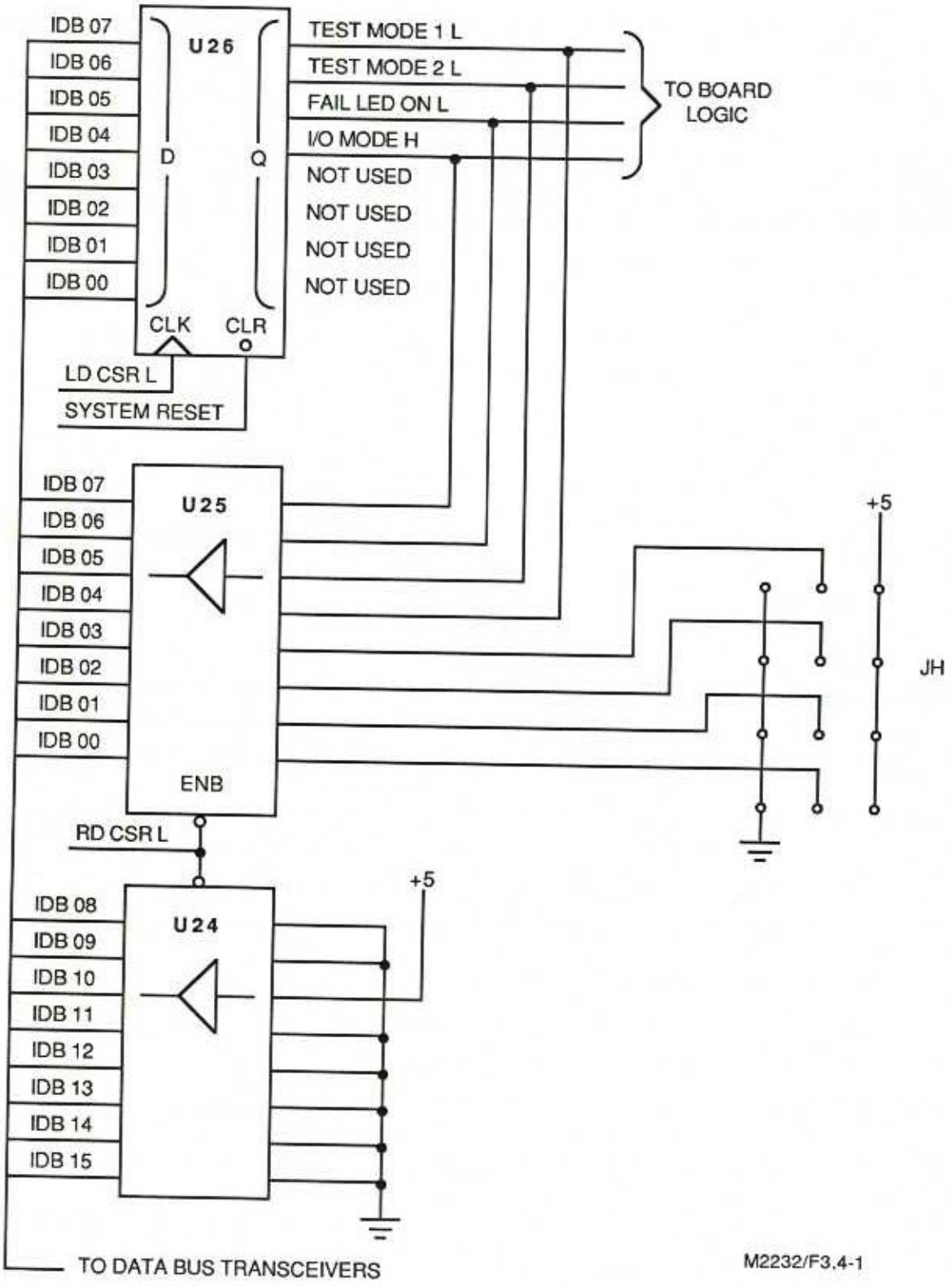


Figure 3.4-1. CSR Block Diagram

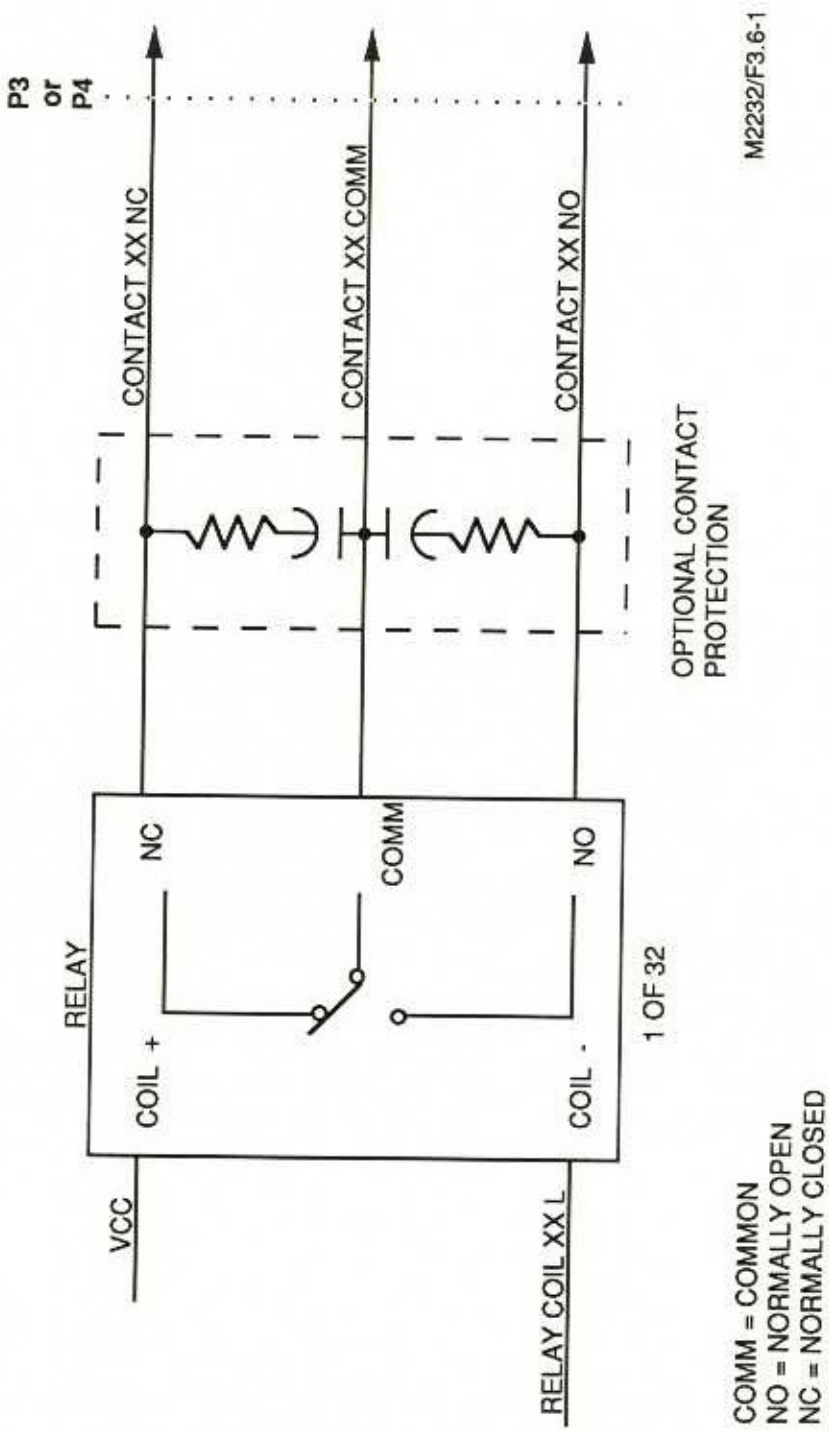


Figure 3.6-1. Typical Relay

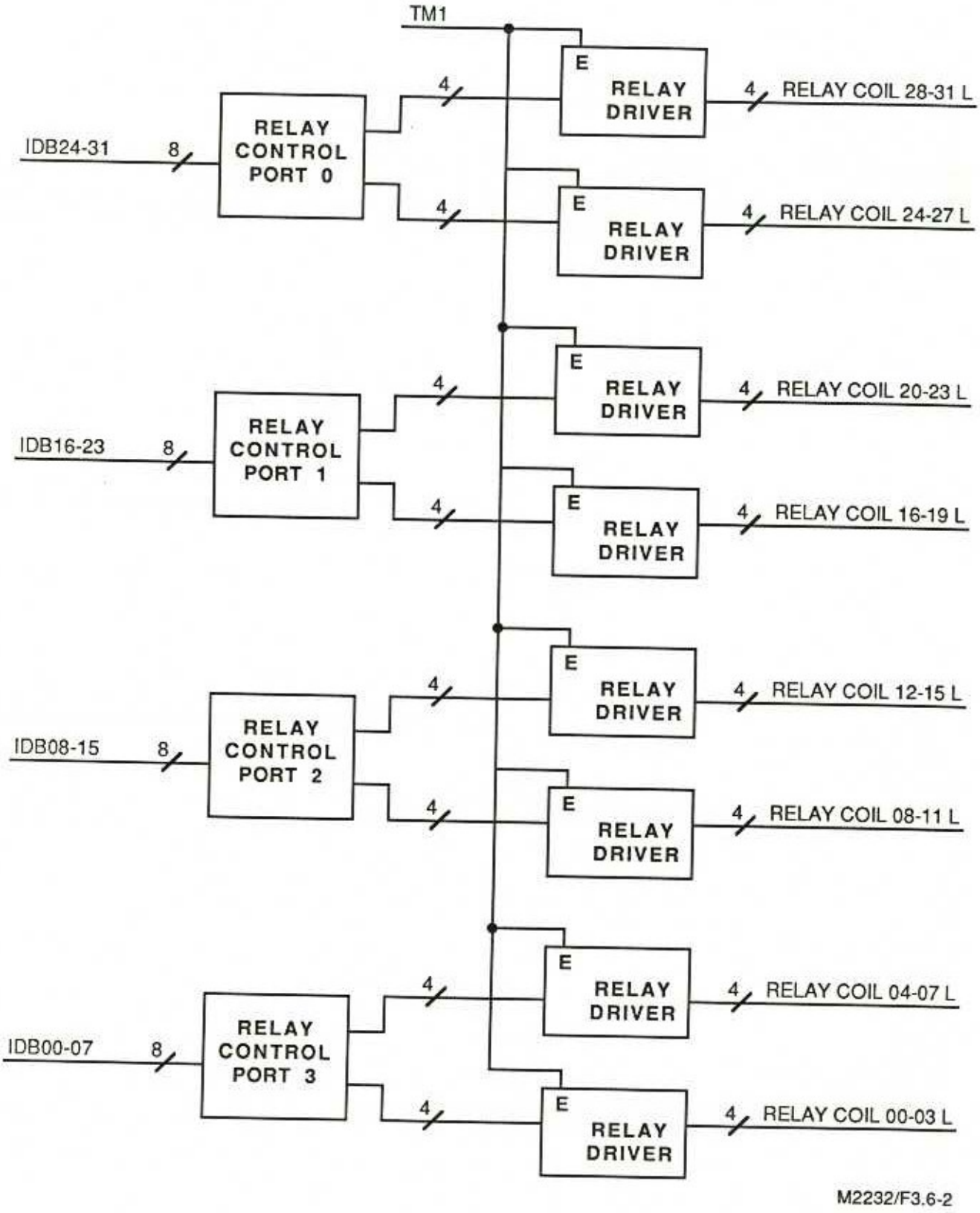


Figure 3.6-2. Relay Control Registers and Relay Driver Functional Block Diagram

3.7 CONTACT PROTECTION

The use of proper contact protection may be necessary to achieve the specified contact life expectancy of the relays used on this board, particularly when the relays are used to switch inductive loads. Circuits that may normally be considered resistive can contain capacitance and inductance in the associated wiring that can cause excessive arcing of relay contacts and reduce contact life.

Inductive loads generate large transient voltages when the energizing circuit is opened. These transients can be 40 or 50 times the value of the applied supply voltage and can cause serious damage to relay contacts.

Figure 3.6-1 shows the contact protection network that is suitable for most applications where these types of relays are used and space is provided on the Relay Output Board to accommodate these components. Formulas to calculate these R and C values are shown below.

$$C = \frac{I^2}{10} \geq 0.001 \text{ MFD}$$

$$R = \frac{E}{10(1)^X} \geq 0.5 \text{ ohms}$$

where: C=microfarads

R=ohms

E=DC volts or 1.4 x rms voltage (immediately prior to contact closure)

$$X = 1 + \frac{50}{E}$$

I=amperes (immediately prior to contact opening)

Also, C may be increased up to ten times the calculated value to aid in reduction of transients when switching inductive loads.

SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The VMIVME-2232 controls relays using the data registers and the Control and Status Register (CSR). Data written to the CSR may be read back at any time. Data written to the data registers can be read when TM2=0. When TM2=1, a read of the data registers actually reads the level of the relay driver outputs (which operate the relays). The relay driver data is inverted from that written to the data registers so as to maintain software compatibility with the VMIVME-2532A. Each bit in the data registers controls one relay.

The base address required for accessing the data registers of the VMIVME-2232 is selected by the address jumpers JC and JF referred to in Section 5. The on-board registers are selected by address bits A01, A02, DS0, and DS1. The base address for the CSR is selected by address jumpers JD and JE. The board is shipped with these jumpers set up with the CSR "stacked on top of the data registers." Please refer to section 5.6 for more detailed information on base address selections.

4.2 CONTROL AND STATUS REGISTER (CSR)

The CSR register controls the two TEST MODE (TM) bits and the front panel Fail LED as shown in Figure 3.4-1. The I/O mode bit is a reserved bit. TM1 enables the relay drivers which operate the relays. TM2 selects between the data register or relay driver outputs as the data source when reading at the data register address. The format of the CSR data and the Output Data Registers (ODRs) is shown in Table 4.2-1. The CSR is initialized to all zeros upon system reset. Thus, the front panel Fail LED is illuminated and the relay drivers are disabled at power-up.

4.3 RELAY CONTROL

The relays are operated by the relay drivers as shown in Figure 3.6-2. When using negative true relay drivers, a relay is ACTIVATED (the normally open contacts are closed) if the data bit corresponding to the relay is set to a logic "zero" in its data register. Likewise, when using positive true relay drivers, a relay is ACTIVATED if the data bit corresponding to the relay is set to a logic "one" in its data register. This assumes the test mode bit TM1 in the CSR is set to a logic "one". This is the case for normal operation and on-line testing of the board. Whenever TM1 is at logic "zero" the relays are deactivated and the normally open contacts are open.

Table 4.2-1. Address Register Bit Definitions

BINARY ADDRESS																	
A15-A4				A3	A2	A1	A0										
X	X	X	X	0	0	0	0	DATA PORT 0 (UPPER BYTE)									
								IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8		
								I/O 31	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	I/O 25	I/O 24		
X	X	X	X	0	0	0	1	DATA PORT 1 (MIDDLE UPPER BYTE)									
								IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0		
								I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16		
X	X	X	X	0	1	0	0	DATA PORT 2 (MIDDLE LOWER BYTE)									
								IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8		
								I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8		
X	X	X	X	0	1	1	1	DATA PORT 3 (LOWER BYTE)									
								IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0		
								I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0		
X	X	X	X	1	0	0	0	BOARD ID									
								BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8		
								0	0	0	0	0	1	0	0		
X	X	X	X	1	0	0	1	CONTROL STATUS REGISTER									
								IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0		
								TM1*	TM2*	FAIL*	I/O MODE	BOARD ID EXTENSION READ ONLY					
X	X	X	X	1	1	0	0	NOT USED									
X	X	X	X	1	1	1	1	NOT USED									
ADDRESS SELECTION JUMPERS																	

M2232/T4.2-1

CSR BIT DEFINITIONS

TM1* Set to a "zero" to disable relay drivers. Set to a "one" to enable relay drivers.
TM2* Set to a "zero" to read back data register. Set to a "one" to read back relay drivers.
FAIL* Fail LED bit. Fail LED is ON if this bit is "zero", OFF if it is "one".
*0 = Active State

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

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**********
*  CAUTION  *
**********
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SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

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**********
*  CAUTION  *
**********
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DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER CONFIGURATION

The locations and factory configurations for the jumpers used on the VMIVME-2232 are shown in Figure 5.3-1. The following sections and figures give a detailed explanation of the use and setup for these jumpers. Jumper JA is factory configured to ground. This jumper is for future enhancements of this board, it should not be moved from its preset position.

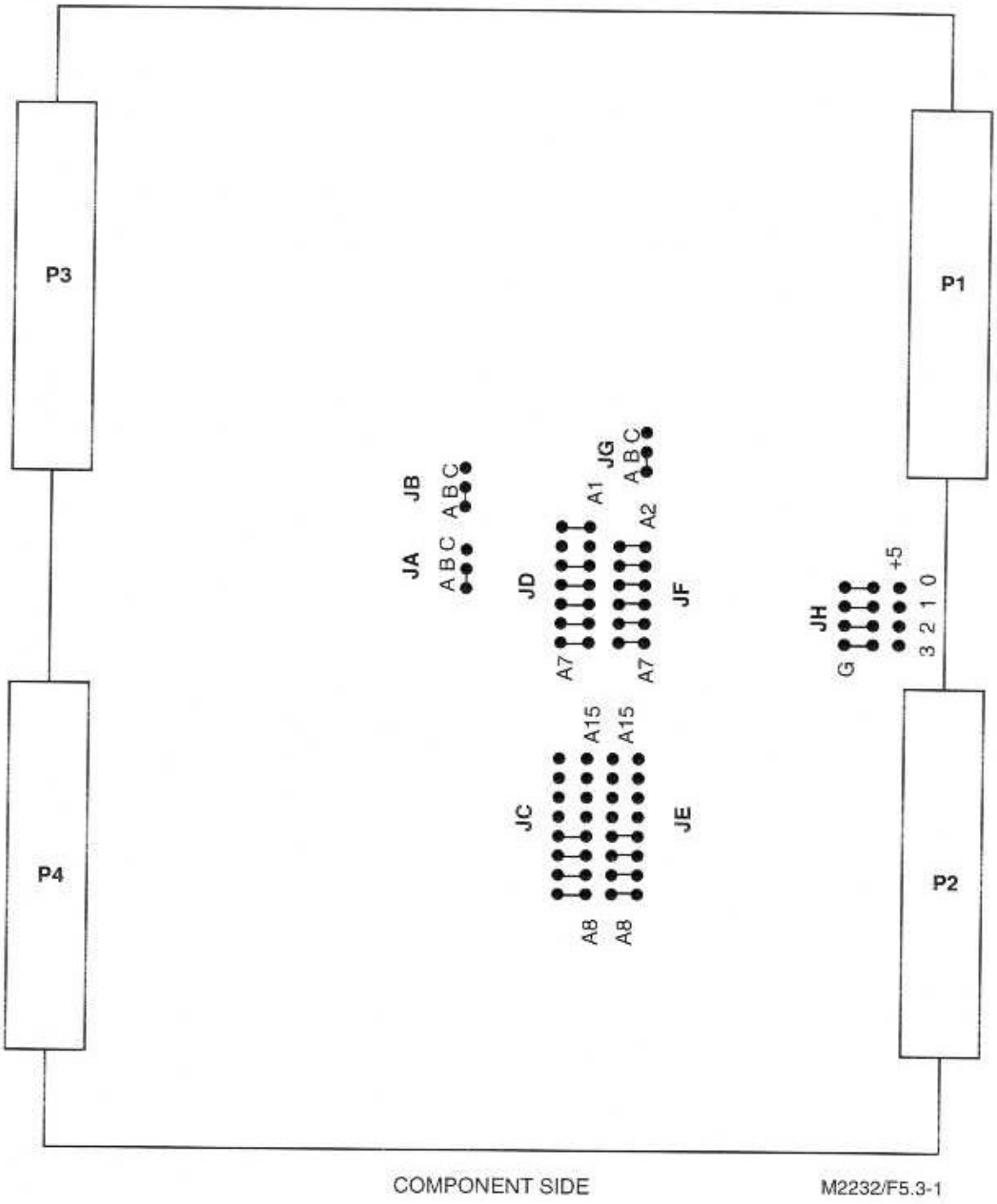
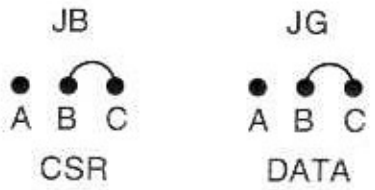


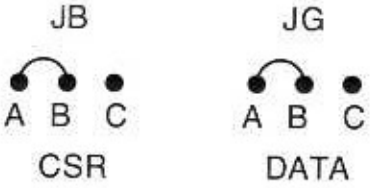
Figure 5.3-1. Jumper Locations

5.4 ADDRESS MODIFIERS

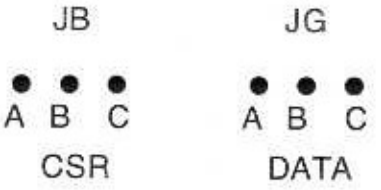
The VMIVME-2232 Board is configured at the factory to respond to either short supervisory I/O access or short nonprivileged I/O access, (jumpers JB and JG installed A to B). This can be changed by installing the AM2 jumpers to fit the need. There are two AM2 jumpers. One is for the data register's base address (jumper JG). The other is for the Control and Status Register (CSR) (jumper JB). There are also three possible selections for each of the AM2 jumpers. Figure 5.4-1 (a) below shows the AM2 jumper for nonprivileged short I/O accesses only, while Figure 5.4-1 (b) shows the AM2 jumper setup for either I/O access type. In this mode, the data registers and/or the CSR will acknowledge either I/O access (short supervisory or nonprivileged). Figure 5.4-1 (c) shows the AM2 jumper setup for short supervisory I/O access only.



(a) AM2 jumpered for short nonprivileged I/O access.



(b) AM2 jumpered for either I/O access.



(c) AM2 jumpered for short supervisory access (no jumpers installed).

M2232/F5.4-1

Figure 5.4-1. Address Modifier Positions

5.5 DATA REGISTERS BASE ADDRESS

The VMIVME-2232 board occupies 4 bytes of the VMEbus short I/O address space. The base address of these bytes is configured by jumpers JC and JF. The factory sets up these headers to a base address of F000 HEX, as shown in Figure 5.5-1.

5.6 CONTROL AND STATUS REGISTER (CSR) BASE ADDRESS

The CSR of the VMIVME-2232 includes a byte for the board ID number. As such, the CSR occupies two bytes of the VMEbus short I/O address space. The CSR has its own set of address jumpers so that data and CSRs in a system can be stacked into separate but contiguous memory locations. The CSR jumpers JD and JE are configured at the factory to a base address of F004 HEX, as shown in Figure 5.6-1.

The selection of jumper JH can be read via four bits in the CSR. The four bits can be used as an extension of the Board ID and/or for automatic configuration (under software control) of some diagnostic function or automatic system configuration. These jumpers are factory configured to logic "zero" and are grounded.

5.7 I/O CABLE AND CARD-EDGE CONNECTOR CONFIGURATION

The I/O connectors (P3 and P4) are SCSI type connectors selected by VMIC because of their high quality. When purchasing cables be sure to specify the required current-carrying capability of the cable. Flat-ribbon cable connectors can typically carry a maximum of one amp.

Details concerning input connections are shown in Figure 5.7-1. Connector pin assignments for the 32 output channels of the VMIVME-2232 are shown in Tables 5.7-1 and 5.7-2. The output connector pin configuration for P3 and P4 is shown in Figure 5.7-2, and the P1/P2 Connector Pin Layout is shown in Figure 5.7-3. A compatible flat-ribbon cable connector for the VMIVME-2232 is Amphenol No. 850-57F-30500-20, and the strain relief is Amphenol No. 850-57F-50-041.

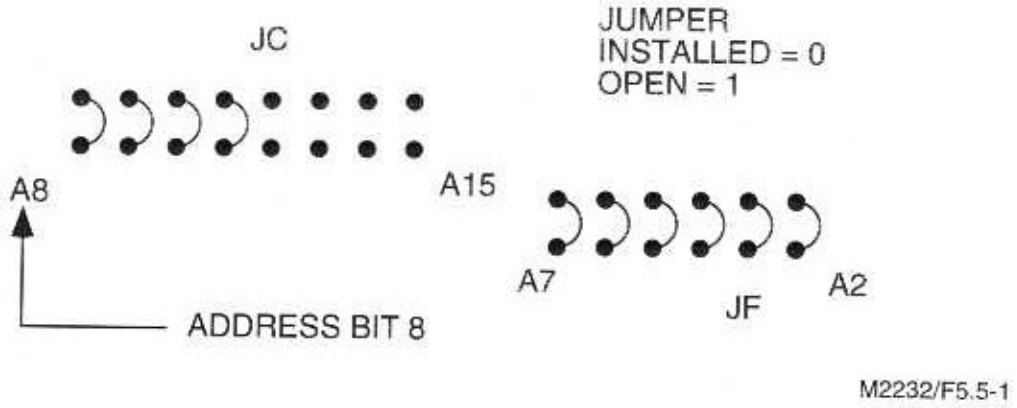


Figure 5.5-1. Data Registers Base Address Configuration

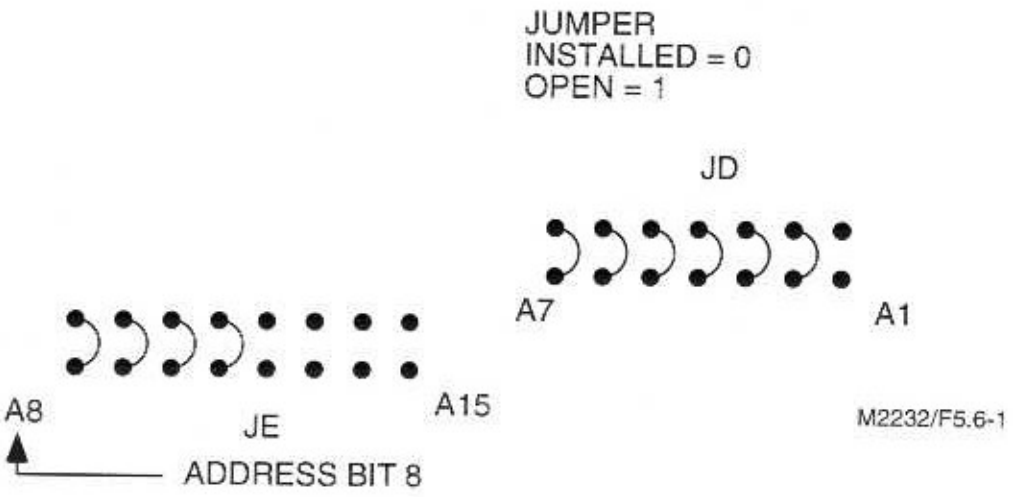


Figure 5.6-1. CSR Base Address Configuration

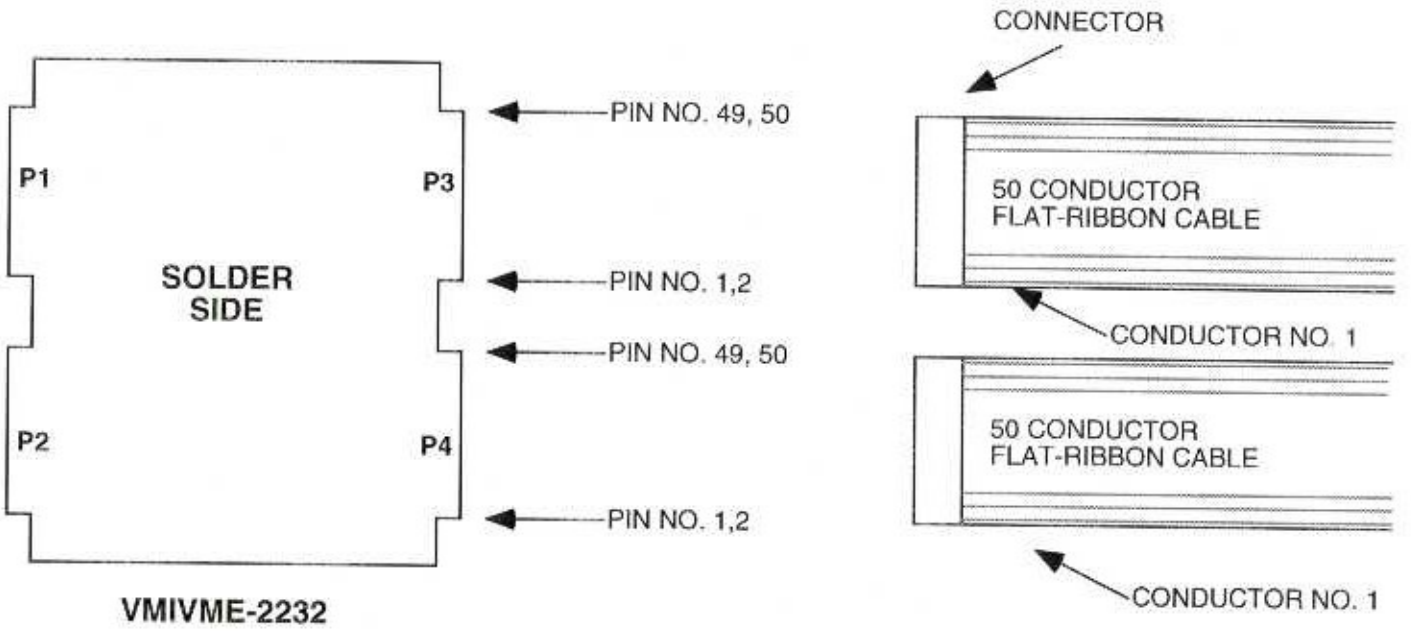


Figure 5.7-1. Cable Connector Configuration

Table 5.7-1. P3 Channel Connector Assignment

RELAY (CONTACT) NUMBER	PIN NUMBER		
	NC	COM	NO
00	01	02	03
01	04	05	06
02	07	08	09
03	10	11	12
04	13	14	15
05	16	17	18
06	19	20	21
07	22	23	24
08	26	27	28
09	29	30	31
10	32	33	34
11	35	36	37
12	38	39	40
13	41	42	43
14	44	45	46
15	47	48	49

M2232/T5.7-1

NC = Normally Closed
COM = Common
NO = Normally Open

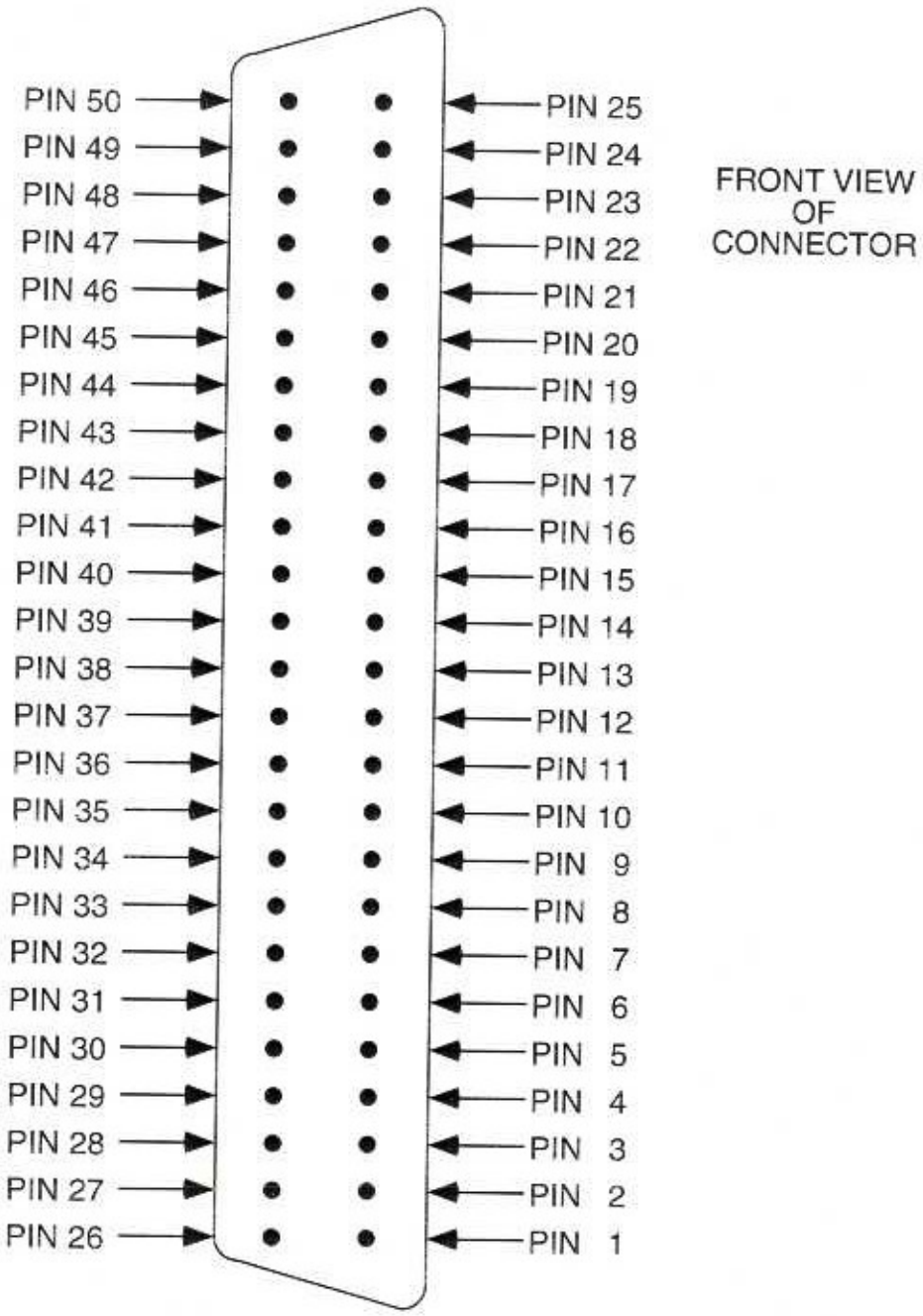


Figure 5.7-2. P3/P4 Connector Pin Layout

Table 5.7-2. P4 Channel Connector Assignment

RELAY (CONTACT) NUMBER	PIN NUMBER		
	NC	COM	NO
16	01	02	03
17	04	05	06
18	07	08	09
19	10	11	12
20	13	14	15
21	16	17	18
22	19	20	21
23	22	23	24
24	26	27	28
25	29	30	31
26	32	33	34
27	35	36	37
28	38	39	40
29	41	42	43
30	44	45	46
31	47	48	49

M2232/T5.7-2

NC = Normally Closed
COM = Common
NO = Normally Open

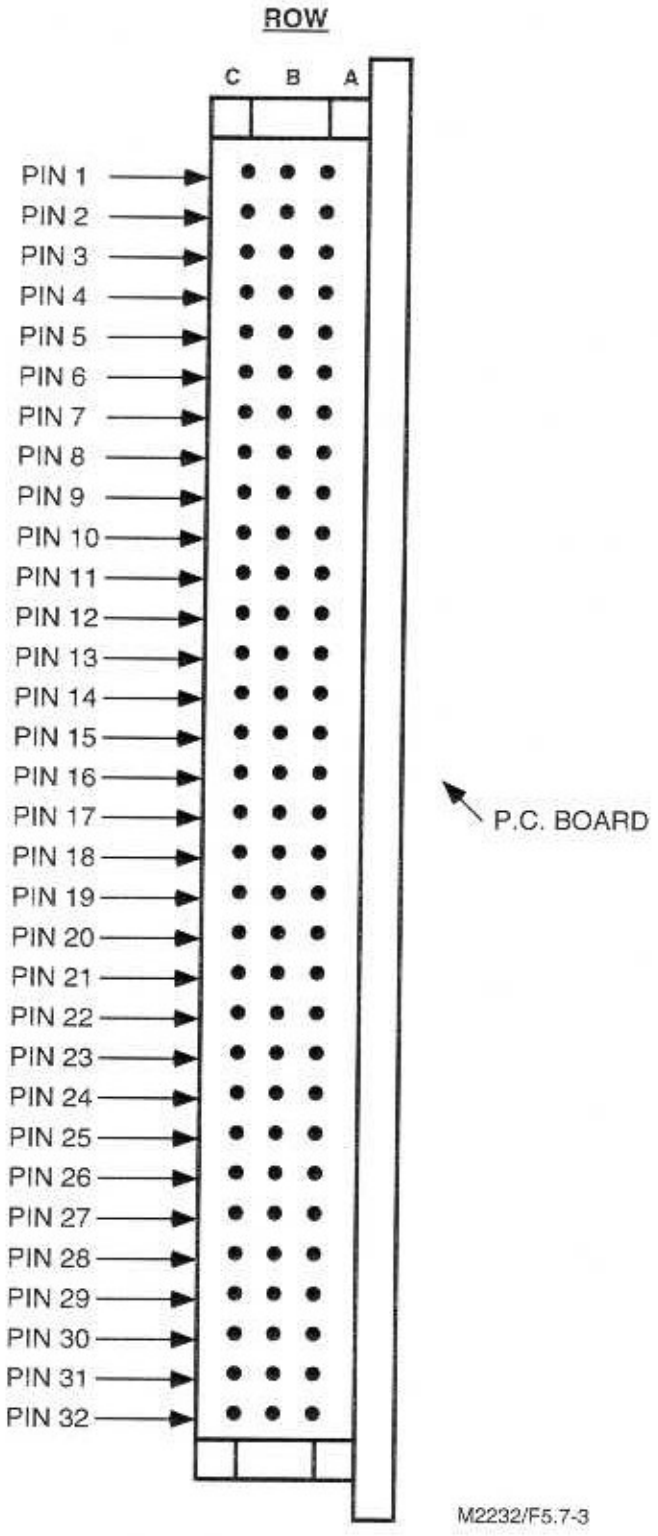


Figure 5.7-3. P1/P2 Connector Pin Layout

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

ACKNOWLEDGEMENTS

DOCUMENTATION EVALUATION FORM

VMIC welcomes your comments and suggestions.

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