VMIVME-2528

128-BIT TTL DIGITAL I/O TURBOMODULE™

INSTRUCTION MANUAL

DOCUMENT NO. 500-002528-000 N

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	03/06/86	Entire Manual	Manual - 01
B	11/21/88	Appendix A	88-0311
C	11/21/88	Update Manual	88-0327
D	03/08/89	Cover, Pages ii, iii, iv, vi, vii, Section 6, and Appendix A	89-0005
E	10/11/89	Cover, Page ii, and Appendix A	89-0114
F	03/07/90	Cover, Page ii, and Appendix A	89-0161
G	03/07/90	Cover, Page ii, and Appendix A	90-0030
H	06/19/90	Cover, Page ii, and 2-2	90-0105
J	08/21/91	Cover, Page ii, and Appendix A	91-0204
K	09/04/91	Page ii and Section 6	91-0237
L	04/21/92	Cover, Page ii, Section 2, Section 6, and Appendix A	92-0101
M	02/16/94	Cover, Pages ii, 5-2, and 5-4	94-0224
N	09/30/94	Cover, Pages ii and 6-1	94-0756

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SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

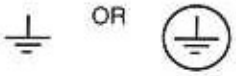
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

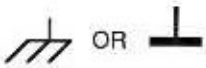
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-2528
128-BIT TTL DIGITAL I/O TURBOMODULE™

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-2528 is a VMEbus compatible 128-bit TTL input/output board. Its features include:

a. 128 bits of TTL input/output
b. Sixteen 8-bit I/O port jumpers to select input or output operations on 8-bit boundaries
c. 24 mA sink capability
d. 8- or 16-bit data transfers

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-2528 is a high density TTL I/O board designed to support up to 128 bits of TTL input or output as selected by user-installed port direction control jumpers. Each jumper sets an 8-bit port as an input or an output port. Each output has up to 24 mA of current sink capability. The VMIVME-2528 is designed with a high quality ground plane that is carried through to alternate I/O pins on each connector to enhance noise immunity. The control logic is designed such that all I/O ports are initialized inactive at system reset. All ports are activated by performing a write to I/O register 7.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. " The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-002528-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

A functional block diagram of the VMIVME-2528 is shown in Figure 3.1-1. The VMIVME-2528 design is partitioned into six subsections which consist of:

a. VMEbus foundation logic
b. Data Transceivers
c. Address Compare Logic
d. Read / Write Register Control Logic
e. Registers 0 through 3
f. Registers 4 through 7

Subsystem block diagrams are provided in Figures 3.1-2 through 3.1-7.

3.2 BOARD ADDRESSING

The VMIVME-2528 is designed to support data transfers in supervisory or non-privileged short I/O memory space. A jumper is provided as shown in Figure 3.1-2 to allow user selection of either I/O access type. The jumper (J9) is shown on logic diagram 141-002528-000, in Appendix A to this manual. The VMIVME-2528 is factory configured (Jumper J9 is not installed) to respond to short supervisory I/O access. The VMIVME-2528 is designed with two board-select DIP switches as shown in Figure 3.1-2, which are used to set the board's base address.

3.3 VMEbus FOUNDATION LOGIC

Typical VMEbus drivers, receivers, and control logic are shown in Figures 3.1-3, 3.1-4, and 3.1-5.

3.4 REGISTER READ/WRITE CONTROL LOGIC

Address bits A01, A02, A03 and the read/write control lines are decoded as shown in Figure 3.1-5 to provide eight write control lines and eight read control lines. These control lines are routed to the enable pins on each AMD2952 bidirectional latch (R0-R7 in Figures 3.1-6 and 3.1-7). These latches are jumper selectable for read or write operations. These jumpers are J10 through J25. If a

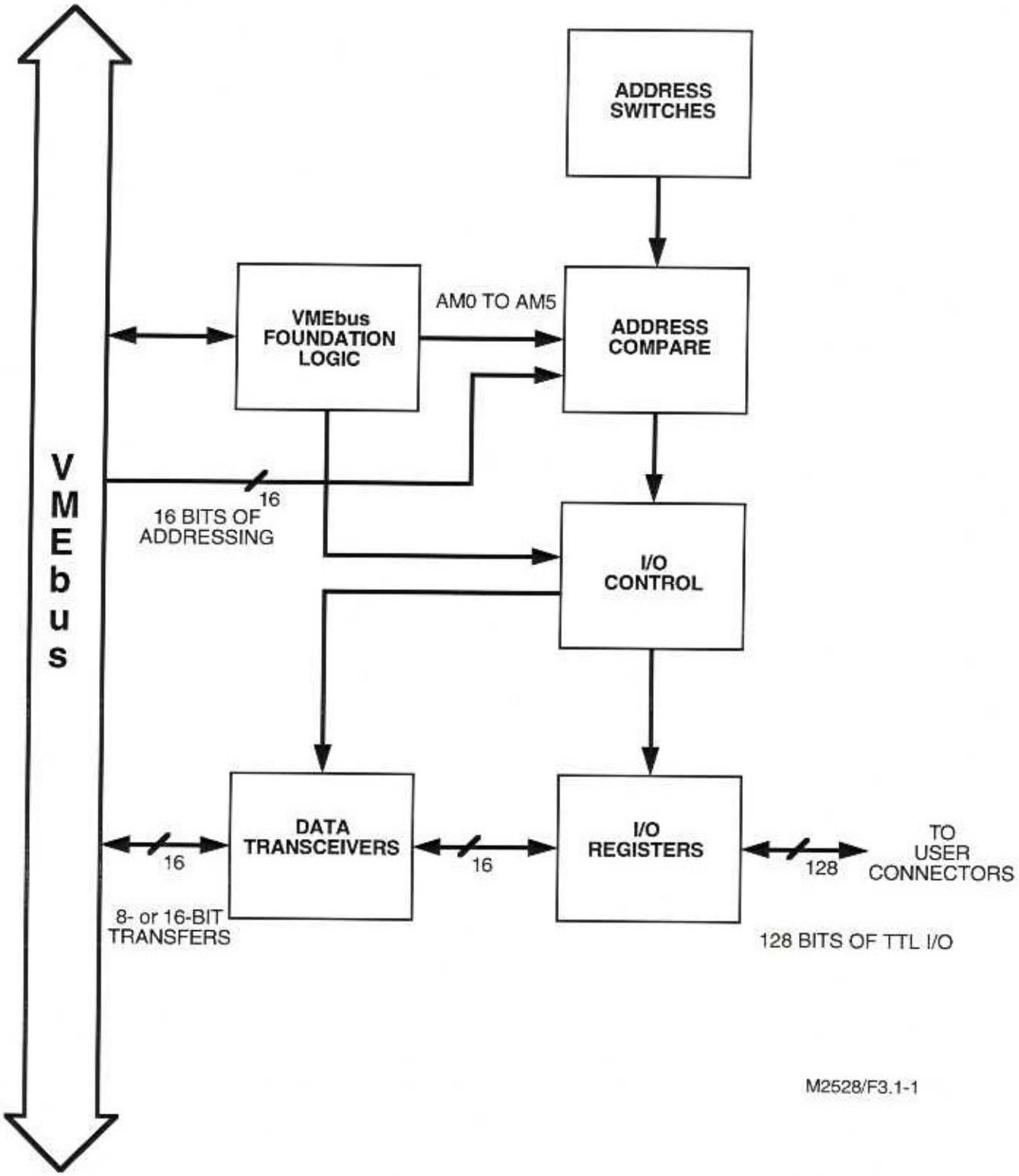

Figure 3.1-1. Functional Block Diagram

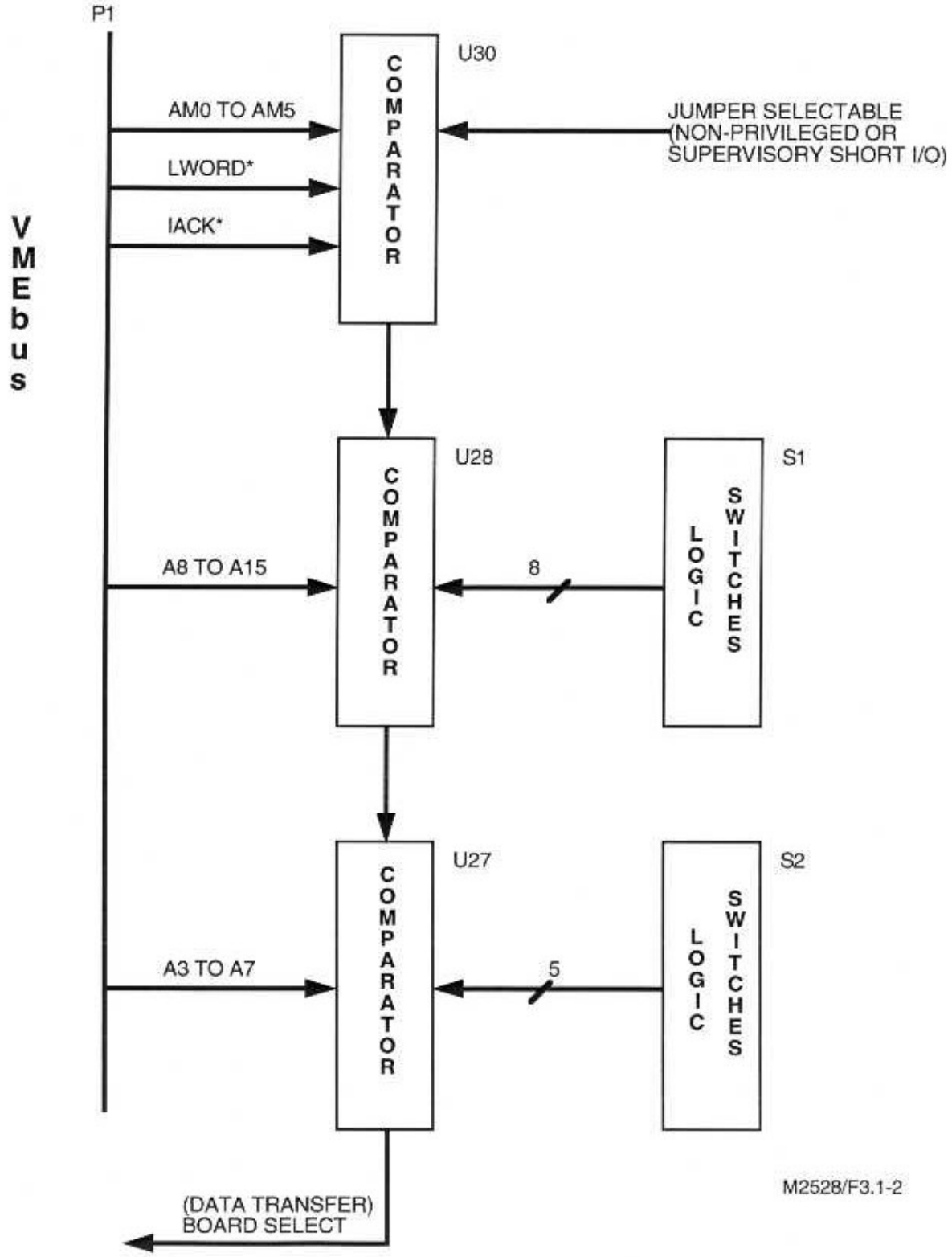

Figure 3.1-2. Address Decode Subsystem Block Diagram

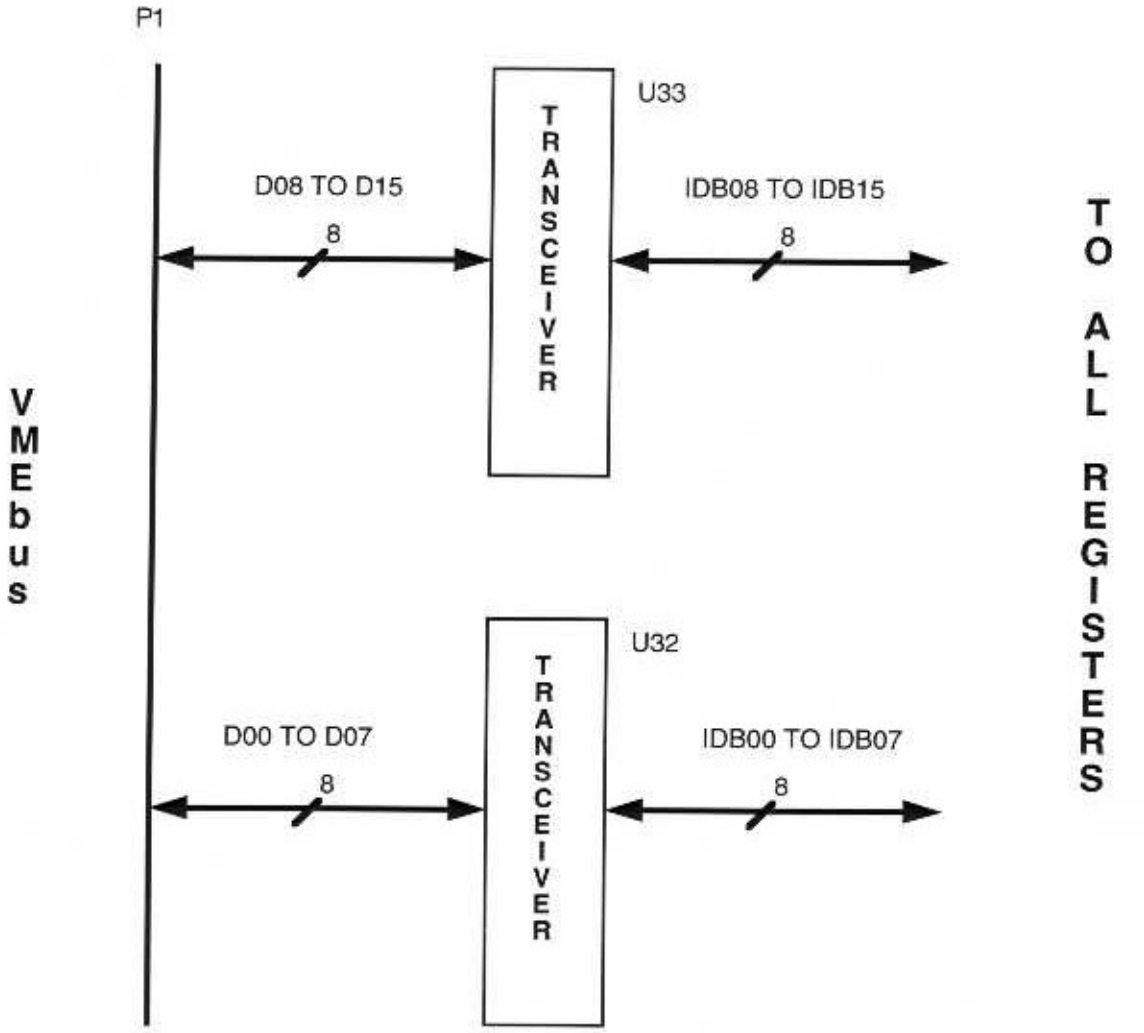

Figure 3.1-3. Data Transceiver Block Diagram

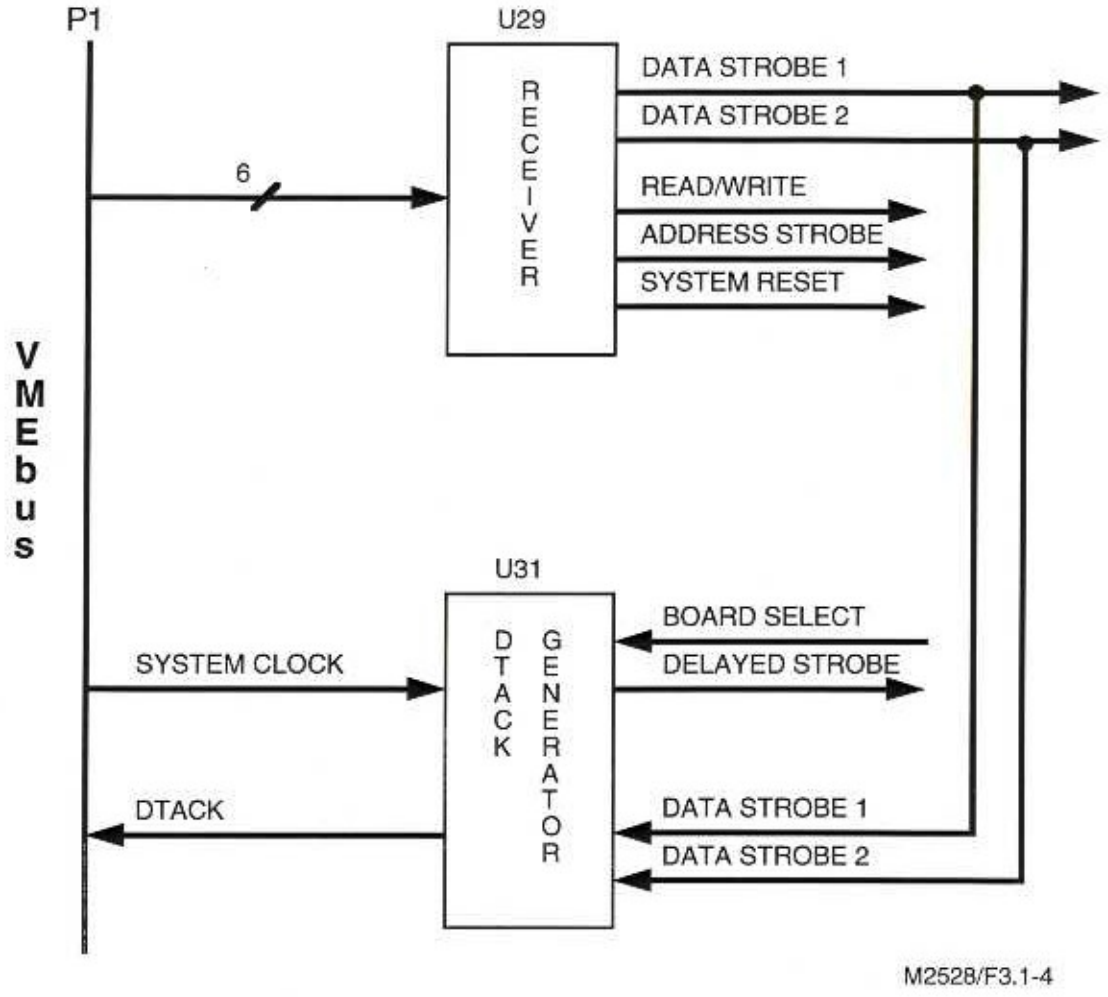

Figure 3.1-4. Control Logic Block Diagram

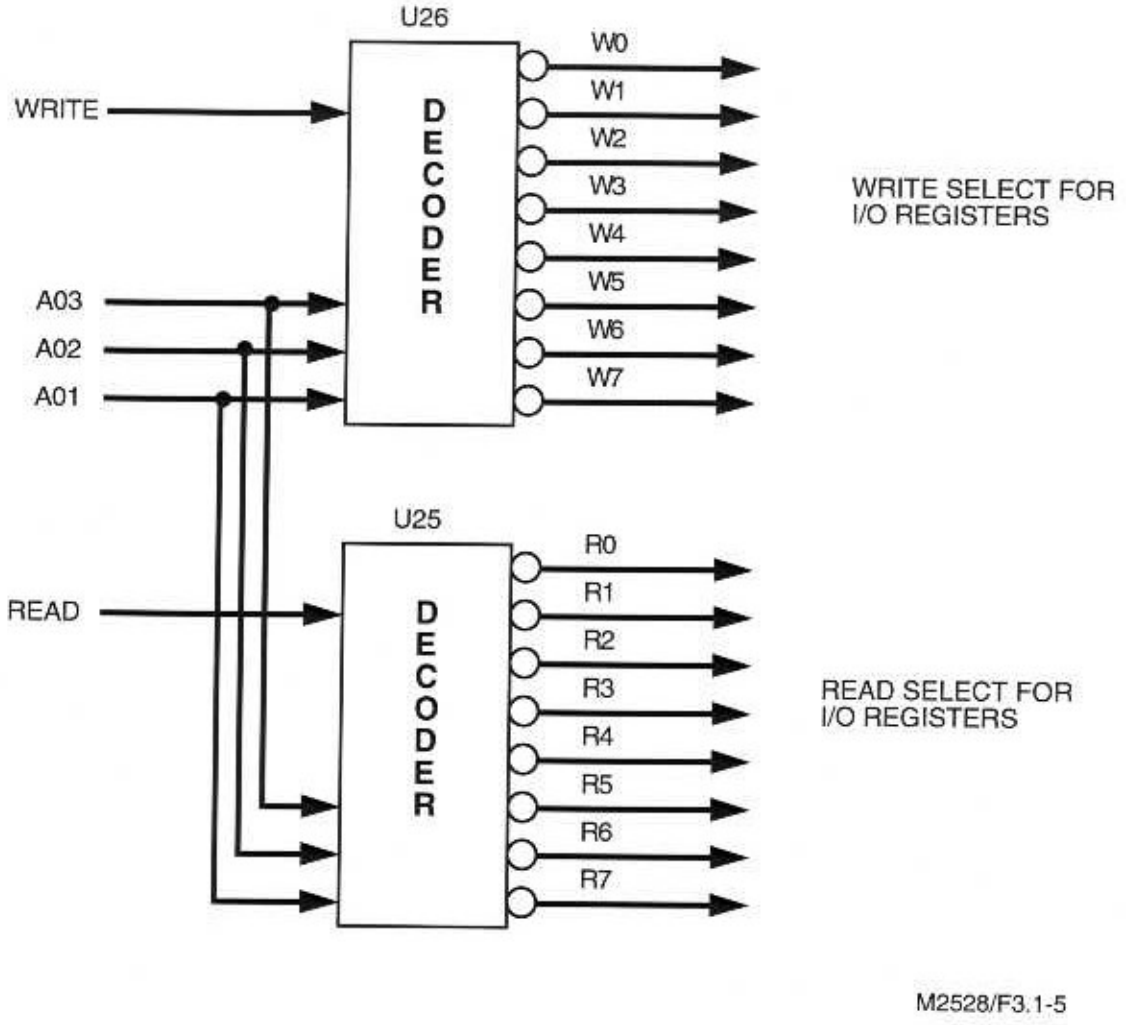

Figure 3.1-5. Read/Write Logic Block Diagram

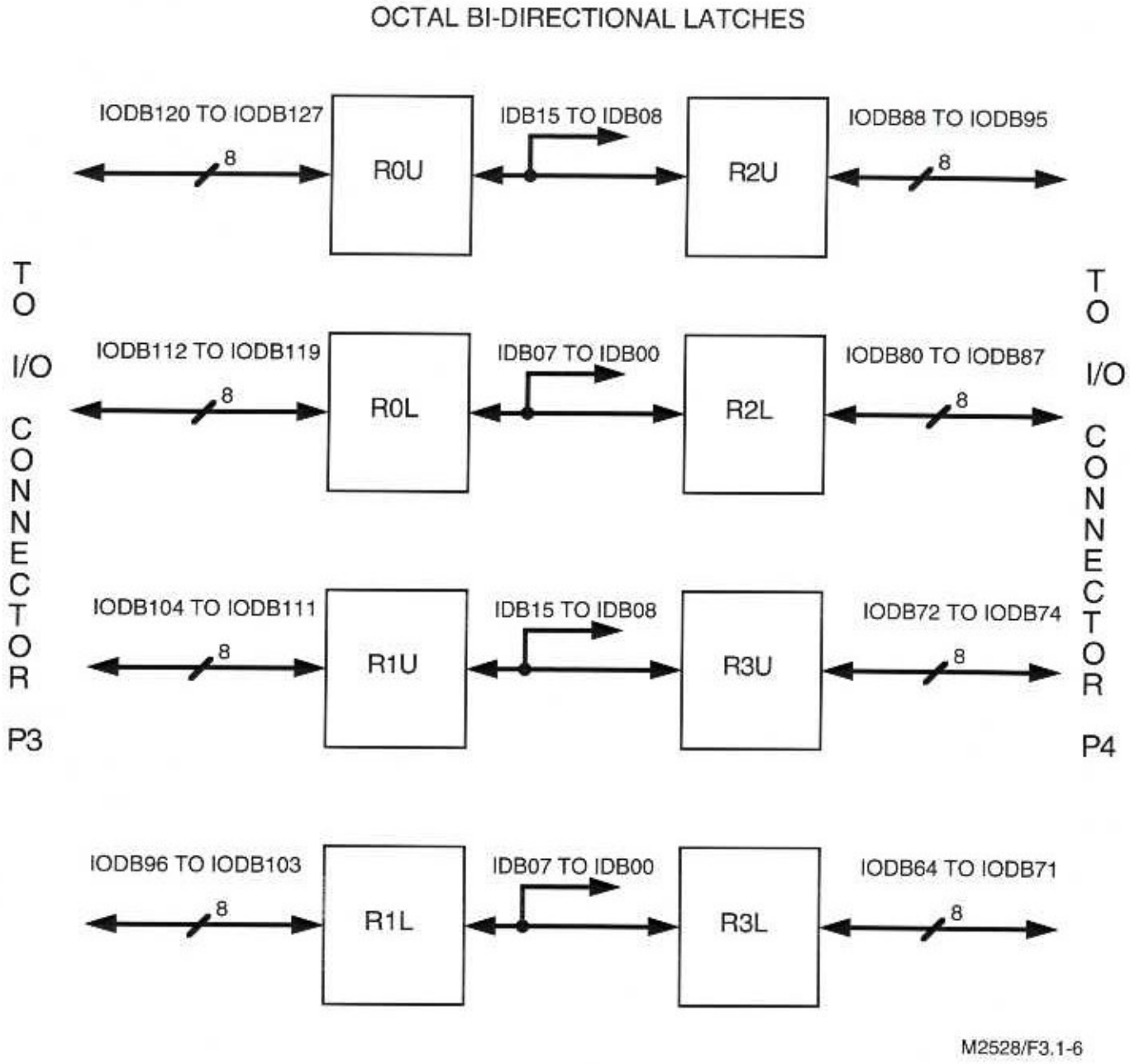

Figure 3.1-6. I/O Registers (R0 to R3) Block Diagram

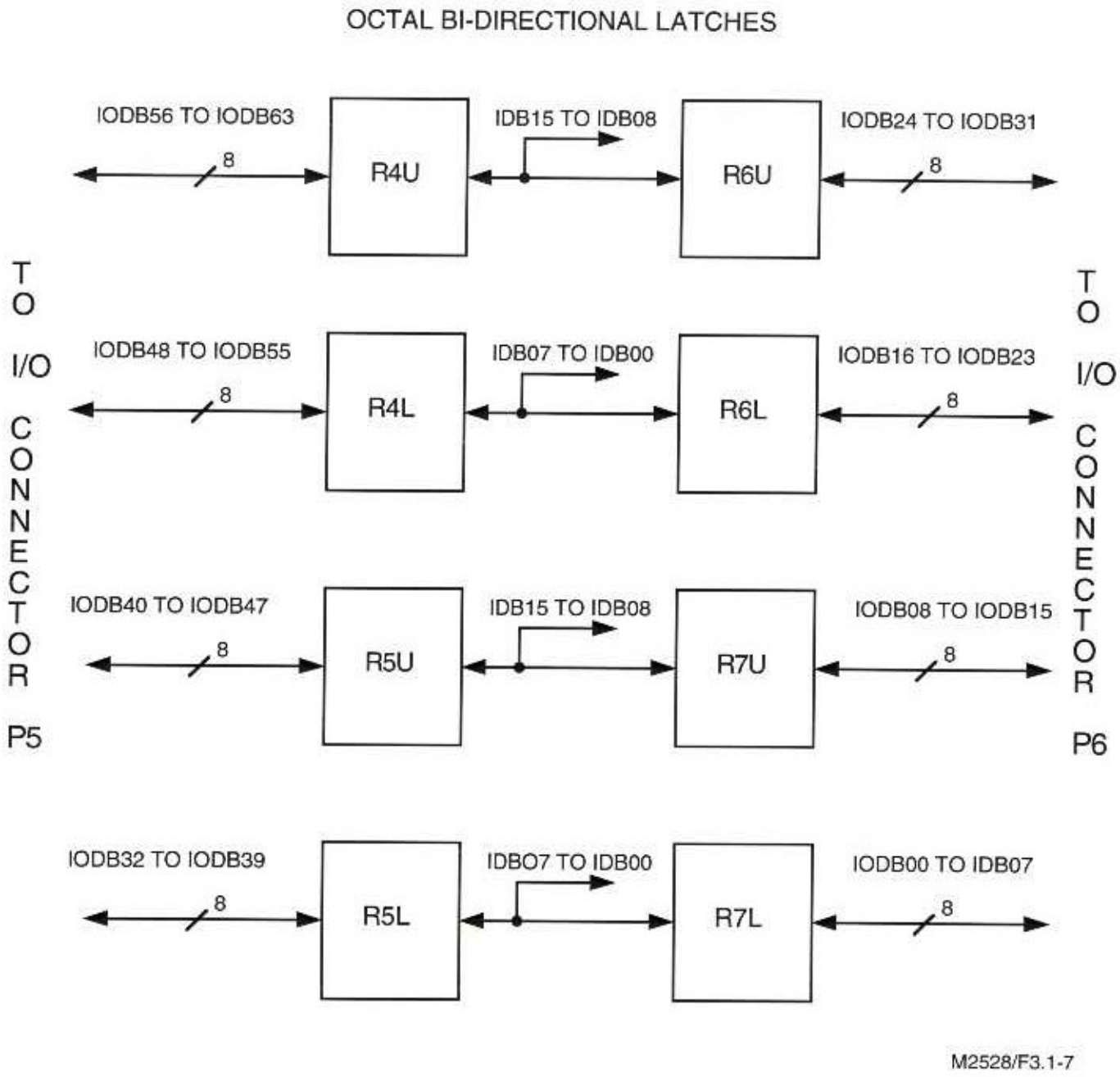

Figure 3.1-7. I/O Registers (R4 to R7) Block Diagram

jumper is installed, the byte it controls can perform input operations only. If the jumper is not installed, the byte it controls can perform read or write operations.

3.5 DATA TRANSFER DESCRIPTION

To perform I/O data transfers, data is transferred to the appropriate I/O data registers. The I/O data registers are selected by address bits A3, A2, and A1 in conjunction with the data strobes. Address bits A1, A2, and A3 select one of eight 16-bit registers with the data strobes performing the appropriate byte transfers within each word of data.

The board select signal is logically gated with DS0 and DS1 to produce active signals for data transfer. Board select also initiates a delay signal to be gated with DS0 and DS1 to produce delayed versions of these signals. The delayed signals allow set-up time through the data transceivers for the write cycle before latching the data into the I/O register. DTACK is generated indicating the data has been latched for the write cycle, or that data is valid for the read cycle.

3.6 I/O PORT ENABLE DESCRIPTION

The system reset signal, which is initiated during power-up or by the VMEbus master, disables all of the I/O ports/registers. This precaution is necessary since the I/O ports could be configured as output ports which would drive invalid data to the field circuitry. The I/O ports are enabled by performing a write to I/O register R7L. This write transfer will enable all I/O ports whether R7L is configured as an output port or not. I/O register block diagrams are shown in Figures 3.1-6 and 3.1-7.

SECTION 4

PROGRAMMING

4.1 I/O REGISTER MAP

Twelve address bits, A15 to A04, are used for board select decoding. A match of the address switch settings with these 12 bits produce the data transfer board-select signal, which enables the I/O control logic as shown in Figure 3.2-1.

The VMIVME-2528 has 128 bits of I/O. These bits are grouped as eight 16-bit registers for word transfers, allowing either byte within the word to be accessed during byte transfers. Three address bits, A03, A02, and A01, are used to decode one of the eight registers. I/O register maps are shown in Table 4.1-1.

4.2 I/O PORT DIRECTION

The programming should be consistent with the I/O configuration chosen by the I/O port direction jumpers. For example, if a particular I/O port is jumpered to be an output port, data should only be written to that particular port. Data should only be read from an I/O port if it is configured as an input port. Details of jumper configuration for I/O direction are discussed in Section 5.

Table 4.1-1. I/O Register Map

BINARY ADDRESS																	
A15	- A8	A7	A6	A5	A4	A3	A2	A1	A0								
X	X	X	X	X	X	0	0	0	0	R0U - REGISTER 0 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 127	CH 126	CH 125	CH 124	CH 123	CH 122	CH 121	CH 120
X	X	X	X	X	X	0	0	0	1	R0L - REGISTER 0 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 119	CH 118	CH 117	CH 116	CH 115	CH 114	CH 113	CH 112
X	X	X	X	X	X	0	0	1	0	R1U - REGISTER 1 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 111	CH 110	CH 109	CH 108	CH 107	CH 106	CH 105	CH 104
X	X	X	X	X	X	0	0	1	1	R1L - REGISTER 1 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 103	CH 102	CH 101	CH 100	CH 99	CH 98	CH 97	CH 96
X	X	X	X	X	X	0	1	0	0	R2U - REGISTER 2 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 95	CH 94	CH 93	CH 92	CH 91	CH 90	CH 89	CH 88
X	X	X	X	X	X	0	1	0	1	R2L - REGISTER 2 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 87	CH 86	CH 85	CH 84	CH 83	CH 82	CH 81	CH 80
X	X	X	X	X	X	0	1	1	0	R3U - REGISTER 3 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 79	CH 78	CH 77	CH 76	CH 75	CH 74	CH 73	CH 72
X	X	X	X	X	X	0	1	1	1	R3L - REGISTER 3 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 71	CH 70	CH 69	CH 68	CH 67	CH 66	CH 65	CH 64

NOTE: X represents user switch selectable positions.

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Table 4.1-1. I/O Register Map (Concluded)

BINARY ADDRESS																	
A15	- A8	A7	A6	A5	A4	A3	A2	A1	A0								
X	X	X	X	X	X	1	0	0	0	R4U - REGISTER 4 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56
X	X	X	X	X	X	1	0	0	1	R4L - REGISTER 4 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	CH 48
X	X	X	X	X	X	1	0	1	0	R5U - REGISTER 5 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40
X	X	X	X	X	X	1	0	1	1	R5L - REGISTER 5 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	CH 32
X	X	X	X	X	X	1	1	0	0	R6U - REGISTER 6 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24
X	X	X	X	X	X	1	1	0	1	R6U - REGISTER 6 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16
X	X	X	X	X	X	1	1	1	0	R7U - REGISTER 7 UPPER							
										IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 09	IDB 08
										CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8
X	X	X	X	X	X	1	1	1	1	R7L - REGISTER 7 LOWER							
										IDB 07	IDB 06	IDB 05	IDB 04	IDB 03	IDB 02	IDB 01	IDB 0
										CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0

NOTE: X represents user switch user selectable positions.

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the card is properly aligned and oriented in the supporting card guides, slide the card smoothly forward against the mating connector until firmly seated.

5.3 JUMPER AND SWITCH LOCATIONS

Refer to Figure 5.3-1 for the locations of the jumpers and switches described in this section.

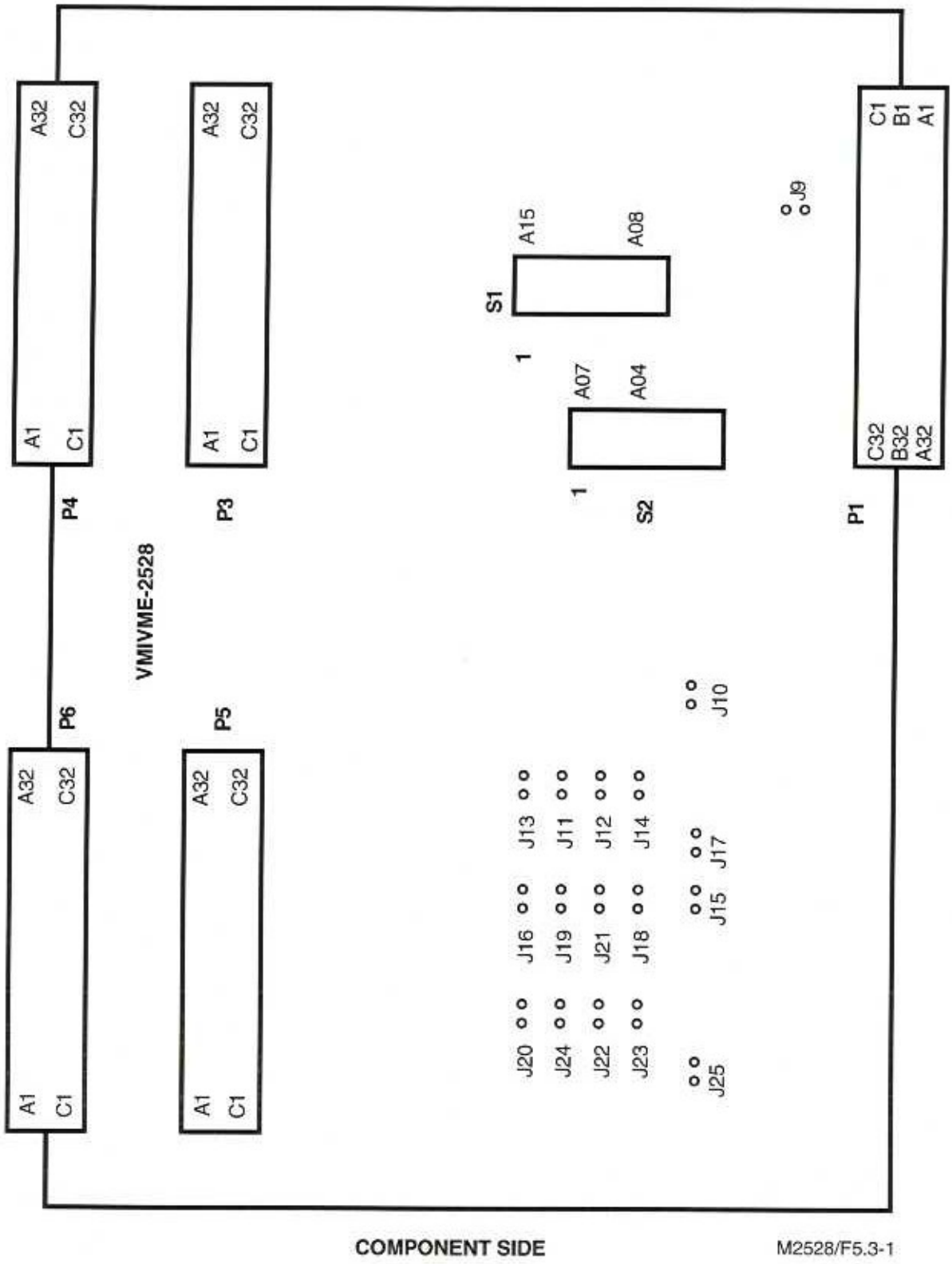

Figure 5.3-1. Diagram of the Physical Location of Jumpers and Switches

5.4 I/O PORT DIRECTION JUMPER CONFIGURATION

Table 5.4-1 below specifies the use of jumpers J10 through J25. Installation of the jumper specified configures that port as an input port.

Table 5.4-1. I/O Port Direction Jumper Configuration

JUMPER	I/O PORT NO.	CHANNELS
J10	1	120-127
J11	2	112-119
J12	3	104-111
J13	4	96-103
J14	5	88-95
J15	6	80-87
J16	7	72-79
J17	8	64-71
J18	9	56-63
J19	10	48-55
J20	11	40-47
J21	12	32-39
J22	13	24-31
J23	14	16-23
J24	15	8-15
J25	16	0-7

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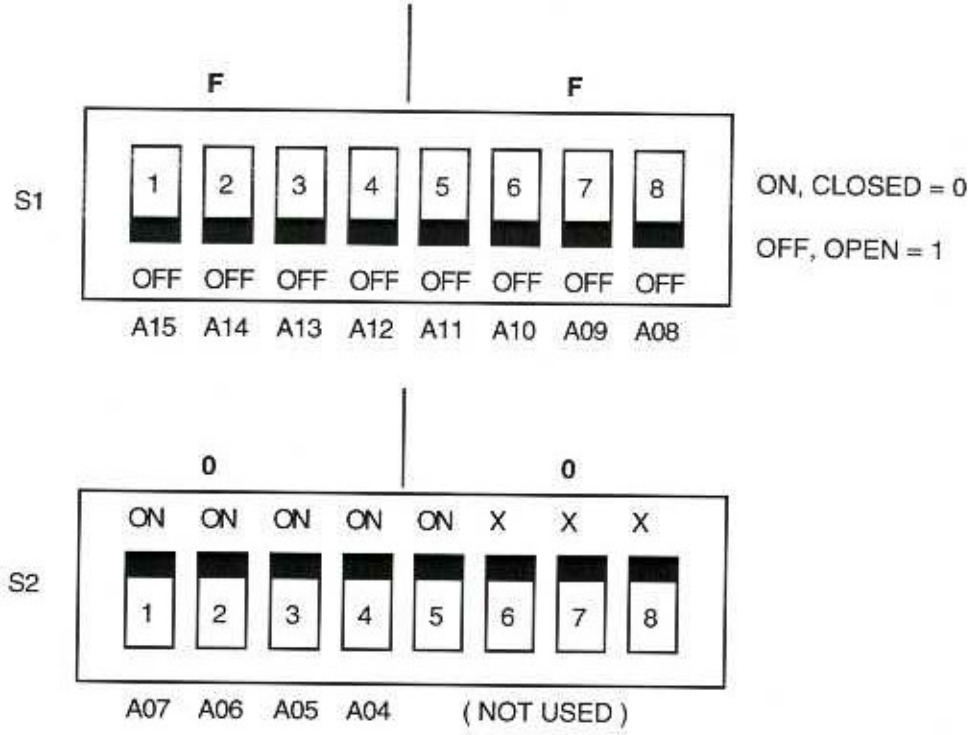
5.5 ADDRESS MODIFIERS

The VMIVME-2528 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper J9 which enables the board to respond to short non-privileged I/O access.

5.6 ADDRESS SELECTION SWITCHES

The following figure (Figure 5.6-1) shows the two address selection switches on board the VMIVME-2528, and their use in the addressing scheme.



The example shown is for a base address of FF00.

M2528/F5.6-1

NOTE: X represents an unused switch whose position is immaterial.

Figure 5.6-1. Address Select Switches

5.7 I/O CABLE AND CARD-EDGE CONNECTOR CONFIGURATION

The I/O connectors (P3 to P6) on the VMIVME-2528 are 64-pin DIN standard and were selected by VMIC because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC Publication Number 825-000000-006) for additional informaton concerning the variety of possible cabling and connector types available.

The VMIVME-2528 is designed with a high quality ground plane that is connected to the VMEbus ground and to alternate I/O pins on connectors P3, P4, P5, and P6 to provide enhanced noise immunity and more reliable operation. The VMIVME-2528 is designed to support I/O via four cables connected to connectors P3, P4, P5, and P6 as shown in Figure 5.7-1. Table 5.7-1 shows the channel assignments of the P3, P4, P5, and P6 connectors.

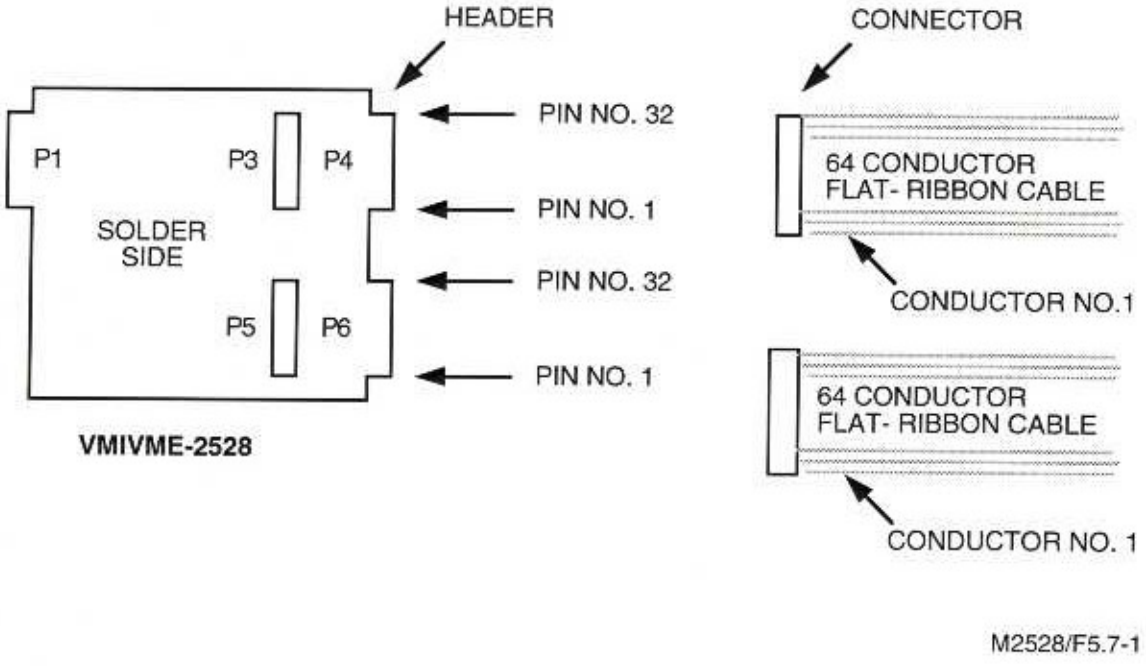


Figure 5.7-1. Cable Connector Configuration

Table 5.7-1. Connector Pin/Channel Assignments

ROW A	P3 CONNECTOR PIN CHANNEL		P4 CONNECTOR PIN CHANNEL		P5 CONNECTOR PIN CHANNEL		P6 CONNECTOR PIN CHANNEL	
	32	127	32	95	32	63	32	31
	31	126	31	94	31	62	31	30
	30	125	30	93	30	61	30	29
	29	124	29	92	29	60	29	28
	28	123	28	91	28	59	28	27
	27	122	27	90	27	58	27	26
	26	121	26	89	26	57	26	25
	25	120	25	88	25	56	25	24
	24	119	24	87	24	55	24	23
	23	118	23	86	23	54	23	22
	22	117	22	85	22	53	22	21
	21	116	21	84	21	52	21	20
	20	115	20	83	20	51	20	19
	19	114	19	82	19	50	19	18
	18	113	18	81	18	49	18	17
	17	112	17	80	17	48	17	16
	16	111	16	79	16	47	16	15
	15	110	15	78	15	46	15	14
	14	109	14	77	14	45	14	13
	13	108	13	76	13	44	13	12
	12	107	12	75	12	43	12	11
	11	106	11	74	11	42	11	10
	10	105	10	73	10	41	10	09
	09	104	09	72	09	40	09	08
	08	103	08	71	08	39	08	07
	07	102	07	70	07	38	07	06
	06	101	06	69	06	37	06	05
	05	100	05	68	05	36	05	04
	04	099	04	67	04	35	04	03
	03	098	03	66	03	34	03	02
	02	097	02	65	02	33	02	01
	01	096	01	64	01	32	01	00

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NOTE: Row C is grounded on all connections.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC