VMIVME-2534

32-BIT HIGH VOLTAGE DIGITAL INPUT OR OUTPUT BOARD WITH P2 I/O AND BUILT-IN-TEST

INSTRUCTION MANUAL

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
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SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THIS OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THE PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

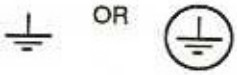
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

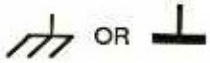
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-2534

32-BIT HIGH VOLTAGE DIGITAL INPUT OR OUTPUT BOARD WITH P2 I/O AND BUILT-IN-TEST

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APPENDIX

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-2534 is a VMEbus Compatible High Voltage Digital I/O Board with 32 channels of high voltage digital outputs and 32 channels of high voltage or differential digital inputs. Its features include:

a. Thirty-two High Voltage Outputs

(1) High sink current (600 mA)
(2) High breakdown voltage (70 V)
(3) Output voltage range options (TTL compatible, 5 V, 12 V, 24 V, and 48 V)
(4) Output clamp diodes
(5) Outputs in the same chip may be paralleled for higher drive capability
(6) 8-, 16-, or 32-bit data transfers
(7) Uses the UDN-2549B incandescent lamp driver (no external warming resistors required)

b. Thirty-two High Voltage/Differential Inputs

(1) Each group of eight inputs are jumper selectable to monitor contact closure, voltage sourcing, current sinking, or differential signals.
(2) Open circuit provides a logic "zero" or (jumper selectable) a logic "one".
(3) Input filter option or RS422/RS485 compatible terminator option
(4) User selectable input voltage thresholds (1.25 V to 66 V)

c. Common Board Features

(1) P2 I/O connection (no front panel connectors)
(2) Built-in-Test (off-line and real-time support)
(3) 100% testing of all active components (including the output drivers)
(4) Front panel with Fail LED
(5) Compatible with Intelligent I/O Controllers
(6) Software compatible with the VMIVME-2532

1.2 FUNCTIONAL DESCRIPTION

The 32-bit Digital Input/Output (DIO) board transfers digital data from the VMEbus backplane to output registers that are interfaced to high voltage output drivers. It also reads high voltage or differential input signals and puts the data on the VMEbus backplane for subsequent transfer to a CPU. A simplified functional block diagram of a 32-bit DIO board is illustrated in Figure 1.2-1.

This high voltage DIO board is designed with a variety of manufacturing options to allow the user to specify the board's input and output configurations. The input signal conditioning circuitry supports a wide variety of topologies. These topologies include differential, single-ended active-high data, single-ended active-low data, and filtered (or debounced) inputs. The single-ended inputs can be configured for contact sensing, voltage sourcing, or current sinking with selectable input threshold voltages on a byte-by-byte basis. These topologies are user configurable. The output configuration is basically open collector, but the input topology permits an input resistor to be used as a pull-up for the output drivers.

The VMIVME-2534 is designed with extensive Built-in-Test electronics that enable the user to test the functioning of the board. Test registers are provided for off-line testing of the board. This test tristates the output drivers to prevent damage to the field circuity. The board's outputs are tied to the input signal conditioning circuits, and by reading the input circuits the outputs can be tested. Thus 100% of the board's I/O circuitry can be tested this way. Figure 1.2-2 is a functional block diagram showing the Built-in-Test features of the VMIVME-2534 board.

1.3 FUNCTIONAL BLOCK DIAGRAM

The VMIVME-2534 DIO board consists of VMEbus compatibility logic, four 8-bit output registers, four 8-bit input ports, a Control Status Register (CSR), and Built-in-Test logic, as shown in Figure 1.3-1. The VMEbus compatibility logic controls data transfers allowing 8-, 16-, or 32-bit VMEbus data transfers. Four 8-bit output registers latch 32-bits of output data, which drive the high voltage output drivers. Four 8-bit input receivers monitor the user field circuitry (and the output drivers if they are being used). The CSR controls the on-board Fail LED, the test functions, and the state of the I/O circuits of the board. The Built-in-Test logic enables the output data to be read back through the input ports without affecting incoming signals from the field. System reset or power-up puts the board in test mode for immediate loopback testing.

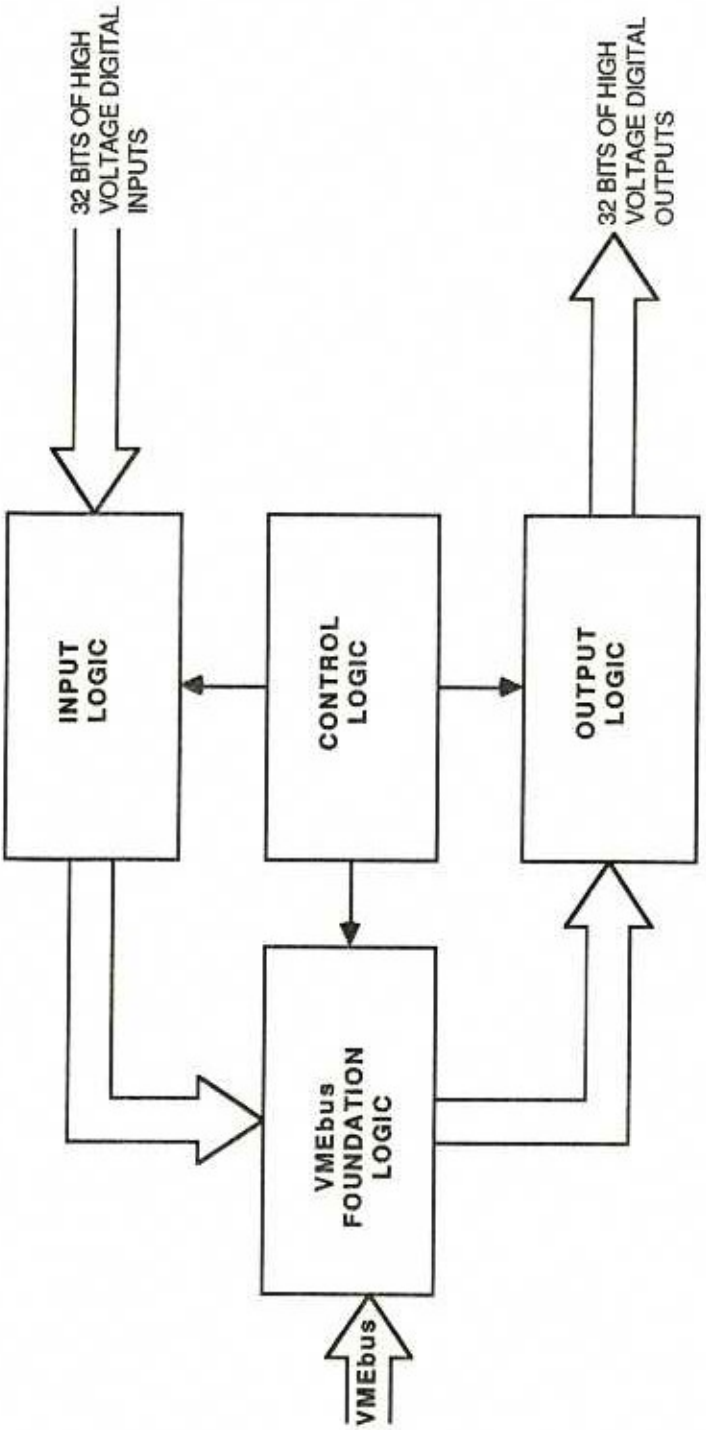


Figure 1.2-1. Basic Digital I/O Board Functions

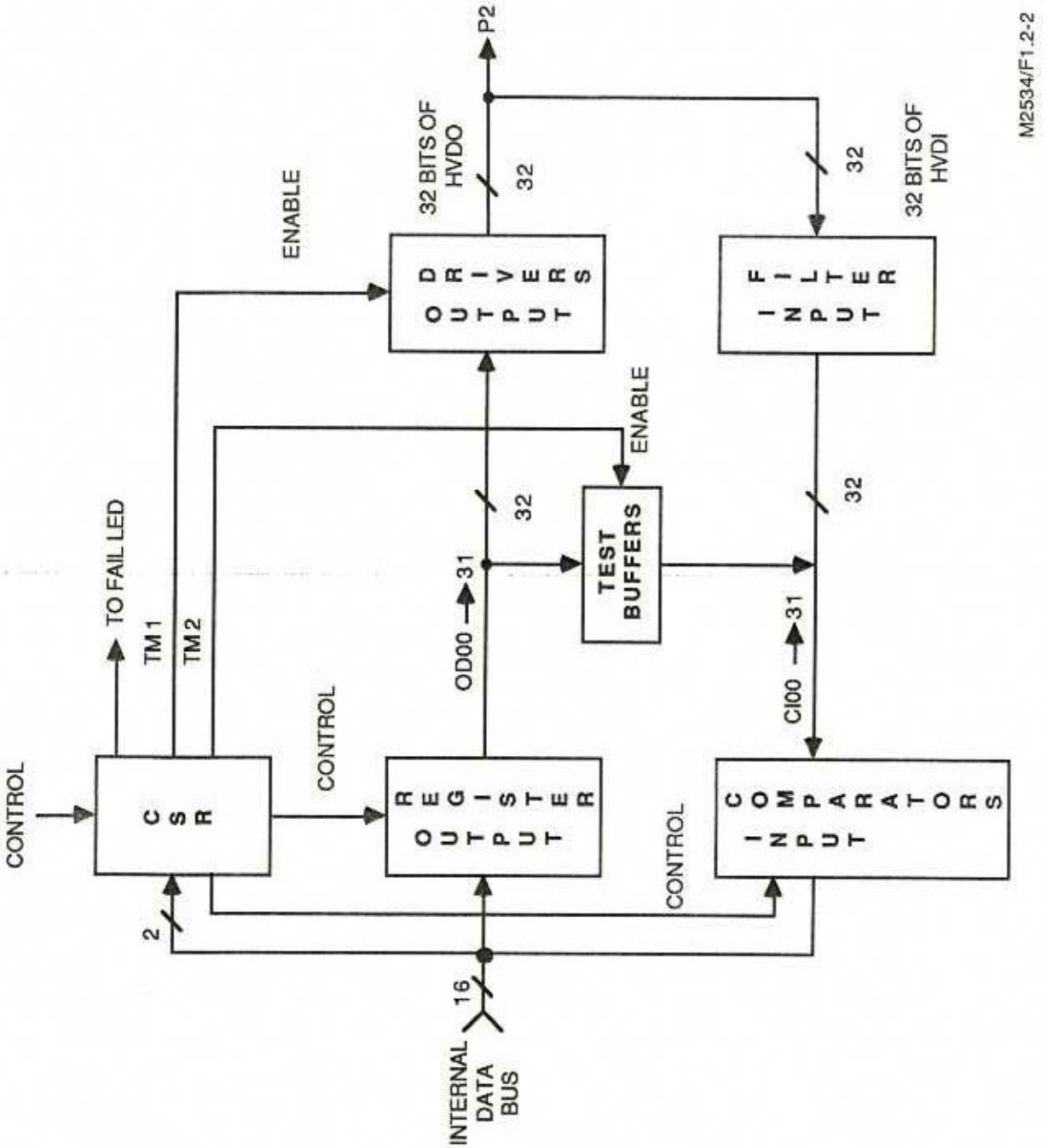


Figure 1.2-2. Simplified Built-in-Test Functional Block Diagram

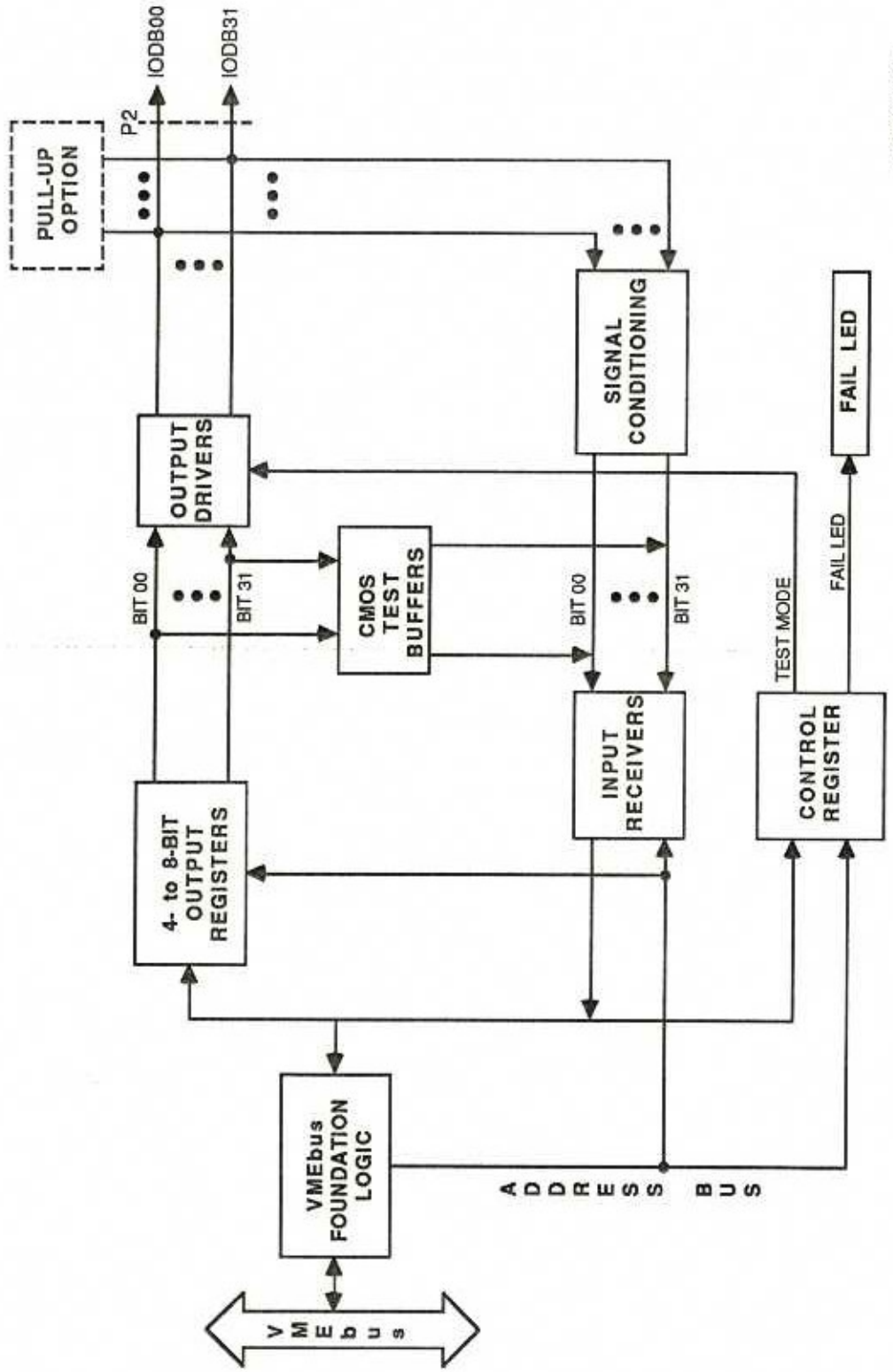


Figure 1.3-1. Functional Block Diagram

1.4 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following applications and configuration guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Connector and I/O Cable Application Guide	825-000000-006
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-002534-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section of the manual presents information concerning the hardware operation of the board. The reader should refer to VMIC Document Number 825-000000-000 (Digital Input Board Application Guide) for a thorough understanding of the voltage sourcing and current sinking concepts.

3.2 OPERATIONAL OVERVIEW

The VMIVME-2534 consists of four primary blocks as illustrated in Figure 3.2-1. These blocks will be described in detail in the following sections. To perform an output data transfer, data is written into the Output Data Registers (ODR) from the VMEbus and controls the output driver stage of the board. The input ports monitor the P2 connector and hence the output drivers. When the drivers are ***NOT*** enabled (tristated) or they are removed from the board (they are socketed), the inputs can monitor the field circuitry and input transfers can be performed via the Input Data Registers (IDR). If the output drivers ***ARE*** enabled, the inputs can monitor their state. In this way the inputs perform the real-time Built-in-Test function.

3.3 VMEbus FOUNDATION LOGIC

The basic VMEbus foundation logic used by the VMIVME-2534 is illustrated in Figure 3.3-1. It consists of control signal receivers, a DTACK generator, and the 32-bit data bus transceivers. The buffer drivers and receivers or transceivers, are used to present minimum VMEbus loading and board logic buffering. The DTACK generator is designed to provide the maximum data transfer rate for this board. The VMIVME-2534 can perform 8-, 16-, or 32-bit data transfers. Figure 3.3-2 shows the data transceivers and the topology used in processing the data transfers. The detailed logic diagram (Document Number 141-002534-000) used in this design can be found in Appendix A to this manual.

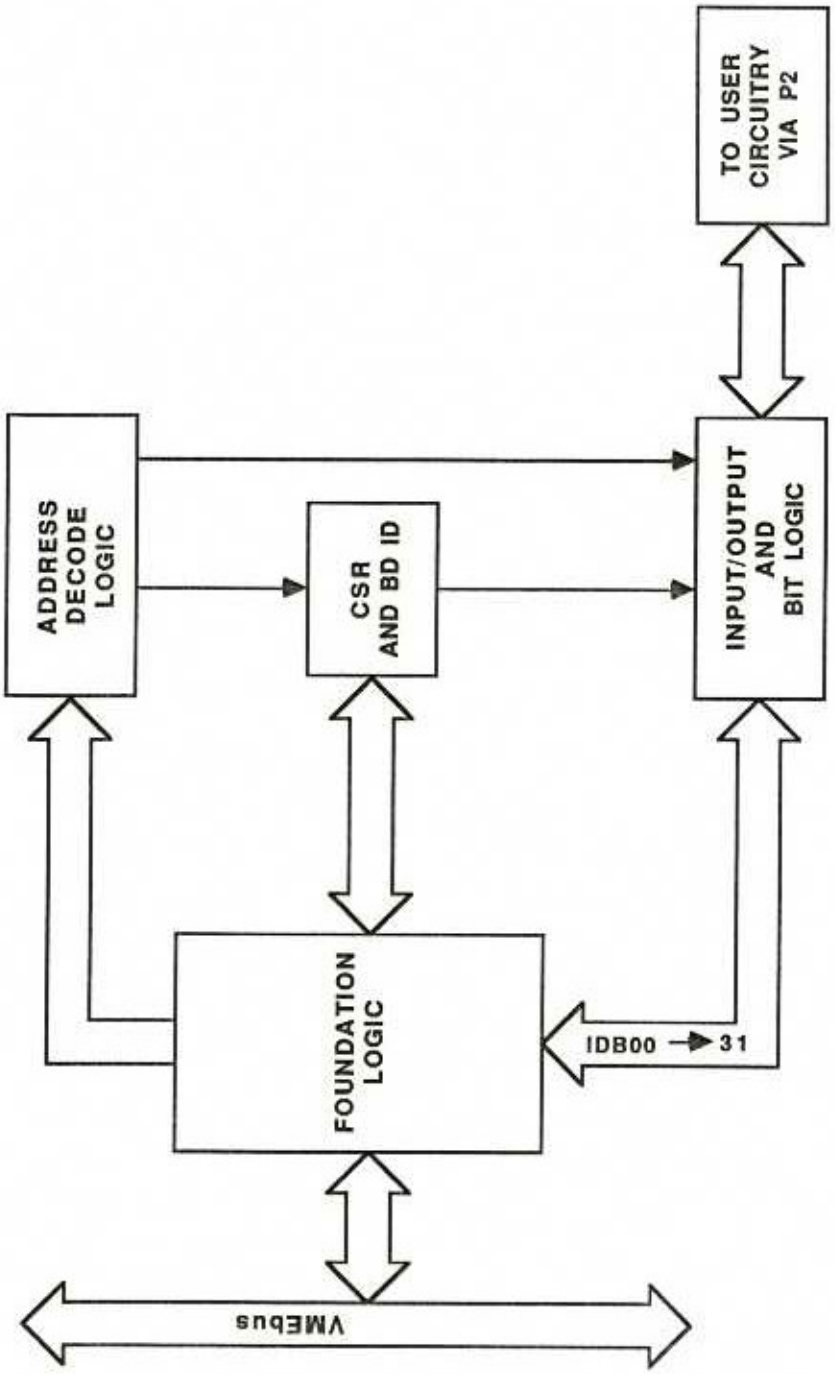


Figure 3.2-1. Functional Block Diagram

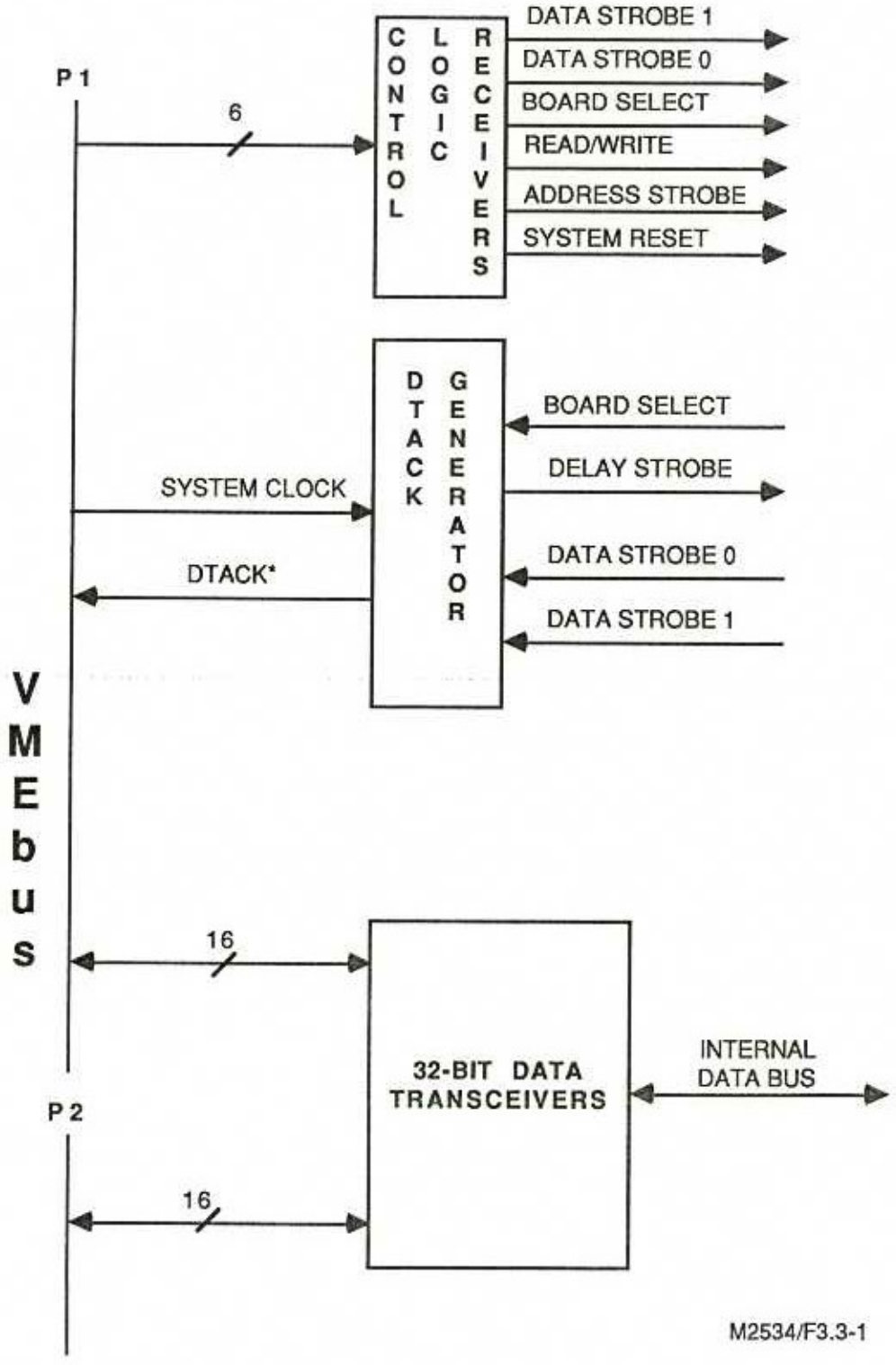


Figure 3.3-1. VMEbus Foundation Logic

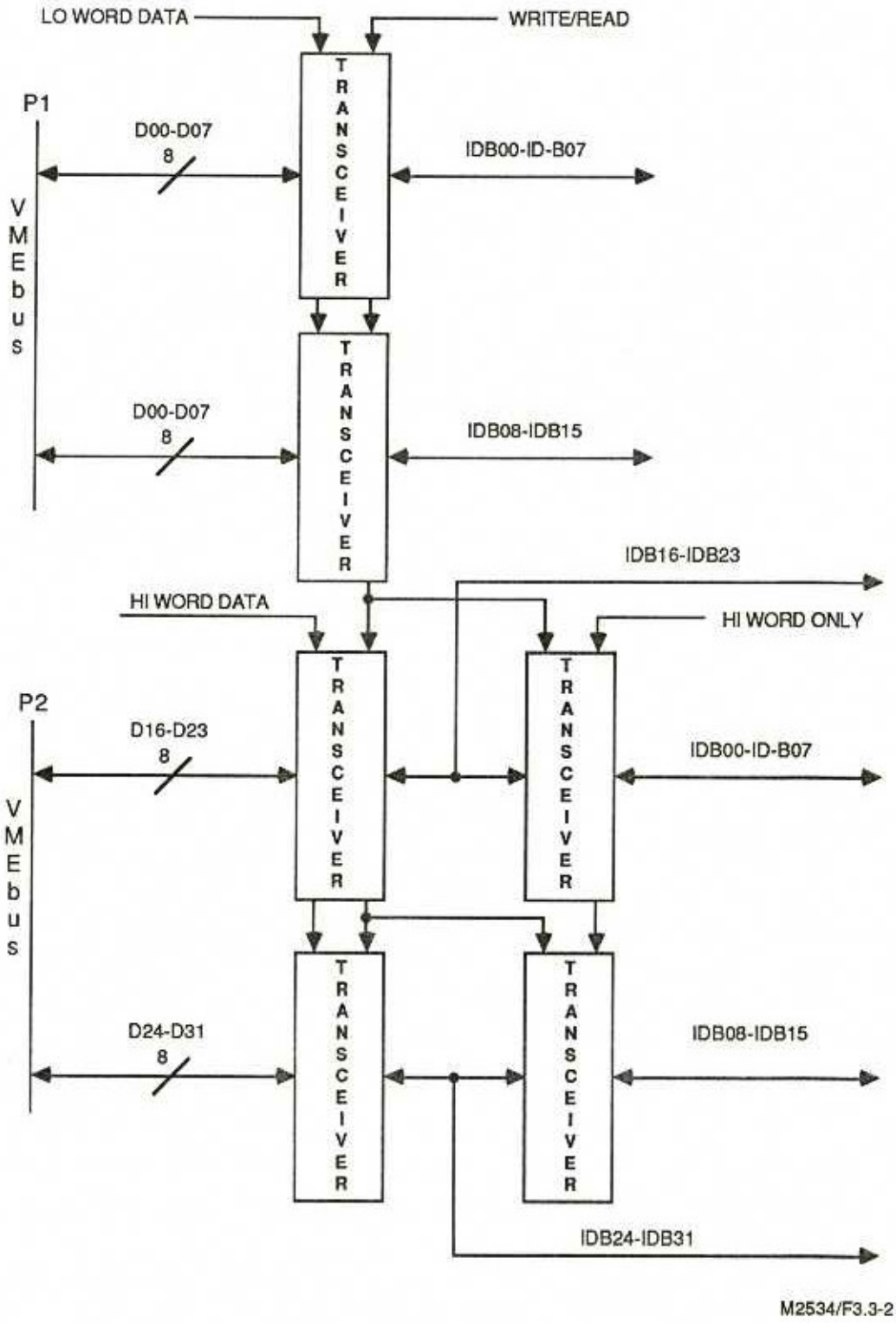


Figure 3.3-2. Data Transfer Block Diagram

3.4 DEVICE ADDRESSING

The address decoding scheme used in this design is shown in Figure 3.4-1. The data registers are decoded separately from the Control Status Register (CSR). This allows the CSRs and data registers of several boards to be mapped into separate, but contiguous, memory addresses. This can help make software more efficient. The board is shipped with the CSR stacked on top of the data registers. This makes it software compatible with the VMIVME-2532 for the shipped address. The user will have to adjust all of the address headers when he sets up this board.

The board is designed to support data transfers in the short I/O memory space. A pair of jumpers (labeled AM2) are used to establish the I/O space to be used. One is used for the data registers and the other is used with the CSR. These jumpers permit the user to select between supervisory, non-privileged or both I/O accesses for the data, or CSR registers. The board is factory configured (jumpers AM2 not installed) to respond to supervisory I/O accesses.

3.5 CONTROL STATUS REGISTER (CSR)

The Control Status Register (CSR) in the VMIVME-2534 is a *read/write* register that controls the test mode bits, a Fail LED, the output drivers, and includes a *read only* board Identification Register (IDR). The CSR and the board IDR are read as a 16-bit word with the IDR in the upper (MSB) byte as shown in Figure 3.5-1. The test mode and the LED bits are in the same BIT positions as the VMIVME-2532. This is to keep these two boards software compatible. These three bits perform the same VMIVME-2532 functions in the 2534; however, test mode bit 1 (TM 1 L) can be programmed (by jumpers J8 and J9) to permit software control of the I/O direction on a byte-by-byte basis. Test mode bit 2 (TM 2 L) is used to enable the CMOS test buffers, which are used during diagnostic testing.

Jumpers JP8 and JP9 are used in conjunction with CSR bits to control the output drivers. The two modes are VMIVME-2532 simulation and VMIVME-2534 mode. JP8 sets the mode to VMIVME-2532 simulation in position B-C. The VMIVME-2532 simulation mode allows the inputs to be configured a byte at a time as input only mode (JP9 in position 2) or I/O control using TM1 bit in the CSR (JP9 in position 1). Installing JP8 in position A-B will set the mode to VMIVME-2534, where the direction is controlled a byte at a time via TM1 and B0H-B3H. Program TM1 to a logic 1 to enable the output drivers. The byte of channels can be programmed using B0H (CH.24-CH.31), B1H (CH.16-CH.23), B2H (CH.8-CH.15), and B3H (CH.0-CH.7), where a logic 1 enables the byte as an output.

A front panel Fail LED is provided by the VMIVME-2534. This Fail LED is illuminated upon power-up or after a system reset. It may be extinguished under

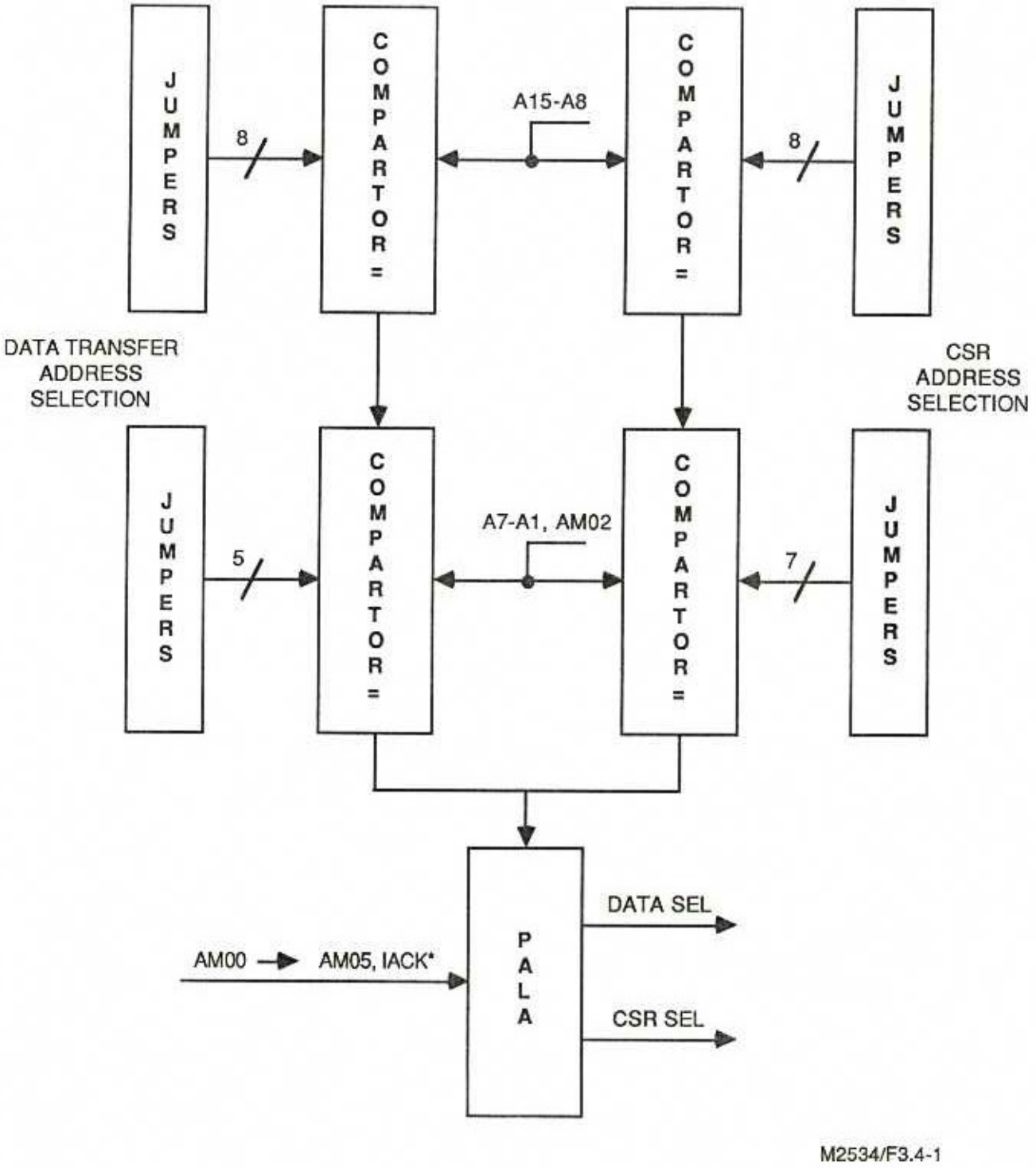


Figure 3.4-1. Device Address Selection Block Diagram

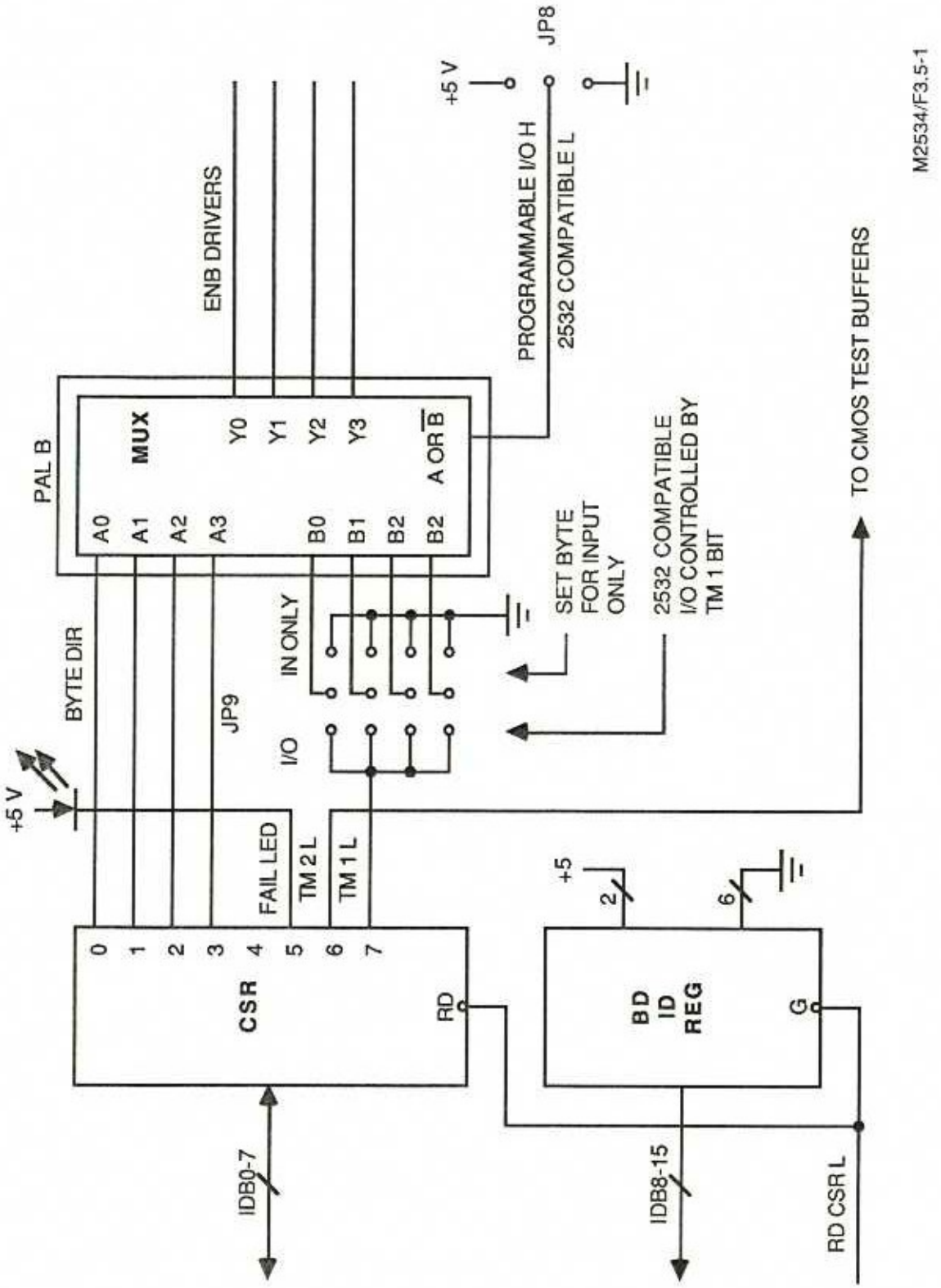


Figure 3.5-1. CSR and Board Input Data Registers

software control after successfully completing some diagnostic software. It can be turned on if the board fails to respond to commands it should. This can be useful in locating faulty boards in a system.

A board IDR is also provided by the VMIVME-2534. This IDR is part of the CSR word. Its value is 05 HEX for positive true output option. The value is FA HEX for negative true output option. This is a *read only* register. It can be used by system start-up software to automatically set up the system configuration, thus, eliminating possible human error.

3.6 OUTPUT DATA PATH

The typical path for a bit of I/O data is shown in Figure 3.6-1. The output path consists of an output data register which controls the associated output driver, and, therefore, the user's field circuitry via the P2 connector. In the on-line (normal) mode of operation, a *write* instruction moves data from the VMEbus via the board's internal data bus to the Output Data Registers (ODRs) and hence to the output drivers. These drivers are open collector devices, thus, the output data gets inverted (a logic "one" turns ON the driver and a logic "zero" is sent to the user's field circuitry). The data registers control this data polarity. If a non-inverting register is used (as in the positive true option) then a logic "one" written to the board issues a logic "zero" to the field circuitry. However, if an inverting latch is used (as in the negative true option) then a logic "one" written to the board turns OFF the driver and the output will go to the state dictated by the passive components in the output circuitry of the board.

3.7 INPUT DATA PATH

The input data path flows from the user's field electronics (via the P2 connector) through the input signal conditioning circuit (consisting of resistor networks for the input and comparator biasing) to the input voltage comparator to the Input Data Register (IDR), and finally the VMEbus via the board's internal data bus. If the output drivers are not enabled (tristated) and a *read* operation is performed, the input data from the voltage comparator is latched in the IDR. From there the data moves through the internal data bus to the VMEbus. The output drivers are socketed and can be removed by the user if their leakage current is to much for the input circuitry.

The input circuitry can be arranged to perform many types of signal conditioning. Voltage sourcing, current sensing, contact closure sensing, differential, positive true or negative true inputs are all supported by various circuit configurations. These set ups may be configured by the user on a byte-by-byte basis. Thus, one byte may be fixed to read voltage sourcing inputs with positive true data, while another byte is set up to read differential inputs, and yet another byte is configured to process contact closures with negative true data. These

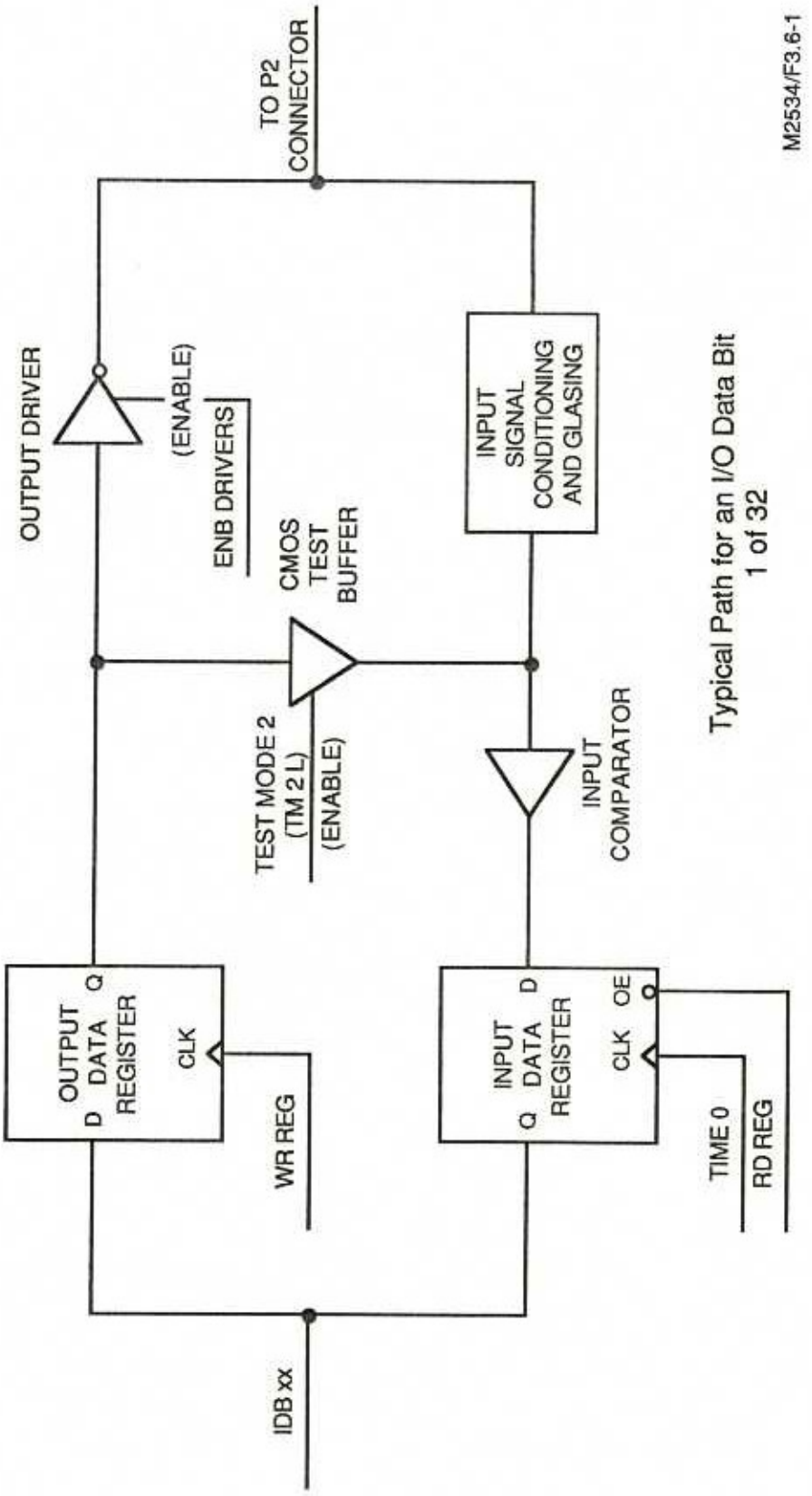


Figure 3.6-1. Digital Input/Output and BIT Block Diagram

configurations are done by jumper selections and the position of input resistor SIP networks. Different voltage levels are handled by different values for the input SIP resistors. The specific SIP and jumper configurations for specific input requirements are discussed in Section 5 of this manual. However, it must be remembered that the outputs must be tristated or removed for these inputs to read the user's external inputs.

3.8 BUILT-IN-FUNCTIONS DESCRIPTION

The VMIVME-2534 test functions are similar to those of the VMIVME-2532. In the normal (on-line) mode of operation data is moved to or from the P2 connector by instructions from the CPU. The VMIVME-2534 (like the VMIVME-2532) provides three different test modes. These are off-line, on-line, and dedicated test modes. These test modes are controlled by two bits in the Control Status Register (CSR) (TM 1 L and TM 2 L) assuming the CSR is configured to behave like the VMIVME-2532. Please refer to Section 3.5 for a more detailed discussion of this subject.

The following discussions assume the board is configured to behave like a VMIVME-2532. In the off-line test mode the output drivers are disabled and the CMOS test buffers are enabled. TM 1 L and TM 2 L are both active (logic "zero"). This is the mode in which the board powers-up in or after a system reset. This is to prevent the output drivers from damaging any external circuitry. In this mode data written to the board is looped back to the input comparators. Thus, on a read command this data is fed back to the VMEbus. The CPU can then compare the read data to the written data and take appropriate action. This mode of testing does not test the output drivers nor the input signal conditioning/biasing circuits.

On-line testing assumes the output drivers are being used, therefore, they pose no problem to the user's circuitry or the board is used in an output only mode. In either event, in this mode of testing, the test mode bit for TM 1 L is not active (a logical "one") while the test mode bit for TM 2 L is active (a logical "zero"). Now the inputs can monitor the activity of the output drivers. By reading the board, the CPU can determine the state of the output drivers and take any appropriate action.

On the VMIVME-2534 the input circuits are always tied to the output drivers like a VMIVME-2532 in the dedicated test mode. Thus, the board can always monitor the outputs. This is the normal operating mode of this board (TM 1 L and TM 2 L are both off or at a logical "one"). However, the output drivers may impede the reading of the input signals or otherwise damage the external circuitry, therefore, the drivers are socketed and may be removed by the user if necessary. The input circuitry has no such effect on the output drivers and can be used to test the output drivers at any time.

SECTION 4

PROGRAMMING

4.1 INTRODUCTION

The VMIVME-2534 performs output transfers by writing data to the appropriate Output Data Registers (ODRs). High voltage digital inputs are read by performing a *read* from Input Data Registers (IDRs). For programming simplicity the registers are mapped into the same address locations, therefore, the bits of each register correspond to an output channel when performing a *write* to that register, and to an input channel when performing a read cycle.

4.2 DATA TRANSFERS

A data transfer operation with this board is initiated when the CPU executes an instruction with an address that is mapped by this board. When the CPU stores data to this board appropriate on-board control signals route the data to the appropriate register. When the CPU reads data from this board appropriate controls signals route the data from the proper register to the VMEbus. In either event DTACK is activated when the board has completed the bus cycle.

4.3 CONTROL STATUS REGISTER (CSR)

The Control Status Register (CSR) is a register that controls the Test Mode (TM) bits, the front panel Fail LED, and the output driver's enable lines. One of the TM bits enables the TRI-STATE outputs of four CMOS buffers, which are used to perform Built-in-Test functions. The other test mode bit is used to disable the output drivers, which supports off-line Built-in-Test functions. The format of the CSR data the board ID data and the I/O data and their relative addresses are shown in Table 4.3-1. The CSR is initialized active (all outputs are a logic "zero") upon a system reset or after power is applied to this board. Thus, the outputs are disabled, the CMOS buffer outputs are enabled and the front panel Fail LED is illuminated assuming the board configuration is set up for VMIVME-2532 compatible operation.

Table 4.3-1. Register Address and Bit Definitions

BINARY ADDRESS																	
A15 - A4			A3	A2	A1	A0											
X	X	X	X	X	0	0	DATA PORT 0 (UPPER BYTE)										
							IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8			
							I/O 31	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	I/O25	I/O 24			
X	X	X	X	X	0	1	DATA PORT 1 (MIDDLE UPPER BYTE)										
							IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0			
							I/O 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16			
X	X	X	X	X	1	0	DATA PORT 2 (MIDDLE LOWER BYTE)										
							IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8			
							I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8			
X	X	X	X	X	1	1	DATA PORT 3 (LOWER BYTE)										
							IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0			
							I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0			
Y	Y	Y	Y	Y	Y	0	BOARD ID REGISTER										
							IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8			
							0	0	0	0	0	1	0	1			
Y	Y	Y	Y	Y	Y	1	CONTROL STATUS REGISTER										
							IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0			
							TM1*	TM2*	FAIL*	NOT USED	B3H*	B2H*	B1H*	B0H*			

ADDRESS SELECTION JUMPERS JP1, JP5 (DATA)

ADDRESS SELECTION JUMPERS JP6, JP3 (CSR)

M2534/T4.3-1

CSR BIT DEFINITIONS

TM1* Set to a "zero" to disable output drivers. Set to a "one" to enable output drivers.

TM2* Set to a "zero" to enable test buffers. Set to a "one" to disable test buffers.

FAIL* Fail mode LED bit. Fail LED is on if the bit is "zero", off if it is a "one".

X is the data address headers.
Y is the CSR address headers.
B0H-B3H are used to control the output drivers when jumper JP8 selects them.

*For negative true output option, invert the data for these bits.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTRO-STATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed-circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

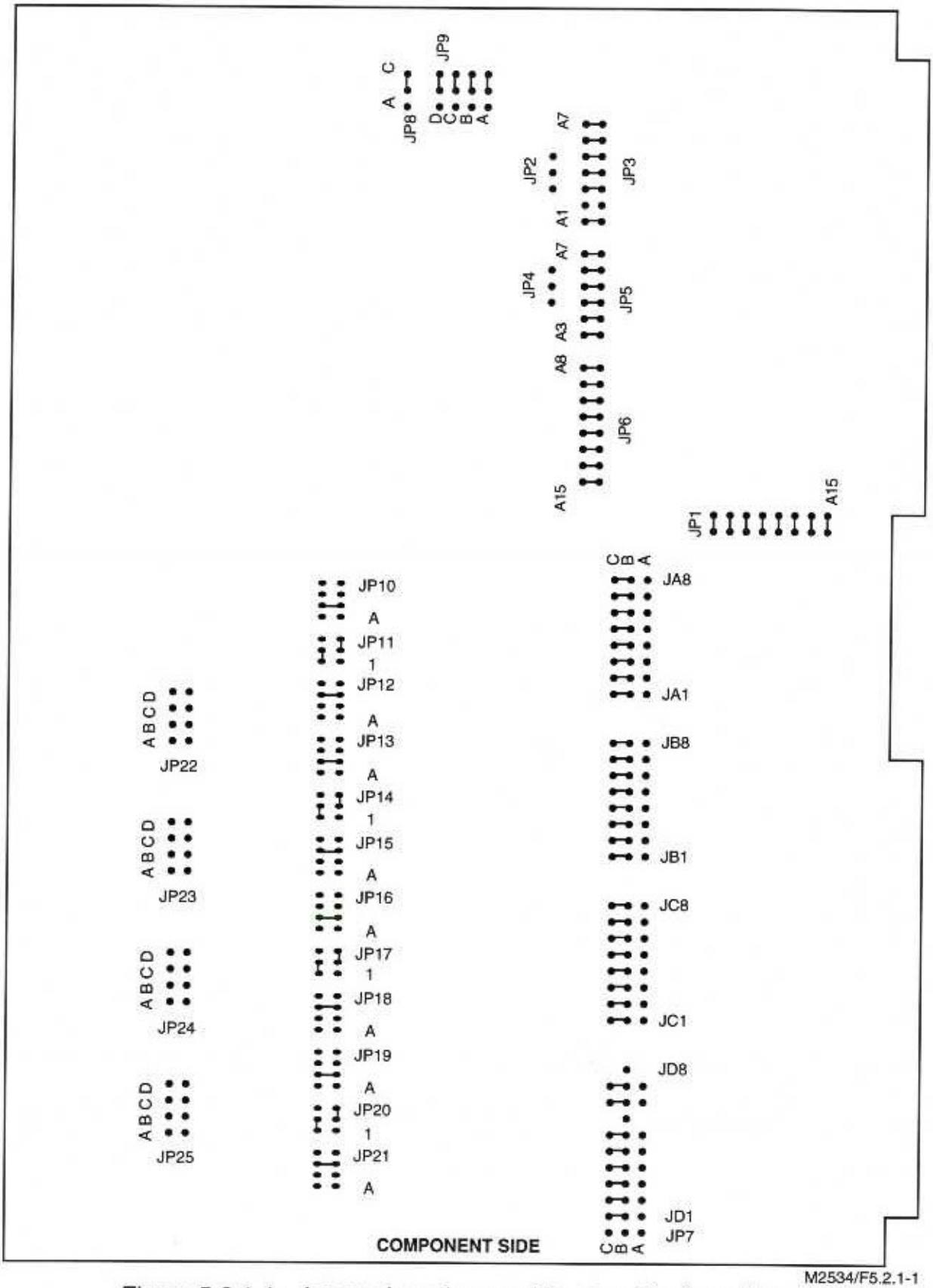
CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While insuring that the card is properly aligned and oriented in the supporting card guides, slide the card smoothly forward against the mating connector until firmly seated.

5.2.1 Installation

This section of the manual describes the various input configurations the VMIVME-2534 can utilize. The VMIVME-2534 can be set up for any particular type of input topology on a byte-by-byte basis. Figure 5.2.1-1 shows the location and factory configuration of all the jumpers used on this board. The P2 connector I/O channel assignments for this board are listed in Table 5.2.1-1, while the pin-out for the connector is shown in Figure 5.2.1-2. Table 5.2.1-2 lists the basic use of the jumpers for a particular input byte. The logic diagram (Document Number 141-002534-000) in the appendix to this manual, and Figure 5.2.1-1 should be



M2534/F5.2.1-1

Figure 5.2.1-1. Jumper Locations and Factory Configuration

Table 5.2.1-1. P2 Connector - Pin Assignments

PIN NO.	ROW A	ROW B[2]	ROW C[1]
1	CH00 HI	+5 VOLTS	CH00 LO
2	CH01 HI	GND	CH01 LO
3	CH02 HI		CH02 LO
4	CH03 HI		CH03 LO
5	CH04 HI		CH04 LO
6	CH05 HI		CH05 LO
7	CH06 HI		CH06 LO
8	CH07 HI		CH07 LO
9	CH08 HI		CH08 LO
10	CH09 HI		CH09 LO
11	CH10 HI		CH10 LO
12	CH11 HI	GND	CH11 LO
13	CH12 HI	+5 VOLTS	CH12 LO
14	CH13 HI		CH13 LO
15	CH14 HI		CH14 LO
16	CH15 HI		CH15 LO
17	CH16 HI		CH16 LO
18	CH17 HI		CH17 LO
19	CH18 HI		CH18 LO
20	CH19 HI		CH19 LO
21	CH20 HI		CH20 LO
22	CH21 HI	GND	CH21 LO
23	CH22 HI		CH22 LO
24	CH23 HI		CH23 LO
25	CH24 HI		CH24 LO
26	CH25 HI		CH25 LO
27	CH26 HI		CH26 LO
28	CH27 HI		CH27 LO
29	CH28 HI		CH28 LO
30	CH29 HI		CH29 LO/VEXT 1
31	CH30 HI	GND	CH30 LO
32	CH31 HI	+5 VOLTS	CH31 LO/VEXT 2

M2534/T5.2.1-1

NOTES:
1. External reference voltages are supplied by the user at the expense of these input channels.
2. Inputs to Board - not required.

Table 5.2.1-2. Jumper Uses

JUMPER REFERENCE	USE
JA	Row C Input Pins for Byte Offset 3
JB	Row C Input Pins for Byte Offset 2
JC	Row C Input Pins for Byte Offset 1
JD	Row C Input Pins for Byte Offset 0
JP1 AND JP5	Data Base Address
JP3 AND JP6	CSR Base Address
JP2	CSR Address Modifier
JP4	Data Address Modifier
JP7	Diode Clamp Voltage
JP8	MUX Select
JP9	Output Direction
JP10 AND JP12	Input Bias Byte Offset 3
JP11	Comparator Bias Byte Offset 3
JP13 AND JP15	Input Bias Byte Offset 2
JP14	Comparator Bias Byte Offset 2
JP16 AND JP18	Input Bias Byte Offset 1
JP17	Comparator Bias Byte Offset 1
JP19 AND JP21	Input Bias Byte Offset 0
JP20	Comparator Bias Byte Offset 0
JP22	Byte Offset 3 Clamp Diodes
JP23	Byte Offset 2 Clamp Diodes
JP24	Byte Offset 1 Clamp Diodes
JP25	Byte Offset 0 Clamp Diodes

M2534/T5.2.1-2

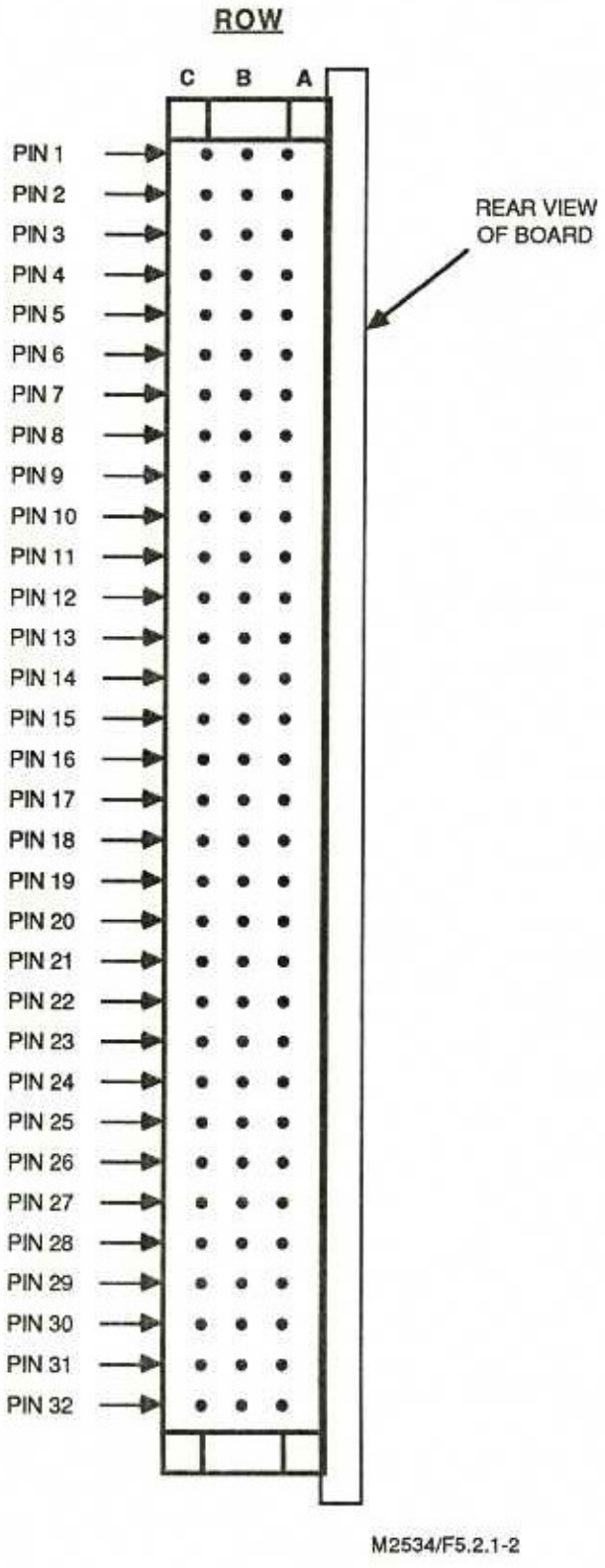


Figure 5.2.1-2. P2 Connector Pin Layout

referred to when configuring these jumpers. These jumpers will be discussed in more detail in the following sections.

5.2.2 Before Applying Power: Checklist

Before installing the board in a VMEbus system, perform the following checklist to verify that the board is ready for the intended operation:

a. Have Sections 3 and 4 on Theory and Programming of the VMIVME-2534 been read and applied to system requirements?__√__

b. Review this chapter to verify factory installation of the jumpers. __√__

   (1) To change the address jumpers refer to Section 5.3.

   (2) To change address modifier response, refer to Section 5-4.

c. The VMIVME-2534 is designed to accommodate a wide variety of input signals. Table 5.2.2-1 lists the types of inputs available, and a figure which shows a typical input jumper configuration and a typical input circuit. Once an input circuit topology has been chosen use Table 5.2.2-1 to find the figure which shows how to configure the jumpers and SIPs for that input byte. Copies of Figure 5.6-4, pp. 5-22, can be used to record these configurations. Then record the value of the pull-up resistor in Table 5.2.2-2. __√__

After completing the check list above, the VMIVME-2534 board may be installed. (Do not install or remove the board with power ON unless the power-on replacement option has been ordered.) Generally the VMIVME-2534 may be installed in any slot position, except slot "one", which is usually reserved for the system controller processing unit.

CAUTION

THE FIGURE INDICATED IN TABLE 5.2.2-1 WILL SHOW THE CONFIGURATION FOR BYTE OFFSET 3 BIT 0, IN OTHER WORDS, INPUT CHANNEL 0. THESE FIGURES ARE HERE AS A GUIDE TO HELP THE USER IN CHOOSING THE PROPER CIRCUIT AND THEN CONFIGURING THE JUMPERS AND RESISTOR SIPS FOR THE ASSOCIATED INPUT BYTE. THE REST OF THE INPUT BYTES ARE CONFIGURED IN A SIMILAR MANNER

5.3 ADDRESS SELECTION JUMPERS

Address selection jumpers are provided on the VMIVME-2534 to select the data port's and the CSR's base addresses. See Figure 5.2.1-1 for the jumper locations. The data port device address is jumpered by the factory as shown in Figure 5.3.1-1. The CSR base address is jumpered by the factory as shown in Figure 5.3.1-2.

Table 5.2.2-1. Input Circuit Configuration

TYPE OF INPUT CIRCUIT	FIGURE NUMBER
a. Differential Inputs	5.5-1
b. Current sinking; positive true	5.5-2
c. Contact closure; positive true	5.5-3
d. Contact closure; negative true	5.5-4
e. Voltage sourcing; positive true	5.5-5
f. Voltage sourcing; negative true	5.5-6
g. Voltage sourcing; TTL compatable positive true	5.5-7
h. Voltage sourcing; TTL compatable negative true	5.5-8

M2534/T5.2.2-1

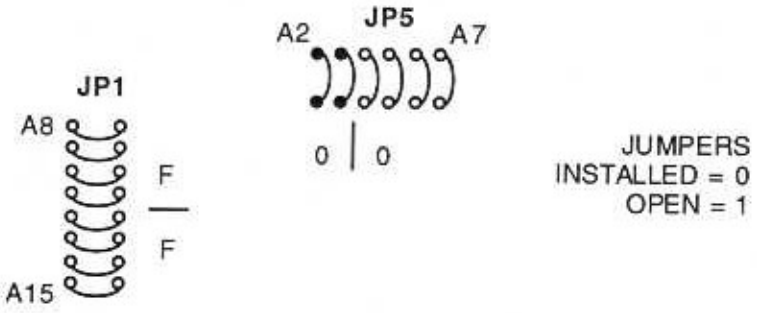
Table 5.2.2-2. Pullup/Pulldown Resistor Installation Sheet

INPUT CHANNEL	PULL UP RESISTOR	PULL DOWN RESISTOR
00 → 07	RP17 Value = ** Value =	RP13 Value = 33k* Value =
08 → 15	RP18 Value = ** Value =	RP14 Value = 33k* Value =
16 → 23	RP19 Value = ** Value =	RP15 Value = 33k* Value =
24 → 31	RP20 Value = ** Value =	RP16 Value = 33k* Value =

*This is the factory selection.

M2534/T5.2.2-2

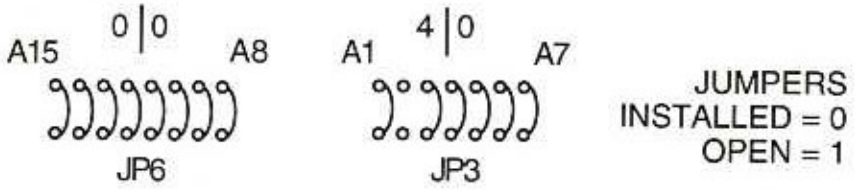
**This value depends on the option ordered.



The example shown is for a base address of 0000.

M2534/F5.3.1-1

Figure 5.3.1-1. Data Port Address Select Jumpers



The example shown is for a base address of 0004.

M2534/F5.3.1-2

Figure 5.3.1-2. CSR Select Jumpers

5.4 ADDRESS MODIFIERS

The VMIVME-2534 is configured at the factory to respond to short supervisory I/O access (no jumpers installed for AM2). This configuration can be changed by installing jumpers at JP2 and/or at JP4. These jumpers are the address modifier jumpers (AM2). The jumper JP4 is used by the data registers, and JP2 is used by the CSR. They can be configured, such that the board will respond to short supervisory (AM2 not installed), or to short non-privileged (AM2 installed to the right) or to either I/O access (AM2 installed to the left). See Figure 5.4-1 for the jumper positions.

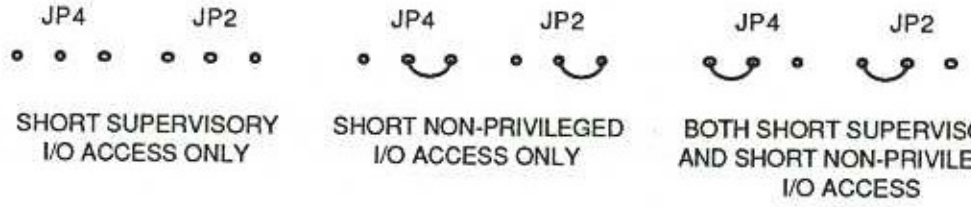


Figure 5.4-1. Address Modifier Selections

5.5 INPUT SIGNAL CONDITIONING SELECTION

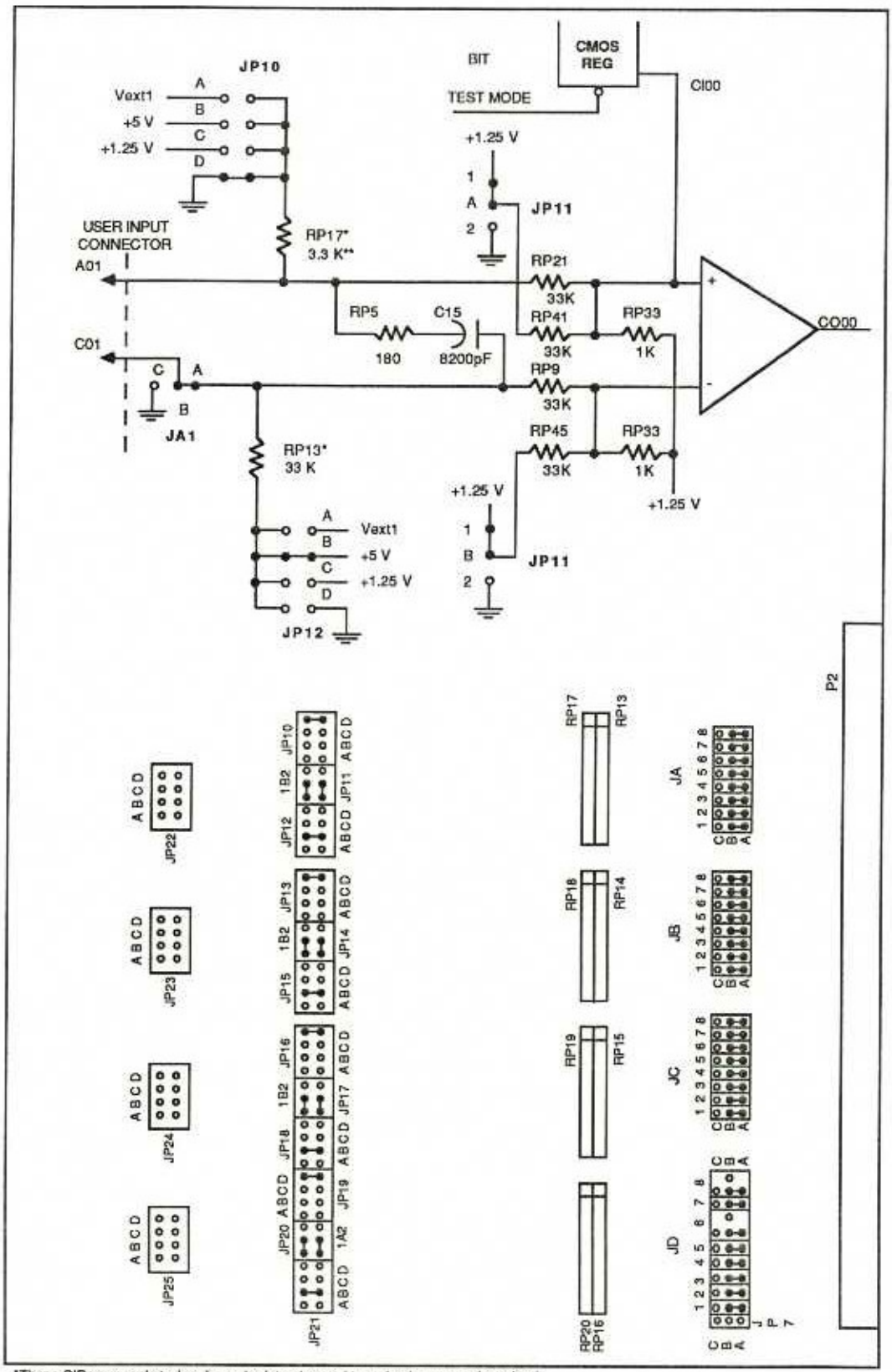
The input circuitry of the VMIVME-2534 allows the user to select the kind of input conditioning he wishes to have without specifying it when ordering. The input circuits can be changed to meet changing needs. Table 5.2.2-1 and Figures 5.5-1 through 5.5-8 at the end of this chapter are guides to help in the configuration of this board.

These figures show only one typical input circuit for a particular topology, but they are applicable to all inputs. The uses of the jumpers on the board are listed in Table 5.2.1-2. The figures will show the reference designators for the jumpers and SIPs for input channel 00. The logic diagram will have to be consulted for the remaining reference designators of any other input channel. These jumpers and SIPs listed work for an entire byte of inputs. Thus, the figures in this section are shown for only input channel 00, but they are used by all the inputs of byte offset 3 (channels 00 through 07).

Once an input circuit topology has been decided upon, refer to Table 5.2.2-1 to find the figure showing this circuit. Using the apporpriate figure, the logic diagram, and Table 5.2.1-2 identify the jumper and SIP reference designators of interest. Next, using copies of Figure 5.5-1, pp. 5-11, note the configuration for any particular byte on this board. This way the board's final configuration is documented and can be easily located if needed.

5.6 EXTERNAL PULLUP/THRESHOLD VOLTAGE

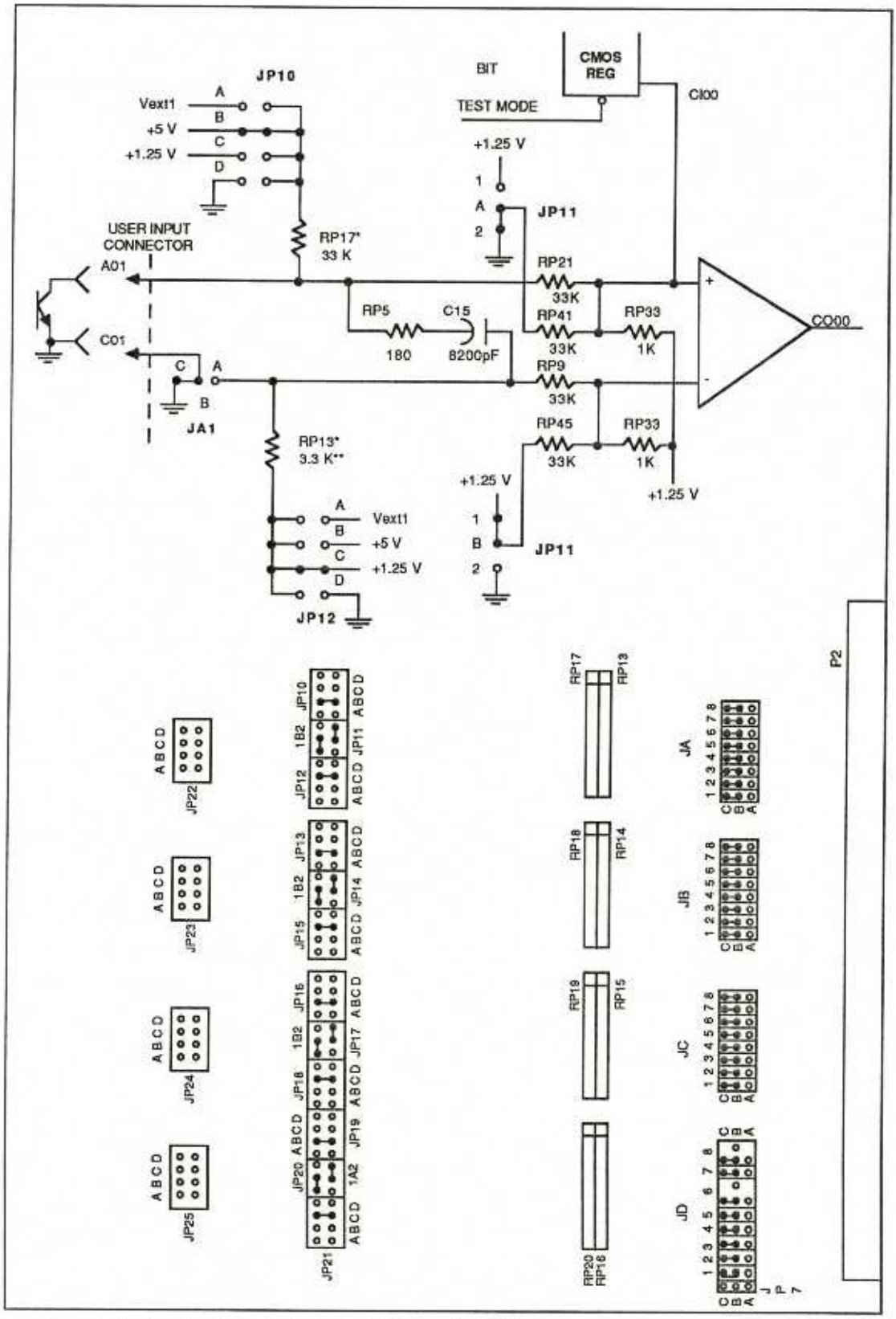
External voltage for the VMIVME-2534 is selected by jumpers JD6 and JD8. The external voltage is brought to the board via the P2 connector at the expense of either the CH29 and/or CH31 channel's inputs (their outputs are not effected). The external voltages can have two different values. One of these voltages goes to the input bias SIP resistors (RP13 through RP20) and the other goes to the inductive flyback diodes of the output driver chips via jumpers JP22 through JP25. This way the user can have one voltage for the input circuits and a different voltage for the output driver diodes. The jumper setup to use the local (on board) +5 V for the output driver's clamp voltage is shown in Figures 5.6-1. Figures 5.6-2 and 5.6-3 show the different configurations for bringing in the external voltages. Figure 5.6-4 is a block diagram showing these jumpers and their use on the board.



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-1

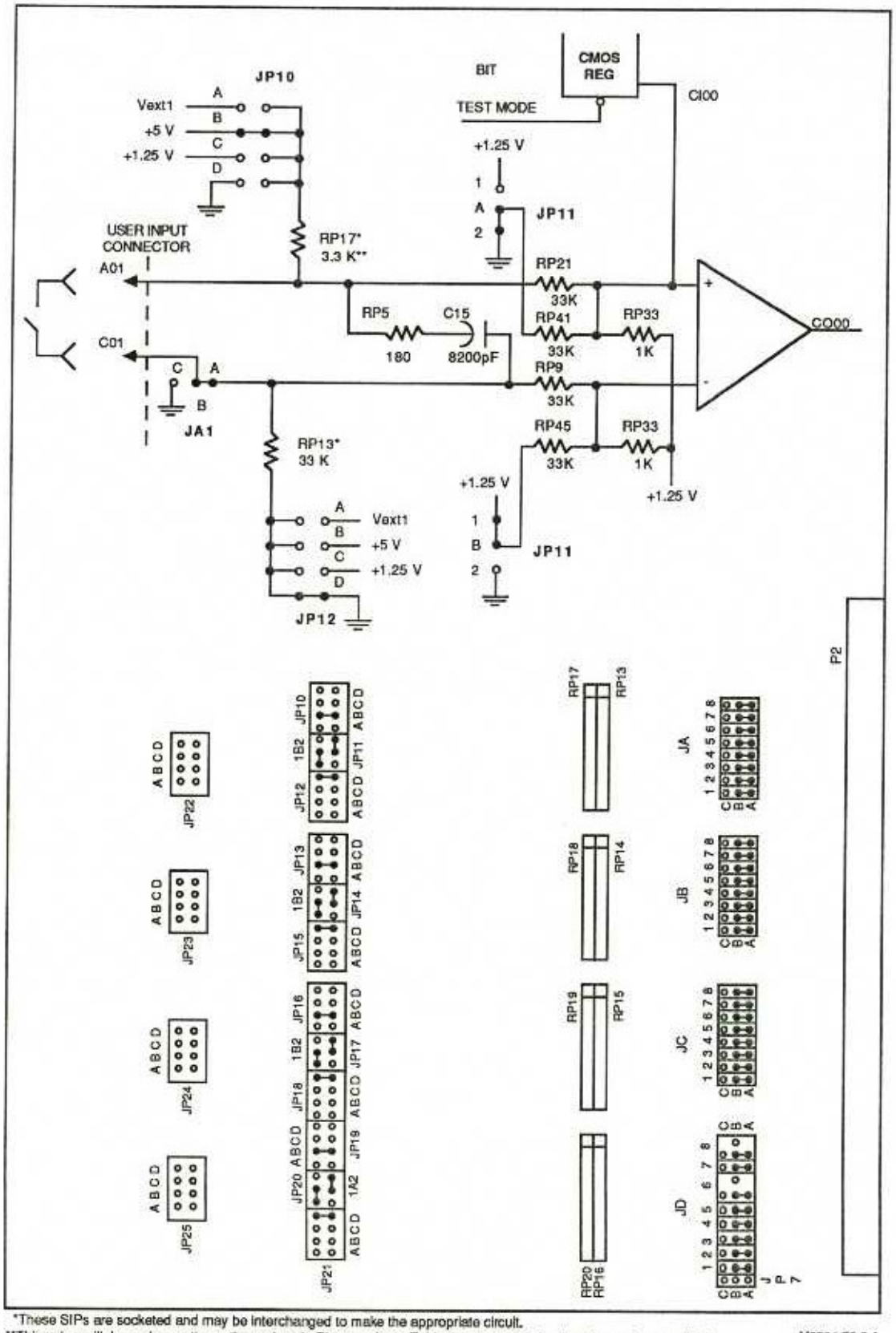
Figure 5.5-1. Jumper Configuration and Typical Input Circuit for Differential Inputs



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-2

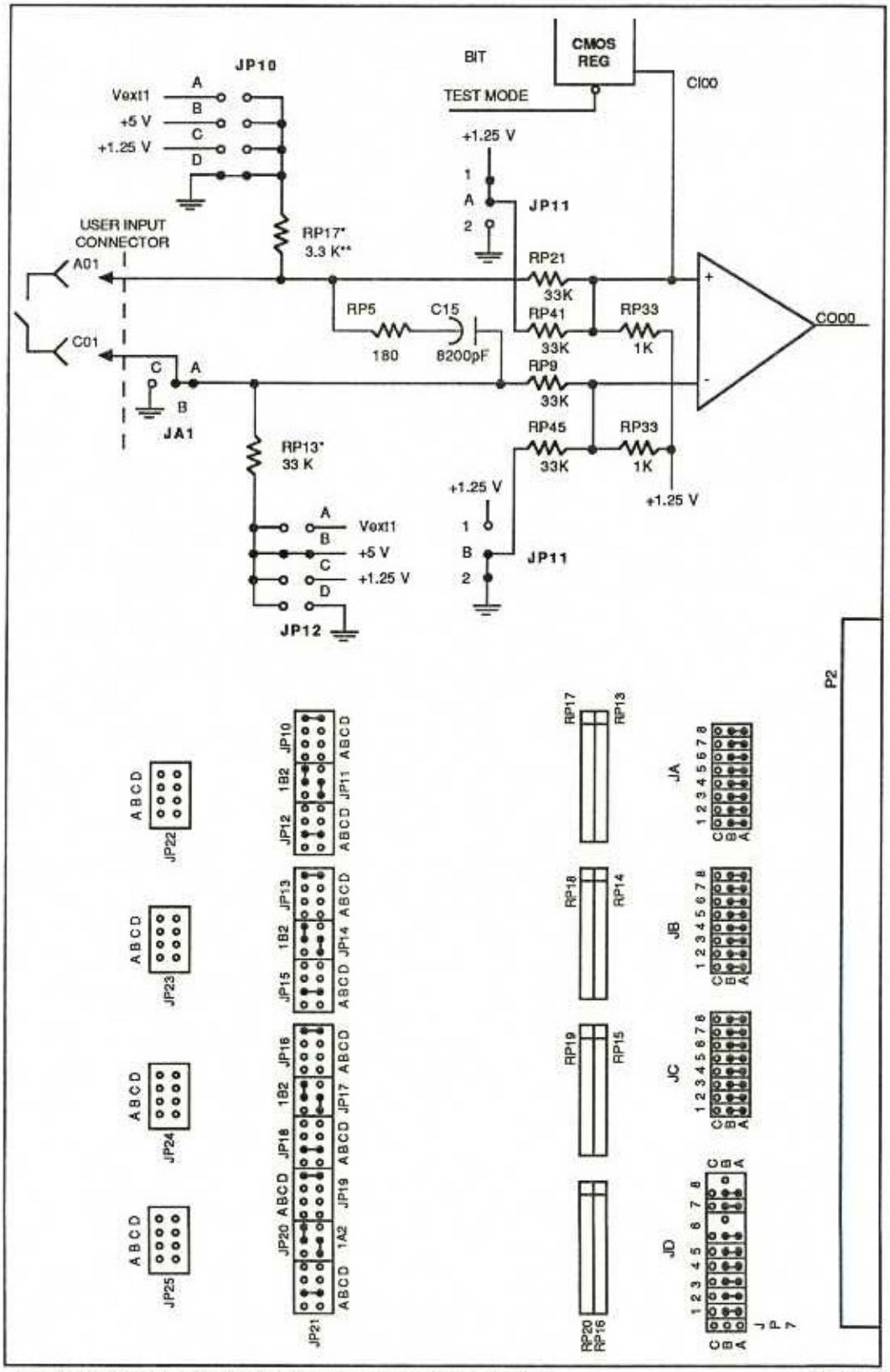
Figure 5.5-2. Jumper Configuration and Typical Input Circuit for Current Sink, Pos True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-3

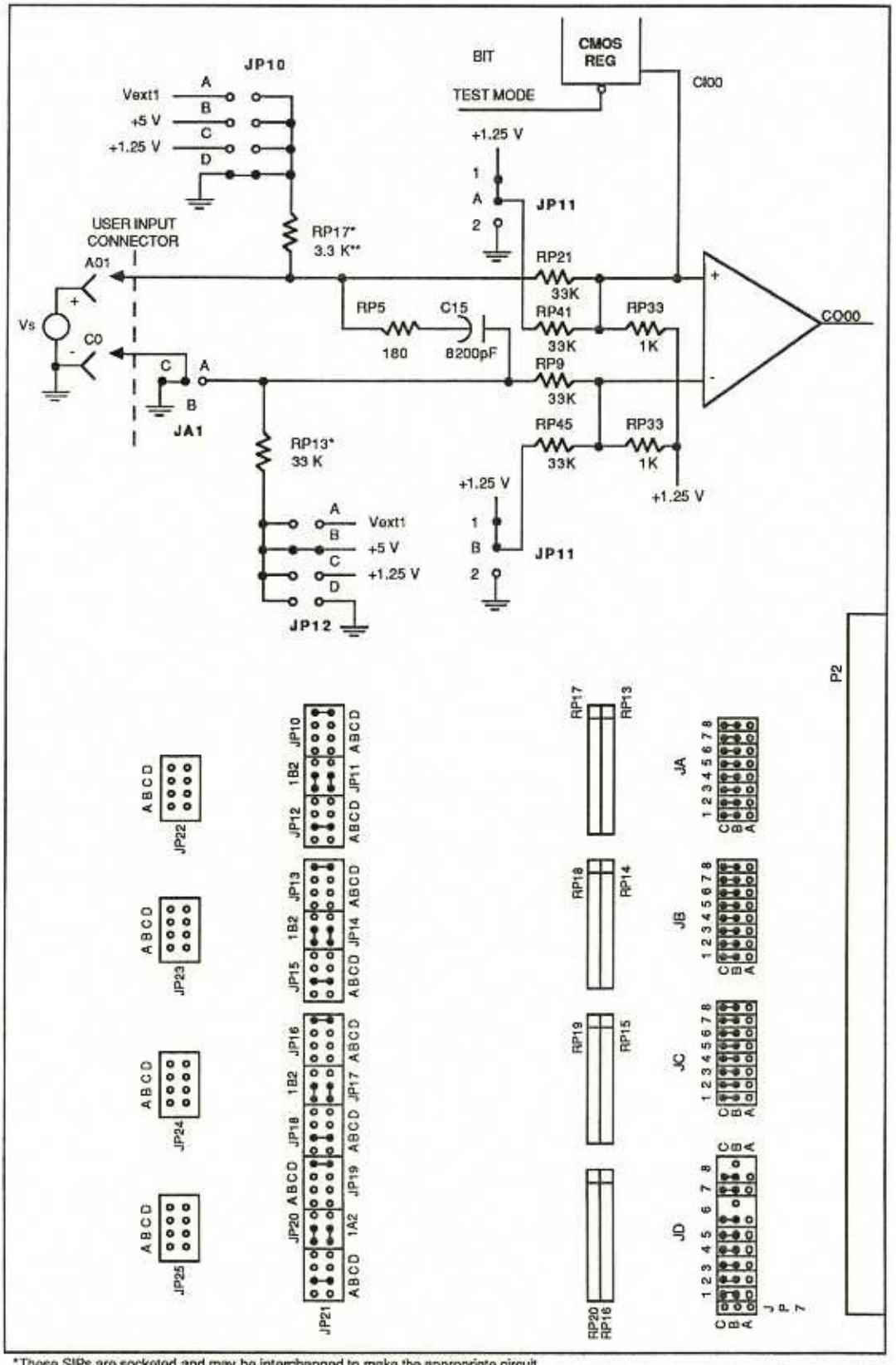
Figure 5.5-3. Jumper Configuration and Typical Input Circuit for Contact Closure, Pos True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-4

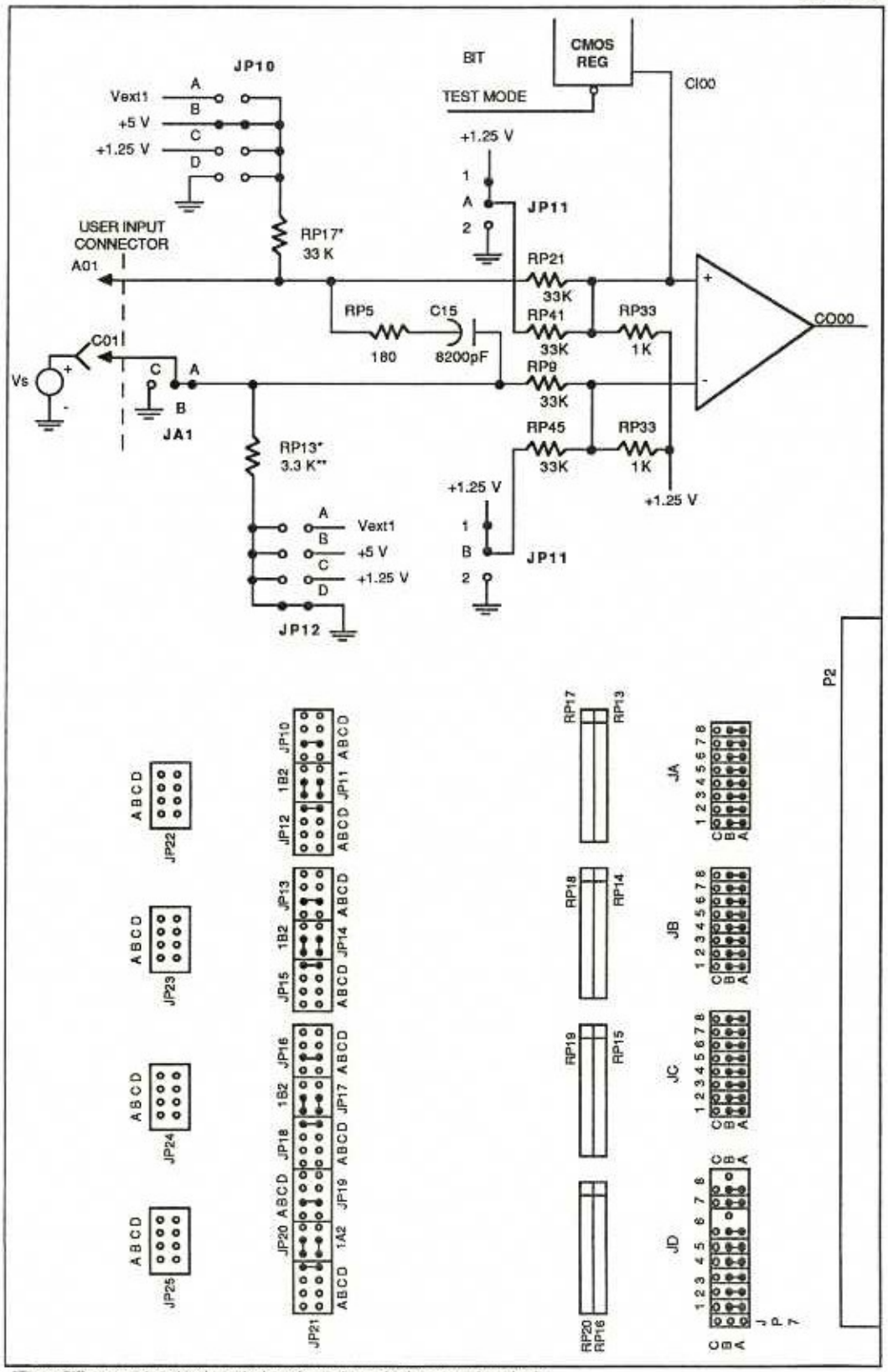
Figure 5.5-4. Jumper Configuration and Typical Input Circuit for Contact Closure, Neg True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-5

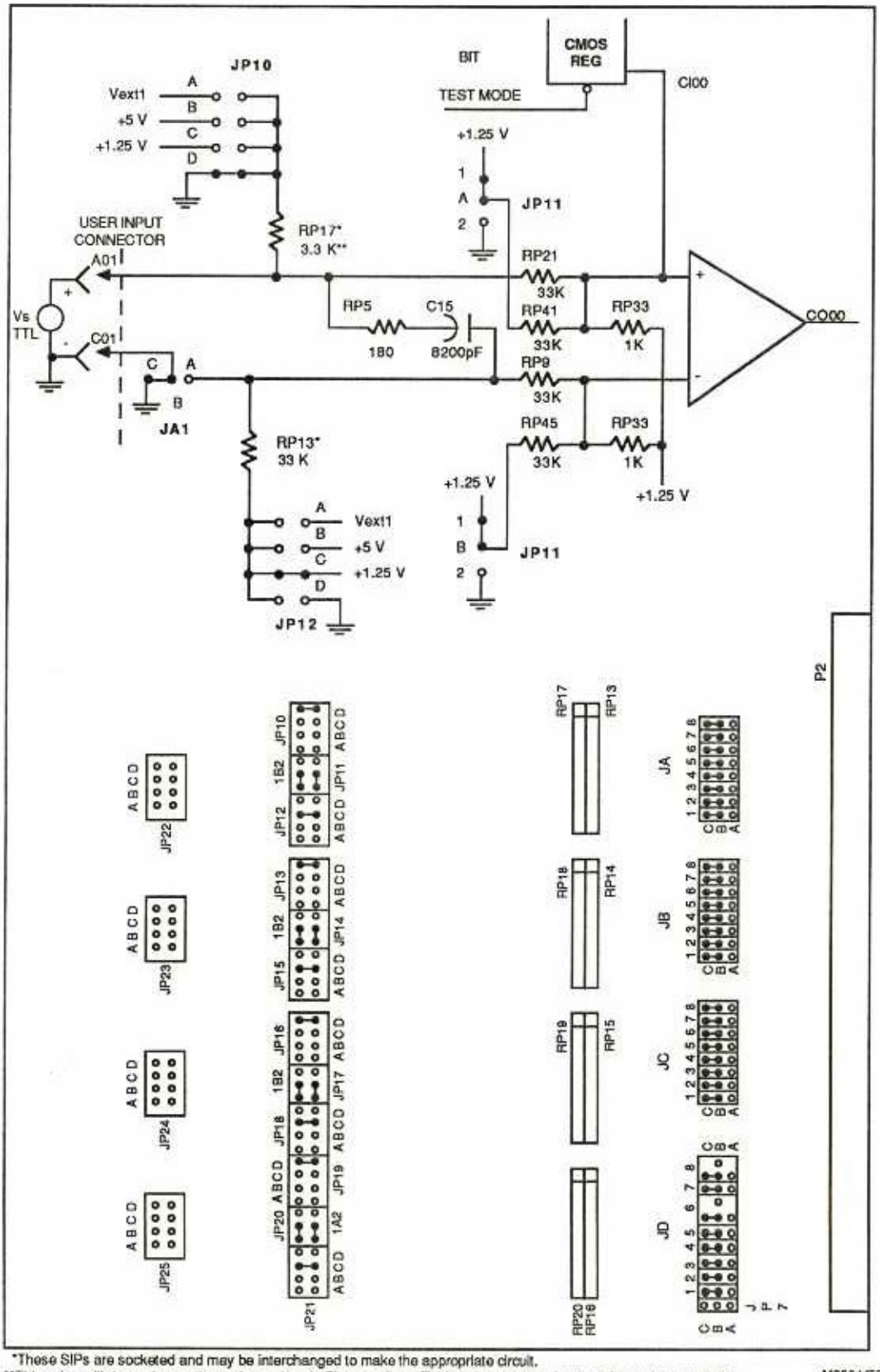
Figure 5.5-5. Jumper Configuration and Typical Input Circuit for Voltage Sourcing, Pos True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-6

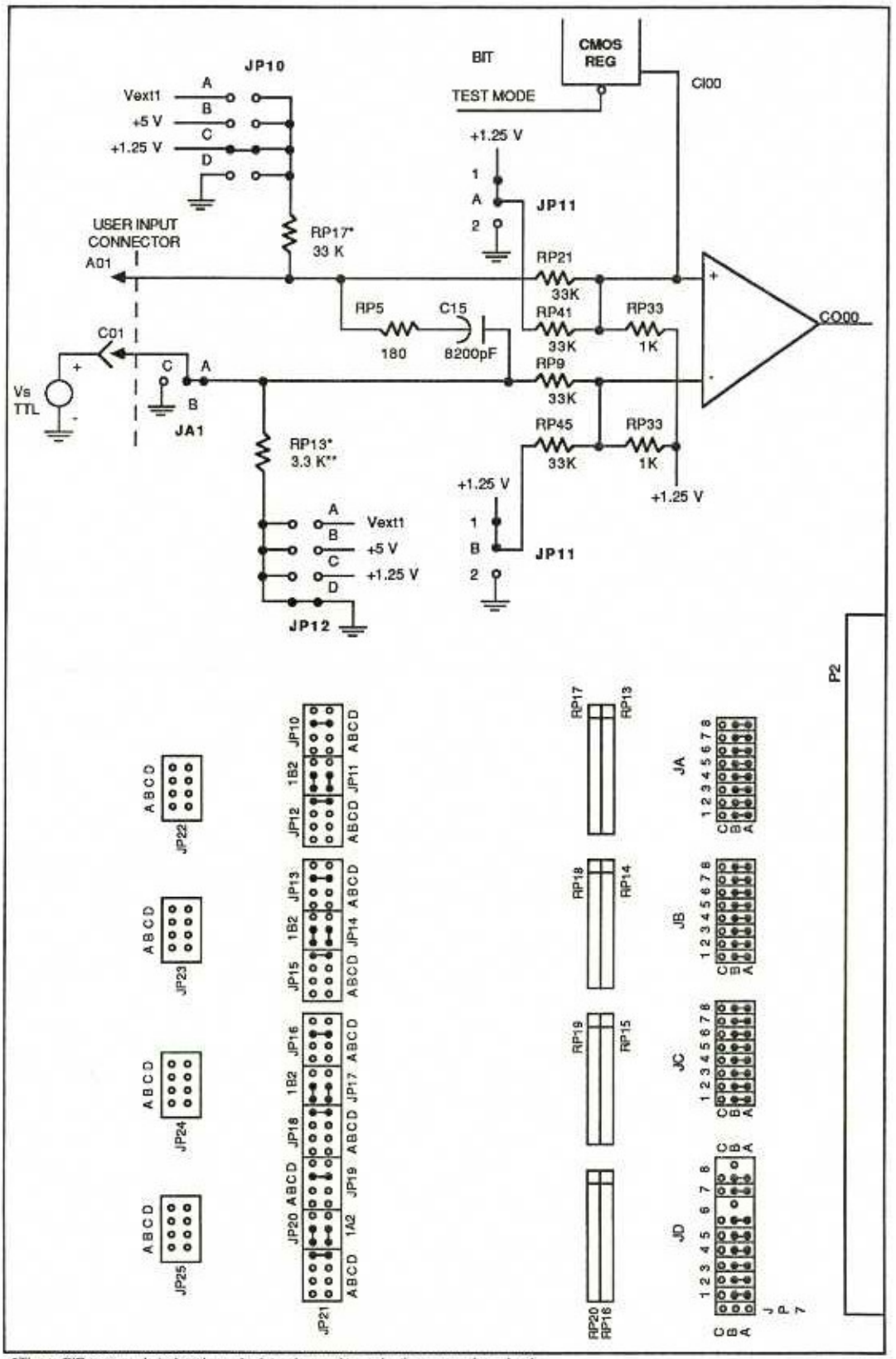
Figure 5.5-6. Jumper Configuration and Typical Input Circuit for Voltage Sourcing, Neg True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-7

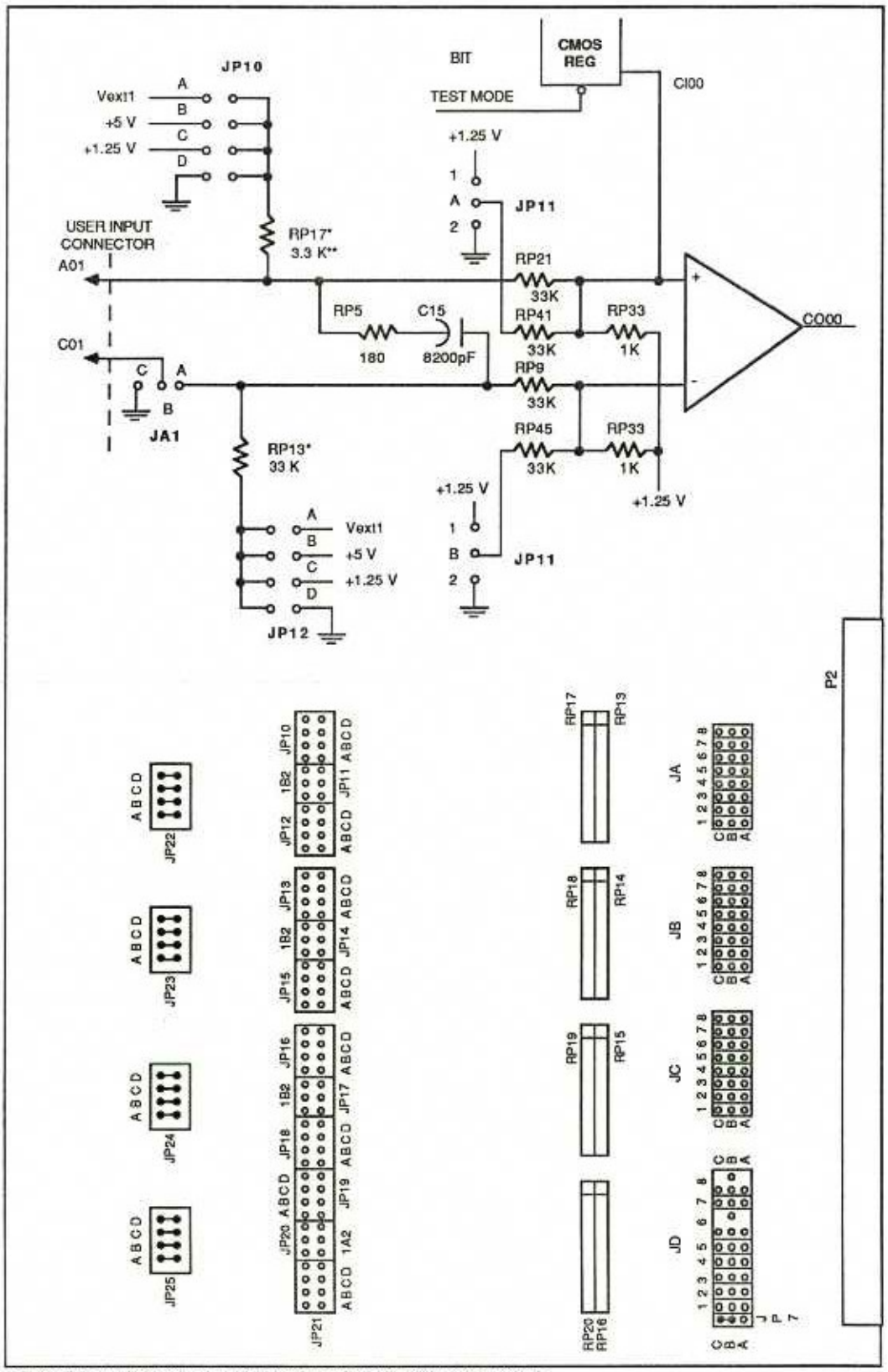
Figure 5.5-7. Jumper Configuration and Typical Input Circuit for Voltage Sourcing, TTL Pos True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.5-8

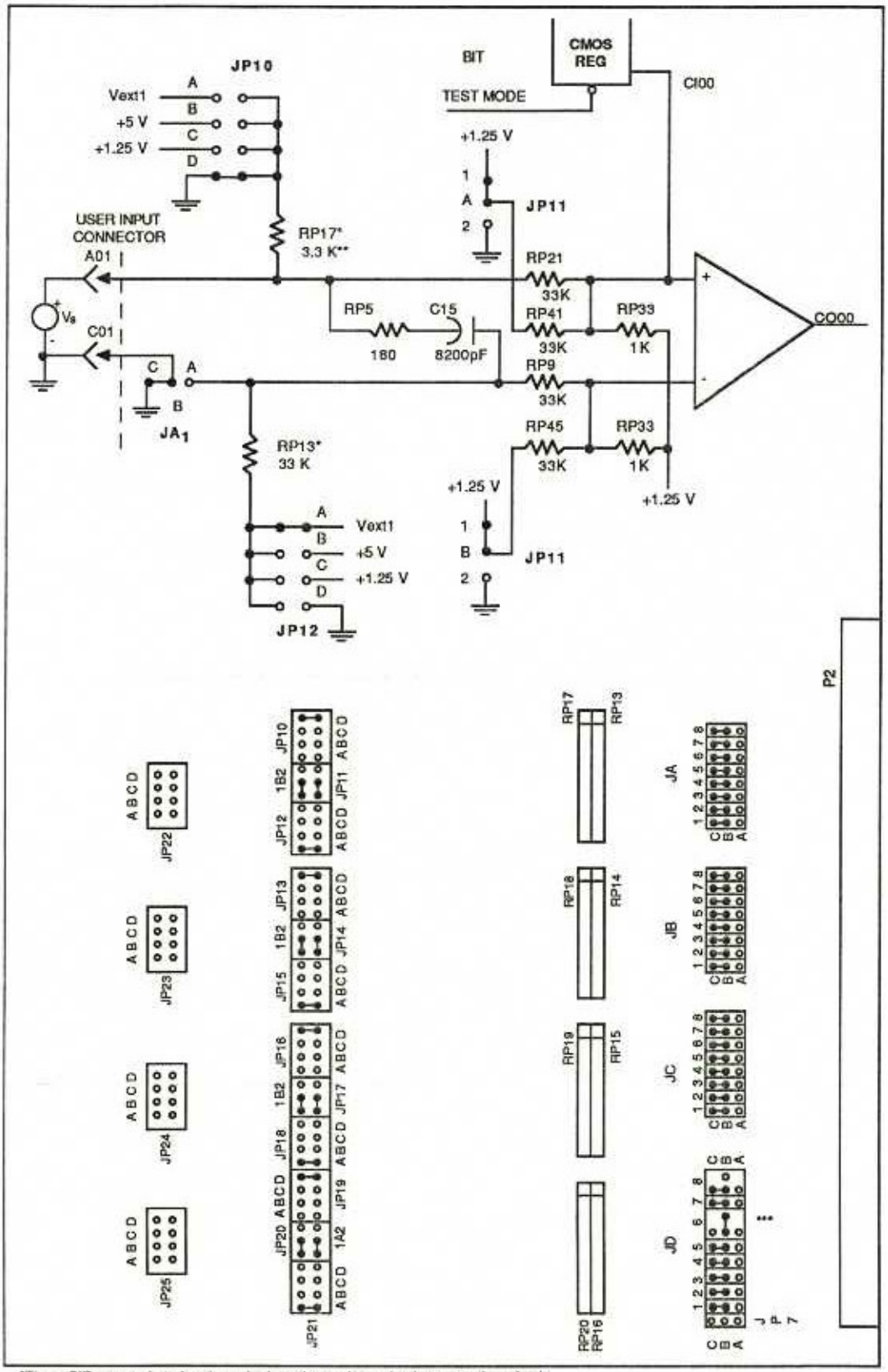
Figure 5.5-8. Jumper Configuration and Typical Input Circuit for Voltage Sourcing, TTL Neg True



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

M2534/F5.6-1

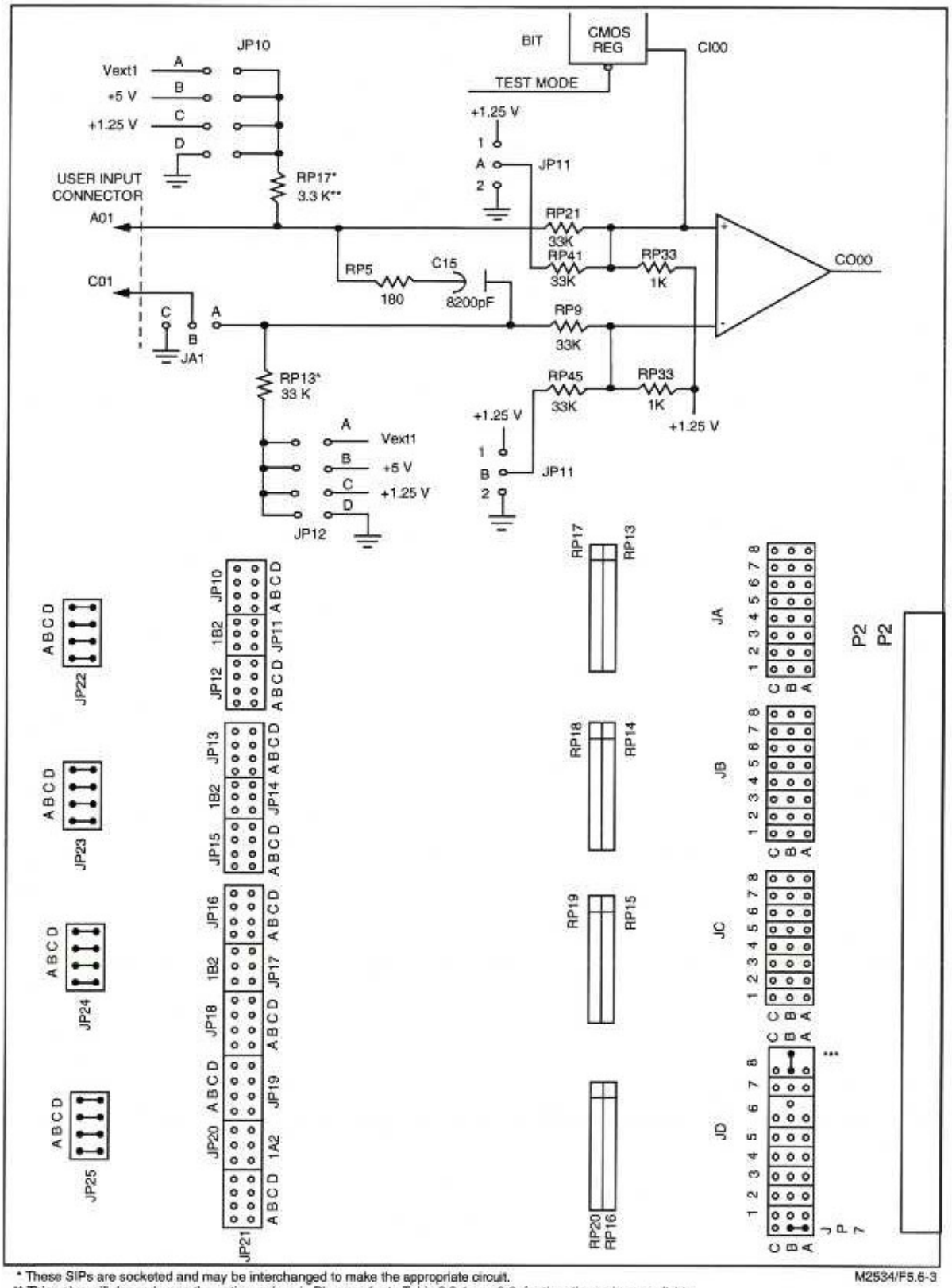
Figure 5.6-1. Jumper Configuration for On Board +5 V Diode Clamp Voltage



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.
***Input Channel 29 is generally not available when this jumper is in this position, refer to Section 5.6 for a complete explanation.

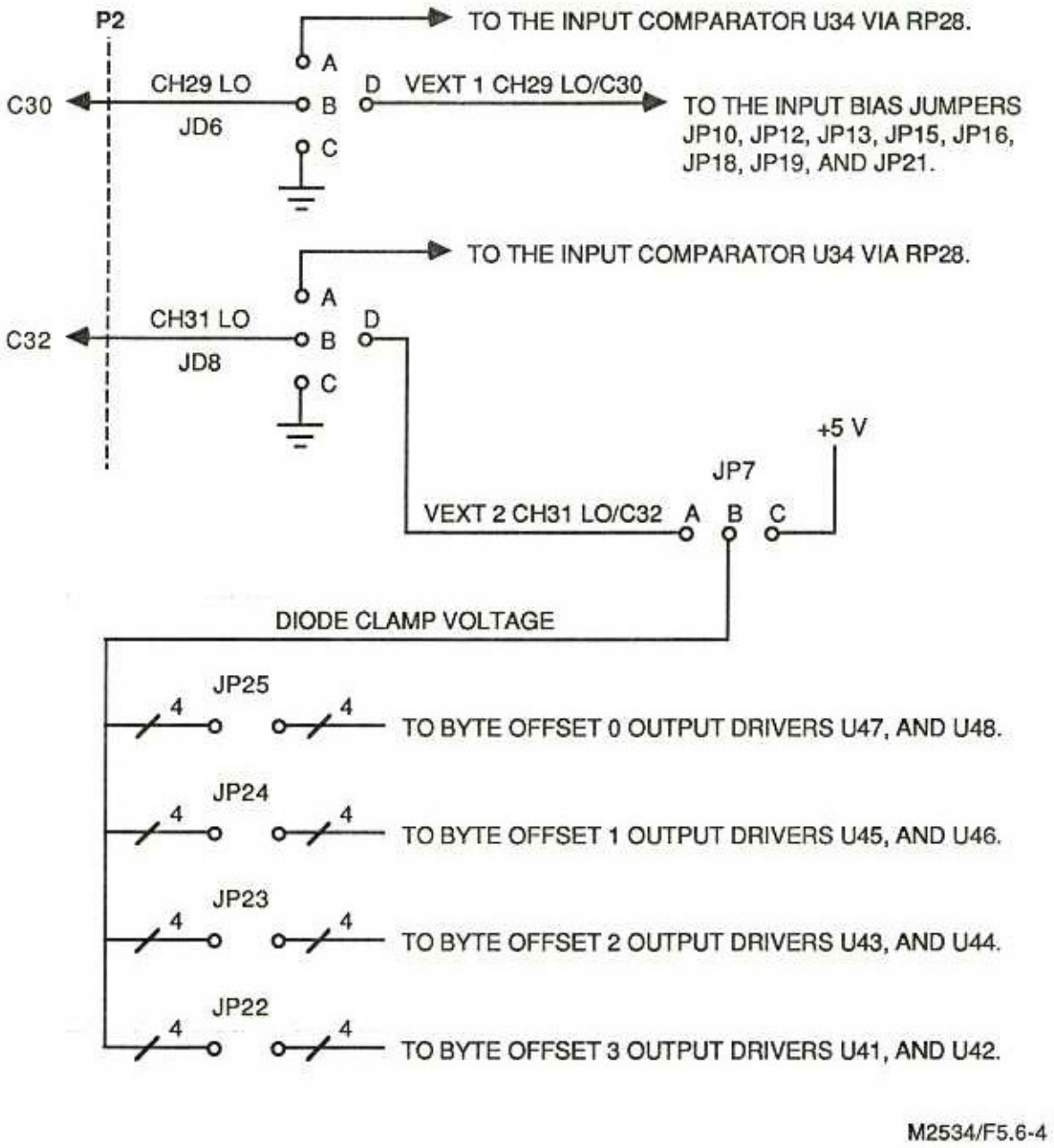
M2534/F5.6-2

Figure 5.6-2. Jumper Configuration for Voltage Sourcing Pos True Using External Voltage



* These SIPs are socketed and may be interchanged to make the appropriate circuit.
** This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.
*** Input channel 31 is not available when this jumper is in this position, refer to Section 5.6 for a complete explanation.

Figure 5.6-3. Jumper Configuration for External Diode Clamp Voltage



M2534/F5.6-4

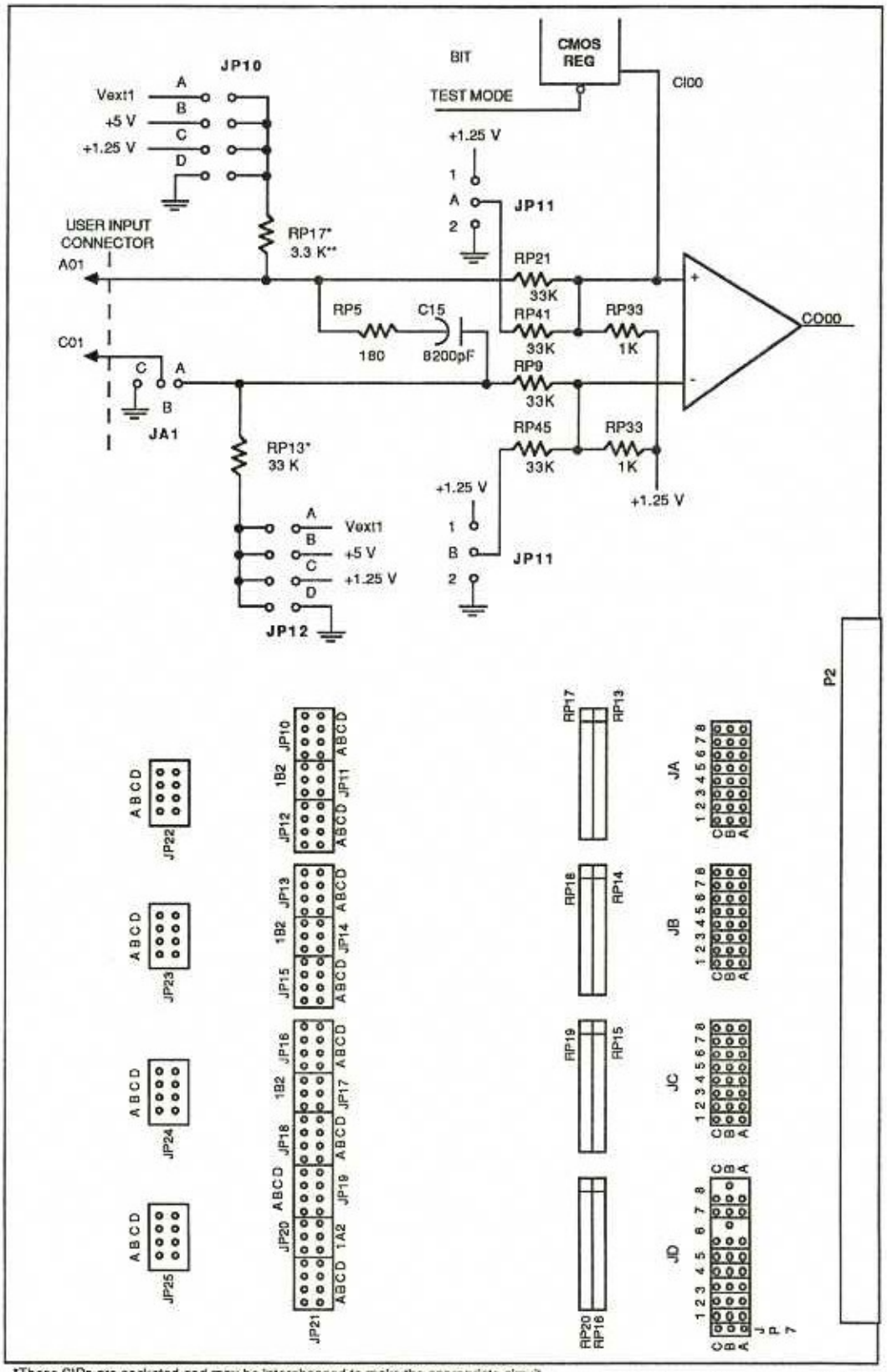
Figure 5.6-4. External Voltage Jumper Definitions

The external voltages come into the board via the P2 connector. The input bias voltage (V EXT 1) uses the CH29 LO line P2 pin C30. With this line jumpered to accept the external voltage, this input should not be used except under certain circumstances. Refer to Figure 5.6-2 for the jumper positions used by voltage source inputs with external voltage. Using the voltage sourcing configuration for this drawing is for convenience only. External voltage can be used with any input topology chosen. The appropriate input bias jumpers can then be jumpered to use V EXT 1 for their bias voltage. The flyback diode voltage (V EXT 2) uses the CH31 LO line P2 pin C32. With this line jumpered to accept the external voltage, this input should not be used except under certain circumstances. The diode jumpers JP22 through JP25 can then be installed to select this voltage. The flyback diodes must also have jumper JP7 positioned to use the external voltage. Please refer to Figure 5.6-3 and the logic diagram in Appendix A of this manual for the particular location and usage of these jumpers. Figure 5.6-4 is a block diagram showing the uses of these jumpers. Figure 5.6-5 is a blank form of the board. Use copies of this page to document the final configuration chosen for the particular bytes of this board.

Under certain circumstances the input channels that are used to bring in the external voltages may be able to perform input functions. These conditions apply to both channels. First, the input function (or circuit topology) must not require the use of P2 Pin C. Examples: The differential and the voltage sourcing negative true inputs violate this rule and the input cannot be used. Second, the signal return ***MUST*** route through the VMEbus chassis ground. If both of these conditions can be met, as well as any others previously mentioned, the input can be used to process data while its jumper brings in some external voltage.

Once these choices have been made, the input bias networks must still select this voltage via their input bias jumpers (JP10, JP12, JP13, JP15, JP16, JP18, JP19, and JP21). This is on a byte-by-byte basis. This means that some of the inputs can use +5 V while others use the external voltage. However, care must be exercised when using the external voltage to prevent excessive power being dissipated in the SIP resistors that make up the input bias network. The smaller resistor's voltage drop must not exceed the power rating of the SIP (0.125 W). Please refer to the VMIVME-2534 Specification Document No. 800-002534-000 for the values of the maximum external voltage for a particular pull-up resistor value.

The SIPs and jumpers called out in the previous figures (Figures 5.5-1 through 5.5-8) are for byte offset 3 bit 0, in other words input channel 00. Refer to the logic diagram in Appendix A of this manual to find the reference designators for the particular byte of interest. These reference designators can be obtained by leafing through the schematic and noting them. Figure 5.6-4 is a blank jumper configuration sheet. It is provided for the user to make copies of and mark with the jumper configuration chosen for a particular input byte. The board is shipped from the factory configured as current sinking positive true inputs.



*These SIPs are socketed and may be interchanged to make the appropriate circuit.
**This value will depend upon the option ordered. Please refer to Table 2.2-1, pp. 2-9, for the other values available.

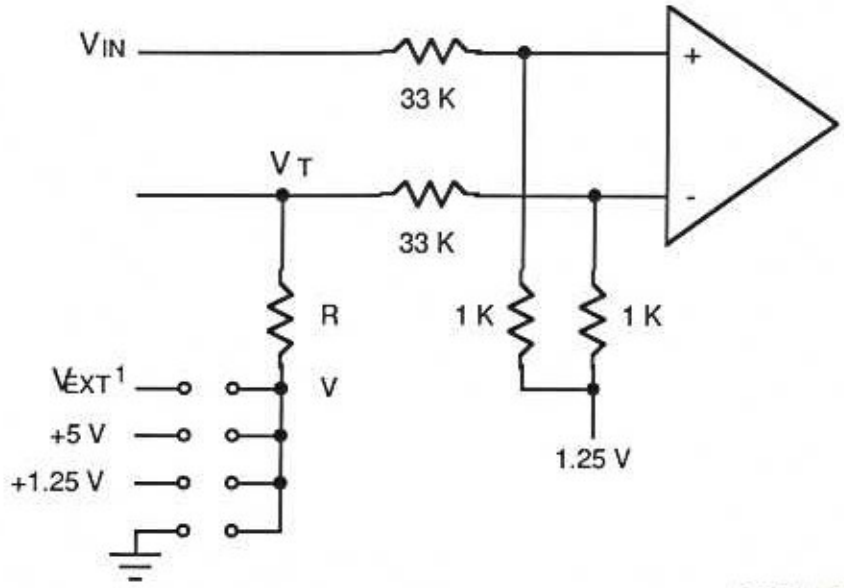
M2534/F5.6-5

Figure 5.6-5. Jumper Configuration and Typical Input Circuit Chosen

Note that the threshold voltage will be equal to approximately one-half of the external voltage, (plus 1.25 V) providing that it is applied through the 33 K ohm SIP resistor. However, if the external voltage is applied through the 3.3 K ohm SIP, the threshold voltage will be equal to 0.92 times the external voltage. The circuit for this threshold voltage is shown in Figure 5.6-6. Some threshold voltages for various external voltages are listed in Tables 5.6-1 through 5.6-7. These tables are based upon the possible values for the threshold resistor (labled R in Figure 5.6-6). Each of these tables contains the voltage equation used to derive these values. However, these tables are valid only if the input configuration is for any of the single-ended circuits. They are ***NOT*** valid for the differential input topology.

5.7 TEST MODE SELECTION

The VMIVME-2534 is shipped from the factory to behave like the VMIVME-2532. This means that the test modes used by the VMIVME-2532 are implemented in the VMIVME-2534. A detailed explanation of how this is done is given in Section 3.5 of this manual. Jumper JP8 is used to select between programmable I/O control or VMIVME-2532 compatible behavior. It is shipped in the VMIVME-2532 compatible position. Jumper JP9 is used to set up a particular byte for input only operations or VMIVME-2532 compatible I/O under the control of the test mode bit 1. This jumper is also configured at the factory in the VMIVME-2532 compatible positions. Test Mode 2 still controls the CMOS test buffers, as it does in the VMIVME-2532.



M2534/F5.6-6

Figure 5.6-6. Threshold Voltage Diagram

Table 5.6-1. Threshold Voltages for R = 3.3 k Ohms

Vt = [(V-1.25) (.91)] + 1.25

V	Vt
0 V *	1.22 V
1.25 V	1.25 V
5 V	4.7 V
12 V	11 V
24 V	22 V
28 V	25.6 V
48 V	43.8 V
66 V	60.2 V

M2534/T5.6-1

Table 5.6-2. Threshold Voltages for R = 33 k Ohms

Vt = [(V-1.25) (.51)] + 1.25

V	Vt
0 V *	1.23 V
1.25 V	1.25 V
5 V	3.2 V
12 V	6.7 V
24 V	12.9 V
28 V	14.8 V
48 V	25.1 V
66 V	34.3 V

M2534/T5.6-2

*These threshold voltages were calculated for Vt at the minus input to the comparator, because when V< 1.25 V the threshold voltage becomes a function of the 1.25 V comparator bias voltage only, and the voltage at the minus input is the threshold voltage.

Table 5.6-3. Threshold Voltages for R = 270 Ohms

Vt = [(V-1.25) (.99)] + 1.25

V	Vt
0 V *	1.21 V
1.25 V	1.25 V
5 V	4.9 V
12 V	11.9 V
24 V	23.8 V
28 V	27.8 V
48 V	47.6 V
66 V	65.5 V

M2534/T5.6-3

Table 5.6-4. Threshold Voltages for R = 560 Ohms

Vt = [(V-1.25) (.98)] + 1.25

V	Vt
0 V *	1.21 V
1.25 V	1.25 V
5 V	4.9 V
12 V	11.9 V
24 V	23.6 V
28 V	27.6 V
48 V	47.2 V
66 V	65.0 V

M2534/T5.6-4

Table 5.6-5. Threshold Voltages for R = 1.5 k Ohms

Vt = [(V-1.25) (.96)] + 1.25

V	Vt
0 V *	1.22 V
1.25 V	1.25 V
5 V	4.8 V
12 V	11.6 V
24 V	23.0 V
28 V	26.9 V
48 V	46.0 V
66 V	63.3 V

M2534/T5.6-5

Table 5.6-6. Threshold Voltages for R = 6.8 k Ohms

Vt = [(V-1.25) (.83)] + 1.25

V	Vt
0 V *	1.22 V
1.25 V	1.25 V
5 V	4.4 V
12 V	10.2 V
24 V	20.2 V
28 V	23.5 V
48 V	40.2 V
66 V	55.2 V

M2534/T5.6-6

Table 5.6-7. Threshold Voltages for R = 27 k Ohms

Vt = [(V-1.25) (.56)] + 1.25

V	Vt
0 V *	1.23 V
1.25 V	1.25 V
5 V	3.3 V
12 V	7.2 V
24 V	13.9 V
28 V	16.2 V
48 V	27.3 V
66 V	37.3 V

M2534/T5.6-7

*These threshold voltages were calculated for V at the minus input to the comparator, because when V< 1.25 V the threshold voltage becomes a function of the 1.25 V comparator bias voltage only, and the voltage at the minus input is the threshold voltage.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC