VMIVME-3119
16-Channel, 16-bit Scanning Analog-to-Digital Board with Programmable Gain and Filter

Product Manual

A GE Fanuc Company

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

500-003119-000 Rev.E

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

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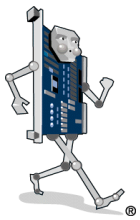

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12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

FCC STATEMENT

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy. If the equipment is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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Overview

Introduction

The VMIVME-3119 Analog Input board provides 16 high accuracy differential analog input channels with high throughput 16-bit Analog-to-Digital conversion. Each input is equipped with a dedicated Programmable Gain Amplifier (PGA), software-selectable fourth-order low pass filter, and autocalibration.

Features

The VMIVME-3119 has many unique features as listed below:

- Sixteen differential analog input channels
- Software programmable gain per channel (x1, x10, x100, and x1,000)
- Input signal range from ±10 mV to ±10 V
- Software programmable fourth-order low pass filter (1 Hz, 10 Hz, 100 Hz, 1 kHz) factory option of Bessel or Butterworth response
- Autocalibration per channel utilizing DSP technology
- 16-bit Analog-to-Digital conversion; high accuracy
- Software programmable sample rate from 305 Hz to 100 kHz aggregate, even lower rates can be obtained using prescaler
- Software programmable scan table
- Large data buffer retains up to four million data samples
- Overvoltage input protection
- Flexible triggering: internal, external, or multiboard synchronous
- VMEbus interrupts at mid scan or end scan
- Two-slot VMEbus configuration
- UIOC® capability
- Self-test
    - — Extensive on-board diagnostic testing capability
    - — Implements precision internal reference voltages
    - — Independent of field connections

Functional Description

The VMIVME-3119 has on-board autocalibration correction for offset and gain errors in real-time. Calibration correction values are determined at user-controlled calibration intervals without removing the board from the system. Individual channel correction is accomplished by DSP technology in real-time for every A / D conversion. Calibration can be verified at any time by implementing the self-test feature. Self-test uses internal precision voltages, which are applied to all channels simultaneously to verify signal path integrity.

The VMIVME-3119 can be jumper configured for either standard or extended address space, and can be jumper configured to occupy 16, 8, 4, 2, and 1 Mbyte, also 512, 256, or 128 Kbyte of address space.

The VMIVME-3119 has a software configurable sample buffer which begins at the base address of the Data RAM (address P, as shown in Table 3-1 on page 62). The size of the sample buffer determines the number of samples to be stored per scan. A user-configurable scan table determines which channels are scanned and in what order they are scanned. The sample buffer size can be configured in any power-of-2 from 1 sample to 4 Megasamples.

A functional block diagram is provided in Figure 1 on page 16.

Overvoltage and Open Input Protection

The input filter resistors provides for current limiting in the event of an overvoltage. The inputs are protected up to ±40 V sustained.

Each input LO side has a 22 MΩ resistor connected to ground. This resistor pulls an open or floating LO side to ground to keep the channel from saturating and causing crosstalk effects on adjacent channels. The HI side **does not** have a pull-down resistor. Care should be exercised in making sure this line is connected to a source or ground.

48 kHz Passive Low Pass Filter

Each input has a passive single-pole RC filter with a cut off frequency of 48 kHz. This filter is intended to limit input noise and bandwidth.

Input/BIT Switches

The field inputs and the Built-in-Test (BIT) voltages go through an analog switch. A control signal on the switch determines if the output of the switch will be the field inputs or the BIT voltages. The switch makes it possible to do BIT and calibration without having to remove the field connections. Also, the BIT voltages follow the same path as the field inputs right at the front panel connector ensuring any component error in the signal path will be corrected. The output of this switch drives the Programmable Gain Amplifier.

Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) provides differential to signal-ended conversion, common-mode rejection, and selectable gains of 1, 10, 100, and 1,000. The gain is user programmable. The output of the PGA drives the active filter.

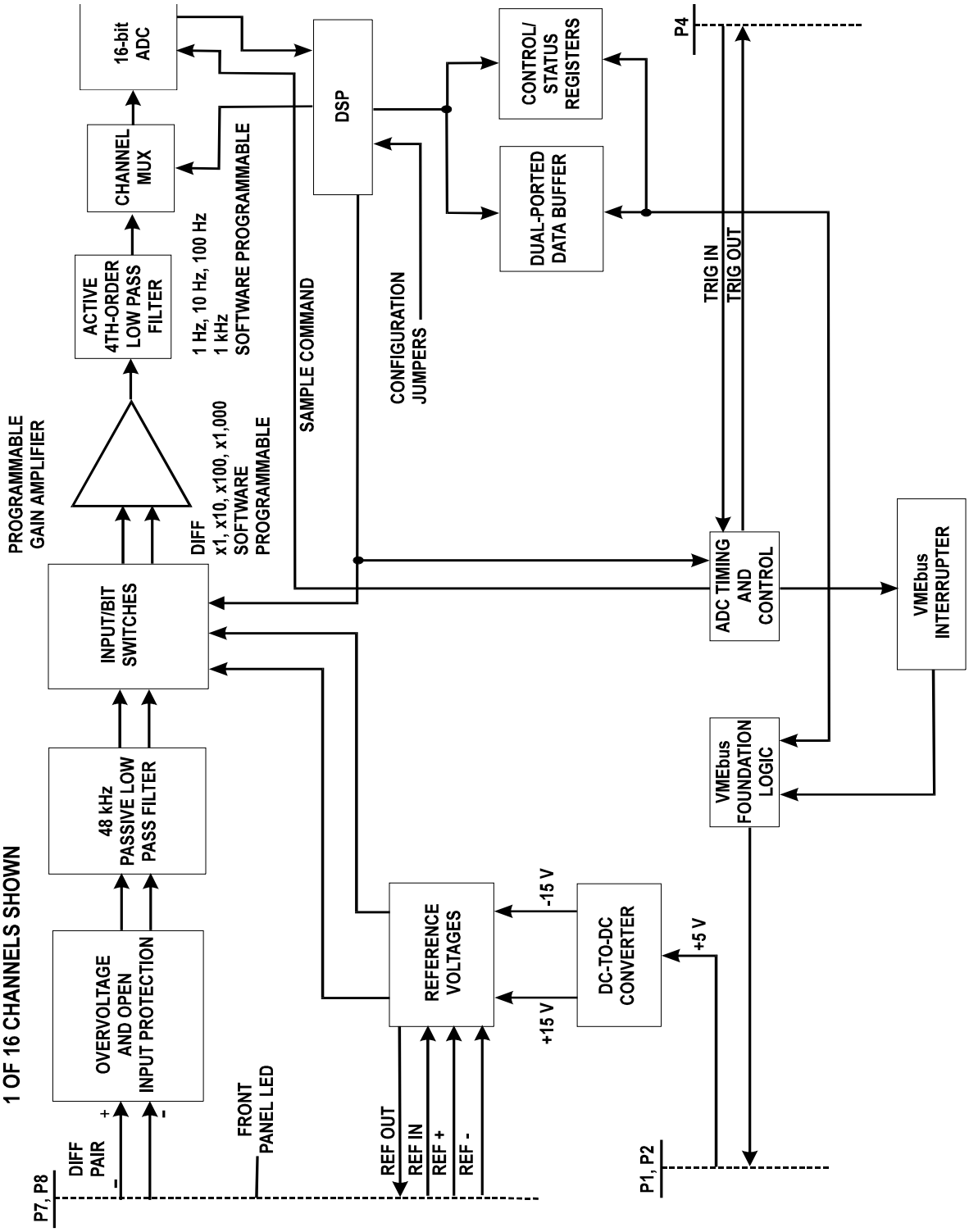


Figure 1 VMIVME-3119 Block Diagram

Active 4TH-Order Low Pass Filter

A four-pole selectable cut off active filter eliminates noise and frequencies which are undesired. The selectable cut off frequencies are 1 Hz, 10 Hz, 100 Hz, and 1 kHz. Each cut off frequency is available and is user programmable. The filter response is a factory option of either Butterworth or Bessel. The output of the filter for each channel is multiplexed to the Analog-to-Digital Converter (ADC).

Channel Multiplexer (MUX)

The VMIVME-3119 is a multiplexed scanning board. There are two multiplexers for all 16 channels, each one supporting 8 channels. The appropriate logic enables each multiplexer to output a specific channel in the correct sequence.

16-bit Analog-to-Digital Converter (ADC)

The VMIVME-3119 utilizes a 100 KS/s switched capacitor/charge redistribution 16-bit ADC with an on-chip sample-hold. The converted data is transmitted serially to the DSP. The DSP is interrupted when the data transmission is complete.

Digital Signal Processor (DSP)

The DSP serves four primary functions which are command interpretation, calibration, self-test, and real-time data correction. Upon user command, the DSP can perform calibration of each channel in all possible configurations. These calibration coefficients are stored in EEPROM. When a scan is active, the DSP receives samples from the 16-bit ADC and applies gain and offset correction before storing these samples in the Sample Buffer. The DSP continually monitors the Control/Status Registers for any change in configuration and configures the hardware for the desired mode of operation.

Data Buffer

The Data Buffer is an 8 Mbyte DRAM (or 4 Mbyte depending on ordering option) which can hold up to 4 million corrected samples. VMEbus block transfers (BLTs) are an efficient way of reading large numbers of samples from this buffer. This RAM can be allocated by setting the buffer size parameter, as either Sample Buffer RAM or user-defined RAM.

Control/Status Registers

The Control/Status Registers are implemented using a 32 Kbyte SRAM. This memory contains all control and status registers, provides a 256-byte scan table, and allows user access to calibration coefficients.

NOTE: Do not use blt operations to access these SRAM-based registers.

Analog-to-Digital Converter (ADC) Timing and Control

The ADC sample rate is user selectable (100 KHz maximum). The DSP internal timer is used for this sample clock and each time this timer expires an ADC sample pulse is issued. The ADC Timing and Control circuit issues an interrupt to the DSP when the ADC input has been sampled. This causes the DSP to advance the Channel MUX to the next channel to be sampled.

VMEbus Foundation Logic

The VMEbus interface is implemented using the Cypress CY7C960 and four CYCC964s. A local bus arbiter directs traffic to and from the Control / Status Register and the Data Buffer. To prevent loss of data, the priority is from the highest to the lowest, DRAM refresh, DSP (data samples), and VMEbus.

VMEbus Interrupter

An interrupt can be issued on any level (jumper selectable) and a single byte vector will be placed on the VMEbus when acknowledged. There is one Release-On-Acknowledge (ROAK) interrupt for the board and it can be generated when the data buffer is 50 percent (Mid Scan) or 100 present (End Scan) filled.

Reference Voltages

All calibration and self-test functions of the VMIVME-3119 are based on several precision reference voltages which can be user calibrated using the three front panel push button switches or using the Control / Status Registers. These voltages are output from a precision DAC under control of the DSP. When the Reference Voltages are calibrated, the DSP calculates gain and offset coefficients for each of the voltage ranges.

DC-to-DC Converter

There are three DC-to-DC converters on the VMIVME-3119 (two on the daughter board and one on the motherboard). Each of these is powered from the VMEbus +5 V supply. Each converter is fused to protect the circuitry it powers.

Front Panel LED

The front panel LED serves two purposes. First, the LED is used to indicate the progression of certain DSP operations such as self-test and at the end of these operations indicates pass / fail by the state of this LED. Second, the user has access to control this LED for any user-defined function. At the completion of self-test the front panel LED will begin to blink in a continuing pattern of three blinks and then cuts off. This indicates that reference calibration has begun.

Reference Material List

For a detailed explanation of the VMEbus and its characteristics, refer to "The VMEbus Specification" available from:

VITA

VMEbus International Trade Association

7825 East Gelding Drive, No. 104

Scottsdale, Arizona 85260

(602) 951-8866

FAX: (602) 951-0720

www.vita.com

Physical Description and Specifications: Refer to Product Specification, 800-003119-000 available from:

VMIC

12090 South Memorial Pkwy.

Huntsville, AL 35803-3308, USA

(256) 880-0444

(800) 322-3616

Fax: (256) 882-0859

www.vmic.com

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

CHAPTER
1

Theory of Operation

Contents

Introduction

This section describes the operational modes of the VMIVME-3119 board, and describes in terms of the user interface how these operational modes are achieved. The user interface to the VMIVME-3119 can be described by the following and are addressed in this order:

1. Configuration Jumpers
2. Analog Inputs
3. Control Parameters
4. Status Parameters
5. Commands
6. Scan Table
7. Sample Buffer RAM
8. User-Defined RAM
9. External Triggers
10. Calibration Coefficients
11. Front Panel LED
12. Reference Voltage Output

Configuration Jumpers

The configuration jumpers are one of the first things that must be considered when installing a VMIVME-3119. The configuration jumpers are discussed in detail in Chapter 2. However, since they are such an important part of the user interface, their use is summarized here.

VMEbus Base Address

Jumpers E4 and E5 determine the base address of the VMIVME-3119. The installation of a jumper causes the associated VMEbus address bit to be compared to a logical “0.” Omitting the jumper causes a comparison to a logical “1.” For the extended address mode, both E4 and E5 must be configured. For the standard address mode only E5 needs be configured.

VMEbus Access Mode

Jumper E6 allows the user to configure the VMIVME-3119 to respond to VMEbus Extended Data Accesses or Standard Data Accesses.

VMEbus Address Mode

Jumper E6 allows the user to configure the VMIVME-3119 to respond to Nonprivileged Data Access or Supervisory Data Accesses.

VMEbus Memory Size

The VMEbus address space occupied by the VMIVME-3119 can be user configured depending upon the application. The address space can be configured using jumper E6 as follows:

- 128 kbytes
- 256 kbytes
- 512 kbytes
- 1 Mbyte
- 2 Mbytes
- 4 Mbytes
- 8 Mbytes
- 16 Mbytes

The lower half of the VMEbus address space is occupied by Configuration, Status, and Command registers, the Scan Table, user-accessible calibration coefficients, and some reserved memory. The upper half of the VMEbus address space is occupied by the Sample Buffer RAM and User-Defined RAM. The size of the Sample Buffer RAM is set by the Buffer Size parameter. The amount of user-defined memory available is:

Size of user-defined memory = 1/2 (VMEbus Memory Size) - Sample Buffer RAM

VMEbus Interrupt Level

The VMIVME-3119 can be configured to request a VMEbus interrupt at the mid point of an scan or at the end of an active scan. The desired interrupt level is configured by jumper E7.

Self-Test Disable

Jumper field E6 contains a jumper that when installed causes the VMIVME-3119 to not perform self-test on power up or VMEbus reset. When this jumper is installed the front panel LED will remain on after power up or reset indicating to the user that self-test has not been performed. In most systems this jumper will never be installed.

Analog Inputs

The VMIVME-3119 accepts either 8 or 16 analog inputs through two front panel DB37 male connectors. These inputs can be either differential or single-ended. In addition, each input has a guard pin tied to analog ground through a 470 Ω resistor.

Each input has a passive RC filter with a cut off frequency of, 34 kHz to limit the input bandwidth and reduce input noise. The resistors for the filter also act as current limiters to the input switch in ease of overvoltage. Each input Low side has a 22 MΩ resistor to ground to stop the channel from saturating, if the Low side cabling gets disconnected.

The input switch allows either the input signal or a Built-in-Test (BIT) signal to be digitized by the ADC. The switch is automatically set into the BIT position for calibration and self-test. In the BIT position, a precision reference section generates the required voltages for calibration and self-test.

A software programmable gain amplifier (PGA) provides the required gain to fully realize each range. The appropriate gain is applied by the board logic corresponding to the range selected by the user in the Low and High Channel Gain registers. This PGA also converts differential inputs to single-ended and provides common-mode rejection.

The output of the PGA is routed to the input of the active filter. This filter is a four-pole active low pass. The available filter responses are Butterworth and Bessel.

Each channel has its own components mentioned above. The range and filter frequency are individually programmable. The output of each filter is routed to a multiplexer, which allows one channel through at a time to be digitized by the ADC. The timing for the multiplexer is handled by the board logic.

If the input range is exceeded, the output data will read either full-scale positive or negative, depending on the polarity of the input signal.

Careful consideration should be placed on the cabling from the field to the inputs to get optimum results. Ribbon cable is suitable for high-level signals, but will cause signal degradation of low level signals. Twisted-shielded pair is recommended for the ranges below ±10 volts.

Control Parameters

The following control parameters, which are described further in Chapter 3, allow the user to control the operational modes of the VMIVME-3119.

Data Ready

This parameter determines if the Data Ready Flag or VMEbus interrupt (if enabled), is generated at the midpoint of an active scan or at the end of an active scan.

Data Format

This parameter determines the data format for the Sample Data RAM. Both two's complement and offset binary data formats are supported.

Scan Modes

There are four scan modes supported by the VMIVME-3119. The operation of the Data Ready Flag and interrupt is the same in all scan modes and can be described by the flowchart (Figure 1-1 on page 27).

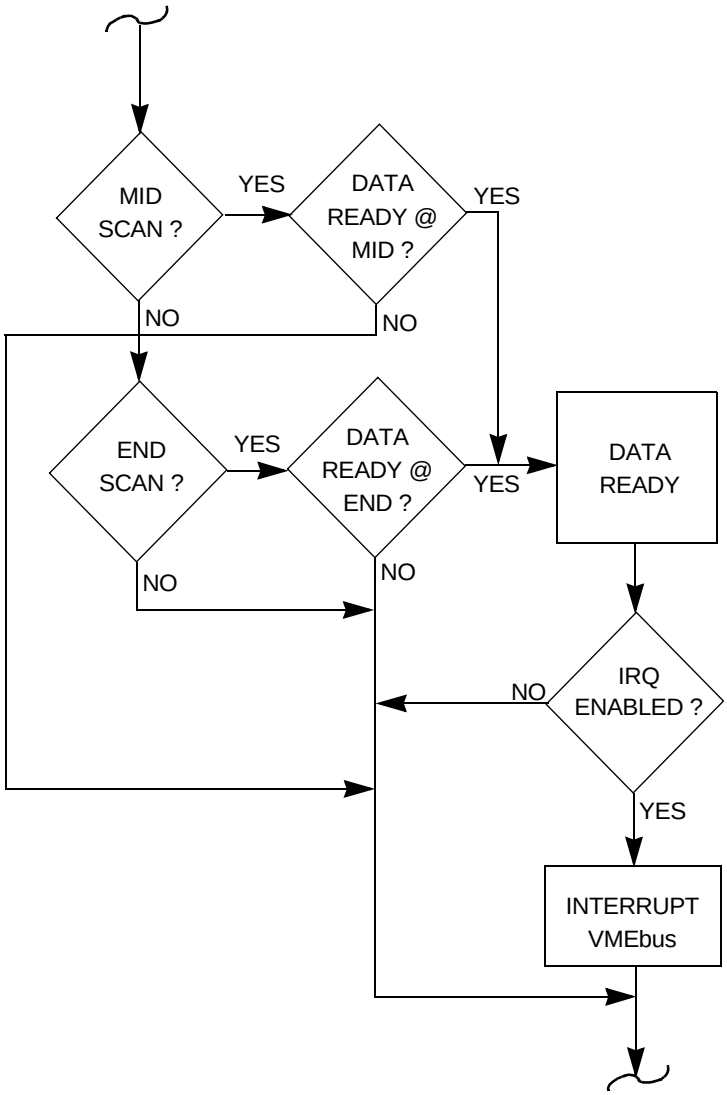


Figure 1-1 Data Ready Operational Flowchart

In the Continuous Scan Mode, each selected channel is continuously sampled at the effective sample rate. When the end of the Sample Data RAM is reached, the scan is automatically retriggered. This operation is described by the following flowchart.

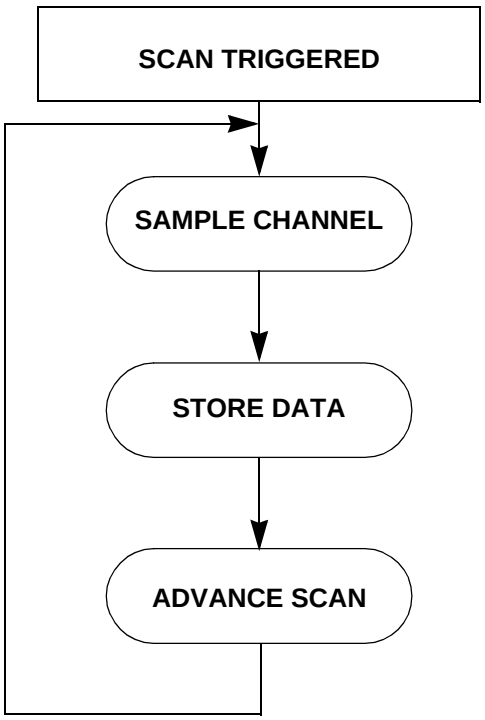
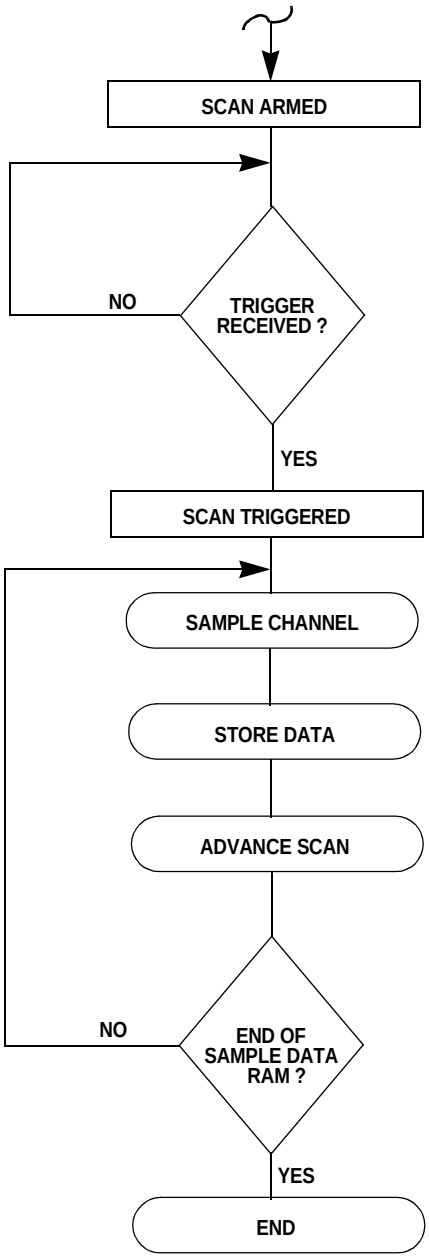


Figure 1-2 Continuous Scan Mode Flowchart

In the Single Scan Mode, a trigger event causes each selected channel to be sampled at the effective sample rate. When the end of the Sample Data RAM is reached, the scan is terminated. This mode, which cannot be retriggered, can be used to mask an unwanted external trigger. This mode is rearmed by the Abort/Restart Scan command. The Single Scan mode is described by the flowchart on page 3-6.



NOTE:

SINGLE SCAN MODE WILL NOT BE REARMED UNTIL AN ABORT/RESTART SCAN COMMAND IS RECEIVED.

Figure 1-3 Single Scan Mode Flowchart

The Single Scan and Rearm Mode is much like the Single Scan mode except that when the end of the Sample Data RAM is reached, the scan is rearmed. This mode is described by the following flowchart:

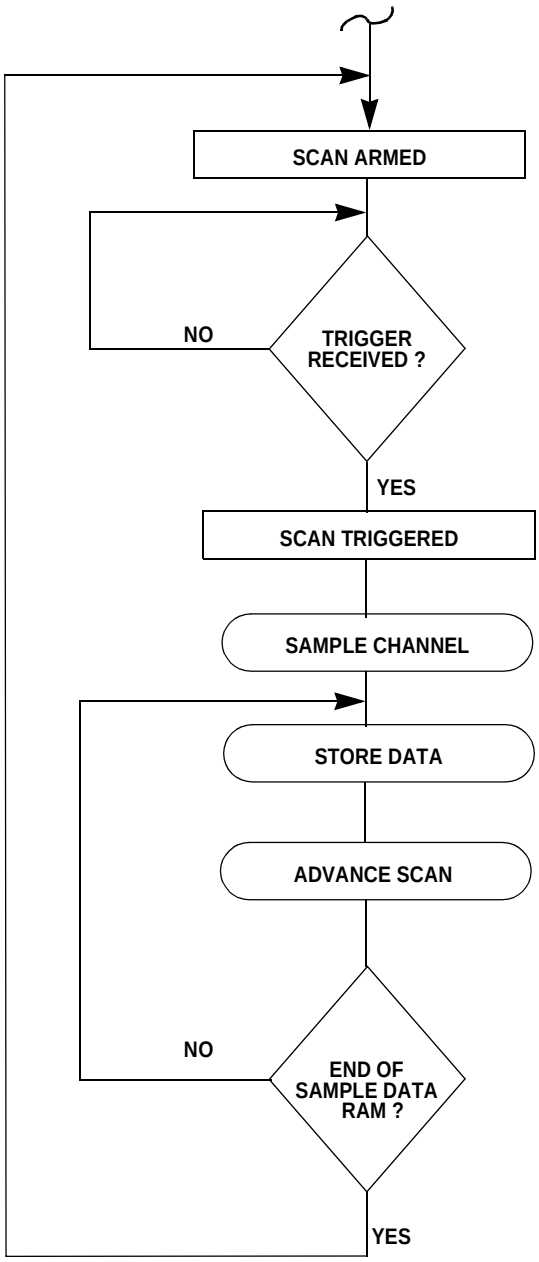


Figure 1-4 Single Scan and Rearm Flowchart

In the Advance Scan on Trigger Mode, the scan is advanced to the next selected channel each time a trigger occurs. This mode is described by the following flowchart:

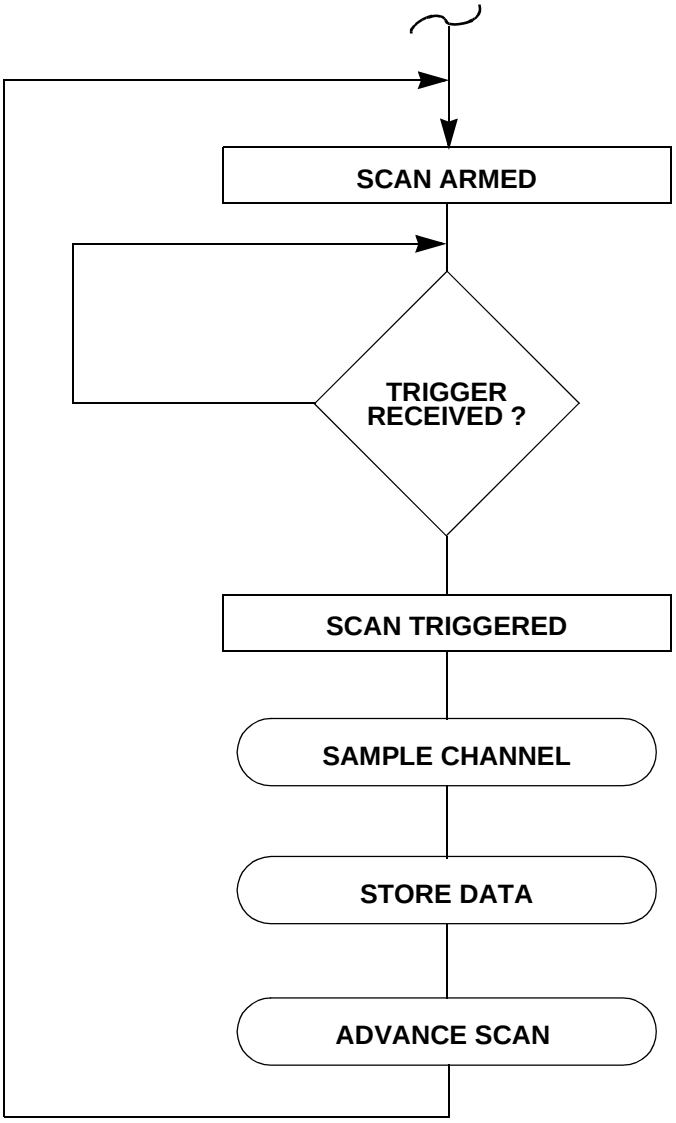


Figure 1-5 Advance Scan on Trigger Flowchart

Trigger Mode

There are six supported trigger modes for the VMIVME-3119. The operation of the Continuous Scan Mode is not affected by the Trigger Mode, however, all other scan modes require one or more trigger events.

When the Trigger Mode is disabled, no trigger events can occur.

The Single-Board Software Trigger Mode allows the VMIVME-3119, when armed, to be triggered by a Software Trigger Command.

The Single-Board Single-Ended External Trigger Mode allows the VMIVME-3119, when armed, to be triggered by a TTL-level high-to-low transition on Pin 8 (EXT_TRIG_L) of P4.

In the Multiboard Master Software Trigger Mode, a Software Trigger Command causes the configured scan mode, when armed, to be triggered and a differential trigger is output on Pins 5 and 9 of P4.

In the Multiboard Master External Trigger Mode, a TTL-level high-to-low transition on EXT_TRIG_L causes the configured scan mode, when armed, to be triggered and a differential trigger is output on Pins 5 and 9 of P4.

In the Multiboard Slave Differential Trigger Mode, a differential trigger received from the Master VMIVME-3119 on Pins 5 and 9 of P4 causes the configured scan mode, when armed, to be triggered.

VMEbus Interrupt

Before a VMEbus Interrupt can be used to indicate Data Ready, the Desired IRQ Vector must be programmed in the IRQ Vector Register. This register also contains an enable which can be used to enable or disable the interrupt request on a Data Ready condition.

Sample Period

The period of the sample clock is programmed through two registers, the Sample Clock Prescale Register and the Sample Clock Period Register.

Sample Period = (Sample Clock Period + 1) x (Sample Clock Prescale + 1) x (50 nsec)

The VMIVME-3119 has one ADC which is shared among all active channels, therefore, the sample period for an individual channel is not necessarily the programmed Sample Period. The Effective Sample Period depends on the programmed Sample Period and the number of channels being scanned.

Consider, as an example, that the following Scan Table is active {x00, x01, x00, x02, x00, x03, x00, x84}.

Effective Sample Period (Channel 0) = Sample Period x (8 / 4) = Sample Period x 2

Effective Sample Period (Channels 1, 2, 3, 4) = Sample Period x (8 / 1) = Sample Period x 8

Channel Gain

The VMIVME-3119 supports input ranges of ±10 V, ±1 V, ±100 mV, and ±10 mV. The Low Channel Gain Register and High Channel Gain Register are used to program each channel of the VMIVME-3119 to the desired input range.

Channel Filter Cutoff Frequency

A VMIVME-3119 with either the Bessel filter option or the Butterworth filter option can be programmed for filter cut-off frequencies of 1 KHz, 100 Hz, 10 Hz, and 1 Hz. The Low Channel Filter Register and High Channel Filter Register are used to program each channel of the VMIVME-3119 to the desired input range.

Buffer Size

The Buffer Size parameter determines the size of the Sample Buffer RAM. The Buffer Size can be programmed, in powers of 2, from 1 sample (2 byte) to 4 Msamples (4,194,304 samples or 8,388,608 bytes) but cannot be more than 1/2 the VMEbus Memory Size set by Jumper Field E6.

Status Parameters

The following status parameters, which are described further in Chapter 3, allow the user to determine the current state of the VMIVME-3119.

Configuration Complete Flag

The Configuration Complete Flag can be used as a handshake between the user and the on-board DSP. When the DSP detects a change in a control parameter, the scan is aborted and reconfigured. When this reconfiguration is complete, the Configuration Complete Flag is set. This flag is cleared by the Clear Flag Command or by the Abort/Restart Scan Command.

The following programming sequence for changing the configuration of the VMIVME-3119 is highly recommended.

Write all desired Control Parameters.
Write Abort/Restart Scan Command.
Read Abort/Restart Scan Command until equal 0.
Read Configuration Complete Flag until equal 1.

Data Ready Flag

The Data Ready Flag indicates to the user that the Sample corresponding to the mid point or end point of the active scan has been written to the Sample Buffer RAM. If a VMEbus interrupt request is enabled, it will be generated when this flag is set. This Flag is cleared by the Clear Flag Command or the Abort/Restart Scan Command.

Trigger Armed Status

This status bit is set to a logical 1 whenever a scan is armed and ready for triggering. This status bit will be set to a logical 0 whenever a valid trigger is received.

Scan Triggered Status

This status bit is set to a logical 1 whenever a valid trigger is received. This bit is set to a logical 0 when the programmed scan ends, when the DSP detected a change in configuration, or when the Abort/Restart Scan Command is received.

Error Code Status

The Error Code Status is used to indicate invalid user-programmed control parameters and self-test failures. If the Channel Failure error code is returned, any channels that have failed self-test are indicated in the Self-Test Status Register. The Error Code Status is cleared when all error conditions are resolved.

VMEbus Interrupt Level Status

There are three status bits that indicate to the user the state of the Interrupt Level configuration jumpers.

Memory Size Status

There are three status bits that indicate to the user the state of the Memory Size configuration jumpers.

Self-Test Disable Status

This Status Bit indicates to the user the state of the Self-Test Disable configuration jumper.

Commands

Each of the commands is described in detail in Chapter 3. Each command is issued by writing a logical 1 to bit 0 of the associated register. The DSP acknowledges the command by returning this bit to a logical 0.

Clear Flag Command

This command allows the user to clear the Configuration Complete and Data Ready Flags.

Abort/Restart Scan Command

Although the DSP monitors command parameters and changes configuration when new user parameters are detected, it is recommended that the Abort/Restart Scan Command be used as a handshake between the user and the DSP. When the Abort/Restart Scan Command is issued, the Configuration Complete Flag indicates to the user that all programmed configuration changes have been completed.

Software Trigger Command

This command allows the user to trigger a scan under software control. The Trigger Armed Status indicates that the VMIVME-3119 is ready to be triggered. The Scan Triggered Status indicates that the trigger has been received and the scan is in progress.

Channel Calibration Command

This command, in conjunction with the Calibration Channel Select Register and the Calibration Configuration Select Register, allows the user to calibrate any group of channels in all possible range and filter configurations. It should be noted that the time required to calibrate the VMIVME-3119 will depend on the number of channels and filters selected. The calibration coefficients are stored in nonvolatile EEPROM.

Self-Test Command

This command allows the user to initiate self-test of the VMIVME-3119. Pass/Fail of user-initiated self-test is indicated in the Error Code Register and the Self-Test Status Register.

Reset Command

This command allows the user, under software control, to return all VMIVME-3119 parameters to their default state. This command does not cause the reset of any hardware circuits.

Scan Table

The scan table is one of the most powerful features of the VMIVME-3119. The Scan table is read by the DSP each time the Abort/Restart Scan Command is issued. The following is a list of possible uses of the Scan Table:

- The effective sample rate of individual channels can be controlled. As an example, assume only the first three channels are to be scanned. Assume also the Scan Table is set as follows: { x00, x01, x00, x82 }. In this case, the effective sample rate of channel 0 is twice that of channel 1 or channel 2. Note that the HEX code x82 indicates channel 2 and the end of the scan table.
- Unused channels can be disabled.
- Channels can be scanned in any order.

Sample Buffer RAM

The Sample Buffer RAM contains the corrected samples collected during a scan. The data format of these samples is programmed by the user to be either two's complement or offset binary. The Data Ready Flag and/or the VMEbus Interrupt can be programmed to indicate to the user that a current sample has been stored at the midpoint or end point of the Sample Buffer RAM. The size of the Sample Buffer RAM is determined by the Memory Size configuration jumpers and the Buffer Size control parameter.

User-Defined RAM

All of the upper half of the VMEbus memory space of the VMIVME-3119 that has been enabled by the Memory Size configuration jumpers and not dedicated to the Sample Buffer RAM by the Buffer Size parameter is available as User-Defined RAM.

External Triggers

There are two external trigger sources for the VMIVME-3119. To trigger a scan with either of these sources, the Enable Trigger bit of the Global Configuration Register must be written to a logical 1. The VMIVME-3119 can be triggered by a single ended TTL level high-to-low transition on Pin 8 of P4. If the VMIVME-3119 is configured as a slave, it may be triggered from a master VMIVME-3119 by the differential trigger signals on Pins 5 and 9 of P4.

Calibration Coefficients

In most applications, the user will not need to directly modify the calibration coefficients, however, it is possible for the user to modify the gain and offset applied to an input signal. Whenever the VMIVME-3119 is calibrated, the calibration coefficients are stored in EEPROM, which is not directly accessible by the user. On power up or reset, these coefficients are written to a user-accessible area of memory. Each time the Abort / Restart Scan Command is issued, these coefficients are moved from user-accessible memory to DSP internal memory where they are retrieved each time a data sample is corrected.

NOTE: Modifying these registers will alter the performance of the VMIVME-3119. Care must be taken not to inadvertently overwrite these registers.

Front Panel LED

The front panel LED serves two purposes. First the LED is used to indicate the progression of certain DSP operations such as self-test and at the end of these operations indicates pass / fail by the its state. Second, the user has program control of this LED for any user-defined function.

Reference Output and Control Switches

Calibration of the VMIVME-3119 is based on a precision on-board voltage reference. This reference can be user calibrated either under software control or from the front panel push-button switches. Initiating reference calibration under software control requires a 32-bit software key.

There are three commands which must be used to calibrate the VMIVME-3119. When using the front panel switches, these commands correspond directly to the switches. The commands are Reference Output Advance, Reference Increment, and Reference Decrement. The Reference Output Advance command will advance the reference calibration to the next voltage and, when all voltages have been calibrated, terminate the reference calibration. The Reference Increment and Reference Decrement commands increment or decrement the digital reference by 1-bit weight. The reference voltages in Table 1-1 are listed in the order inwhich they are calibrated.

Table 1-1 Calibration Reference Voltages

Reference Voltage	Status Code Read from Reference Calibration Status Register
0.3125000 V	x100
5.0000000 V	x101
9.9218750 V	x102
0.0312500 V	x200
0.5000000 V	x201
0.9921875 V	x202
3.1250000 mV	x300
50.000000 mV	x301
99.218750 mV	x302
0.3125000 mV	x400
5.0000000 mV	x401
9.9218750 mV	x402

The following procedure should be followed when calibrating the VMIVME-3119 reference voltages using the front panel switches:

1. Connect an eight-digit or better Precision Voltmeter to the front panel BNC connector labeled REF OUT.
2. With the VMIVME-3119 installed in a standard VMEbus chassis, power up the VMIVME-3119 and allow a mimimum of 15 minutes for the board to warm-up.
3. Depress the switches labeled Mode and REF- and hold these as the VMEbus is reset. When the front panel LEDs begin to blink, release the switches.
4. The VMIVME-3119 will go through the normal power up and self-test sequence at this time. At the completion of self-test, the front panel LED will begin to blink in a continuing pattern of three blinks and off. This indicates that reference calibration has begun. The meter connected to REF OUT should read a voltage near 0.3125000 V.

5. Use the REF+ or REF- to increase or decrease the voltage measured at REF OUT until it is as close as possible to 0.3125000 V. Noise and quantization errors make it impossible to get the reading exactly.
6. Push the switch labeled Mode and hold it until the front panel LED stops blinking and remains on. Now release this switch. This should advance the reference voltage and the meter should read a voltage near 5.0000000 V.
7. Continue in this method until all the reference voltages are calibrated. When the last voltage has been calibrated, pushing the Mode switch will end reference calibration. The front panel LED will blink 10 times indicating that reference calibration is complete and all reference calibration values are stored in EEPROM.
8. At this point the VMIVME-3119 is ready for normal operation.

The following procedure should be followed when calibrating the VMIVME-3119 reference voltages using the software interface:

1. Connect an eight-digit or better Precision Voltmeter to the front panel BNC connector label REF OUT.
2. At this time, the VMIVME-3119 should be allowed to warm up for approximately 15 minutes before reference calibration continues.
3. Write x50B6 to Reference Calibration Enable HW
4. Write x033F to Reference Calibration Enable LW
5. Issue the Abort/Restart Scan Command
6. The front panel LED will begin to blink in a continuing pattern of three blinks and off. This indicates that reference calibration has begun. The meter connected to REF OUT should read a voltage near 0.3125000 V.
7. Read the Reference Calibration Code Register. This is a 16-bit binary code representing the voltage (0 to 10 V) at the REF OUT connector. Modify this code to cause the meter to read a voltage as close as possible to 0.3125000 V.
8. Write a logical 1 to the Reference Calibration Mode Register. This will cause the reference to advance to the next voltage. The Reference Calibration Status Register may be read to determine the current reference voltage. This should advance the reference voltage and the meter should read a voltage near 5.0000000 V.
9. Continue in this method until all the reference voltages are calibrated. When the last voltage has been calibrated.
10. At this point, the VMIVME-3119 is ready for normal operation.

CHAPTER

1

Configuration and Installation

Introduction

This chapter describes the installation and configuration of the board. Cable configuration, jumper / switch configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

CAUTION: Do not install or remove the boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Verify that the sections pertaining to configuration (Chapter 2), have been reviewed and applied to system requirements.
2. Verify that the I/O cables are properly terminated for the input/output connectors.
3. Ensure that all system cable connections are correct.
4. Verify that IACK* and BG* daisy chain jumpers are installed in passive VMEbus backplanes where needed.

After the checklist above has been completed, the board can be installed in a VMEbus chassis. This board can be installed in any slot position, except slot one which is reserved for the system controller.

NOTE: The second slot occupied by the VMIVME-3119 has no VMEbus connectors and therefore does not pass IACK* or BG* signals. For passive VMEbus backplanes jumpers must be installed to complete the daisy chains.

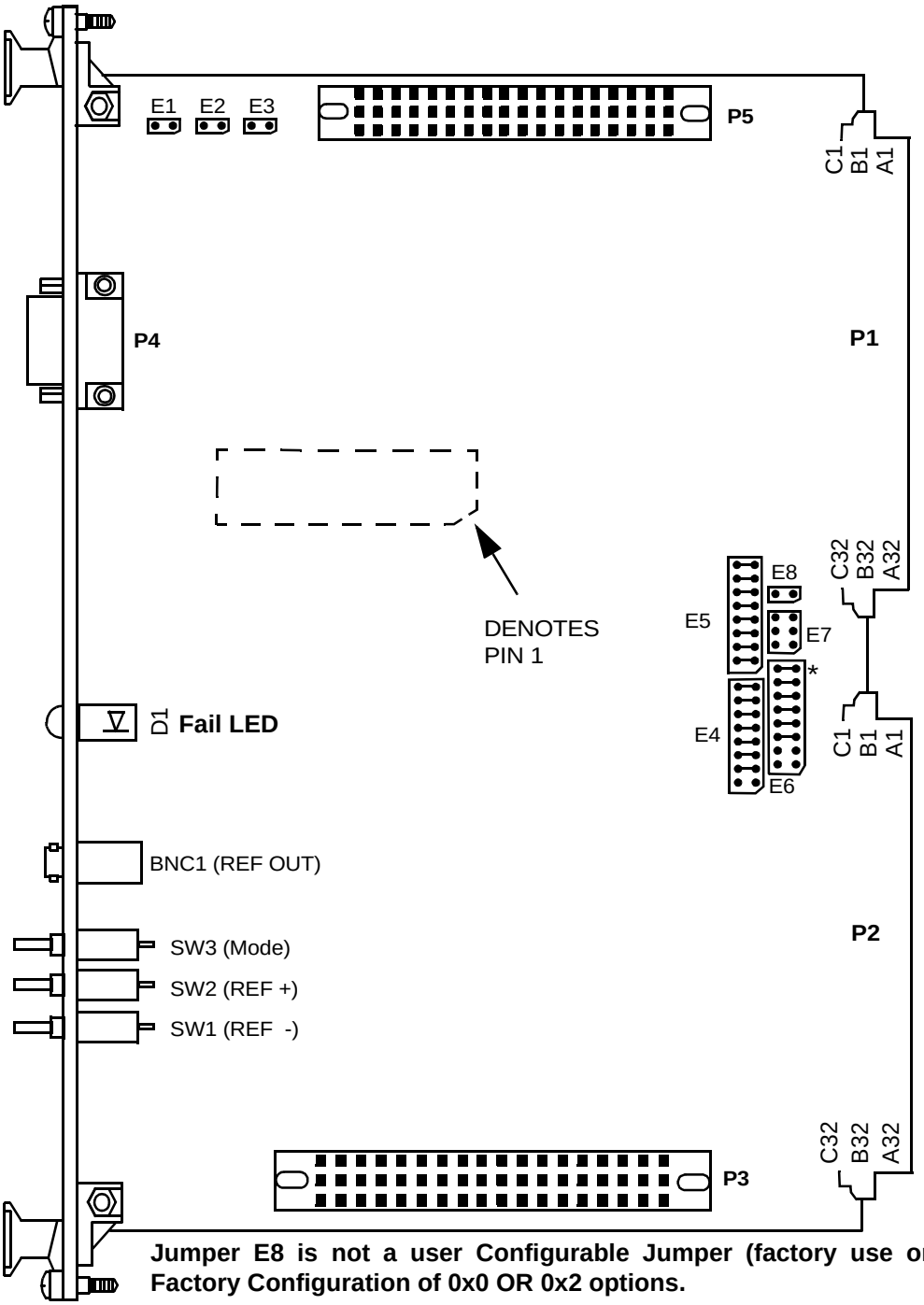
Base Address and Board Configuration

There are 19 jumper positions to establish the base address, address mode, and access mode. The address mode can be configured for extended or standard address space. The base address is determined by the presence (address bit compared to logic zero) or absence (address bit compared to logic one) of a jumper shunt at each appropriate address jumper position. The access mode can be configured for supervisory, nonprivileged, or for both supervisory and nonprivileged access.

The location of Jumpers, connectors, and switches are illustrated in Figure 2-1 on page 73. Figure 2-2 on page 74 through Figure 2-4 on page 76 illustrates the functions of user configurable jumpers. Omission of a jumper shunt produces a HIGH (logic “1”) requirement for the associated bit. Installation of the jumper shunt produces a LOW (logic “0”) requirement. The factory configuration for the board is:

- Extended address space
- Supervisory and nonprivileged access mode
- Memory size of 16 or 8 Mbyte depending on option
- Interrupt disabled
- Base address set at 0X8000 0000

NOTE: Jumper E8 is not a user configurable jumper (factory use only.)



Jumper E8 is not a user Configurable Jumper (factory use only). Factory Configuration of 0x0 OR 0x2 options.

* E6 15-16 removed for 0x1 or 0x3 options (2 megasample option).

Figure 2-1 VMIVME-3119 Board Layout

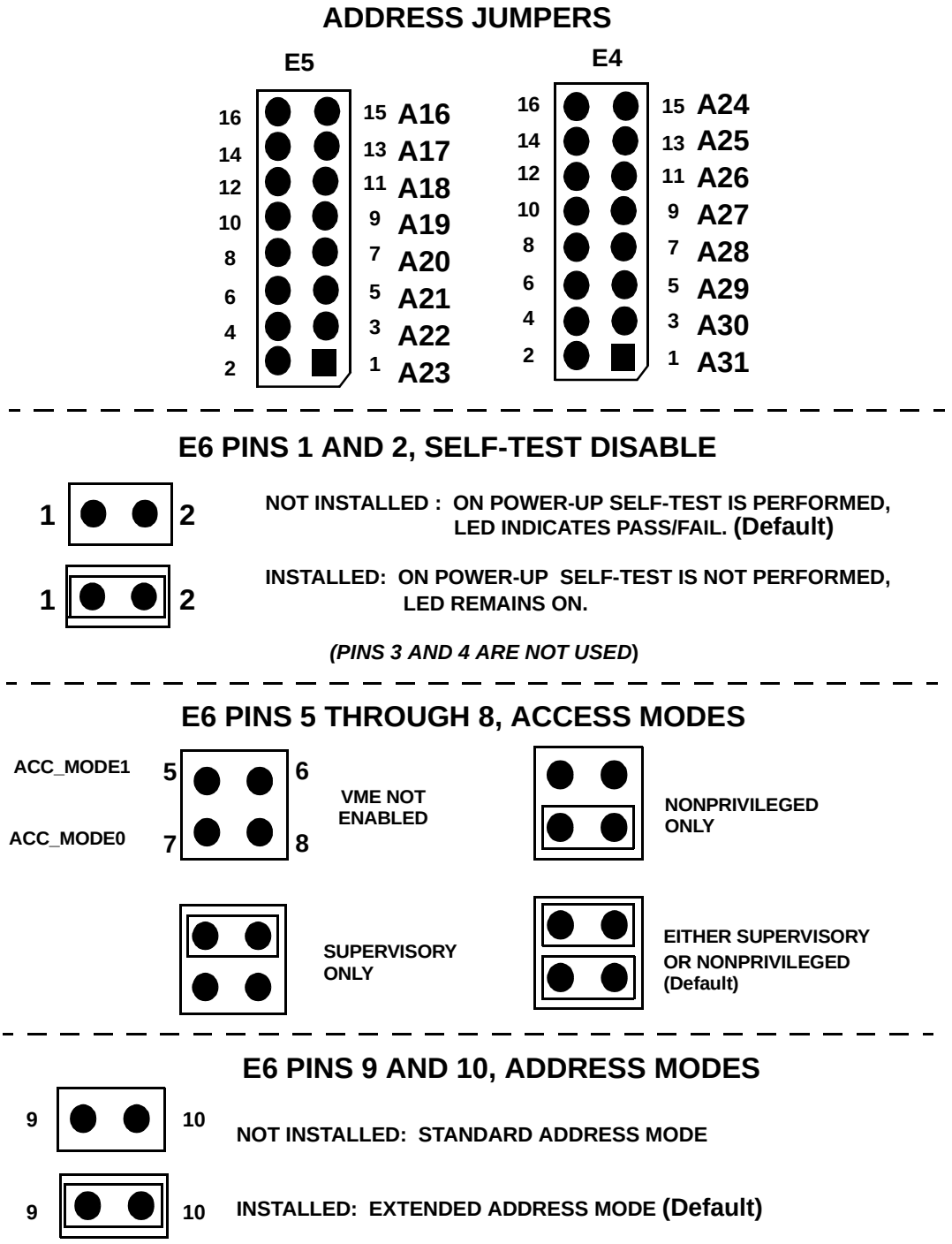


Figure 2-2 Access and Address Mode Configurations

E6 MSIZE [2:0] (Memory Sizes)

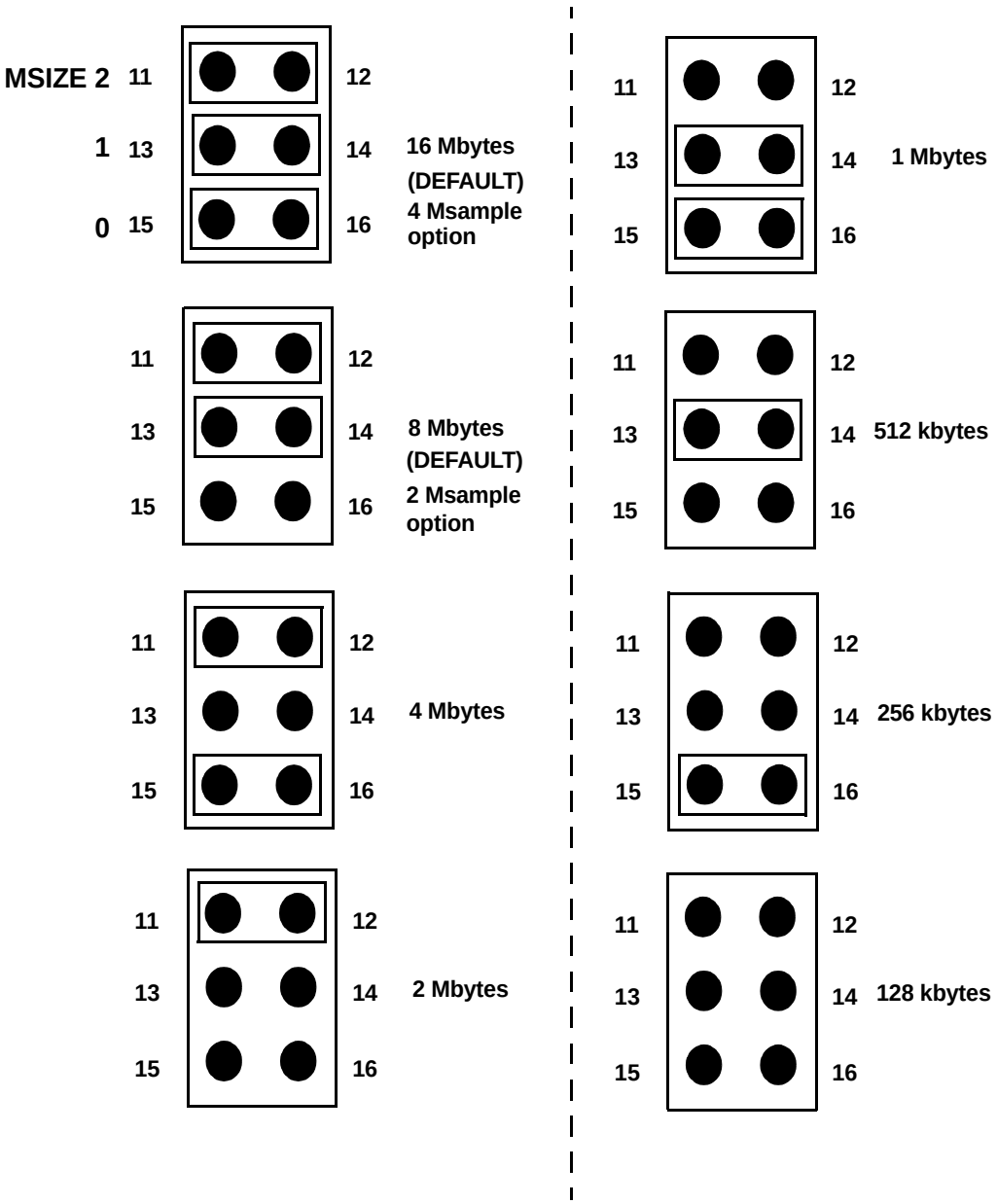


Figure 2-3 Memory Size Configurations

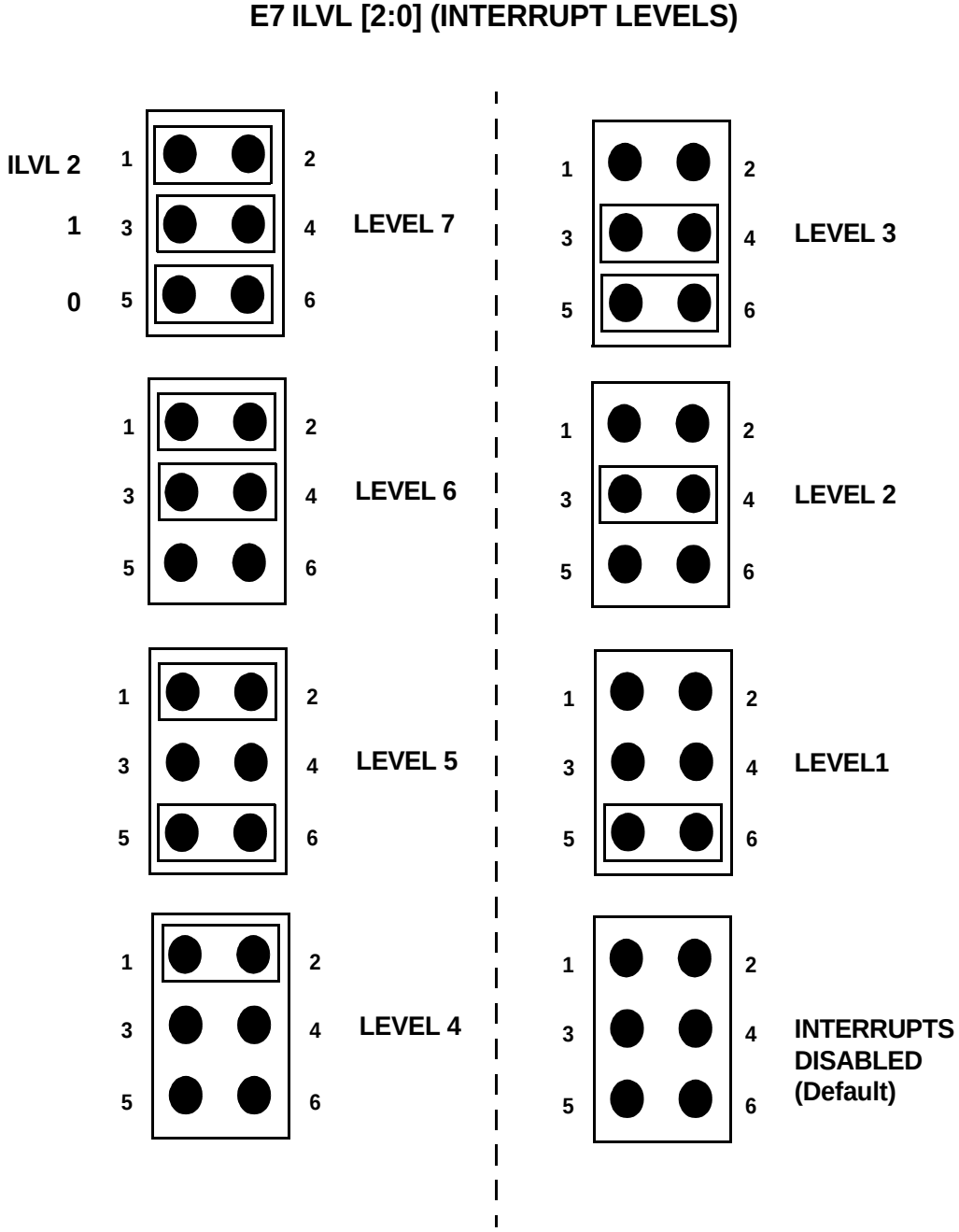


Figure 2-4 Jumper E7 Interrupts Configuration

Several other jumpers and their functions are described below.

Jumper E1: This jumper is for RS422 termination. With E1 installed, RS422 termination is enabled through a 200 Ω resistor. When E1 is not installed, termination is not present. (Default = no jumper installed.)

NOTE: In a multi-board system, E1 should be installed on the master and the last (end of cable) slave board.

Jumper E2: This jumper provides a return for triggering. With E2 installed, a DC return is supplied on pins 2, 4, and 7 of the front panel connector P4. With E2 Omitted (not installed), an AC return is supplied on the same pins. (Default = no jumper installed.)

NOTE: In a multi-board system, E2 should be installed on only one VMIVME-3119.

Jumper E3: This jumper is normally not installed by the user. The jumper causes a reset to the VMIVME-3119. This is used for test purposes at the factory.

System Connections

The VMIVME-3119 has two DB-37 male connectors on the front panel. These connectors are the inputs to the channels. The pinouts for each connector is shown in Table 2-1 on page 80 and Table 2-2 on page 80. Figure 2-5 on page 79 is an illustration of the front panel. Figure 2-6 on page 80 is an illustration of the P1 and P2 connectors. Figure 2-7 on page 81 illustrates the P4 connector, Table 2-3 on page 81 is the connector pinout.

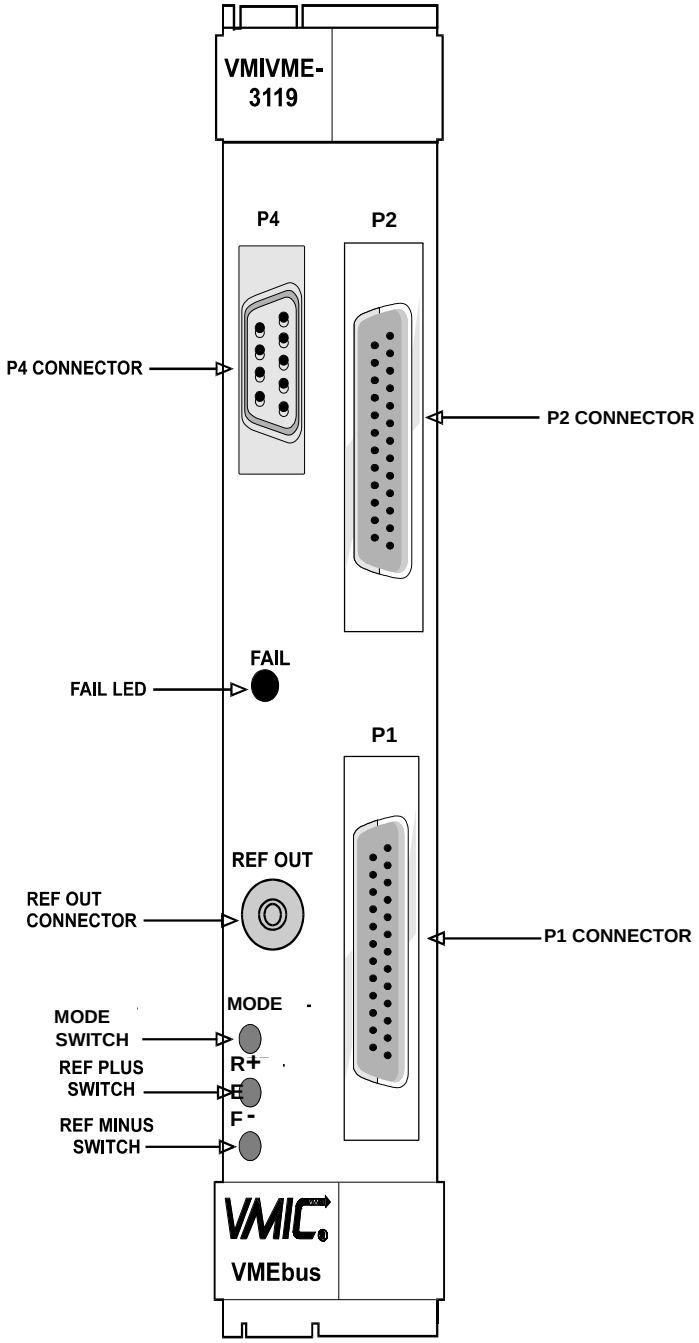


Figure 2-5 Front Panel for the VMIVME-3119

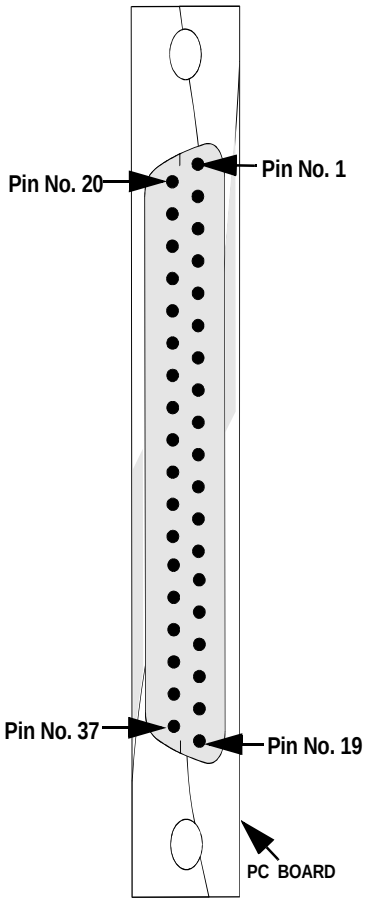


Figure 2-6 P1 and P2 Connector

Table 2-1 P1 Connector Pinout

Pin No.	Function	Pin No.	Function
20	Channel 7 HIGH	1	Channel 7 Guard
21		2	Channel 7 LO
22	Channel 6 HIGH	3	Channel 6 Guard
23		4	Channel 6 LO
24	Channel 5 HIGH	5	Channel 5 Guard
25		6	Channel 5 LO
26	Channel 4 HIGH	7	Channel 4 Guard
27		8	Channel 4 LO
28	Analog GND	9	Analog GND
29	Analog GND	10	Analog GND
30	Analog GND	11	Analog GND
31	Channel 3 HIGH	12	Channel 3 Guard
32		13	Channel 3 LO
33	Channel 2 HIGH	14	Channel 2 Guard
34		15	Channel 2 LO
35	Channel 1 HIGH	16	Channel 1 Guard
36		17	Channel 1 LO
37	Channel 0 HIGH	18	Channel 0 Guard
		19	Channel 0 LO

Table 2-2 P2 Connector Pinout

Pin No.	Function	Pin No.	Function
20	Channel 15 HIGH	1	Channel 15 Guard
21		2	Channel 15 LO
22	Channel 14 HIGH	3	Channel 14 Guard
23		4	Channel 14 LO
24	Channel 13 HIGH	5	Channel 13 Guard
25		6	Channel 13 LO
26	Channel 12 HIGH	7	Channel 12 Guard
27		8	Channel 12 LO
28	Analog GND	9	Analog GND
29	Analog GND	10	Analog GND
30	Analog GND	11	Analog GND
31	Channel 11 HIGH	12	Channel 11 Guard
32		13	Channel 11 LO
33	Channel 10 HIGH	14	Channel 10 Guard
34		15	Channel 10 LO
35	Channel 9 HIGH	16	Channel 9 Guard
36		17	Channel 9 LO
37	Channel 8 HIGH	18	Channel 8 Guard
		19	Channel 8 LO

Each guard is connected to the board's analog ground through 470 Ω resistor.

External triggering is accomplished through the P4 connector on the front panel. The pinout for the connector is shown in Figure 2-7 below. Table 2-3 shows the connector pinout for the P4 connector.

Table 2-3 P4 Connector Pinout

Pin No.	Function	Pin No.	Function
9	Differential Trigger LO	5	Differential Trigger HI
8	External Trigger LO Input	4	Digital GND (E2 Installed)
7	Digital GND (E2 Installed)	3	Not Used
6	Not Used	2	Digital GND (E2 Installed)
		1	Not Used

External Trigger LO is the input for an external trigger to be applied to the board. The Differential Trigger HI and LO are used in a multiboard system. The master board will receive the external trigger on the External Trigger LO pin. This will drive the Differential Trigger HI and LO pins to the other boards (slaves).

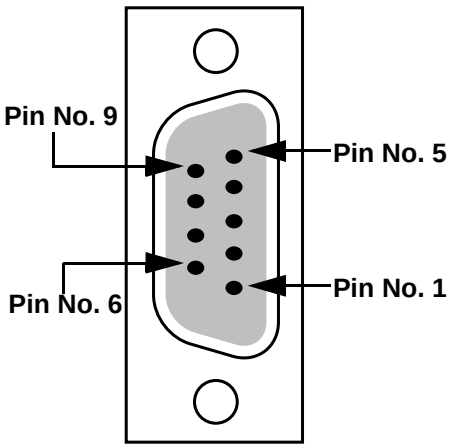


Figure 2-7 P4 Connector

CHAPTER

3

Programming

Introduction

This Chapter of the manual deals with the VMEbus software interface to the VMIVME-3119 board. Programming the VMIVME-3119 assumes a properly installed board accessed from an appropriate VMEbus system controller. Installation and hardware jumper configuration requirements are described in Chapter 2.

VMEbus Slave Interface

The user directs the operation of the VMIVME-3119 Local DSP through an interface of command registers, status registers, configuration registers, and data buffers which are implemented with dual-ported RAM. The VMIVME-3119 can be jumper configured for either A24 or A32 VMEbus address space and can be jumper configured to occupy 16, 8, 4, 2, 1 Mbyte, and 521, 256, or 128 Kbyte. The Sample buffer resides in the upper half of the VMIVME-3119 address space and can be configured to store from 1 to 4,194,304 samples (2,097,152 samples maximum for the 2 Msample option).

NOTE: The VMIVME-3119 VMEbus interface is implemented using the Cypress CY7C960 Chipset. This chipset is not programmed, and therefore the slave interface is not available until power up self-test is complete. With the self-test disable jumper not installed power up initialization takes approximately 25 seconds. with the jumper installed, the power up initialization takes approximately 2 seconds. The VMIVME-3119 should not be accessed during the power up initialization.

Since the user interface is designed around dual-ported RAM, the user must not overwrite locations defined as “read-only” and must not access locations defined as reserved.

VMIVME-3119 Memory Map

Table 3-1 VMIVME-3119 Memory Map

Offset Address	Function	Mnemonic	Access
$00 0000	Board ID Register	BID	Read Only
$00 0002	Firmware Revision Register	FRR	Read Only
$00 0004	Global Control Register	GCR	Read / Write
$00 0006	Global Status Register	GSR	Read Only
$00 0008	Sample Clock Prescale Register	PSR	Read / Write
$00 000A	Sample Clock Period Register	SPR	Read / Write
$00 000C	IRQ Control Register	ICR	Read / Write
$00 000E	IRQ Status Register	ISR	Read Only
$00 0010 $00 0012	Low Channel Gain Register High Channel Gain Register	LGR HGR	Read / Write
$00 0014 $00 0016	Low Channel Filter Register High Channel Filter Register	LFR HFR	Read / Write
$00 0018	Buffer Size Register	BSR	Read / Write
$00 001A	Clear Flag Command Register	CFC	Read / Write
$00 001C	Calibrate Channel Select Register	CSR	Read / Write
$00 001E	Calibrate Configuration Select Register	CCR	Read / Write
$00 0020	Reset Command Register	RST	Read / Write
$00 0022	Calibration Command Register	CAL	Read / Write
$00 0024	Self-Test Command Register	TST	Read / Write
$00 0026	Self-Test Status Register	TSR	Read Only
$00 0028	Software Trigger Register	TRG	Read / Write
$00 002A	Abort / Restart Scan Register	ABT	Read / Write
$00 002C	DSP Peek Address Register	PAR	Read / Write
$00 002E	DSP Peek Data Register	PDR	Read Only
$00 0030	LED Control Register	LCR	Read / Write
$00 0032	Reserved	---	---
$00 0040	Reference Calibration Mode Register	RCM	Read / Write
$00 0042	Reference Calibration Code Register	RCC	Read / Write
$00 0044	Reference Calibration Status Register	RCS	Read Only
$00 0046	Reference Calibration Enable HW Register	REH	Read / Write
$00 0048	Reference Calibration Enable LW Register	REL	Read / Write
$00 004A $00 03FE	Reserved	---	---
$00 0400 $00 04FE	Scan Table	SCN	Read / Write
$00 0500 $00 07FE	Reserved	---	---
$00 0800 $00 0BFE	User Calibration Coefficients	UCC	Read / Write
$00 C000 P-2	Reserved	---	---
P P + BS / 2-2	Sample Buffer RAM	SPL	Read / Write
P + BS / 2 2P-2	User-Defined RAM	UDR	Read / Write

P: The base address of the Sample Buffer which is set by configuration jumpers. P = Base Address (refer to Figure 2-2 on page 51) + Sample Buffer Offset (SBO).

BS: The Buffer Size (bytes) which is set by the Buffer Size Register.

SBO: Sample Buffer Offset as referenced from the Board Base Address (physical memory size / 2).

SBO= $01 0000,
$02 0000,
$04 0000,
$08 0000,
$10 0000,
$20 0000,
$40 0000,
or $80 0000

(dependent on jumper configuration, refer to Figure 2-2 on page 51

NOTE: Do not use blt operations to access SRAM-based registers at offset address $00 0000 through $00 7FFE.

Board ID Register (BID)

The board ID register is an read-only status register, the contents of which identifies the VMIVME-3119 and its factory ordering options.

Table 3-2 Board ID Register Bit Map

Board ID Register (Offset $00 0000) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	0	1	1	0	1

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	FL1	FL0	CH	MEM

Board ID Register Bit Definitions

Bits 03 and 02: **FL[1:0], Filter Option** - This field indicates the factory installed filter option of the VMIVME-3119 according to Table 3-3.

Table 3-3 Filter Options

FL[1:0]	Filter Option
00	No Filter
01	Bessel Filter
10	Butterworth
11	Reserved

Bit 01: **CH, Channel Option** - A logical one indicates that the board is a 8-channel VMIVME-3119. A logical zero indicates that the board is a 16-channel VMIVME-3119.

Bit 00: **MEM, Memory Option** - A logical one indicates that the board has 2 Msamples (4 Mbyte) of DRAM. A logical zero indicates that the board has 4 Msamples (8Mbyte) of DRAM.

Firmware Revision Register (FRR)

The FRR is a read-only status register indicating the VMIVME-3119 DSP firmware revision level. Both major and minor revision levels are indicated and are interpreted as version (major revision) (minor revision).

Table 3-4 Firmware Revision Register Bit Map

Firmware Revision Register (Offset $00 0002) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
MAR7	MAR6	MAR5	MAR4	MAR3	MAR2	MAR1	MAR0
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
MIR7	MIR6	MIR5	MIR4	MIR3	MIR2	MIR1	MIR0

Firmware Revision Register Bit Definitions

Bits 15 through 08: MAR[7:0]: Major Revision - Hexadecimal code indicating the "major" revision level from 0 to 255.

Bits 07 through 00: MIR[7:0]: Minor Revision - Hexadecimal code indicating the "minor" revision level from 0 to 255.

Example: $0102 is interpreted as version 1.02.

Global Control Register (GCR)

The GCR is a read / write register which controls global parameters of the VMIVME-3119.

Table 3-5 Global Control Register Bit Map

Global Control Register (Offset $00 0004) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	RDY HF	Enable Trigger	Data FMT	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
ST EN	SM2	SM1	SM0	TM3	TM2	TM1	TM0

Global Control Bit Definitions

Bit 15: Default is logical zero.

Bit 14: **RDY HF - Ready on Buffer Half-Full** - When this bit is set to a logical one, the Data RDY status flag will become active when the Sample Buffer becomes half-full. When this bit is set to a logical zero, the Data RDY status flag will become active when the Sample Buffer is full. If the Buffer Size is set to one sample, this bit does not affect the Data RDY status flag which will be set each time the sample is stored in the Sample Buffer. (Default is logical zero.)

Bit 13: **Enable Trigger** - When this bit is set to a logical one, the VMIVME-3119 can be triggered from an external source. (Default is logical zero.)

Bit 12: **Data FMT - Data Format** - When this bit is set to a logical one the data samples will be stored in offset binary format. When this bit is a logical zero the data samples will be stored in two's complement format. (Default is logical zero.)

Bits 11 through 08: **Reserved** - These bits are reserved and should be written as zero.

Bit 07: **ST_EN, Scan Table Enable** - When this bit is set to a logical zero all channels will be stored in order (i.e. 0 through 15 for a 16-channel VMIVME-3119). When this bit is set to a logical one the channels will be scanned in the order defined in the Scan Table. (Default is logical zero.)

Global Control Bit Definitions (Continued)

Bits 06 through 04: SM[2:0], Scan Mode - This field is used to select the scan mode of the VMIVME-3119 as shown in Table 3-6. (Default is 000.)

Table 3-6 Scan Modes (SM[2:0])

SP[2..0]	Scan Mode
000	Continuous Scan
001	Single Scan
010	Single Scan and Rearm
011	Advance Scan on Trigger
100	Disabled (reserved for future use)
101	Disabled (reserved for future use)
110	Disabled (reserved for future use)
111	Disabled (reserved for future use)

Bits 03 through 00: TM[3:0], Trigger Mode - This field is used to select the trigger mode of the VMIVME-3119 as shown in Table 3-7.

Table 3-7 Trigger Modes

TM[3:0]	Trigger Mode
0000	Disabled
0001	Single-Board, Software
0010	Single-Board, Single-Ended External
0011	Multiboard, Master - Software
0100	Multiboard, Master - Single-Ended External
0101	Multiboard, Slave - Differential External
0110	Disabled (reserved for future use)
0111	Disabled (reserved for future use)
1000	Disabled (reserved for future use)
1001	Disabled (reserved for future use)
1010	Disabled (reserved for future use)
1011	Disabled (reserved for future use)
1100	Disabled (reserved for future use)
1101	Disabled (reserved for future use)
1110	Disabled (reserved for future use)
1111	Disabled (reserved for future use)

Global Status Register (GSR)

The GSR is a read-only status register which indicates global status of the VMIVME-3119. Table 3-8 shows the bit map.

Table 3-8 Global Status Register Bit Map

Global Status Register (Offset $00 0006) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
RSVD1	MSIZE2	MSIZE1	MSIZE0	ERR3	ERR2	ERR1	ERR0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
DATA RDY	Armed	TRIGD	0	0	TEST DIS	RSVD0	CFG CMPLT

Global Status Register Bit Defintions

Bit 15: **RSVD1** - This bit indicates the status of jumper E8. A logical zero indicates that the jumper is installed. This jumper is not currently used.

Bits 14 through 12: **MSIZE [2:0]** - This field indicates the state of the VMEbus Memory size jumpers. A logical zero indicates that the corresponding jumper is installed.

Bits 11 through 08: **ERR[3:0], Error Code** - This field indicates the VMIVME-3119 errors as defined in Table 3-9.

Table 3-9 Error Codes (ERR[3:0])

ERR [3:0]	Error Code
0000	No Error
0001	DRAM Failure
0010	SRAM Failure
0011	ADC Failure
0100	Channel Failure
0101	Invalid Scan Mode
0110	Invalid Trigger Mode
0111	Invalid Buffer Size
1000	Invalid Sample Rate
1001	Invalid Scan Table Length
1010	Reserved
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Catastrophic Error - No error code returned or multiple error codes returned.

Global Status Register Bit Defintions (Continued)

Bit 07: **DATA RDY: Data Ready** - A logical one indicates that the Data Buffer is full or half-full, depending on the state of Flag HF. This bit is set to a logical zero by the Clear Flag Command.

Bit 06: **Armed, Scan Armed** - A logical one indicates that the scan is armed but not yet triggered. This bit is returned to a logical zero by VMIVME-3119 firmware when a change in configuration has been detected or when a scan is triggered.

Bit 05: **TRIGD: Scan Triggered** - A logical one indicates that a trigger has been received and a scan is in progress. This bit is returned to a logical zero by VMIVME-3119 firmware when a scan is completed or the Abort / Restart Scan Command is received.

Bits 04 and 03: **Reserved** - These bits are reserved and should be written to zero.

Bit 2: **TEST DIS, Test Disabled** - This bit indicates the state of the self-test disable jumper. A logical one indicates that self-test has been disabled.

Bit 1: **RSVD0** - This bit indicates the state of the RSVD0 jumper in jumper field E6. A logical zero indicates that the jumper is installed. This jumper is not currently used.

Bit 00: **CFG CMPLT, Configuration Complete** - A logical one indicates that the change in configuration programmed through any of the VMIVME-3119 registers has been detected and processed by the on-board DSP. This bit is returned to a logical zero by the Clear Flag Command.

Sample Clock Prescale Register (PSR)

The PSR is a read / write data register which controls the (prescale) clock input of the Sample Rate Counter.

Table 3-10 Sample Clock Prescale Register Bit Map

Sample Clock Prescale Register (Offset $00 0008) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

Sample Clock Prescale Bit Defintions

Bits 15 through 08: Reserved - These bits are reserved and should be written to zero.

Bits 07 through 00: PS[7:0], Sample Clock Prescale - This field determines the period of the (prescale) clock input of the Sample Rate Counter according to the equation:

Period of (prescale) clock input = (Sample clock prescale +1) x (50 nsec)
(Default is 0x00)

Sample Clock Period Register (SPR)

The SPR is a read / write data register which determines (in conjunction with the Sample Clock Prescale Register) the period of the internally generated Sample Rate Clock. The bit map for the Sample Clock Period Register is shown below. The bit definitions can be found below.

Table 3-11 Sample Clock Period Register Bit Map

Sample Clock Period Register (Offset $00 000A) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

Sample Clock Period Register Bit Definitions

Bits 15 through 00: **SP[15:0], Sample Clock Period** - This field determines the period of the sample clock of the VMIVME-3119 according to the equation: Sample Period = (Sample clock period + 1) x (Sample clock prescale + 1) x (50 nsec) (Default is 0x03E7 - providing a sample period of 50 µsec)

NOTE: The minimum sample period of the VMIVME-3119 is 10 µsec, therefore, the following equation must hold for all values of sample clock prescale and sample clock period:

(Sample clock period + 1) x (Sample clock prescale + 1) ≥ 200

Example: A sample rate of 50 kHz is desired.

(Sample clock period + 1) x (Sample clock prescale + 1) = 20 msec / 50 nsec = 400

let (Sample clock prescale) = 0

and (Sample clock period) = 399 = 0x018F

IRQ Control Register (ICR)

The ICR is a read / write data register which enables the VMEbus interrupt and contains the VMEbus interrupt Vector for the VMIVME-3119. Table 3-12 shows the bit map for the IRQ Control Register. The bit definitions can be found on below.

Table 3-12 IRQ Control Register Bit Map

IRQ Control Register (Offset $00 000C) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	I EN

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
I VEC7	I VEC6	I VEC5	I VEC4	I VEC3	I VEC2	I VEC1	I VEC0

IRQ Control Register Bit Definitions

Bits 15 through 09: Reserved - These bits are reserved and should be written to zero.

Bit 08: I EN, Interrupt Enable - A logical zero causes the VMEbus interrupt request to be disabled, independent of the state of the interrupt level configuration jumpers. This bit must be set to a logical one to enable the VMEbus interrupt on a Data Ready condition. (Default is logical zero.)

Bits 07 through 00: I VEC[7:0], Interrupt Vector - This field contains the VMIVME-3119 VMEbus Interrupt Vector which will be returned during a VMEbus interrupt acknowledge cycle. (Default is 0x000.)

IRQ Status Register (ISR)

The ISR is a read-only status register which returns the status of the interrupt level configuration jumpers of the VMIVME-3119. The bit definitions for this register are shown below.

Table 3-13 IRQ Status Register Bit Map

IRQ Status Register (Offset $00 000E) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	I LVL2	I LVL1	I LVL0

IRQ Status Register Bit Definitions

Bits 15 through 03: Reserved - These bits are reserved.

Bits 02 through 00: I LVL[2:0]: Interrupt Level - This field indicates the level of the VMIVME-3119 VMEbus IRQ according to Table 3-14. This field is status (read only); the IRQ level is set by configuration jumper E7.

Table 3-14 IRQ Status Interrupt Level [2:0]

I LVL [2:0]	VMEbus IRQ Level
000	Disabled
001	IRQ1*
010	IRQ2*
011	IRQ3*
100	IRQ4*
101	IRQ5*
110	IRQ6*
111	IRQ7*

Low Channel Gain Register (LGR)

The LGR is a read / write data register which controls the gain of channels 0 through 7 of the VMIVME-3119.

Table 3-15 Low Channel Gain Register Bit Map

Low Channel Gain Register (Offset $00 0010) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH7 G1	CH7 G0	CH6 G1	CH6 G0	CH5 G1	CH5 G0	CH4 G1	CH4 G0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH3 G1	CH3 G0	CH2 G1	CH2 G0	CH1 G1	CH1 G0	CH0 G1	CH0 G0

Low Channel Gain Register Bit Definitions

Bits 15 through 00: CHx G[1:0] - This field controls the gain for channel x according to Table 3-16. (Default is 00 - corresponding to a gain of 1.)

Table 3-16 Low Channel Gain Bit Definitions (CHx G[1:0])

CHx G[1:0]	Gain	Input Voltage Range for CHx
00	1	±10 V
01	10	±1 V
10	100	±100 mV
11	1,000	±10 mV

High Channel Gain Register (HGR)

The HGR is a read / write data register which controls the gain of channels 8 through 15 of the VMIVME-3119.

Table 3-17 High Channel Gain Register Bit Map

High Channel Gain Register (Offset $00 0012) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH15 G1	CH15 G0	CH14 G1	CH14 G0	CH13 G1	CH13 G0	CH12 G1	CH12 G0
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH11 G1	CH11 G0	CH10 G1	CH10 G0	CH9 G1	CH9 G0	CH8 G1	CH8 G0

High Channel Gain Register Bit Definitions

Bits 15 through 00: CHx G[1:0], Channel Gain - This field controls the gain for channel x according to Table 3-18. (Default is 00 - corresponding to a gain of 1.)

Table 3-18 High Channel Gain Bit Definitions (CHx G[1:0])

CHx G[1:0]	Gain	Input Voltage Range for CHx
00	1	±10 V
01	10	±1 V
10	100	±100 mV
11	1,000	±10 mV

Low Channel Filter Register (LFR)

The LFR is a read / write data register which controls the cutoff frequency of the Bessel or Butterworth filter options for channels 0 through 7 of the VMIVME-3119. These bits should always be written to zero for a no filter option board.

Table 3-19 Low Channel Filter Register Bit Map

Low Channel Filter Register (Offset $00 0014) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH7 F1	CH7 F0	CH6 F1	CH6 F0	CH5 F1	CH5 F0	CH4 F1	CH4 F0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH3 F1	CH3 F0	CH2 F1	CH2 F0	CH1 F1	CH1 F0	CH0 F1	CH0 F0

Low Channel Filter Register Bit Definitions

Bits 15 through 00: **CHx F[1:0]** - This field controls the cutoff frequency of the Bessel or Butterworth filter options according to Table 3-20. (Default is 00 - corresponding to a cutoff frequency of 1000 Hz.)

Table 3-20 Low Channel Filter Register Bit Definitions (CHx G[1:0])

CHx F[1:0]	Cutoff Frequency
00	1,000 Hz
01	100 Hz
10	10 Hz
11	1 Hz

High Channel Filter Register (HFR)

The HFR is a read / write data register which controls the cutoff frequency of the Bessel or Butterworth filter options for channels 8 through 15 of the VMIVME-3119. These bits should always be written to zero for a no filter option board.

Table 3-21 High Channel Filter Register Bit Definitions

High Channel Filter Register (Offset $00 0016) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH15 F1	CH15 F0	CH14 F1	CH14 F0	CH13 F1	CH13 F0	CH12 F1	CH12 F0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH11 F1	CH11 F0	CH10 F1	CH10 F0	CH9 F1	CH9 F0	CH8 F1	CH8 F0

High Channel Filter Register Bit Definitions

Bits 15 through 00: CHx F[1:0] - This field controls the cutoff frequency of the Bessel or Butterworth filter options according to Table 3-22. (Default is 00 - corresponding to a cutoff frequency of 1,000 Hz.)

Table 3-22 High Channel Filter Register Bit Definitions

CHx F[1:0]	Cutoff Frequency
00	1,000 Hz
01	100 Hz
10	10 Hz
11	1 Hz

Buffer Size Register (BSR)

The BSR is a read / write data register which controls the size of the VMIVME-3119 Sample Buffer.

Table 3-23 Buffer Size Register Bit Map

Buffer Size Register (Offset $00 0018) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	BS4	BS3	BS2	BS1	BS0

Buffer Size Register Bit Definitions

Bits 15 through 05: Reserved - These bits are reserved and should be written to zero.

Bits 04 through 00: BS[4:0]: Buffer Size - This field controls the size of the VMIVME-3119 Scan Buffer according to Table 3-24.

Table 3-24 Buffer Size Register Bit Definitions (BS[4:0])

BS[4:0]	Buffer Size (bytes)	Buffer Size (Samples)
0 0000	2	1
0 0001	4	2
0 0010	8	4
0 0011	16	8
0 0100	32	16
0 0101	64	32
0 0110	128	64
0 0111	256	128
0 1000	512	256
0 1001	1 k	512
0 1010	2 k	1 k
0 1011	4 k	2 k
0 1100	8 k	4 k
0 1101	16 k	8 k
0 1110	32 k	16 k
0 1111	64 K	32 K
1 0000	128 K	64 K
1 0001	256 K	128 K
1 0010	512 K	256 K
1 0011	1,024 K	512 K
1 0100	2,048 K	1,024 K
1 0101	4,096 K	2,048 K
1 0110	8,192 K	4,096 K
1 0111 . 1 1111	Reserved	

Clear Flag Command Register (CFR)

The CFR is a read / write register, used to clear the Data Ready and the Configuration Complete status flags of the GCR.

Table 3-25 Clear Flag Command Register Bit Map

Clear Flag Command Register (Offset $00 001A) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	CLR FLG

Clear Flag Command Register Bit Definitions

Bits 15 through 01: **Reserved** - These bits are reserved and should be written to zero.

Bit 00: **CLR FLG: Clear Flag Command** - A logical one causes the VMIVME-3119 to clear the Data Ready and the Configuration Complete status flags of the GCR. This bit is returned to a logical zero by VMIVME-3119 firmware when the Data Ready and Configuration Complete flags have been cleared.

Calibration Channel Select Register (CSR)

The CSR is a read / write data register which selects channels to be calibrated when the Calibration Command is issued. Table 3-26 is the bit map for Calibration Channel Select Register.

Table 3-26 Calibration Channel Select Register Bit Map

Calibration Channel Select Register (Offset $00 001C) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CS15	CS14	CS13	CS12	CS11	CS10	CS9	CS8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0

Calibration Channel Select Register Bit Definitions

Bits 15 through 00: CS[15:0]: Calibration Select - A logical one in bit location CSx selects channel x to be calibrated when the Calibrate Command is issued. (Default is logical zero for each channel.)

Calibration Configuration Select Register (CCR)

The CCR is a read / write data register that selects which gain and filter configuration to be calibrated when the Calibration Command is issued.

Table 3-27 Calibration Configuration Select Register Bit Map

Calibration Configuration Select Register (Offset $00 001E) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CAL 1 Hz	CAL 10 Hz	CAL 100 Hz	CAL 1 kHz	CAL 10 mV	CAL 100 mV	CAL 1 V	CAL 10 V

Calibration Configuration Select Register Bit Definitions

Bits 15 through 08: **Reserved** - These bits are reserved and should be written to zero.

Bits 07 through 04: **CAL xHz: Calibrate with xHz Filter** - A logical one in bit location CAL xHz causes the calibration routine, when executed, to generate new gain and offset coefficients for the xHz filter with all gains selected by bits CAL xV. (Default for each is logical zero.) For a no filter option board, bits 5 through 7 should always be written to zero, and bit 4 should be written to one.

Bits 03 through 00: **CAL xV: Calibrate with ±x V Range** - A logical one in bit location CAL xV causes the calibration routine, when executed, to generate new gain and offset coefficients for the xV range with all filter cutoffs selected by bits CAL xHz. (Default for each is logical zero.)

Reset Command Register (RST)

The RST is a read / write register which is used to command the VMIVME-3119 to be reset.

Table 3-28 Reset Command Register Bit Map

Reset Command Register (Offset $00 0020) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	Reset

Reset Command Register Bit Definitions

Bits 15 through 01: **Reserved** - These bits are reserved and should be written to zero.

Bit 00: **Reset, Reset Command** - A logical one causes the VMIVME-3119 to run self-test and return all registers, tables, and buffer to their default conditions. This bit is returned to a logical zero by VMIVME-3119 firmware when reset is complete.

Calibration Command Register (CAL)

The CCR is a read / write register which allows selected channels of the VMIVME-3119 to calibrate. Table 3-29 is the bit map for the Calibration Command Register. When a scan is active, this command will not be processed until a Abort / Restart Scan Command is received.

Table 3-29 Calibration Command Register Bit Map

Calibration Command Register (Offset $00 0022) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	CAL

Calibration Command Register Bit Definitions

Bits 15 through 01: **Reserved** - These bits are reserved and should be written to zero.

Bit 00: **CAL, Calibration Command** - A logical one causes the VMIVME-3119 to calibrate all channels selected in the CSR. This bit is returned to a logical zero by VMIVME-3119 firmware when the calibration is complete.

Self-Test Command Register (STC)

The STC is a read / write register which is used to command the VMIVME-3119 to execute its self-test routine. The results of the self-test are stored in the Self-Test Status Register. See Table 3-30 for register bits. When a scan is active, this command will not be processed until an Abort / Restart Scan Command is received.

Table 3-30 Self-Test Command Register Bit Map

Self-Test Command Register (Offset $00 0024) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	Test

Self-Test Command Register Bit Definitions

Bits 15 through 01: **Reserved** - These bits are reserved and should be written to zero.

Bit 00: **Test, Self-Test Command** - A logical one causes the VMIVME-3119 to execute self-test routine. This bit is returned to a logical zero by VMIVME-3119 firmware when the self-test is complete.

Self-Test Status Register (TSR)

The TSR is a read-only status register which indicates any channels which have failed to pass self-test.

Table 3-31 Self-Test Status Register Bit Map

Self-Test Status Register (Offset $00 0026) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fail CH15	Fail CH14	Fail CH13	Fail CH12	Fail CH11	Fail CH10	Fail CH9	Fail CH8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Fail CH7	Fail CH6	Fail CH5	Fail CH4	Fail CH3	Fail CH2	Fail CH1	Fail CH0

Self-Test Status Register Bit Definitions

Bits 15 through 00: **Fail CH[15:0]** - A logical one indicates that the corresponding channel has failed self-test. A logical zero indicates that the corresponding channel has not failed self-test. For 8-channel option of the VMIVME-3119, Fail CH[15:8] will always be logic zero.

Software Trigger Command Register (TRG)

The TRG is a read / write register which is used to trigger a VMIVME-3119 scan.

Table 3-32 Software Trigger Command Register Bit Map

Software Trigger Command Register (Offset $00 0028) Read Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	TRIG

Software Trigger Command Register Bit Definitions

Bits 15 through 01: Reserved - These bits are reserved and should be written to zero.

Bit 00: TRIG, Trigger Command - A logical one causes the VMIVME-3119, if armed, to be triggered. This bit is returned to a logical zero by VMIVME-3119 firmware when the trigger is detected.

Abort/Restart Scan Command Register (ABT)

The ABT is a read / write register which is used to command the VMIVME-3119 to abort an active scan.

Table 3-33 Abort/Restart Scan Command Register Bit Map

Abort/Restart Scan Command Register (Offset $00 002A) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	Abort / Restart

Abort/Restart Scan Command Register Bit Definitions

Bits 15 through 01: Reserved - These bits are reserved and should be written to zero.

Bit 00: Abort, Abort/Restart Scan Command - A logical one causes the VMIVME-3119 to abort an active scan. This bit is returned to a logical zero by VMIVME-3119 firmware when the scan is aborted.

DSP Peek Address Register (PAR)

The PAR is a read / write data register which is used as a debug interface to the VMIVME-3119 DSP. Writing the address of a word in the DSP internal data RAM will cause that word to be returned to the DSP Peek Data Register. This is not a user programmable register.

Table 3-34 DSP Peek Address Register Bit Map

DSP Peek Address Register (Offset $00 002C) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	PA13	PA12	PA11	PA10	PA9	PA8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

DSP Peek Address Register Bit Definitions

Bits 15 through 14: Reserved - These bits are reserved and should be written to zero.

Bits 13 through 00: PA[13:0], Peek Address - The address of the word in internal DSP data RAM that is to be returned to the DSP Peek Data Register.

DSP Peek Data Register (PDR)

The PDR is a read-only data register which is used as a debug interface to the VMIVME-3119 DSP. The data in this register will correspond to the word in internal DSP data RAM pointed to by the address in the Peek Address Register. This register is not a user programmable register.

Table 3-35 DSP Peek Data Register Bit Map

DSP Peek Data Register (Offset $00 002E) Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

DSP Peek Address Register Bit Definitions

Bits 15 through 00: PD[15:0]: Peek Data - The word in DSP data RAM that is pointed to by the DSP Peek Address Register.

LED Control Register (LCR)

The LCR is a read / write register which is used to control front panel LED of the VMIVME-3119.

Table 3-36 LED Control Register Bit Map

LED Control Register (Offset $00 0030) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	LED On

LED Control Register Bit Definitions

Bit 00: **LED On** - A logical one causes the VMIVME-3119 front panel LED to turn on. A logical zero turns the LED off.

Reference Calibration Mode Register (RCM)

The RCM is a read / write register which is used to advance the reference voltage during voltage reference calibration under software control.

Table 3-37 Reference Calibration Mode Register Bit Map

Reference Calibration Mode Register (Offset $00 0040) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	ADV

Reference Calibration Mode Register Bit Definitions

Bit 00: **ADV, Advance** - During reference calibration, a logical one causes the VMIVME-3119 to advance the reference voltage (see Chapter 1 “Theory of Operation”.) This bit is returned to a logical zero by the DSP.

Reference Calibration Code Register (RCC)

The RCC is a read / write register which is used to calibrate the reference voltages under software control.

Table 3-38 Reference Calibration Code Register Bit Map

Reference Calibration Code Register (Offset $00 0042) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
RCC15	RCC14	RCC13	RCC12	RCC11	RCC10	RCC9	RCC8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0

Reference Calibration Code Register Bit Definitions

Bits 15 through 00: RCC[15:0], Reference Calibration Code - This code controls the voltage output by the VMIVME-3119 during reference voltage calibration. This is a binary code representing a voltage between 0 V and 10 V.

Reference Calibration Status Register (RCS)

The RCS is a read / write register which indicates the current reference voltage being calibrated (see Chapter 1).

Table 3-39 Reference Calibration Status Register Bit Map

Reference Calibration Status Register (Offset $00 0044) Read/Write							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
0	0	0	0	0	0	0	0

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
0	0	0	0	RCS3	RCS2	RCS1	RCS0

Reference Calibration Status Register Bit Definitions

Bits 15 through 04: **Reserved** - These bits are reserved.

Bits 03 through 00: **RCS[3:0]: Reference Calibration Status** - When performing reference calibration under software control, this code indicates the current reference voltage value being calibrated as described in Chapter 1 “Theory of Operation”.

Reference Calibration Enable HW and LW Registers (REH and REL)

Table 3-40 Reference Calibration Enable HW and LW Registers, Bit Map

Reference Calibration Enable HW Register (Offset $00 0046) Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
RCK31	RCK30	RCK29	RCK28	RCK27	RCK26	RCK25	RCK24

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
RCK23	RCK22	RCK21	RCK20	RCK19	RCK18	RCK17	RCK16

Reference Calibration Enable LW Register (Offset $00 0048) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 012**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
RCK15	RCK14	RCK13	RCK12	RCK11	RCK10	RCK9	RCK8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
RCK7	RCK6	RCK5	RCK4	RCK3	RCK2	RCK1	RCK0

Reference Calibration Enable Register Bit Definitions

Bits 31 through 00: **RCK[31:0] -** This is a software key which allows reference calibration to be performed under software control. The procedure for reference calibration is described in Chapter 1 “Theory of Operation”.

Scan Table (SCN)

The SCN is a 256-byte table used for entering the desired scan sequence of the VMIVME-3119. The Scan Table determines the scan sequence when the ST_EN bit of GCR is a logical one.

Table 3-41 Scan Table

Offset	Function	Access
$0 0400	Table Entry o	Read / Write
$0 0401	Table Entry1	Read / Write
. . .	. . .	. . .
$0 04FE	Table Entry 244	Read / Write
$0 04FF	Table Entry 255	Read / Write

Table 3-42 Scan Table Bit Map

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
End ST	0	0	0	CH S3	CH S2	CH S1	CH S0

Scan Table Bit Defintions

Bit 07: **End ST, End of Scan Table** - This bit, when set to a logical one indicates the last entry of the scan table. The length of the Scan Table must be a power-of-two and must be equal to or less than the Buffer Size.

Bits 06 through 04: **Reserved** - These bits are reserved and should be written to zero.

Bits 03 through 00: **CH S[3:0]: Channel Select** - The field selects the channel to be scanned.

Example: A Buffer Size of eight has been programmed in the Buffer Size Register. The desired scan sequence is (0, 1, 0, 2, 0, 3, 0, 4.)

The Scan Table for this example would be as follows:

Offset	Scan Table Entries	
$0 0400	0x00	
$0 0401	0x01	
$0 0402	0x00	
$0 0403	0x02	Length of
$0 0404	0x00	Scan Table = 8
$0 0405	0x03	
$0 0406	0x00	
$0 0407	0x84	
$0 0408	Don't Care	
.	Don't Care	
$0 04FF	Don't Care	

User Calibration Coefficients

This area of SRAM contains the gain and offset coefficients for each channel in each of the gain / filter settings. These coefficients may be user modified to compensate for gain or offset errors in input signal sources such as sensors or amplifiers. In response to a power up or VMEbus reset or in response to a Calibration Command, this area is overwritten with the gain / offset coefficients stored in EEPROM. Updates to the User Calibration Coefficients are retrieved by the DSP when a change in configuration is detected or when the Abort / Restart Scan Command is issued. The organization of these coefficients is as shown in Table 3-43.

Table 3-43 User Calibration Coefficients

$00 0800 . $00 081E	Channel 0 Gain 10 V / 1 kHz, or no filter . Channel15 Gain 10 V.1 kHz, or no filter
$00 0820 . $00 083E	Channel 0 Offset 10 V / 1 kHz, or no filter . Channel 15 Offset 10 V / 1 kHz, or no filter
$00 0840 . $00 085E	Channel 0 Gain 1 V / 1 kHz, or no filter Channel 15 Gain 1 V / 1 kHz, or no filter
$00 0860 . $00 087E	Channel 0 Offset 1 V / 1 kHz, or no filter . Channel 15 Offset 1 V / 1 kHz, or no filter
$00 0880 . $00 089E	Channel 0 Gain 100 mV / 1 kHz, or no filter . Channel 15 Gain 100 mV / 1 kHz, or no filter
$00 08A0 . $00 08BE	Channel 0 Offset 100 mV / 1 kHz, or no filter . Channel 15 Offset 100 mV / 1 kHz, or no filter
$00 08C0 . $00 08DE	Channel 0 Gain 10 mV / 1 kHz, or no filter . Channel 15 Gain 10 mV / 1 kHz, or no filter
$00 08E0 . $00 08FE	Channel 0 Offset 10 mV / 1 kHz, or no filter . Channel 15 Offset 10 mV / 1 kHz, or no filter
$00 0900 . $00 091E	Channel 0 Gain 10 V / 100 Hz . Channel 15 Gain 10 V / 100 Hz
$00 0920 . $00 093E	Channel 0 Offset 10 V / 100 Hz . Channel 15 Offset 10 V / 100 Hz
$00 0940 . $00 095E	Channel 0 Gain 1 V / 100 Hz . Channel 15 Gain 1 V / 100 Hz
$00 0960 . $00 097E	Channel 0 Offset 1 V / 100 Hz . Channel 15 Offset 1 V / 100 Hz
$00 0980 . $00 099E	Channel 0 Gain 100 mV / 100 Hz . Channel 15 Gain 100 mV / 100 Hz
$00 09A0 . $00 09BE	Channel 0 Offset 100 mV / 100 Hz . Channel 15 Offset 100 mV / 100 Hz

Table 3-43 User Calibration Coefficients (Continued)

$00 09C0 . $00 09DE	Channel 0 Gain 10 mV/100 Hz . Channel 15 Gain 10 mV/100Hz
$00 09E0 . $00 09FE	Channel 0 Offset 10 mV/100 Hz . Channel 15 Offset 10 mV/100 Hz
$00 0A00 . $00 0A1E	Channel 0 Gain 10 V/10 Hz . Channel 15 Gain 10 V/10 Hz
$00 0A20 . $00 0A3E	Channel 0 Offset 10 V/10 Hz . Channel 15 Offset 10 V/10 Hz
$00 0A40 . $00 0A5E	Channel 0 Gain 1 V/10 Hz . Channel 15 Gain 1V/10 Hz
$00 0A60 . $00 0A7E	Channel 0 Offset 1 V1 KHz . Channel 15 Offset 1 V/1 KHz
$00 0A80 . $00 0A9E	Channel 0 Gain 100 mV/10 Hz . Channel 15 Gain 100 mV/10 Hz
$00 0AA0 . $00 0ABE	Channel 0 Offset 100 mV/10 Hz .. Channel 15 Offset 100 mV/10 Hz
$00 0AC0 . $00 0ADE	Channel 0 Gain 10 mV/10 Hz .. Channel 15 Gain 10 mV/10 Hz
$00 0AE0 . $00 0AFE	Channel 0 Offset 10 mV/10 Hz . Channel 15 Offset 10 mV/10 Hz
$00 0B00 . $00 0B1E	Channel 0 Gain 10 V/1 Hz . Channel 15 Gain 10 V/1 Hz
$00 0B20 . $00 0B3E	Channel 0ffset 10 V/1 Hz . Channel 15 Offset 10 V/1 Hz
$00 0B40 . $00 0B5E	Channel 0 Gain 1 V/1 Hz .. Channel 15 Gain 1 V/1 Hz
$00 0B60 . $00 0B7E	Channel 0 Offset 1 V/1 Hz . Channel 15 Offset 1 V/1 Hz
$00 0B80 . $00 0B9E	Channel 0 Gain 100 mV/1 Hz . Channel 15 Gain 100 mV/1 Hz
$00 0BA0 . $00 0BBE	Channel 0 Offset 100 mV/1 Hz .. Channel 15 Offset 100 mV/1 Hz
$00 0BC0 . $00 0BDE	Channel 0 Gain 10 mV/1 Hz . Channel 15 Gain 10 mV/1 Hz
$00 0BE0 . $00 0BFE	Channel 0 Offset 10 mV/1 Hz .. Channel 15 Offset 10 mV/1 Hz

Table 3-44 User Gain Coefficient

User Gain Coefficient							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	GN13	GN12	GN11	GN10	GN9	GN8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
GN7	GN6	GN5	GN4	GN3	GN2	GN1	GN0

User Gain Bit Definitions

Bit 15: **GNl13:0]** - Code representing the residual (in excess of 1) gain applied to the given channel.

Table 3-45 User Offset Coefficient

User Offset Coefficient							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
OFST15	OFST14	OFST13	OFST12	OFST11	OFST10	OFST9	OFST8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
OFST7	OFST6	OFST5	OFST4	OFST3	OFST2	OFST1	OFST0

User Offset Bit Definitions

Bits 15 through 00: Offsetl15:0] - Two's Complement code representing the channel offset.

Example:

A VMIVME-3119 has channel 0 configured for the ±10 V range and 1 kHz Filter. A User wishes to change the gain coefficient to provide a gain of 1.01 instead of the default 1.00 and wishes also to offset the input signal by +1.0 mV. The user must first read the gain and offset for channel 0. The gain is read from address offset $00 0800 and is denoted here by m. The offset is read from address offset $00 0820 and is denoted here by b. Note that m and b as read from the VMIVME-3119 are HEX codes.

First, the user must determine the uncorrected channel gain denoted here by an a. This is found by solving the equation:

$\mathbf{a} \times (1 + \mathbf{m} / 2^{15}) = 1.00$

For this example, let **m** = 140h =320. Also let **b** = 4h = 4.

$\mathbf{a} = 1.00 / (1 + 320 / 2^{15}) = 0.99032882$

Next, solve for the new gain coefficient, denoted here by **m**',

$\mathbf{a} \times (1 + \mathbf{m'} / 2^{15} = 1.01$ so $\mathbf{m}' = \{ (1.01 / 0.99032882) - 1 \} \times 2^{15}$

= 650.879 ~ 28Bh

Therefore for a gain of 1.01, the code to be written back to address offset $00 0800 is 28Bh.

The desired offset is +1.0 mV. Determine the HEX code corresponding to this offset and denote as **c**. Also denote the new offset as **b'**.

c = +0.001 V / (10 V / 2^{15}) = 3.278 ~ 3h

and **b'** = **b** + **c** = 4h +2h = 6h

Therefore, the new offset to be written to address offset $00 0820 is 6h.

NOTE: Since the VMIVME-3119 is normally calibrated to produce an overall gain near 1.0 and an OFFSET near 0, the user should be aware that a change in either gain or OFFSET will affect the usable dynamic range of the altered channel.

Sample Buffer (SPL)

The SPL is a up to 8 Mbyte (4 MSample) buffer for sample storage. The size of the buffer is programmed in the Buffer Size Register. Table 3-46 shows the Sample Buffer, Table 3-47 is the bit map for the Sample Buffer Register.

Table 3-46 Sample Buffer Register Map

Offset	Function	Access
P	Sample 0	Read / Write
P + 2	Sample 1	Read / Write
. . .	. . .	. . .
P + BS - 4	Sample (n - 2)	Read / Write
P + BS - 2	Sample (n -1)	Read / Write

BS = Buffer Size (bytes) set in the Buffer Size Register.

P = base address of Sample Buffer set by configuration Jumpers.

n = Buffer Size (Samples).

Table 3-47 Sample Buffer Bit Map

Sample Buffer, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SMPL15	SMPL14	SMPL13	SMPL12	SMPL11	SMPL10	SMPL9	SMPL8

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SMPL7	SMPL6	SMPL5	SMPL4	SMPL3	SMPL2	SMPL1	SMPL0

Sample Buffer Bit Defintions

Bits 15 through 00: SMPL[15:0] - Data representing the sample voltage. Table 3-48 and Table 3-49 give examples for the three possible data formats.

Table 3-48 Example: Bipolar Input Voltages and Data Representation (Two's Complement Data Format)

Input Voltage	Data Representation
Negative Full-Scale	$8000
Mid-Scale	$0000
Positive Full-Scale	$7FFF

Table 3-49 Example: Bipolar Input Voltages and Data Representation (Offset Binary Data Format)

Input Voltage	Data Representation
Negative Full-Scale	$0000
Mid-Scale	$8000
Positive Full-Scale	$FFFF

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Care at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.