VMIVME-3125
Analog Input Board

Product Manual

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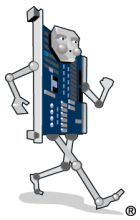

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Overview

Features

The VMIVME-3125 Analog Input boards provide automatic scanning of 16 differential or 32 single-ended analog input channels. The channels are digitized with a 12-bit resolution Analog-to-Digital Converter (ADC). Each input is overvoltage protected and low-pass filtered. The board is very easy to use, no software setup is required. After powerup or system reset, the VMIVME-3125 automatically starts scanning each of its 16 or 32 input channels. Conversion data is stored automatically in a dual-port memory, making it immediately accessible from the VMEbus. The VMIVME-3125 provides on-board voltage references to perform an on-line or off-line built-in self-test. The input voltage range and gain are user-programmable with jumpers. The VMEbus base address and the access mode are fully selectable.

Some of the distinguishing features of the VMIVME-3125 include:

- VMEbus 6U single height format
- 16 differential or 32 single-ended analog input channels
- One 12-bit A / D converter with built-in track-and-hold
- Automatic scanning of all inputs at 40 kHz aggregate rate
- No software initialization required to begin scanning
- Input ranges from ±50 mV to ±10 VDC
- Input overvoltage protection
- Analog inputs are low-pass filtered at 50 kHz
- Optional add on 40 Hz low-pass filter daughter board
- Discrete wire or mass terminated cables
- Input pull-down resistors prevent floating inputs
- Supports on-line and off-line Built-In-Test (BIT)
- Jumper programmable gains of x1, x10, x100
- Selectable A / D ranges of ±5 VDC, ±10 VDC and 0 to 10 VDC
- Data Accesses: D16, D08(EO), D08(O)
- Front panel LED

- 1,000 VDC isolation between analog and digital ground
- Optional 0 - 20, 4 - 20, and 5 - 25 mA current input ranges

The VMIVME-3125 occupies 128 bytes of short I/O VMEbus addressing space. Jumpers are provided to place the board on any 128-byte boundary. The board may also be jumper-programmed to respond to supervisory, nonprivileged, or both accesses.

Conversion data is available from a 16-bit register (12-bit right justified with optional sign extension). This data is stored in on-board dual-ported memory for easy access.

The Built-In-Test (BIT) capability permits the user to verify the on-board ADC using high precision, user-programmable reference voltages. Software controls the BIT functions.

After a system reset, the board returns to a fixed configuration: all bits in the Control/Status Register are cleared and the front panel FAIL LED is illuminated. The LED is then extinguished under software control. This LED can be used to visually locate a faulty board in a system.

References

VMEbus Specification Rev. C. and the VMEbus Handbook

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(602) 951-0720 (FAX)
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Physical Description and Specification

Refer to 800-003125-000 Specification

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

CHAPTER

1

Theory of Operation

Contents

Introduction

The VMIVME-3125 is a flexible, low-cost analog input board that provides 16 differential or 32 single-ended analog input channels. The channels are scanned continuously at an aggregate rate of 40 kHz using a 12-bit resolution Analog-to-Digital Converter (ADC). Channels can be randomly or sequentially read at any time. The current address of the channel being digitized is read from the Channel Pointer Register. Scanning may be halted at the current channel using the Stop Auto Scan bit in the Control / Status Register. This will disable further channel address increments. The board will then lock onto that channel. This allows a single channel to be digitized every 25 µsec. The following sections discuss the functional components of the VMIVME-3125 in detail.

Functional Organization

The VMIVME-3125 is divided into the following functional categories. Each category is discussed in detail.

- VMEbus Interface
- Analog-to-Digital Converter (ADC) and Control Logic
- Analog Input Multiplexing, Gain, and Conversion
- BIT Voltage Reference and multiplexer
- Board ID register

Figure 1-1 on page 18 illustrates the functional blocks of the VMIVME-3125.

VMEbus Interface

The VMIVME-3125 communications registers are memory mapped as 64 16-bit words (128 bytes) in memory. The registers are contiguous and can be located on any 128 byte boundary within the short I/O space of the VMEbus. The board can be configured to respond to short supervisory or short nonprivileged data accesses, or both. See “Configuration and Installation” on page 27 for address jumper locations and configurations.

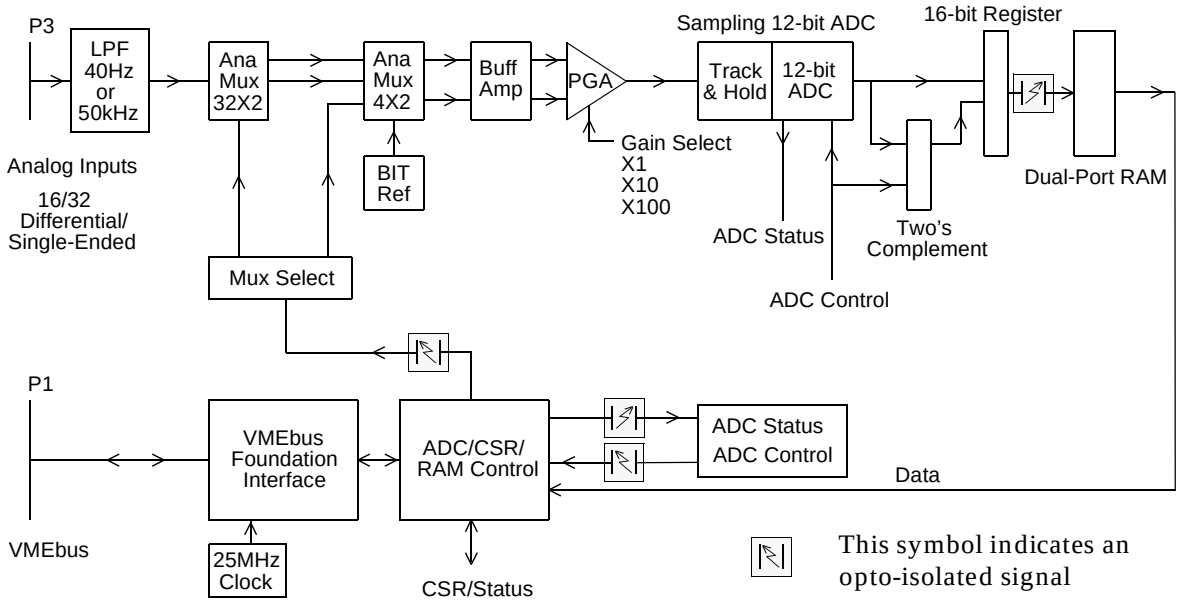

Figure 1-1 VMIVME-3125 Functional Block Diagram

During each read or write operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers and the address and address modifier line from the backplane. The appropriate board response occurs if a valid match is detected. The open collector DTACK interface signal is then asserted (driven low). Subsequent completion of the bus master's read or write cycle causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communication with the board. They are as follows:

- Data bus lines D00 to D15
- Address lines A01, A02, A03, A04, A05, A06, A07
- Bus Control Signals:
  Write
  DS0*, DS1*
  SYSCLK
  SYSRESET*

Data bus lines are bi-directional and move data to and from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data

transceiver serves as a buffer for the internal data bus, that interconnects all data devices on the board. Address lines A01 through A07 map the 64 registers into 128-byte range within the VMEbus address space described in “Programming” on page 41. The control signals determine whether data is to be moved *to* the board (write) or *from* the board (read). The control signals also provide the necessary data strobes (DS0,DS1). A SYSRESET input resets all CSR bits.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board.

Analog-to-Digital Control and Timing

Control commands and status flags associated with controlling the Analog-to-Digital Converter (ADC) are described in Chapter 3.

There are two modes of operation for this board. The first is to continuously scan all 16 or 32 analog input channels. The second is to halt scanning and lock onto a single channel. Either way, the electrical process of analog-to-digital conversion is similar.

The VMIVME-3125 uses a 12-bit ADC. The ADC has a conversion time of 8.5 µsec. Settling time is required for the multiplexers and the programmable gain amplifier before the ADC cycle may begin. The total channel acquisition cycle occurs every 25 µsec. All conversion timing is provided by internal sources. This gives an aggregate scan rate for all channels of 40 kHz. The ADC's built-in track-and-hold amplifier prevents signals that vary during a conversion cycle from giving false ADC readings.

After the multiplexer and gain amp have settled, the ADC is placed into the convert mode. The ADC's BUSY signal then goes **"active high"** to indicate the ADC is currently working on a new conversion cycle. The internal track-and-hold automatically changes from the track to the hold mode. The ADC then begins its successive approximation conversion cycle. The conversion digitizes the analog signal from the track-and-hold amp into a 12-bit data word.

The ADC signals the completion of its cycle by lowering the BUSY signal to a logic "0". If the 2's Complement bit is set in the CSR, the ADC's 12-bit output is modified into this format. At this point the 12-bit word is latched for storage to the dual-port RAM.

Built-in-Test Reference

The board is equipped with a programmable precision voltage reference which can be used as a Built-In-Test (BIT) of the board. When selected, the BIT voltage is fed through the programmable gain amplifier to the ADC, bypassing the external analog input on channel number zero. Therefore, the channel zero location in the dual-port RAM will be written with the BIT voltage's equivalent digital value. After enabling the BIT voltage (Mode 0 bit set), the user should wait for enough time to elapse (810 msec maximum), to allow sequencing through channel zero before checking its value. The BIT is used to test the programmable gain amplifier, the ADC, and the dual-port RAM memory. The BIT can be enabled at any time during initial board installation or in real time for system self-diagnostics.

The BIT reference is selected from one of three internal precision reference voltages: +4.980 VDC, +0.4928 VDC, +9.915 mVDC, or analog ground (0.0 VDC).

The selection is provided by setting the Mode bits 0, 1, and 2 in the CSR register according to the Control / Status Register details in "Programming" on page 41.

If mode bit zero is a logical "0", the board scans all 16 or 32 channels in a normal mode of operation. If the mode bit is set in the CSR register, channel zero corresponds to the selected reference voltage VREF0, VREF1, VREF2, or Analog Ground according to the settings of Mode bit 1 and Mode bit 2. The digital value received should be within ±10 LSBs of the selected reference voltage. The remaining channels (1-15 or 1-31) digitize their respective external input sources. Thus, channel zero may be periodically checked during run time to verify the ADC's operation. Please note that the current gain and unipolar / bipolar modes must be considered when selecting the reference voltage. The BIT voltage precedes the programmable gain amplifier and multiplies the selected reference voltage. Selecting a reference voltage which exceeds the ADC's range when multiplied by the gain amplifier is not recommended.

Analog Inputs

There are 16 differential or 32 single-ended analog inputs available on the front panel connector. VMIC recommends that the differential mode be used for decreased noise and greater common mode rejection. Unused inputs should be grounded, including the low side of all unused differential inputs. The board has internal 22 MΩ pull-down resistors on the low side of the differential inputs. This prevents the differential input pair from drifting up past the input multiplexers' maximum voltage limit.

NOTE: When configured for single-ended mode, channel 31 is jumper configurable as a common ground.

Low-Pass Filters

The VMIVME-3125 provides passive single-pole low-pass input filters on all inputs. The normal -3 dB cut-off frequency is 50 kHz. This provides some high frequency noise protection for the board. The board can also be configured with an add-on daughter board option. The daughter board provides a low pass filter with a cut-off frequency of 40 Hz. This lower cut-off provides some protection from local 60 Hz AC line noise. This option is normally installed by the factory at the time of order. It can be removed by the user at a later date if new applications arise. If the board is running in single-ended mode, the user must install the two (2) 0 Ω SIP jumpers in locations J4 and J5. This allows the low pass filter to perform in the single-ended configuration. Note that the VMIVME-3125 requires a jumper change if the 40 Hz daughter board is added.

Input Multiplexers

The board has two tiers of analog multiplexing. Each of the 32 inputs is selected using one of four 8x1 first-tier analog input multiplexers. The second-tier multiplexer is configured as a 4x2 board. It selects one or two of the first-tier output signals to provide the single-ended or differential mode of operation. The second-tier multiplexer also selects the BIT reference voltage, if it is enabled in the Control / Status Register. The second-tier output is differentially transferred to the programmable gain amplifier.

Current Input

The VMIVME-3125-200 and VMIVME-3125-300 models include current termination resistors. This allows a current signal to be terminated to ground. The voltage developed across this resistor is read by the VMIVME-3125. The VMIVME-3125-200 option provides 250 Ω (±0.01%) resistors. The VMIVME-3125-300 option provides 500 Ω (±0.01%) resistors. To support this option, the 50 kHz low pass filter is removed. All other functionality of the board remains the same. The 332-000206-ABC option board contains the precision termination resistors. This board is installed in the position which is normally reserved for the 332-00206-ABC 40 Hz module.

Programmable Gain Instrumentation Amplifier

Once an input channel has been selected and routed through the input multiplexers, it enters the programmable gain amplifier as a differential input. The differential amplifier rejects common mode noise and delivers a scaled, single-ended output to the ADC. The programmable gain amplifier may be hardware jumpered for gains of 1, 10, and 100. This allows for inputs as low as ±50 mV up to ±10 VDC in range. There is no increase in acquisition time for any change in the gain setting.

Channel Sequencer and Dual-Ported RAM Memory

The VMIVME-3125 is normally operated in the scanning mode. When the board is powered up or reset, conversions start immediately. Once the A/D conversion is completed, the dual-port control logic takes the converted data and stores it in the channel's appropriate dual-port register. The channel counter is incremented by one. This selects the next channel to be multiplexed to the ADC. After selecting the next channel, a new A/D conversion sequence is initiated. When all input channels have been converted and stored (16 or 32), the channel counter is reset and starts the channel scanning sequence again.

The Stop Auto Scan bit in the Control/Status Register may be set to halt the channel sequencer at its current address. This address may be read from the Channel Pointer Register. This feature allows the controlling software to lock onto a channel and digitize it at the maximum rate of 40 kHz. Please note that the channel desired can not be directly set. The software must wait for the desired channel to appear in the Channel Pointer register to set the Stop Auto Scan bit within 25 µsec.

Board ID Register

The first location in the VMIVME-3125 register set is a read-only Board ID Register. It always reads $37. Other VMIC products have similar registers which read different constants. This allows general-purpose system software to automatically determine what boards have been installed.

Built-in Power Converter and ADC Power Supply

Electrical power for the VMIVME-3125 analog circuitry is supplied by an on-board DC-to-DC converter. The converter transforms +5 VDC power from the VMEbus into a regulated ±15 VDC power. The VMIVME-3125 does not require any 12 VDC from the VMEbus.

The ADC's +5 VDC logic power is provided by an on-board voltage regulator. Some of the +15 VDC from the DC-to-DC converter's output is used as the input voltage to this regulator.

In addition to the ±15 V DC-to-DC converter, the VMIVME-3125 uses a separate +5 V DC-to-DC converter to provide an isolated analog ground for the ADC.

CHAPTER
2

Configuration and Installation

Contents

Introduction

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

NOTE: Do not install or remove board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

Jumper Installations

Figure 2-1 on page 30 identifies the location of configuration jumpers and calibration potentiometers for the VMIVME-3125. Jumpers E6 through E14 are address jumpers which must be set to the desired base address of the board as described in the following paragraph. Jumper E16 controls the VMEbus access mode; supervisory, nonprivileged or both. This function is documented in the *Address Modifier* section on page 31. The remaining jumpers must be set according to the *Input Configuration* section on page 31 to configure the board's analog inputs.

Board Address

The VMIVME-3125 occupies 128 contiguous bytes of short I/O address space (see Chapter 3 for register details). The base address is controlled by jumpers E6 through E14 according to Table 2-1. Each installed jumper corresponds to a binary 0, while each uninstalled jumper corresponds to a binary 1. For base address calculation, note that address bits A0 through A6 are assumed to be zero. The factory default address is at short I/O $0000 (all jumpers installed).

Table 2-1 Address Selection Jumpers

Short I/O Address Bit	Jumper # (installed=0 removed=1)
A15	E14*
A14	E13*
A13	E12*
A12	E11*
A11	E10*
A10	E9*
A9	E8*
A8	E7*
A7	E6*

* installed for factory default address of $0000

To change the address, first determine the new address in hexadecimal (note that the address must be an even multiple of 128 decimal, or $80). Convert the address to binary and assign the address bits A0 through A15 to the binary address starting from the LSB and refer to Table 2-1 above. All clear bits should have a jumper installed on the corresponding address bit jumper, and all set bits should have a jumper removed.

For example, assume a target address of $3A00 is desired. In binary, that number is %0011 1010 0000 0000. Assigning address bits to these shows that only bits A13, A12, A11, and A9 are set. Checking Table 2-1, all jumpers should be installed (for the clear address bits) except for jumpers E12, E11, E10, and E8 (for the set address bits).

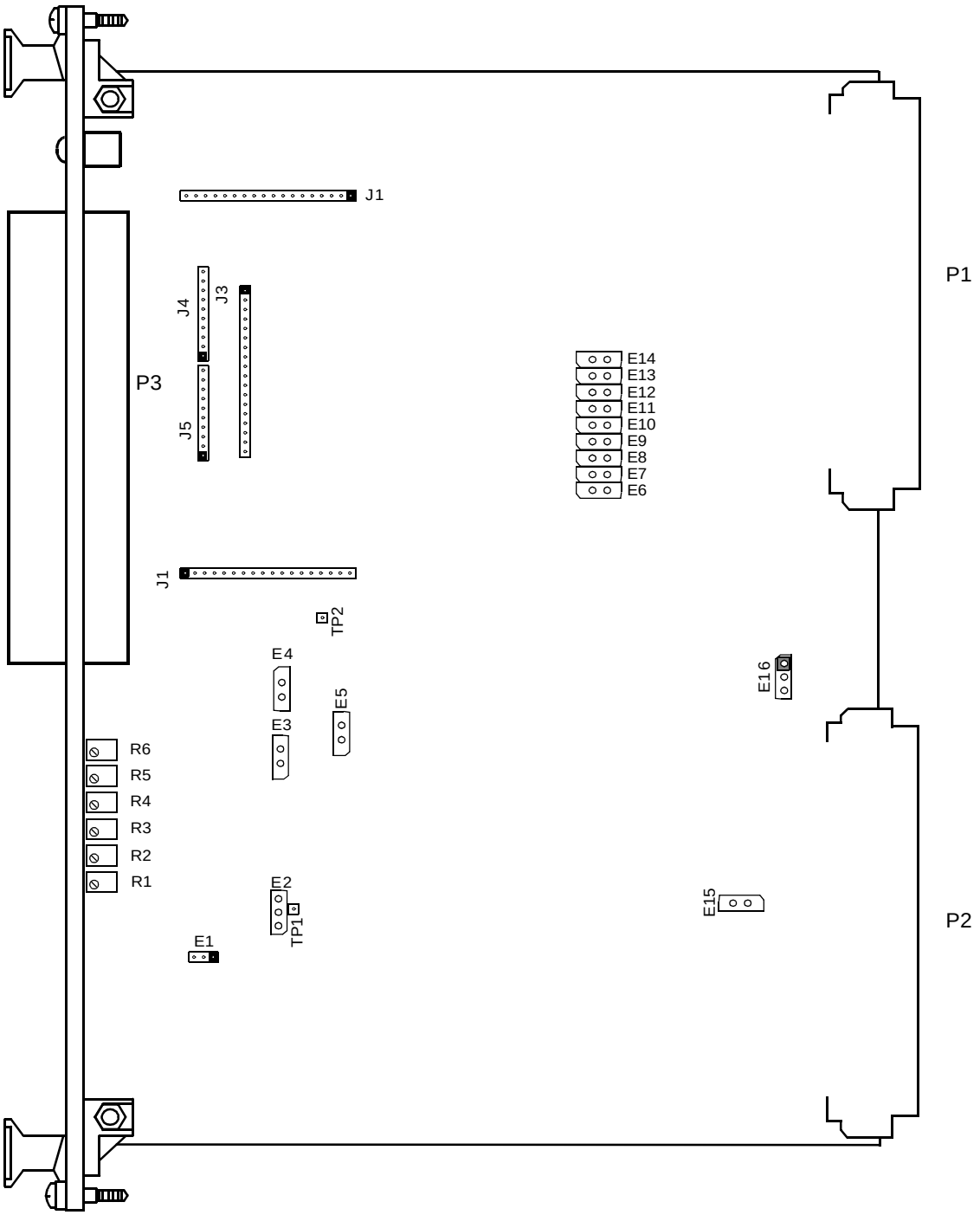

Figure 2-1 VMIVME-3125 Configuration Jumper Locations

Address Modifier

Jumper E16 determines whether the VMIVME-3125 responds to supervisory, nonprivileged, or both accesses according to Table 2-2.

Table 2-2 Address Modifier Jumper Settings

Short I/O Addressing Mode	Jumper E16 Setting
Supervisory	1-2
Nonprivileged	2-3
Both	no jumper

Input Configuration

Three jumpers (J4, J5, and E5) are used to configure the VMIVME-3125 for single-ended or differential inputs. Two jumpers (E1 and E2) control the input voltage range, and two jumpers (E3 and E4) control the amount of gain. The jumpers are shown in Table 2-3 below. The factory default configuration is single-ended, ±10 V range, and unity gain.

Table 2-3 Input Configuration Jumpers

Input Configuration Option		Jumper Configuration
MODE	Single-ended inputs*	Install jumpers J4†, J5†; remove E5
	Differential inputs	Remove jumpers J4, J5; install E5
RANGE	±10 V range*	Install jumpers E1 pins 1 and 2; E2 pins 2 and 3
	±5 V range	Install jumpers E1 pins 1and 2; E2 pins 1 and 2
	0-10 V range	Install jumpers E1 pins 2 and 3; E2 pins 1and 2
GAIN	Unity Gain*	Remove jumpers E4 and E3
	X10 gain	Remove jumper E4; install jumper E3
	X100 gain	Install jumper E4; remove jumper E3
FILTER	50 kHz low-pass filter (no daughter board)	Remove jumper E15
	40 Hz low-pass filter (daughter board installed)	Install jumper E15
* indicates factory default		†note that J4 and J5 must be jumpered with a “zero ohm” SIP pack (included)

NOTE: The VMIVME-3125-200 and VMIVME-3125-300 current input options require the input configuration jumpers to be set as single ended, 0 - 10 V range, unity gain, and for jumper E15 to be installed.

Note that the board comes factory configured for either 50 kHz input filters or 40 Hz input filters, depending upon the ordering option. If the 40 Hz input filter option is ordered, a daughter board is factory installed into sockets J1, J2, and J3. If the 50 kHz input filter option is ordered, no daughter board installed and sockets J1, J2, and J3 remain empty.

Analog Input Connector Description

The 16 differential or 32 single-ended analog input connections to the VMIVME-3125 board are made using the front panel 37-pin D-Shell connector labelled P3. See Table 2-4 for connector pin and signal assignments

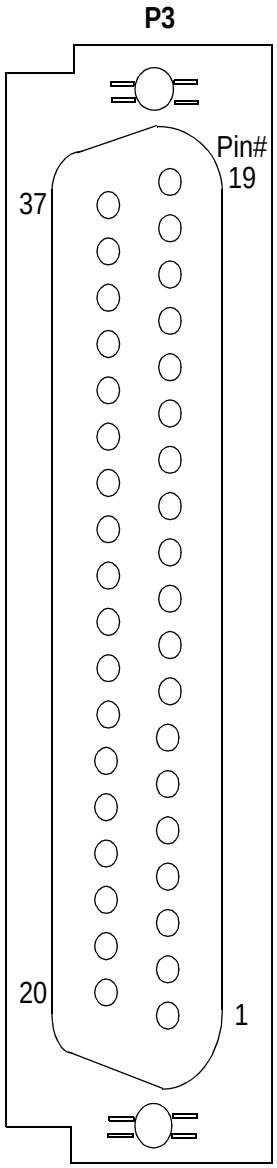

Figure 2-2 P3 Connector

Table 2-4 P3 Analog Connector Pinout

Pin #	Single-Ended Signal	Differential Signal
1	Analog Ground CH 24-31 LO	Analog Ground
2	CH30-HI	CH15-HI
3	CH28-HI	CH14-HI
4	CH26-HI	CH13-HI
5	CH24-HI	CH12-HI
6	CH23-HI	CH11-LO
7	CH21-HI	CH10-LO
8	CH19-HI	CH09-LO
9	CH17-HI	CH08-LO
10	Analog Ground CH 08-15 LO	Analog Ground
11	CH14-HI	CH07-HI
12	CH12-HI	CH06-HI
13	CH10-HI	CH05-HI
14	CH08-HI	CH04-HI
15	CH07-HI	CH03-LO
16	CH05-HI	CH02-LO
17	CH03-HI	CH01-LO
18	CH01-HI	CH00-LO
19	Analog Ground	Analog Ground
20	CH31-HI	CH15-LO
21	CH29-HI	CH14-LO
22	CH27-HI	CH13-LO
23	CH25-HI	CH12-LO
24	Analog Ground CH 16-23 LO	Analog Ground
25	CH22-HI	CH11-HI
26	CH20-HI	CH10-HI
27	CH18-HI	CH09-HI
28	CH16-HI	CH08-HI
29	CH15-HI	CH07-LO
30	CH13-HI	CH06-LO
31	CH11-HI	CH05-LO
32	CH09-HI	CH04-LO
33	Analog Ground CH 00-07 LO	Analog Ground
34	CH06-HI	CH03-HI
35	CH04-HI	CH02-HI
36	CH02-HI	CH01-HI
37	CH00-HI	CH00-HI

Calibration Procedures

In order to obtain the specified accuracy for analog measurements, the VMIVME-3125 must be calibrated for the range and input topology desired. For greatest possible accuracy, VMIC recommends calibrating the board after it has been installed in its target chassis with power applied for at least thirty minutes. Always perform the Instrumentation Amp Offset and BIT Calibration procedures first. Then select the offset and gain calibration procedure for the input topology desired. See Figure 2-1 on page 30 for the locations of test points and user-adjustable potentiometers used in the calibration of the board.

Equipment Required

- 5-digit Digital Voltmeter (DVM)
- Precision Voltage Reference

Instrumentation Amp Offset and BIT Voltage Calibration

NOTE: This procedure must be performed first.

1. Configure the board for differential unipolar 0 to 10 V range: Install jumpers E1 pins 2 and 3, E2 pins 1 and 2, and E5. Remove jumpers E3, E4, J4, and J5.
2. If this is the first run through this procedure, center potentiometer R5.
3. Attach the DVM positive lead to ADC input at TP1; attach the negative lead to analog ground at TP2.
4. Stop scanning on channel 0 and monitor the ADC output (a small program will be needed to do this).
5. Short the channel 0's HI and LO inputs together.
6. Install jumper E4 (sets the gain to x100).
7. Adjust the instrument amp's input offset potentiometer R6 until DVM reads as near 0.000 mVDC as possible (acceptable range is 0.0 mV to 0.3 mV).
8. Remove jumper E4 (sets the gain to x1).
9. Adjust the instrument amp's output offset potentiometer R5 until DVM reads as near 0.000 VDC as possible (acceptable range is 0.0 mV to 0.3 mV).
10. Repeat steps 6 through 9 until there is no change in the output (acceptable range is 0.0 mV to 0.3 mV).

Now calibrate the BIT reference voltage

11. Set the gain of the board to x1 by removing the jumper from E4.
12. Apply the 4.980 VDC BIT voltage to channel 0 by writing the appropriate value to the mode bits in the Control/Status Register of the board.
13. Adjust potentiometer R4 until the DVM reads the correct value.
14. Leave the DVM connected to the board and skip to the calibration procedure for the input topology and range desired.

Unipolar 0-10 V Differential Input Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for unipolar 0 to 10 V inputs by Installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2.
2. Configure the board for the gain to use:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI, and negative (-) lead to input LO).
4. Input a voltage (depending on the gain) that is 1/2 LSB above ground.

Gain	Vin:
x1	1.22.1 mVDC
x10	122.1 mVDC
x100	12.21 mVDC

5. While monitoring the ADC output of channel 0, adjust the unipolar offset potentiometer R3 until the display is fluctuating between $000 and $001.
6. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	9.996338 VDC
x10	0.999634 VDC
x100	0.099963 VDC

7. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display fluctuates between $FFE and $FFF.
8. Repeat steps 4 through 7 at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3125.

Bipolar ±5 V Differential Input Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for bipolar ±5 V inputs by installing a jumper on E1 pins 1 and 2, E2 pins 1 and 2.
2. Configure the board for the desired gain:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI and negative (-) lead to input LO).
4. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

Gain	Vin:
x1	-4.998779 VDC
x10	-0.499878 VDC
x100	-0.049988 VDC

5. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display fluctuates between $000 and $001.
6. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	4.996338 VDC
x10	0.499634 VDC
x100	0.049963 VDC

7. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
8. Repeat steps 4 through 7 at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3125.

Bipolar ±10 V Differential Inputs Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for bipolar ±10 V inputs by installing a jumper on E1 pins 1 and 2, E2 pins 2 and 3.
2. Configure the board for the desired gain:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0 (positive (+) lead to input HI and negative (-) lead to input LO).
4. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

Gain	Vin:
x1	-9.997559 VDC
x10	-0.999756 VDC
x100	-0.099976 VDC

5. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.
6. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	9.992676 VDC
x10	0.999268 VDC
x100	0.099927 VDC

7. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
8. Repeat steps 4 through 7 at least once or until no adjustment is necessary.

This concludes the calibration of the VMIVME-3125.

Unipolar 0 - 10 V Single-Ended Inputs Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for unipolar 0-10 V single-ended inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2, E5, J4, and J5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)
2. Configure the board for the desired gain:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)
4. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector).
5. Input a voltage (depending on the gain) that is 1/2 LSB above ground.

Gain	Vin:
x1	1.221 mVDC
x10	122.1 mVDC
x100	12.21 mVDC

6. While monitoring the ADC output of channel 0, adjust the unipolar offset potentiometer R3 until the display is fluctuating between $000 and $001.
7. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	0.996338 VDC
x10	0.999634 VDC
x100	0.099963 VDC

8. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
9. Repeat steps 6 through 8 at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3125.

Bipolar ±5 V Single-Ended Inputs Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for bipolar ±5 V single-ended inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2, E5, J4, and J5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)
2. Configure the board for the desired gain:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)
4. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector).
5. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

Gain	Vin:
x1	-4.998779 VDC
x10	-0.499878 VDC
x100	-0.049988 VDC

6. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.
7. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	4.996338 VDC
x10	0.499634 VDC
x100	0.049963 VDC

8. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
9. Repeat steps 6 through 8 at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3125.

Bipolar ±10 V Single-Ended Inputs Offset and Gain Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Configure the board for bipolar ±10 V single-ended inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2, E5, J4, and J5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)
2. Configure the board for the desired gain:

E4	E3	Gain
Off	Off	x1
Off	On	x10
On	Off	x100
On	On	x109 (Do Not Use)

3. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)
4. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector).
5. Input a voltage (depending on the gain) that is 1/2 LSB above the lowest voltage.

Gain	Vin:
x1	-9.997559 VDC
x10	-0.999756 VDC
x100	-0.099976 VDC

6. While monitoring the ADC output of channel 0, adjust the bipolar offset potentiometer R1 until the display is fluctuating between $000 and $001.
7. Input a voltage (depending on the gain) that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	9.992676 VDC
x10	0.999268 VDC
x100	0.099927 VDC

8. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
9. Repeat steps 5 through 8 at least once or until no adjustments are necessary.

This concludes the calibration of the VMIVME-3125.

VMIVME-3125-200 and -300 Current Input Option Calibration

NOTE: Run this calibration procedure only if the board is to remain in this configuration when installed in the system.

1. Remove the 332-000206-ABC termination board during the calibration procedures.
2. Configure the board for unipolar 0-10 V single-ended inputs by installing a jumper on E1 pins 2 and 3, E2 pins 1 and 2, E5, J4, and J5. (This will cause a shift in the instrumentation amp's output shown on the DVM.)
3. Configure the board for x1 gain

E4	E3	Gain
Off	Off	x1

4. Adjust the instrumentation amp's input offset potentiometer R6 until the DVM reads between 0.0 mV and 0.3 mV. (Do not change R5.)
5. Remove the short (channel 0 HI and LO) and connect the precision voltage source to channel 0, (positive (+) lead to channel 0 and negative (-) lead to ground on the P3 connector).
6. Input a voltage that is 1/2 LSB above ground.

Gain	Vin:
x1	1.221 mVDC

7. While monitoring the ADC output of channel 0, adjust the unipolar offset potentiometer R3 until the display is fluctuating between $000 and $001.
8. Input a voltage that is 1 1/2 LSB below the maximum input.

Gain	Vin:
x1	9.996338 VDC

9. While monitoring the ADC output of channel 0, adjust the gain potentiometer R2 until the display is fluctuating between $FFE and $FFF.
10. Repeat steps 5 through 8 at least once or until no adjustments are necessary.
11. Re-install the 332-000206-ABC termination board.

This concludes the calibration of the VMIVME-3125.

CHAPTER

3

Programming

Contents

Memory Map

The VMIVME-3125 occupies 128 bytes of addressing space including four information and control registers plus the conversion data registers. Table 3-1 on page 42 through Table 3-3 on page 44 map this addressing space relative to the base address as set by configuration jumpers (see Chapter 2 for details concerning setting the base address and address modifier jumpers).

The appropriate table is determined by two factors: whether the board is jumpered for single-ended or differential inputs, and whether the user has selected the normal or maximum data buffer for differential inputs. If the board is jumpered for differential inputs and the Max Buffer bit in the Control / Status Register is clear, Table 3-1 on page 42 applies. If the board is jumpered for differential inputs and the Max Buffer bit is set, Table 3-2 on page 43 applies. If the board is jumpered for single-ended inputs, Table 3-3 on page 44 is the only map that applies (see Chapter 2 for details concerning setting the input configuration jumpers).

Table 3-1 VMIVME-3125 Memory Map: Differential Inputs, Normal Buffer

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60-$7E	Reserved		

Table 3-2 VMIVME-3125 Memory Map: Differential Inputs, Maximum Buffer

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60	Channel 0 Data	word	read/(write)
$62	Channel 1 Data	word	read/(write)
$64	Channel 2 Data	word	read/(write)
$66	Channel 3 Data	word	read/(write)
$68	Channel 4 Data	word	read/(write)
$6A	Channel 5 Data	word	read/(write)
$6C	Channel 6 Data	word	read/(write)
$6E	Channel 7 Data	word	read/(write)
$70	Channel 8 Data	word	read/(write)
$72	Channel 9 Data	word	read/(write)
$74	Channel 10 Data	word	read/(write)
$76	Channel 11 Data	word	read/(write)
$78	Channel 12 Data	word	read/(write)
$7A	Channel 13 Data	word	read/(write)
$7C	Channel 14 Data	word	read/(write)
$7E	Channel 15 Data	word	read/(write)

Table 3-3 VMIVME-3125 Memory Map: Single-Ended Inputs

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60	Channel 16 Data	word	read/(write)
$62	Channel 17 Data	word	read/(write)
$64	Channel 18 Data	word	read/(write)
$66	Channel 19 Data	word	read/(write)
$68	Channel 20 Data	word	read/(write)
$6A	Channel 21 Data	word	read/(write)
$6C	Channel 22 Data	word	read/(write)
$6E	Channel 23 Data	word	read/(write)
$70	Channel 24 Data	word	read/(write)
$72	Channel 25 Data	word	read/(write)
$74	Channel 26 Data	word	read/(write)
$76	Channel 27 Data	word	read/(write)
$78	Channel 28 Data	word	read/(write)
$7A	Channel 29 Data	word	read/(write)
$7C	Channel 30 Data	word	read/(write)
$7E	Channel 31 Data	word	read/(write)

Register Descriptions

The VMIVME-3125 control registers are all byte-wide registers, while the data registers are all 16 bits wide. The control registers can also be accessed as 16-bit words, in which case two successive registers are accessed.

NOTE: All bits documented as "Reserved" read as zero and, if written, must always be written as zero.

Board ID Register

The Board ID Register is an 8-bit read-only register at offset $00 with a constant value set $37 for the VMIVME-3125. This ID number uniquely identifies the board from other VMIC products.

Board Configuration Register

The Configuration Register is an 8-bit read only register at offset $01. It indicates the current configuration of the VMIVME-3125 board. It contains two bits of configuration status information, each determined by the state of jumpers on the board. See Table 3-4 below for the definition of these bits. The Input Mode bit indicating single-ended or differential operation is controlled by a jumper shunt and can be set as desired (see Chapter 2 for details). Note that the 40 Hz bit indicating analog input filter bandwidth is also determined by a jumper, the jumper should be installed if the 40 Hz filter option daughter board is installed.

Table 3-4 Board Configuration Register Contents*

Bit Position	Bit Name	Function
0	Input Mode	0 = 16 Differential Inputs 1 = 32 Single-Ended Inputs
1	40 Hz	0 = 50 kHz Input Filters 1 = 40 Hz Input Filters
2-7		Reserved
* For the VMIVME-3125-200 and VMIVME-3125-300 options, the bit position 1=0 indicates the 332-000206-ABC current termination board is not present, while the bit position 1=1 indicates the termination board is present.		

Control/Status Register

The Board Control / Status register is an 8-bit read / write register at offset $02 that allows software to control the VMIVME-3125 and also indicates its current status. Seven of the eight bits provide control and indication functions. Table 3-5 defines the contents of this register.

Table 3-5 Board Control/Status Register Contents

Bit Position	Bit Name	Function
0	Stop Auto Scan	0 = Scan All Channels (Default) 1 = Scan Single Channel
1	Max Buffer	0 = 16 Differential Data Registers (Default) 1 = 32 Differential Data Registers
2	2's Complement	0 = Binary Data (Default) 1 = Two's Complement Data
3	Mode 0	Channel 0 BIT Mode 0
4	Mode 1	Channel 0 BIT Mode 1
5	Mode 2	Channel 0 BIT Mode 2
6		Reserved
7	LED Off	0 = Board LED On (Default) 1 = Board LED Off

Normally, the VMIVME-3125 automatically scans all input channels, continually converting each successive input. The user can set the Stop Auto Scan bit, however, to cause the VMIVME-3125 to stop on a single channel. If the Stop Auto Scan bit is set, only the Data Register pointed to by the Channel Pointer Register is updated. It is updated much faster than usual – approximately every 25 µsec. The best way to stop on a single desired channel for such close monitoring is to observe the Channel Pointer Register while auto-scanning. Then set the Stop Auto Scan bit within 25 µsec as soon as the desired channel appears. Auto scanning proceeds from the current channel as soon as this bit is cleared again.

The Max Buffer bit is only significant when the hardware is configured for differential inputs. In that case, it controls whether there are 16 Data Registers (one for each input) or 32 Data Registers (two for each input). The difference between these two scanning modes is discussed in detail in the Data Register description. Table 3-1 on page 42 (Max Buffer clear) and Table 3-2 on page 43 (Max Buffer set) detail the differences in the overall VMIVME-3125 memory map.

If the 2's Complement bit is set, all information in the Data Registers will be in two's complement format. This data format is only useful when the inputs are configured as bipolar, in which case the two's complement data format causes the Data Registers to contain values already sign-extended. This saves the programmer from having to convert the data in the host code. The three Mode bits determine the stimulus to channel zero, according to Table 3-6.

Table 3-6 Board Control/Status Register: Modes

Mode 2	Mode 1	Mode 0	Channel 0 Stimulus
X	X	0	External Input (Default)
1	1	1	Internal 0.000 V Reference
1	0	1	Internal 9.915 mV Reference
0	1	1	Internal 492.8 mV Reference
0	0	1	Internal 4.980 V Reference

The LED Off bit is self-explanatory. Note that the LED is ON by default and should normally be turned off after powerup or reset by the host software. The LED can be used to visually verify that the board has been initialized.

Channel Pointer Register

The Channel Pointer Register is an 8-bit read-only register at offset $03. Under most circumstances, the Channel Pointer Register holds the channel number of the current input being sampled and converted by the VMIVME-3125. The only exception occurs when the board is configured for differential input and the Max Buffer bit in the Control / Status Register is set. In this case, two data pages get updated such that each input is converted in two separate passes. The Channel Pointer Register can be used to determine which of the two Data Registers has been most recently updated. The address offset of the Data Register being converted may be calculated as follows:

(Channel Pointer Register value x 2) + $40 = Offset Address of Current Data Register

Note that the corresponding channel number is simply the Channel Pointer Register value modulo 16. Also note that the value in this register represents the current channel under conversion. Decrement the value by one (modulo 16 for differential inputs or 32 for single-ended inputs) to determine the location of the most recently completed channel data.

Data Registers

There are either 16 or 32 Data Registers beginning at offset $40, depending on the condition of the Max Buffer bit. Each Data Register contains 12 bits of conversion data for its associated channel. The data is right-justified within each 16-bit Data Register. Each register should generally be treated as read-only, and each should be accessed as a 16-bit word. The hardware does not restrict the user from accessing the Data Registers via two consecutive byte reads. When accessing the Data Registers as bytes, it is possible for the value in the Data Register being read to be updated *between* byte reads, potentially scrambling the perceived data. *Accessing Data as Bytes* on page 51 provides methods to avoid scrambled byte data reads.

The data is a linear binary representation of the input voltage on the corresponding channel at the time of the most recent conversion. The LSB weight (that is, the voltage value corresponding to a single bit of data) depends on the input voltage range, which, in turn, depends on the range and gain jumper configuration (see Chapter 2 for details). Calculate the LSB weight by dividing the full-scale range by 4096. For example, the LSB weight for a VMIVME-3125 configured for ±10 V at unity gain would be 4.883 mV (20 / 4096). Table 3-7 lists the LSB weights for all possible VMIVME-3125 configurations.

Table 3-7 LSB Weight

Voltage Range	LSB Weight		
	Gain x1	Gain x10	Gain 100
±5 V	2.441 mV	.2441 mV	24.41 µV
±10 V	4.883 mV	.4883 mV	48.83 µV
0-10 V	2.441 mV	.2441 mV	24.41 µV

The voltage on any channel can be determined by multiplying the Data Register value (converted to decimal) by the appropriate LSB Weight from Table 3-7 on page 47.

Two other values are very important in determining the meaning of the values in the Data Registers: the Channel Pointer Register and the Max Buffer bit, both previously described. The Channel Pointer Register holds the channel number of the Data Register currently being updated, therefore, the most recent complete conversion data is for the channel one less than the value of the Channel Pointer Register (modulo 32 or 16, depending upon the number of active Data Registers). The Max Buffer bit in the Control/Status Register determines whether there are 16 or 32 active differential data registers. If the bit is set, all 32 registers are actively updated, but if the bit is clear, only the first 16 registers are updated.

If the board is configured for single-ended inputs (i.e., if the Single-Ended bit in the Configuration Register is set), then the Max Buffer bit is meaningless. In this configuration, the 32 Data Registers contain the data for channels 0-31 consecutively, beginning with channel 0 at offset $40.

If the board is configured for differential inputs (i.e., if the Single-Ended bit in the Configuration Register is clear), then the Max Buffer bit can be either set or cleared, depending on the user's wishes. The trade-off is between simplicity of access (Max Buffer bit clear; 16 Data Registers) and relaxed access requirements (Max Buffer bit set; 32 Data Registers).

By clearing the Max Buffer bit, only the first 16 Data Registers are updated, corresponding to channels 0-15 consecutively, beginning with channel 0 at offset $40. This is the simplest configuration, but it may require more bus overhead than desired if the user wishes to avoid constantly reading the board but still wants to capture every single data sample.

On the other hand, the user may want to set the Max Buffer bit to increase the time interval by extending the aggregate sample time from just under 500 µsec to nearly a millisecond. By setting the Max Buffer bit, all 32 Data Registers are updated. Data for channels 0-15 is stored consecutively, first in the lowest 16 Data Registers (channel 0 data at offset $40), then in the higher 16 Data Registers (channel 0 data at offset $60). Using this technique, the two most recent scans are always available in the Data Registers. The Channel Pointer Register must be read to determine which of the two data sets is most recent. In this case, the Channel Pointer Register value does not hold a channel number, but rather an offset value into the extended data buffer. The code must still be structured such that the previously updated data is read prior to being overwritten by new data.

NOTE: The Data Registers are actually writeable. Since the registers physically consist of RAM, writes are allowed to facilitate testing of the data RAM. Unless auto-scanning is halted, however, any data written to a Data Register is overwritten with new data the next time that channel is scanned and converted.

Built-in-Test Functions

The VMIVME-3125 has the ability to test its functionality by applying various internal reference voltages to the channel zero input. Host software can then read the value for channel zero and compare it to its predicted quantity. Table 3-8 through Table 3-10 below show all possible BIT values.

Table 3-8 BIT Values for 0-10V Range

BIT Voltage	Gain Setting X 1	X 10	X 100
0.000 V	$0000	$0000	$0000
9.915 mV	$0004	$0028	$0196
492.8 mV	$00C9	$07E2	$0FFF
4.980 V	$07F8	$0FFF	$0FFF

Table 3-9 BIT Values for ±5 V Range

BIT Voltage	Gain Setting X 1	X 10	X 100
0.000 V	$0800	$0800	$0800
9.915 mV	$0804	$0828	$0996
492.8 mV	$08C9	$0FE2	$0FFF
4.980 V	$0FF8	$0FFF	$0FFF

Table 3-10 BIT Values for ±10 V Range

BIT Voltage	Gain Setting X 1	X 10	X 100
0.000 V	$0800	$0800	$0800
9.915 mV	$0802	$0814	$08CB
492.8 mV	$0864	$0BF1	$0FFF
4.980 V	$0BFB	$0FFF	$0FFF

Of course, these tables assume precisely calibrated BIT reference voltages. Check the specification for exact tolerances of these voltages. Note also that these tables assume pure binary data. The two's Complement bit in the Control/Status Register must be clear. Any value of $0FFF indicates an overvoltage condition.

Range and Gain Determination

While the VMIVME-3125 analog gain and range can be set by the user, there is no direct way to read these settings in software (see Chapter 2 for hardware gain and range configuration). Software can apply a BIT voltage stimulus and attempt to determine the current gain and range settings by comparing the data to the values in Table 3-8 through Table 3-10 on page 49. This technique is not recommended, however, since the board must be calibrated to a single gain and range setting.

Accessing Data as Bytes

As stated in the Data Register description, the Data Registers should generally be accessed using single 16-bit word transfers. It is possible to access a Data Register using two successive byte transfers, although there are risks involved. The data as interpreted by the host can be completely scrambled if the VMIVME-3125 happens to update the Data Register in between the two byte accesses. There are two methods to avoid this:

One method uses the Halt bit in the Control / Status Register to temporarily suspend automatic scanning while the two bytes are being read. Valid data can be guaranteed by carefully monitoring the Channel Pointer Register to avoid accessing channel data that is currently being converted or is about to be converted and by temporarily stopping all conversions with the Halt bit in the Control / Status Register. Once scanning is halted, any Data Register can be safely read as bytes except for the Data Register pointed to by the Channel Pointer Register. The drawbacks to such a method are that it is inherently slow and the user loses a regular time reference, since the clock is essentially stopped while the Halt bit is set. That is, the data is frozen for all channels except the one pointed to by the Channel Pointer Register, whose input gets converted constantly.

The other method to read the Data Registers as bytes avoids interrupting the regular automatic scanning process and thus, preserves the conversion frequency of all channels. This method requires the user to structure the code so that the two byte accesses are guaranteed to be consecutive and uninterrupted. The Channel Pointer Register must be monitored and interrupts disabled to avoid accessing a Data Register while the data is being updated – preferably one should access a channel immediately after it has been updated. Interrupts should always be disabled before accessing a Data Register to avoid a long interrupt service routine coming between the two-byte accesses.

Of course, there are no problems or concerns if the Data Registers are accessed as a single word as recommended. For reference, however, the MSB of the data is in the lower byte address, while the LSB is in the higher byte address.

Current Input VMIVME-3125-200 and VMIVME-3125-300 Option

The VMIVME-3125-200 provides the current signal a 250 Ω (±0.01%) path to ground, and the VMIVME-3125-300 provides the current signal a 500 Ω (±0.01%) path to ground. Table 3-11 lists the voltages seen by the ADC.

Table 3-11 Voltage at the Input of the ADC

Current Range (mA)	Termination Resistor (Ω)	ADC Input Voltage (V_{ADC})
0 - 25	250	0 - 6.25 V
0 - 25	500	Not Recommended
0 - 20	250	0 - 5 V
0 - 20	500	0 - 10 V
4 - 20	250	1 - 5 V
4 - 20	500	2 - 10 V
5 - 25	250	1.25 - 6.25 V
5 - 25	500	Not Recommended

Use the formula $I = V_{ADC}/R_{Termination}$ in order to calculate the current signal from the ADC voltage.

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.