VMIVME-3126

HIGH RESOLUTION, ISOLATED ANALOG-TO-DIGITAL CONVERTER BOARD

PRODUCT MANUAL

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VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
(205) 880-0444
(800) 322-3616
FAX NO.: (205) 882-0859

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RECORD OF REVISIONS

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VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

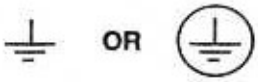
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

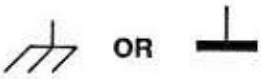
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

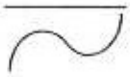
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).



Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-3126

HIGH RESOLUTION, ISOLATED ANALOG-TO-DIGITAL CONVERTER BOARD

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SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-3126 Analog Input board has 16 independent isolated input channels with 16-bit resolution. Each input has a dedicated Analog-to-Digital Converter (ADC), input conditioning, reference, and power supply. Each channel is isolated with opto-isolators from the VMEbus and the digital circuitry. Self-test is initiated by a VMEbus system reset or by execution of a software command. A Digital Signal Processor (DSP) provides control and software correction of data. An Electrically Eraseable Programmable Read-Only Memory (E^2PROM) loads offset and gain coefficients into the DSP during a reset condition. The offset and gain coefficients can be recalculated by the user by entering the calibration mode. Software filtering is also done by the DSP to a user defined cut-off frequency.

The following brief overview of principal features illustrates the flexibility and performance that is available with the VMIVME-3126 Board:

a. 16-Analog input channels:
   - Input-to-input and input-to-VMEbus isolation
   - ADC per channel

b. RTD Excitation Source (200 µA/400 µA) per channel

c. Open transducer detector per channel

d. Full board or user selected channel calibration

e. Unipolar/Bipolar full-scale ADC ranges from 50 mV to 10 V

f. Self-Test:
   - Initiated on power-up or any reset condition
   - Extensive on-board diagnostic testing capability
   - Status to user accessible register

1.2 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA

VMEbus International Trade Association
7825 East Gelding Drive No. 104
Scottsdale, AZ 85260
(602) 951-8866
FAX: (602) 951-0720
Internet: http://www.vita.com/

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003126-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3126 Analog Input board provides 16-independent, fully isolated input channels. This capability is attained by the principal hardware functions listed below (see Figure 3.1-1 for a block diagram of these functions).

a. VMEbus Interface

b. Digital Signal Processor

c. EPROM

d. E^2PROM

e. Control Logic

f. Analog Inputs

3.2 VMEbus INTERFACE

The VMIVME-3126 responds to word (D16) or byte (D08(EO)) data accesses. Nonprivileged, supervisory, or both access modes are supported along with short and standard address modes.

3.2.1 Control and Status Registers (CSRs)

The VMIVME-3126 contains several registers available to the user for control and status of the board. A brief description of the registers is shown in Table 3.2.1-1 on page 3-3. The registers are explained in detail in Section 4. The Control and Status registers begin at offset address $XX00.

3.2.2 Data Registers

The Data registers offset address begins at $XX40. Each channel has a unique location in this 16-word deep buffer. The data format for unipolar inputs is binary and the format for bipolar is either offset binary or two's complement as programmed in each Channel Control Status Register. A Data Ready Flag is set in the Board Status register indicating new data is available from the data registers.

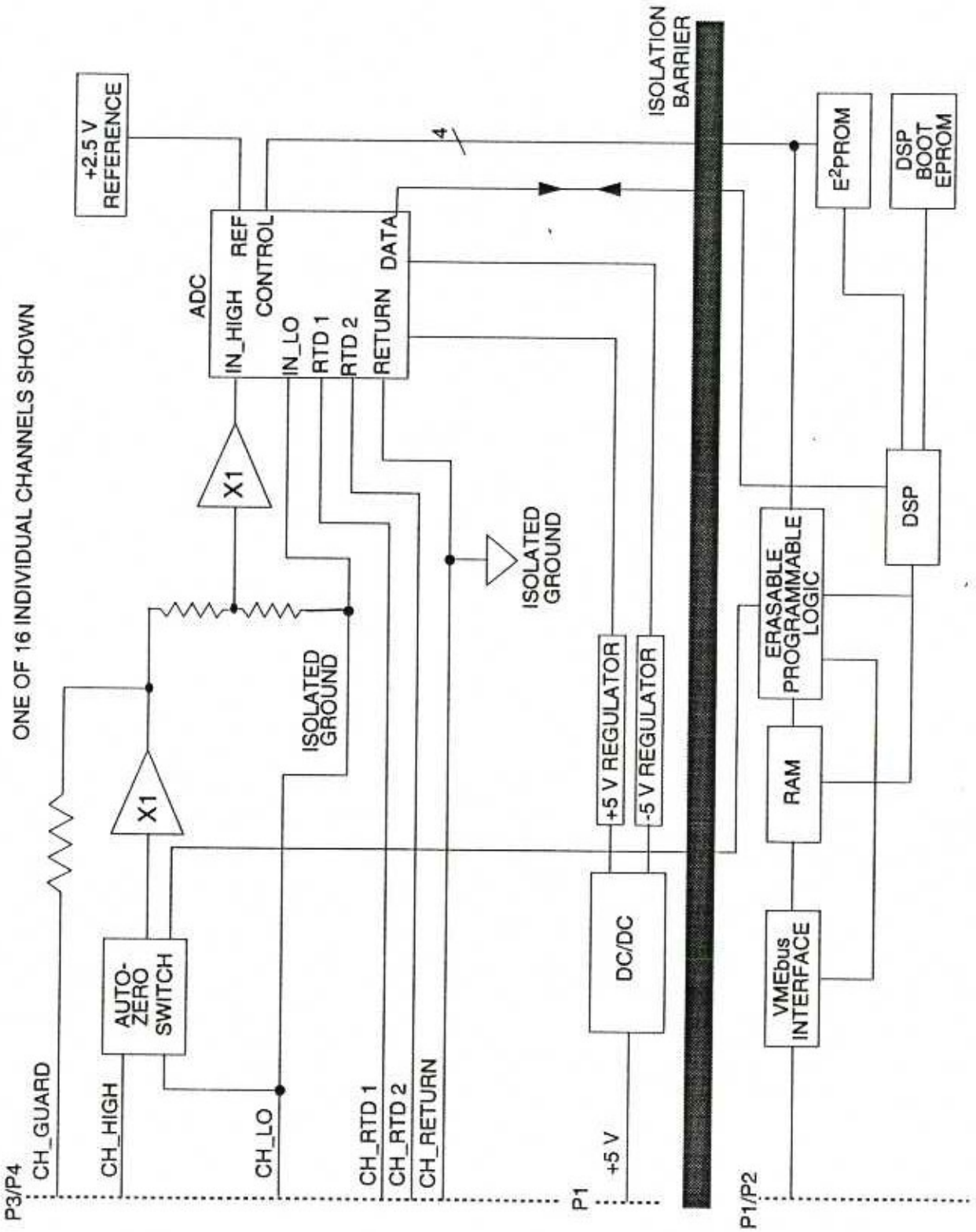


Figure 3.1-1. VMIVME-3126 Block Diagram

Table 3.2.1-1. Control and Status Registers

Register	Mnemonic	Description
Board ID Register	BIR	Contains code identifying the board as a VMIVME-3126
Board Ready Register	BRR	Status indicating when the board can be accessed for read/write operations
Board Control Register	BCR	Control functions for board operation
Select Channel Register	SCR	User-select of channels for calibration or reconfiguration
Pass/Fail Status Register	PFS	Status of channels following self-test
Target Calibration Voltage Register High	TCVH	Upper 16-bits of expected value - entered by the user for calibration
Target Calibration Voltage Register Low	TCVL	Lower 16-bits of expected value - entered by the user for calibration
Firmware Revision Register	FRR	Contains current revision level of DSP code
EEPROM Writes Register	EWR	Contains the number of times the EEPROM has been written
Channel Control Status Register	CSR	Provides control of range, data format, input format, and filter cut-off frequency for each channel

3.2.3 Modes of Operation

The VMIVME-3126 operates in several different modes. Each mode is enabled by the user through the Board Control Register (BCR). The operating modes are described below.

3.2.4 Normal Mode

The board enters the normal mode after completing the power-on self-test routines. In this mode, each input is scanned, digitized, and stored in user-accessible RAM. When the on-board DSP is not processing data, it is reading the BCR to see if the user has changed operating modes.

3.2.5 Calibration Mode

The board enters the calibration mode when the INIT CAL bit in the BCR is set by the user. Entering this mode causes the board to stop processing data and await further input from the user. If jumper E10 is omitted, the front panel LED is illuminated for a visual indication of the change in modes from normal mode to calibration mode. The front panel field connections must be removed for calibration. A calibration adapter for the front panel inputs is available from the factory. Calibration voltages can be from external sources or a P2 backplane source. A jumper on the calibration adapter determines which source to use. During the calibration process, VMEbus access should be limited to reading and writing to the BRR, and writing to the TCVH and TCVL registers. The BRR's

data appears as $3B00 ($3B01 for 8-channel option) while calibration is active. Prior to setting the INIT CAL bit, the user must enter the channels to calibrate into the SCR and the digital representation of the expected result of the calibration voltage into the TCVH and TCVL. The DSP uses these values in determining the gain and offset coefficients. The equation for determining the digital representation of the expected result is given in Section 4.3.6.

The DSP will read the SCR to determine which channels to calibrate. The channels selected will be digitized and stored in DSP memory. After all the selected channels data has been stored for the present calibration voltage, the board sets a status bit (Chan Cal'd in the BCR), clears the INIT CAL bit, writes $0000 to the BRR letting the user know the board can be accessed, and waits for the user to respond in one of two ways.

1. The user can enter another value into TCVH and TCVL and set the INIT CAL bit. This adds another point in the calibration curve for determining gain and offset coefficients. A minimum of three points is required for a successful calibration. Failure to enter three calibration voltages results in an error message to the BRR. A maximum of seven points is allowed. Attempting to enter more than seven calibration voltages results in an error message to the BRR. If this error occurs, set the CAL Done bit in the BCR or terminate calibration. During the calibration process, the BRR will read the board ID. If a calibration error occurs, as described above, the BRR will indicate the error per Table 4.3.2-2 on page 4-4.

2. If the user has entered at least the minimum and not greater than the maximum number of calibration points and is finished with calibrating, the Cal Done bit in the BCR must be set. This tells the DSP the user has finished calibration and to calculate the gain and offset coefficients. After the DSP is finished calculating the coefficients, the Cal Done bit is cleared, the front panel LED is turned OFF and $0000 is written to the BRR. When a VMEbus read indicates $0000, the user knows the coefficients have been calculated and the board is accessible.

The calibration mode can be terminated up to the point preceding the CAL Done bit being set without affecting the current coefficients. This is done by setting **both** the INIT CAL and CAL Done bits in the BCR. The DSP will recognize this as the user terminating calibration and will return to the Normal mode. Figure 3.2.5-1 on page 3-6 shows the calibration flowchart from the user's standpoint.

3.2.6 Reconfiguration Mode

The board enters the Reconfiguration Mode when the SYS RECONFIG bit in the BCR is set by the user. The board will stop processing data and the front panel LED will illuminate if Jumper E10 is omitted. During the reconfiguration process, VMEbus access should be limited to reading the Board Ready Register. The BRR's data appears as $3B00 and $3B01 for the 8-channel option while reconfiguration is active. The user must enter the channels to be reconfigured in the SCR. Also, the CSR of each channel to be reconfigured must have the new information written to it prior to the SYS RECONFIG bit being set. After completing the reconfiguration of the indicated channels, the SYS

RECONFIG bit in the BCR will be cleared and $0000 written to the BRR. When a VMEbus read indicates $0000, the user knows the reconfiguration mode is complete and the board is accessible. Figure 3.2.6-1 on page 3-7 shows the reconfiguration flowchart from the user's standpoint. Reconfiguration of a single channel takes approximately 44 msec. Reconfiguring all 16 channels takes approximately 101 msec.

3.2.7 Autozero Mode

The board enters the Autozero Mode when the Autozero bit in the BCR is set by the user. An input switch disconnects the field inputs and connects analog ground to the inputs. The present range of each channel is still active. An average of 1024 samples are collected by the DSP and this value is compared to the expected reading for a grounded input. The offset coefficient is adjusted by the difference in the two values. The advantage of this mode of operation is correcting errors in offset due to temperature variations without having to invoke a calibration cycle.

The new offset coefficients are used by the DSP and are not written to the E^2PROM unless the user sets the WRITE COEF bit in the BCR after this mode is complete. The Autozero bit in the BCR is reset by the DSP when the new coefficients are determined, and is an indication that the board has resumed normal operation. The Autozero operation takes approximately 11 seconds to complete.

3.3 DIGITAL SIGNAL PROCESSOR (DSP)

The DSP is responsible for gathering data from the ADC and providing offset and gain correction along with filtering. The DSP and the Erasable Programmable Logic Device (EPLD) combine to control all board operations. During calibration, the DSP collects up to seven different sets of data from user defined inputs. A least mean square estimate of the channel transfer function is determined using this data. A gain and offset coefficient for each channel is calculated from this estimate and stored internally.

The data samples collected from the ADCs are corrected in real-time using the calculated gain and offset coefficients. All DSP math operations are performed in 32-bit format, thereby preserving the high resolution provided by the ADCs. Output data is truncated to 16 bits for consistency with reasonable limitations on linearity within the input channel circuitry. The Firmware Revision Register contains the current revision of the DSP code. A Watchdog Timer monitors the DSP to ensure the code is processing normally. The DSP clears the watchdog timer every 30 msec. If for some reason the DSP does not clear the timer, the timer times out causing the WDOG bit in the BCR to be set. This alerts the user of a problem and requires the user to software reset the board through the BCR.

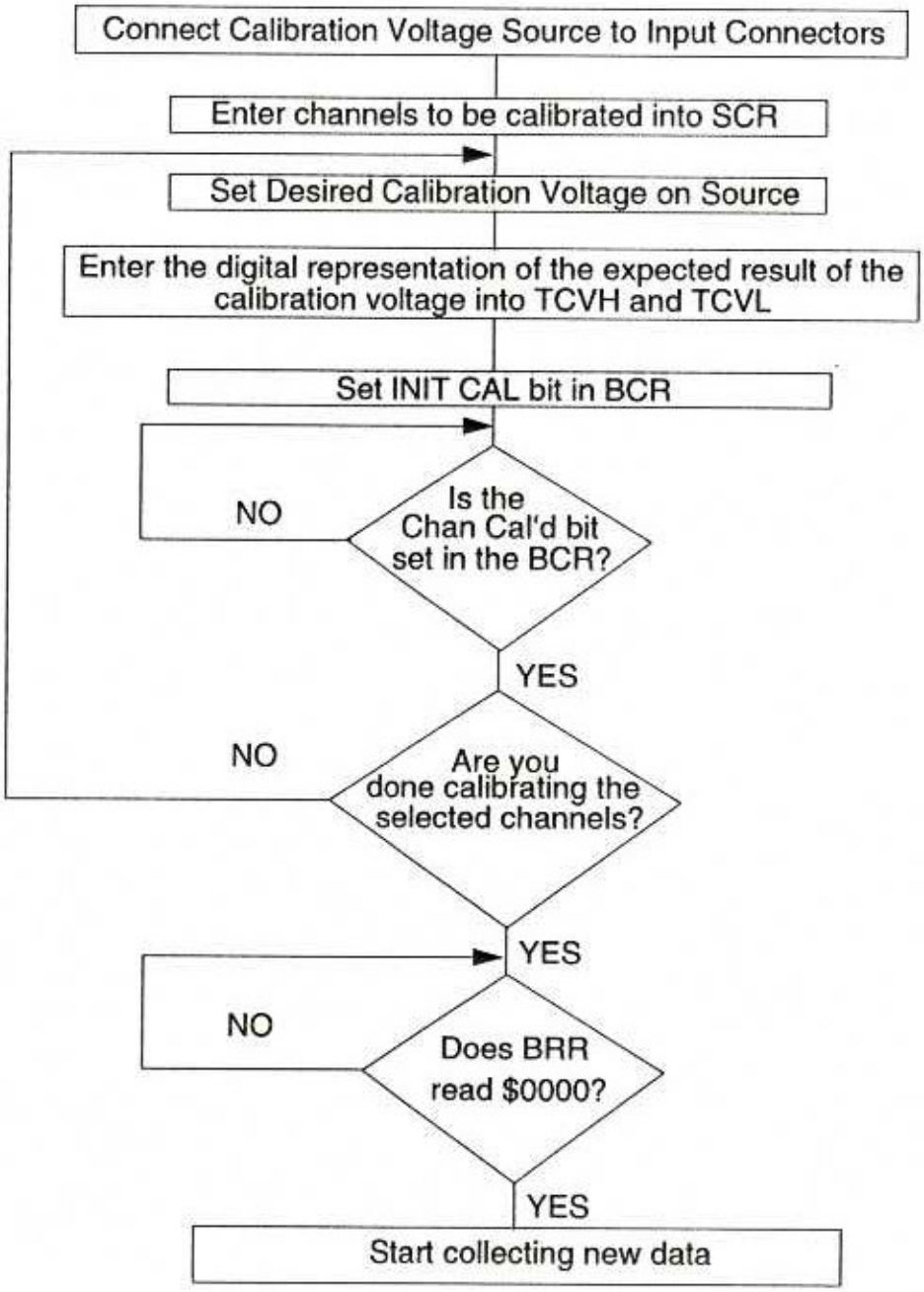


Figure 3.2.5-1. User's Calibration Flowchart

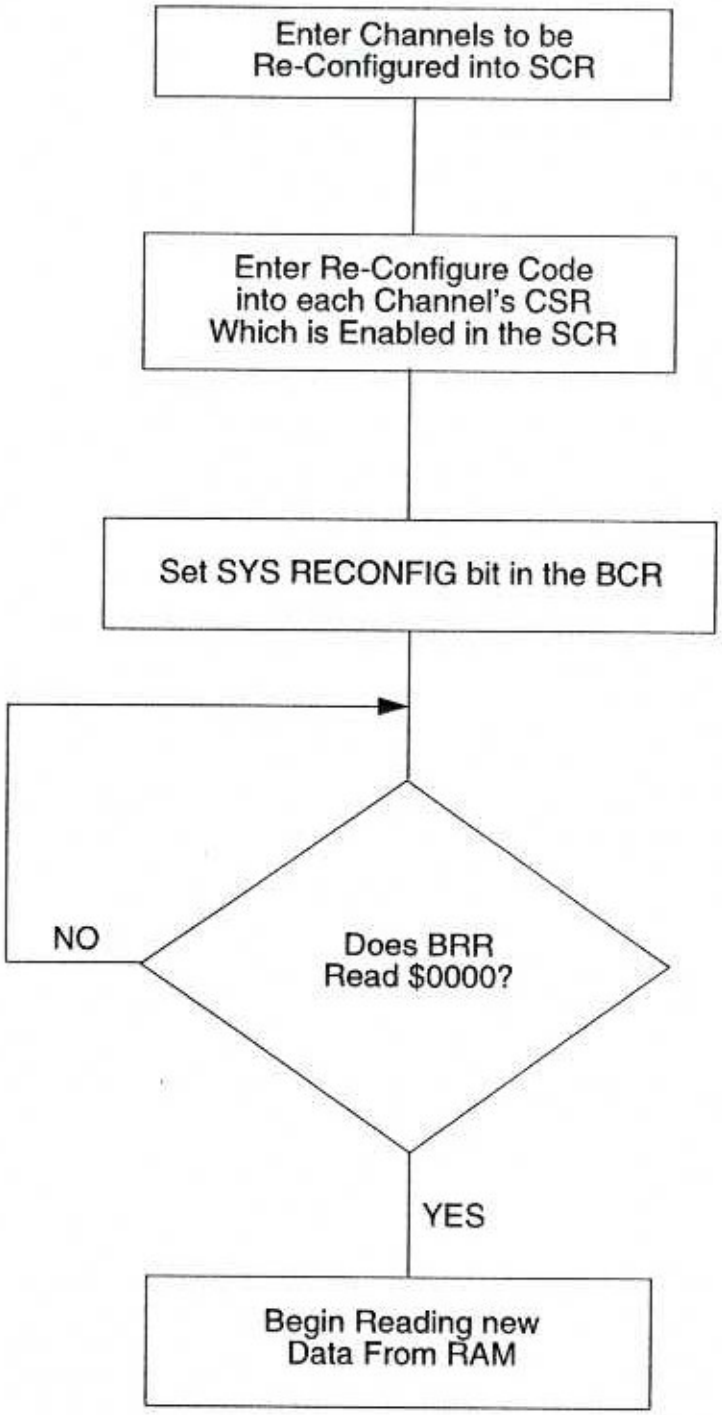


Figure 3.2.6-1. Channel Reconfiguration Flowchart

3.4 ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY (EPROM)

The DSP firmware is stored in the EPROM. There are four main boot pages stored in the EPROM. These are the power-up/reset boot page, the main routine boot page, the calibration boot page, and the reconfiguration boot page. Each boot page contains code specifically written for the particular function.

3.5 ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (E^2PROM)

The gain and offset coefficients calculated in the calibration mode can be stored in the E^2PROM. The board is shipped with factory determined coefficients. When the user initiates a calibration, newly calculated coefficients are stored in the DSP for use in real-time correction. The new coefficients are not automatically stored in the E^2PROM. The bit in the BCR allows the user control over writing the results to the E^2PROM, which writes over any coefficients that were present. The DSP uses the range code in each channel's CSR to determined where the coefficients is written. This allows the user to run new correction coefficients (from the DSP) but not corrupt coefficients stored in the E^2PROM. Most commercially available E^2PROM's have a guaranteed 100,000 write cycles lifetime. A EEPROM Writes Register (EWR) is available to the user indicating how many writes have occurred. If this number becomes close to the 100,000 limit, it is suggested the E^2PROM be replaced so data is not lost or corrupted. Writing coefficients to the E^2PROM once a day would not reach the limit of 100,000 write cycles for over twenty five years.

WARNING

AN INADVERTENT WRITE TO THIS BIT WILL RESULT IN THE COEFFICIENTS CURRENTLY IN THE DSP TO BE WRITTEN TO THE E^2PROM. PREVIOUSLY STORED COEFFICIENTS WILL BE WRITTEN OVER.

3.6 CONTROL LOGIC

The control logic consists of the logic required to read and write the RAM and E^2PROM, initiate ADC conversions, and arbitrate between the board and the VMEbus. The control logic consists of an EPLD.

3.7 ANALOG INPUTS

The VMIVME-3126 can accept bipolar and unipolar signals in the ranges stated in the Specification.

3.7.1 Analog-to-Digital Converter (ADC)

The Analog-to-Digital Converter (ADC) uses a sigma-delta conversion technique to digitize input signals with up to 24-bits of no missing code performance. The ADC also provides internal gain and digital filtering. There is one ADC per channel with all channels updating their output registers simultaneously.

3.7.1.1 ADC Control Interface

There are four control signals used on the ADC. The purpose of these signals is described below. Each signal is opto-isolated from the VMEbus and unique to the particular channel.

Receive Frame Synchronization (RFS) - Active low input signal used to read serial data from the ADC.

Transmit Frame Synchronization & Address A0 (TFS & A0) - Two active low inputs connected together to enable writes of serial data to the ADC.

Synchronization (SYNC) - Active low input signal used to synchronize the digital filters of all the ADCs. Resets the nodes of the digital filter and allows all ADCs to update their output registers simultaneously.

Serial Clock (SCLK) - Clock signal used to write control data to the ADC or clock output data from the ADC.

There is one serial data pin on the ADC used for incoming and outgoing data. The direction of the data depends on the state of the RFS and TFS signals.

3.7.1.2 Programmable Gain Amplifier (PGA)

The ADC contains an internal PGA with software controlled gains of 1 to 128 in seven binary steps. The DSP automatically selects the appropriate gain required for the range selected.

3.7.2 RTD Excitation

The VMIVME-3126 is capable of supplying excitation current to Resistance Temperature Detectors (RTDs). The excitation current is enabled under software control by writing to the RTD bit in the desired channel's CSR. The actual current supplied to the RTD is determined by the connections made at the P3 or P4 input connectors. There are two pins per channel for RTD excitation. The current on each pin is 200 µA. Wiring the two pins together yields 400 µA of current excitation.

An RTD is essentially a resistor whose resistance value changes with temperature. A constant excitation current produces a voltage corresponding to the resistance of the RTD. This voltage is measured and digitized by the board. Using the digitized results, the user can calculate the temperature knowing the temperature coefficient of the RTD.

Application and configurations for RTD control are discussed in Section 5 of this manual.

3.7.3 Open Transducer Detection

The ADC supplies software controlled open transducer detection. Open transducer detection allows the user to check if an input transducer is still connected or an open condition has occurred. This function only works on ranges from ±1 V (0-to-1 V) to ±50 mV (0-to-50 mV). If the transducer connection has opened, the output for that channel will read positive full-scale (0xFFFF in offset binary or 0x7FFF in two's complement). The user sets the Open Sensor bit in the desired CSRs and follows the rule for reconfiguration. The DSP will determine if the selected channels have open sensors. Status will be displayed in the PFS register and the Open Sensor bit reset in each CSR.

3.7.4 Filtering

Digital filtering is done internally in the DSP. The filter setting in each channels CSR is stored and used to restore the proper filter coefficients to applied in real-time.

The filter approximates a 6^{th} order bessel response. For the best performance, use the lower filter settings on the lower ranges. For example, using the 0.05 Hz filter on the ±50 mV scale considerably reduces the noise spread.

The digital filter for each channel is zeroed after a reconfiguration of that channel. This puts the filter in a known state and eliminates illegal filter states. Depending on the selected frequency, there will be a delay after reconfiguration while the filter settles to the signal present on the inputs.

3.7.5 OPTO Isolation

Optical Isolation is provided on every signal going to or coming from each channel. These signals consist of those mentioned in Section 3.7.1.1 as well as the output data from the ADC's and the Input Autozero Switch.

3.7.6 DC-to-DC Power Converters

Each channel has a dedicated DC-to-DC Converter. The DC-to-DC Converters are powered by the VMEbus +5 VDC power bus at the P1 and P2 connectors. The output of each converter is 33 mA at ±15 V. Input-to-output isolation of >1500 VDC maintains channel to VMEbus isolation.

3.7.7 Current Loop Termination Option

For the current loop termination option, a resistor is added between the HI and LO inputs on the board. The resulting voltage from the current flowing through the resistor is digitized and stored in RAM. The actual current would then be determined by the user, converting the digitized code into a voltage for the range selected and dividing by 400.

WARNING

CURRENTS GREATER THAN 25 mA ARE NOT SUPPORTED AND COULD CAUSE COMPONENT FAILURE.

3.7.8 Increased Input Voltage Range Option

For the increased input voltage range option, a resistor divider is added to the HI input side on the board. Input voltage up to ±200 V are supported.

SECTION 4

PROGRAMMING

4.1 INTRODUCTION

This section describes the programming operations necessary for controlling the VMIVME-3126 board. The VMEbus slave interface is summarized first and followed by a detailed description of the VMIVME-3126 register set.

VMEbus communication takes place through several registers which can be jumpered in either the A16 short I/O space or the A24 standard space.

The board automatically enters self-test on power-up. This self-test consists of writing and reading the on-board RAM, verifying that each ADC is functioning correctly, and loading calibration coefficients from the E^2PROM.

The user can initiate a calibration sequence by writing to the Board Status Register. A calibration sequence halts all operations and proceeds with calibrating the selected channels to the user specified inputs. After calibration of selected channels is complete, status is indicated in the BCR and the board waits for a bit in the BCR to be set by the user before resuming normal operations.

Digitized input data is accumulated in a data buffer which consists of 16 data words, where each data word contains the 16-bit digitized value of a single analog input channel.

4.2 GENERAL CONTROL FEATURES

4.2.1 Addressing Modes and Board Locations

Programmable address jumpers permit the VMIVME-3126 board to be located in either short I/O (A16) space or in standard (A24) space.

The board can be located on any 256 byte boundary. Access privilege is jumper selectable for either supervisory, nonprivileged, or both supervisory and nonprivileged.

4.2.2 Data Transfers

The VMIVME-3126 respond to both D8 (E0) and D16 data transfers.

4.2.3 Reset Operations and Initialization

All control registers are reset by either a VMEbus system reset or a software reset caused by writing to a bit in the BCR. Either reset operation will initialize the self-test mode which will perform the following:

a. Auto-detect 8 or 16 channel option and write the Board ID to the BRR

b. Read/write test of the on-board RAM

c. Self-test each ADC and check the digitized value against a constant to insure proper function

d. Load channel gain and offset calibration coefficients from E^2PROM

e. Write results from step b. above to BRR

f. Write results from step c. above to the PFS register and BRR

g. Extinguish LED after successful self-test

4.3 CONTROL REGISTERS

Register designations and location are summarized in Table 4.3-1.

NOTE:

REGISTERS DESIGNATED AS READ ACCESS SHOULD ONLY BE READ. DO NOT WRITE TO READ-ONLY ACCESS REGISTERS.

Table 4.3-1. VMIVME-3126 Board Register Map

Register Address (Hex)	Register Designation	ABBREV	Access
$0000	Board Identification Register	BIR	Read Only
$0002	Board Ready Register	BRR	Read Only
$0004	Board Control Register	BCR	Read/Write
$0006	Select Channel Register	SCR	Read/Write
$0008	Channel Pass/Fail Status	PFS	Read Only
$000A	Target Calibration Voltage Hi	TCVH	Read/Write
$000C	Target Calibration Voltage Lo	TCVL	Read/Write
$000E	Firmware Revision Register	FRR	Read Only
$0010	EEPROM Writes Register 1	EWR1	Read Only
$0012	EEPROM Writes Register 2	EWR2	Read Only
$0014 to $001F	Reserved	-	N/A
$0020 to $003F	Control Status Registers	CSR0 - 15	Read/Write
$0040 to $005F	Data Register		Read/Write
$0060 to $007F	Reserved	-	N/A
$0080 to $00BF	Offset Coefficients		Read/Write
$00C0 to $00FF	Gain Coefficients		Read/Write

4.3.1 Board Identification Register (BIR)

The Board Identification Register is a fixed, read only data register. The contents of this register identifies the VMIVME-3126. The board ID for the VMIVME-3126 16-channel option is $3B00, and $3B01 for the 8-channel option.

Table 4.3.1-1. Board ID Register Map

Board ID Register (Offset $0000) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	1	1	0	1	1
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	BIR0

Power-up/Reset Default = $3B00 - 16CH
$3B01 - 8 CH

Board Identification Register bit definitions:

Bits 8-15: These bits contain the Board ID ($3B00)

Bits 0, BIR0: This bit indicates the number of channels. It is set to a logic "0" for the 16-channel option and is set to a logic "1" for the 8-channel option.

Bits 7 through 1: Reserved - Forced to zeroes

4.3.2 Board Ready Register (BRR)

The Board Ready Register (BRR) tells the user when the board is able to be accessed from the VMEbus for read/write operations following a reset condition.

Table 4.3.2-1. Board Ready Register Bit Map

Board Ready Register (Offset $0002) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0

Power-up/Reset Default = $0000

Board Ready Register bit definitions:

Bits 0-15 BR [15..0]: This code indicates the response of the local DSP after a reset condition has been processed and is interpreted as shown in Table 4.3.2-2 on page 4-4.

Table 4.3.2-2. Board Ready Register Bit Definitions (BR[15..0])

BR[15..0]	Function	Notes
$0000	Null (Self-Test/Calibration/Configuration not active)	
$3B00/$3B01	Self-Test/Calibration/Configuration is Active	1
$0001	RAM Self-Test has failed	2
$0002	ADC has failed self-test	3
$0003	Not Enough Calibration Points Entered	4
$0004	Attempted to Enter more than Seven (7) Calibration Voltages	5

Note 1 - The board is performing either self-test, calibration, or configuration of channels. The board is not available for VMEbus accesses.

Note 2 - The on-board RAM has failed the RAM test. The DSP has stopped processing the reset condition. Replace RAM or check to see that it is properly installed.

Note 3 - One or more ADC's has failed initial self-test. Refer to the Channel Pass/Fail Register to determine the status of each ADC. The board will function with the failed channel (s) but the data for the channel (s) will not be correct.

Note 4 - Minimum number of calibration voltages is three. An attempt to calibrate with fewer than three calibration voltages occurred. Either enter more calibration voltages or terminate calibration process.

Note 5 - Maximum number of calibration voltages is seven. An attempt to calibrate with more than seven calibration voltages occurred. After entering the maximum number of calibration voltages, the CAL Done bit must be set in the BCR to inform the DSP to calculate the coefficients.

4.3.3 Board Control Register (BCR)

The Board Control Register (BCR) contains status and control of the board's operations. The user can initiate channel reconfiguration, channel calibrations, autozeroing of channels, and a software reset.

Table 4.3.3-1. Board Control Register Bit Map

Board Control Register (Offset $0004) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED	WDOG	WRITE COEF	COEF Status	Reserved			Reset_A

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reset_B	Autozero	Data Ready	USER COEF	SYS Reconfig	Chan Cal'd	INIT CAL	CAL Done

Power-up/Reset Default = $0000

Board Control Register bit definitions

Bit 15 - LED: The front panel LED is turned ON by writing a logical "1" to this bit. After successfully completing self-test, the LED will extinguish if the UIOC jumper (E10) is not installed. If the UIOC jumper is installed, the LED will remain ON after completing self-test. The user can extinguish the LED by writing a logical "0" to this bit.

Bit 14 - WDOG: This is a status bit, informing the user that a watchdog time-out has caused a reset. The user must acknowledge this bit being set by writing a logical "1" to the RESET_B bit located in this register. This will cause the DSP to initiate a board reset as described in Section 4.2.3. The DSP resets this bit to a logical "0" after completing the board reset.

Bit 13 - WRITE COEF: When this bit is set, the gain and offset coefficients stored in the DSP internal memory are written to the E^2PROM. This bit is automatically cleared after the coefficients are written to the E^2PROM.

Bit 12 - COEF Status: This is a status bit, indicating, whether user-defined coefficients are being used in the offset and gain correction of data. This bit is set to a logical "1" for user defined coefficients. The bit is reset if the coefficients are written to the E^2PROM or a reset condition occurs.

Bits 9 through 11- Reserved: These bits are reserved and should be written as logical "0".

Bits 8 and 7 - Reset[A and B]: These bits cause the board to return to its power-up reset state. This reset is a two step process to ensure fault tolerance. To initiate a proper reset, the following steps must be adhered to:

1. Write a logical "1" to RESET_A and a logical "0" to RESET_B bit.
2. Wait for RESET_A bit to be reset by DSP.
3. Write a logical "0" to RESET_A bit and a logical "1" to RESET_B bit. The maximum time allowed between setting RESET_A bit then setting RESET_B bit is approximately 2 seconds. If this time is exceeded, the reset sequence must be performed again. The RESET_B bit stays set indicating a reset did not occur.

Bit 6 - Autozero: When this bit is set to a logical "1" by the user, the inputs from all channels are internally disconnected from the field and connected to the channel's analog ground. This bit is reset automatically by the DSP after new offset coefficients are determined.

Bit 5 - Data Ready: This is a status bit informing the user new data is available in the RAM. The user must reset this bit to a logical "0" after reading the new data.

Bit 4 - USER COEF: The user sets this bit if user-defined gain and offset coefficients are going to be used. This gives the user control of the gain and offset applied to the raw ADC data. The user must first write the gain and offset coefficients to the appropriate location ($XX80 starting address of offset coefficients and $XXC0 starting address for gain coefficients) for the channel(s) of interest. The gain and offset coefficients are 32-bits wide and must be entered in 2's complement format. This requires two 16-bit registers. The coefficients must be entered MSW (first 16-bits) followed by the LSW (last 16-bits). For example: gain coefficients for channel 0 would be entered MSW

at $XXC0 and the LSW at $XXC2 (see Table 4.3.3-2). The USER COEF bit is then set informing the DSP of pending changes. The DSP will load all the coefficients into its internal memory and use the values during the correction process. The user-defined values **will not** be written to the E^2PROM unless the user sets the WRITE COEF bit located in this register. This bit is reset after the DSP reads the last coefficient. Also, the COEF Status bit will be set indicating user-defined coefficients are being used. The DSP will have control of the internal bus for approximately 21 µsec to read in all the coefficients.

Table 4.3.3-2. User Gain Coefficients MSW and LSW

Address	Word	Channel
$XXC0	MSW	0
$XXC2	LSW	0
$XXC4	MSW	1
$XXC6	LSW	1

Bit 3 - SYS Reconfig: The user sets this bit to a logical "1" whenever a change in channel configuration is desired (i.e., gain, frequency). The channel or channels reconfigured are entered into the Select Channel Register (SCR) prior to setting this bit. The DSP periodically polls this bit to determine if the configuration has changed. Sensing a change, the DSP reads the SCR and begins processing the new configurations. While the channel is being reconfigured, VMEbus activity should be limited to reading the BRR for indications on when normal accesses can take place. The SYS Reconfig bit is reset after the channel has been reconfigured.

Bit 2 - Chan Cal'd: This is a status bit set by the DSP after the data for the present calibration voltage is stored. This informs the user that additional calibration voltage can be entered. The bit is reset by the DSP after each INIT CAL or CAL Done operation.

Bit 1 - INIT CAL: This bit is set to a logical "1" by the user to initiate calibration. Also, this bit is set for each voltage entered for calibration. The bit is reset automatically by the calibration routine.

Bit 0 - CAL Done: The user sets this bit to a logical "1" upon completion of calibration. The DSP reads this bit to determine when the user is finished and proceeds calculating the gain and offset coefficients. The bit is reset to logical "0" after the DSP finishes its calculations.

4.3.4 Select Channel Register (SCR)

The Select Channel Register (SCR) selects the channels for calibration or reconfiguration. See Table 4.3.4-1 on page 4-7 for the Select Channel Register bit map.

Table 4.3.4-1. Select Channel Register Bit Map

Select Channel Register (Offset $0006) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Power-up/Reset Default = $0000

Select Channel Register bit definitions

Bits 0-15,CH [15...0]: A logical "0" written to the bit field inhibits that channel. A logical "1" written to the bit field enables that channel for calibration or reconfiguration. After calibration or reconfiguration is complete, the bit is reset to a logical "0". (Default is logic 0).

4.3.5 Channel Pass/Fail Status Register (PFS)

The Channel Pass/Fail Status (PFS) register contains pass/fail status of the self-test performed on the ADC's during the power-up/reset condition. It also contains status after performing open sensor detection.

Table 4.3.5-1. Channel Pass/Fail Status Register

Channel Pass/Fail Status Register (Offset $0008) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Power-up/Reset Default = $0000

Channel Pass/Fail Status Register bit definitions

Bits 0-15, CH [15...0]: A logical "0" indicates the channel has passed. A logical "1" indicates the channel has failed. (Default is logic 0).

4.3.6 Target Calibration Voltage Register (TVC)

The Target Calibration Voltage register (TCV) consists of two registers. The user writes the digital value of the expected result for a given calibration input voltage. The Target Calibration Voltage HI Register contains the upper word of a 32-bit value. The Target Calibration Voltage LO Register contains the lower word of a 32-bit value. Table 4.3.6-1 shows the HI register and Table 4.3.6-2 shows the LO register. The gain and offset coefficients are determined using the values in these registers and the data from the ADC. A precision low noise voltage source should be used for the calibration process to insure the accuracy of the final corrected data.

Table 4.3.6-1. Target Calibration Voltage Register HI Bit Map

Target Calibration Voltage Register HI (Offset $000A) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
TVH15	TVH14	TVH13	TVH12	TVH11	TVH10	TVH9	TVH8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TVH7	TVH6	TVH5	TVH4	TVH3	TVH2	TVH1	TVH0

Power-up/Reset Default = $0000

Table 4.3.6-2. Target Calibration Voltage Register LO Bit Map

Target Calibration Voltage Register LO (Offset $000C) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
TVL15	TVL14	TVL13	TVL12	TVL11	TVL10	TVL9	TVL8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TVL7	TVL6	TVL5	TVL4	TVL3	TVL2	TVL1	TVL0

Power-up/Reset Default = $0000

Target Calibration Voltage HI and Lo Register bit definitions

Bits 0-15,TVH & TVL [15...0]: The user writes a digital value to this register which represents the expected result for the calibration voltage connected to the inputs. The digital value must be in two's complement format. Below is an example explaining the use of this register.

Example: Input +2.25 V for calibration on the ±5 V scale. The 32-bit code for the expected value can be determined by the following equation:

$E_{in} = E_{fsr} \times N_{adc}/2^{32}$

where: E_{in} = Input voltage

E_{lo} = Lower end of Input Range

E_{fsr} = Full scale Input Range

N_{adc} = A/D Converter reading

Solving for N_{adc} yields:

$$N_{adc} = \frac{E_{in} * 2^{32}}{E_{fsr}}$$

For the above example, N_{adc} = $3999 9999. This number is in two's complement format and would be entered in the TCV register as:

Target Calibration Voltage HI = $3999
Target Calibration Voltage LO = $9999

NOTE:

DUE TO THE WAY THE DSP HANDLES CALIBRATION, UNIPOLAR RANGES MUST USE E_{FSR} OF THEIR BIPOLAR RANGE. FOR EXAMPLE, A UNIPOLAR RANGE OF 0 TO 10 V USES A E_{FSR} OF ±10 V (20 V) IN THE AFORE MENTIONED EQUATION.

4.3.7 Firmware Revision Register (FRR)

The Firmware Revision Register (FRR) contains the revision of code for the DSP.

Table 4.3.7-1. Firmware Revision Register Bit Map

Firmware Revision Register (Offset $000E) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
MJR15	MJR14	MJR13	MJR12	MJR11	MJR10	MJR9	MJR8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
MNR7	MNR6	MNR5	MNR4	MNR3	MNR2	MNR1	MNR0

Power-up/Reset Default = Depends on DSP

Firmware Revision Register bit definitions

Bits 15 through 8, MJR[15...8]: This code represents the code for the current revision for the DSP.

Bits 7 through 0, MNR[7...0]: This code represents the current minor revision for the DSP code.
For example, a current revision of 1.07 would be displayed as $0107.

4.3.8 EEPROM Writes Registers (EWR1 and EWR0)

The EEPROM Writes Register (EWR1 and EWR0) is a 32-bit number representing the number of times the E^2PROM has been written to. This 32-bit number is made from two 16-bit registers. EWR1 contains the upper 16 bits and EWR0 contains the lower 16 bits. Tables 4.3.8-1 and 4.3.8-2 shows these registers.

Table 4.3.8-1. EEPROM Writes Register 1 Bit Map

EEPROM Writes Register 1 (Offset $0010) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
EW15	EW14	EW13	EW12	EW11	EW10	EW9	EW8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
EW7	EW6	EW5	EW4	EW3	EW2	EW1	EW0

Table 4.3.8-2. EEPROM Writes Register 0 Bit Map

EEPROM Writes Register 0 (Offset $0012) Read Only, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
EW15	EW14	EW13	EW12	EW11	EW10	EW9	EW8
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
EW7	EW6	EW5	EW4	EW3	EW2	EW1	EW0

EEPROM Write Register bit definitions

Bits 15 through 0, EW1 [15...0]: The upper 16 bits represents the number of times the E^2PROM has been written to in hexadecimal format.

Bits 15 through 0, EW1 [15...0]: The lower 16 bits represents the number of times the E^2PROM has been written to in hexadecimal format.

4.3.9 Control and Status Register (Channel 0 Example)

This register contains information pertinent to channel 0. Each channel has its own CSR which is identical in operation to the one described in Table 4.3.9-1.

Table 4.3.9-1. Control and Status Register Bit Map

Channel 0 Control and Status Register (Offset $0020) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Format	RTD	Open Sensor	Reserved	Range Bit 3	Range Bit 2	Range Bit 1	Range Bit 0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved					FC2	FC1	FC0

Power-up/Reset Default = $0807

Control and Status Register bit definitions

Bit 15 - Format: This bit controls the format of the data written to the RAM. A logical "0" returns offset binary format. A logical "1" returns two's complement format. The Default is offset binary. This bit is ignored for unipolar ranges. For unipolar ranges, the output is always binary.

Bit 14 - RTD: This bit enables the RTD Excitation supply when set to a logical "1". The default condition is a logic "0".

Bit 13 - Open Sensor: This bit enables the Open Sensor detection on the inputs when set to a logical "1". The default condition is a logic "0". The range for the channel must be less than or equal to ±1 V (0-1 V) for open sensor detect to work properly. Refer to Table 4.3.9-2 on page 4-11 for the code to enter for these ranges. This bit is reset automatically by the DSP after the open sensor detection has completed. Status of whether or not the sensor was open is reported in the PFS register.

Bit 12 and Bits 7 through 3 - Reserved: Set these bits to a logical "0".

Bits 11 through 8, Range Bits [3...0]: This field determines the input range for the channel. The range code is used by the DSP to determine the channel gain. Tables 4.3.9-2 and 4.3.9-3 on page 4-11 show the range code, and associated input voltage range. The default setting is 1000.

Bits 2 through 0, FC [2...0]: This field is the channel's -3 dB cutoff frequency as shown in Table 4.3.9-4. The default setting is 111.

Table 4.3.9-2. Input Range Control

Range Code (HEX)	Input Range
0	0-10 V
1	0-5 V
2	0-1 V
3	0-500 mV
4	0-100 mV
5	0-50 mV
6	Reserved
7	Reserved
*8	±10 V
9	±5 V
A	±1 V
B	±500 mV
C	±100 mV
D	±50 mV
E	Reserved
F	Reserved

Denotes Default setting

Table 4.3.9-3. Input Range Control (Increased Voltage Range)

Range Code (HEX)	Input Range
0	0-200 V
1	0-100 V
2	0-20 V
3	0-10 V
4	0-2 V
5	0-1 V
6	Reserved
7	Reserved
*8	±200 V
9	±100 V
A	±20 V
B	±10 V
C	±2 V
D	±1 V
E	Reserved
F	Reserved

Denotes Default setting

Table 4.3.9-4. Channel -3 dB Cutoff Frequency

-3 dB Frequency	FC2	FC1	FC0
0.05 Hz	0	0	0
0.12 Hz	0	0	1
0.30 Hz	0	1	0
0.70 Hz	0	1	1
1.7 Hz	1	0	0
4.0 Hz	1	0	1
10.0 Hz	1	1	0
*26.0 Hz	1	1	1

Denotes Default setting

4.3.10 Offset Coefficients

A copy of the offset coefficients determined during calibration are placed in locations $0080 to $00BF. The offset coefficients are in two's complement 32-bit wide integer format.

4.3.11 Gain Coefficients

A copy of the gain coefficients determined during calibration are placed in locations $00C0 to $00FF. The offset coefficients are in two's complement 32-bit wide integer format.

4.3.12 Data Register

The corrected and filtered data is placed in locations $0040 to $005F. Each location corresponds to each channel starting with channel 0. The data is a 16-bit integer in the format selected in each CSR.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BASE ADDRESS CONFIGURATION

There are 20 jumper positions to establish the base address, address mode, and access mode. The address mode can be configured for standard or short address space. The base address is determined by the presence (address bit compared to logic zero) or absence (address bit compared to logic one) of a jumper shunt at each appropriate address jumper position. For short and standard address mode configurations, the address jumper positions which must be configured are A[15:8] or A[23:8], respectively. The access mode can be configured for supervisory, nonprivileged, or for both supervisory and nonprivileged access.

Jumper Functions are illustrated in Figures 5.3-1, and 5.3-2. Figure 5.3-4 shows the location of user configurable jumpers. Omission of a jumper shorting plug produces a HIGH (logic "1") requirement for the associated control bit. Installation of the jumper shorting plug produces a LOW (logic "0") requirement. The factory configuration for the board is: Standard address mode, supervisory and nonprivileged access mode, base address set at 0XFB00 0000.

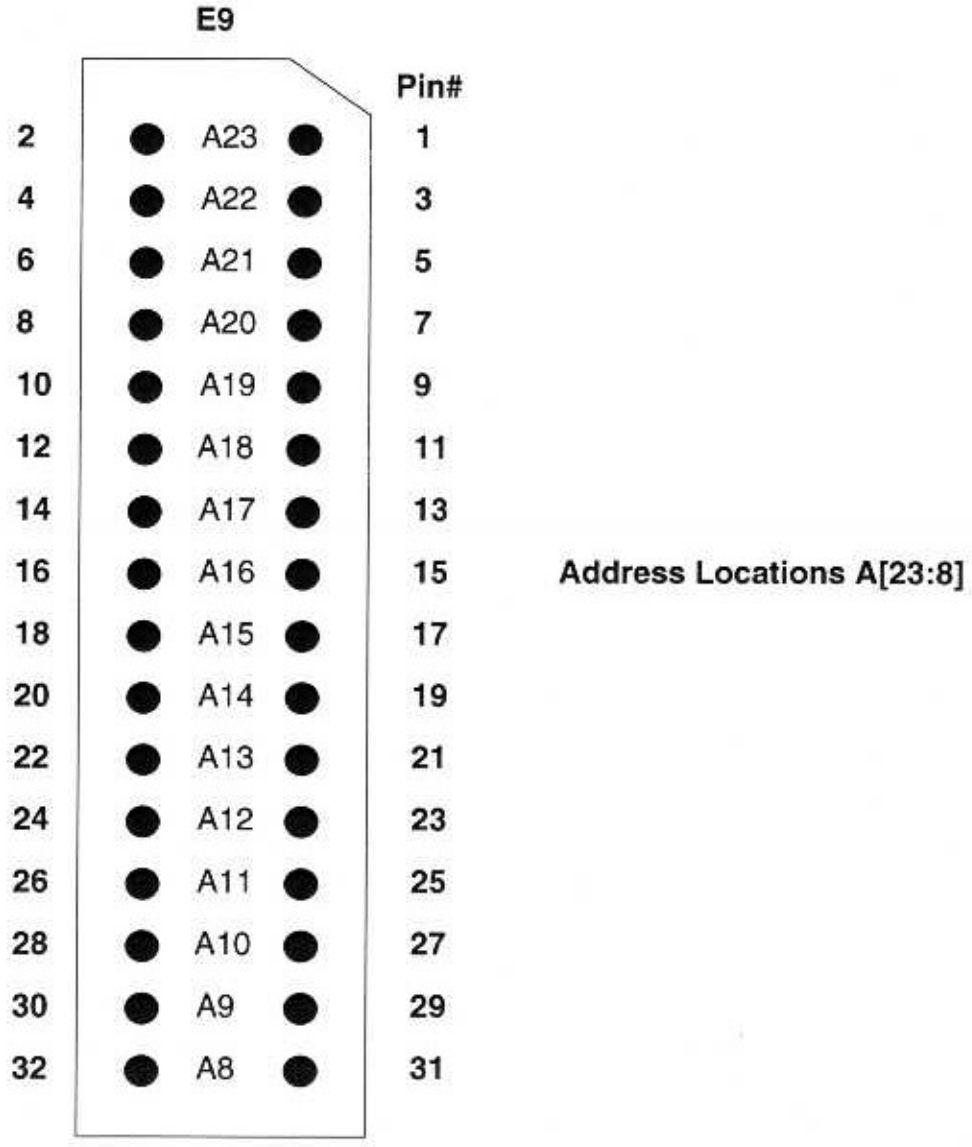


Figure 5.3-1. Address Locations and Configuration

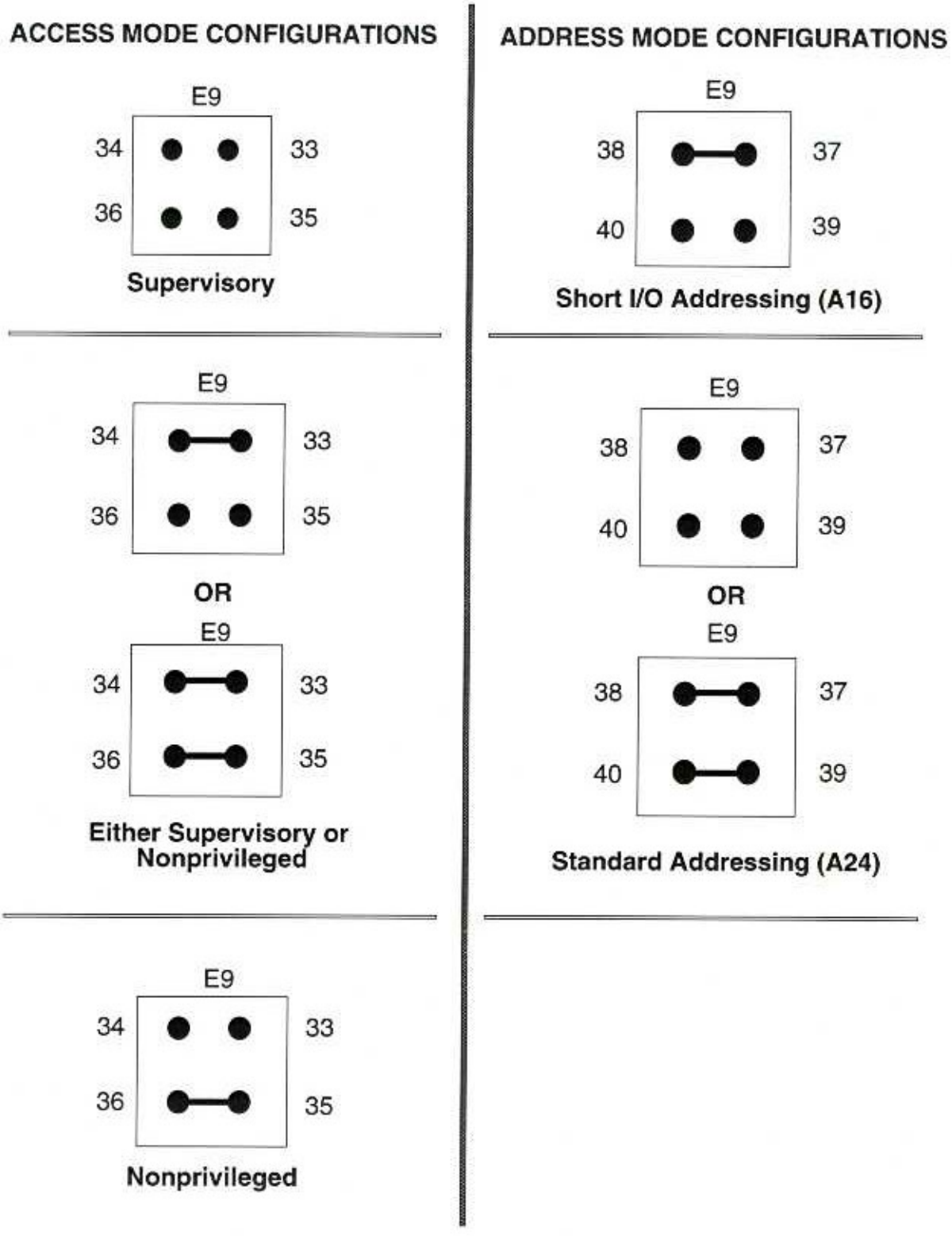


Figure 5.3-2. Access and Address Mode Configurations

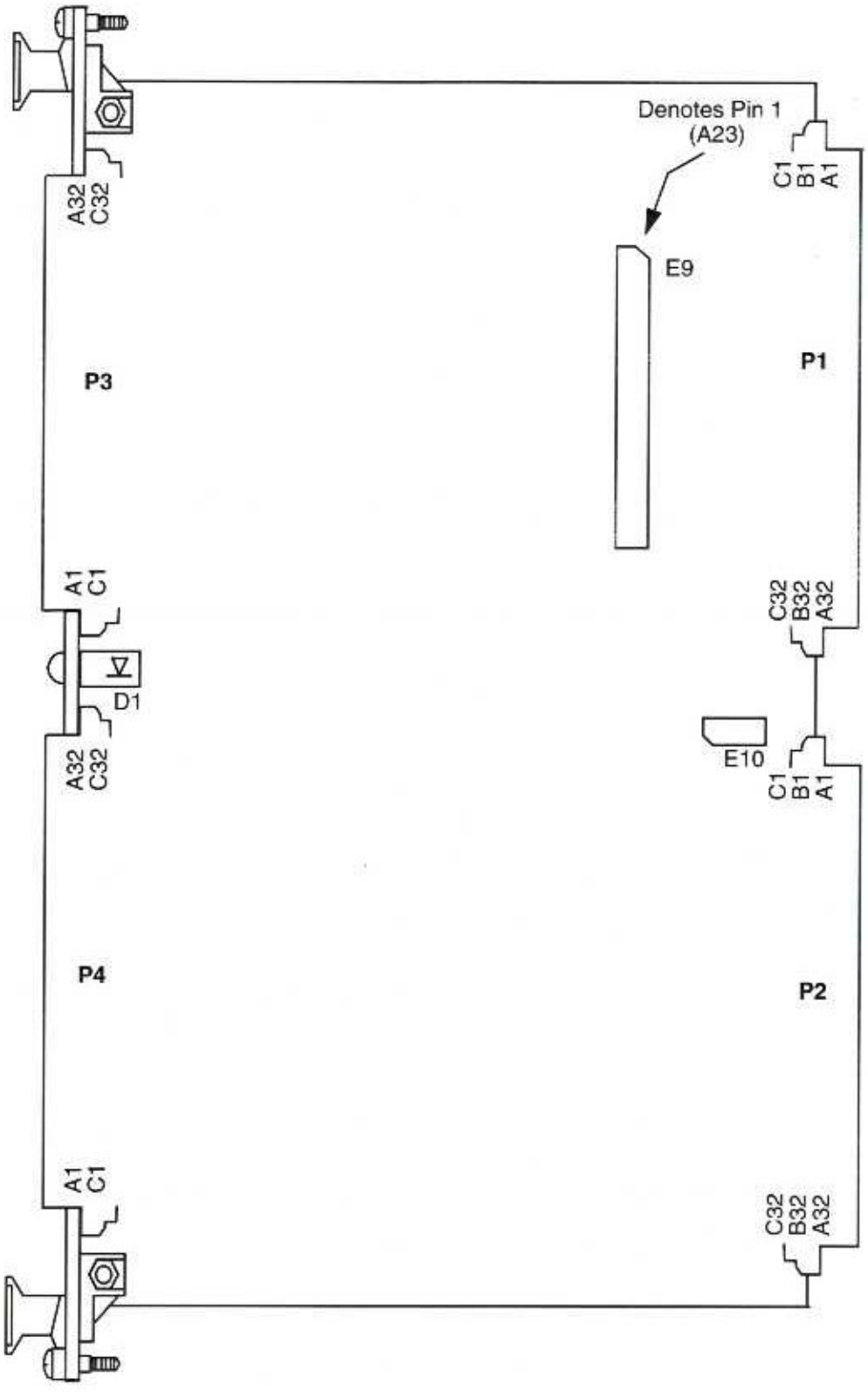


Figure 5.3-3. Location of User Configuration Jumpers

5.4 UIOC JUMPER

The UIOC Jumper alerts the DSP if the board is being used with VMIC's I/O controllers. This jumper is labelled E10. If the jumper is installed, the DSP recognizes that the board is controlled by the I/O controller. The DSP will not extinguish the front panel LED after completing self-test. If the jumper is not installed, the DSP will extinguish the front panel LED after completing self-test. The factory configuration for this bit is installed.

5.5 SYSTEM CONNECTIONS

Table 5.5-1 and 5.5-2 lists the P3 and P4 connector inputs. The connectors are shown in Figure 5.5-1. Each connector is a 64-pin DIN type connector which contains eight analog inputs.

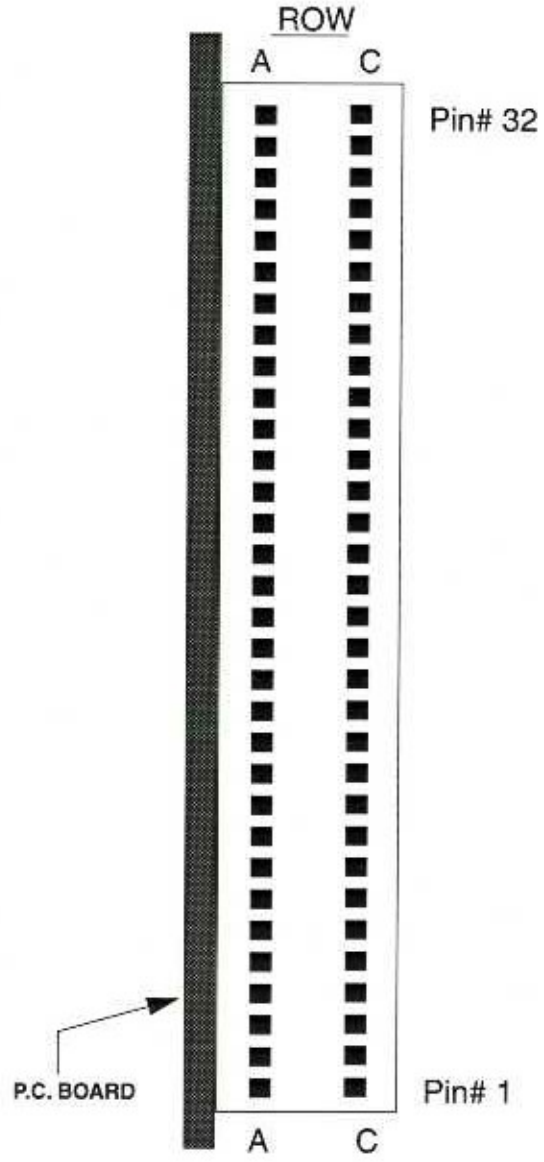


Figure 5.5-1. P3 and P4, 64-Pin DIN Type Connector

Table 5.5-1. P3 Connector Assignments

Pin#	Row A	Row C
32	Ch15_High	RTD2_Ch15
31	Ch15_Guard	RTD1_Ch15
30	Ch15_Low	Ch15_AGND
29		
28	Ch7_High	RTD2_Ch7
27	Ch7_Guard	RTD1_Ch7
26	Ch7_Low	Ch7_AGND
25		
24	Ch14_High	RTD2_Ch14
23	Ch14_Guard	RTD1_Ch14
22	Ch14_Low	Ch14_AGND
21		
20	Ch6_High	RTD2_Ch6
19	Ch6_Guard	RTD1_Ch6
18	Ch6_Low	Ch6_AGND
17		
16	Ch13_High	RTD2_Ch13
15	Ch13_Guard	RTD1_CH13
14	Ch13_Low	Ch13_AGND
13		
12	Ch5_High	RTD2_Ch5
11	Ch5_Guard	RTD1_Ch5
10	Ch5_Low	Ch5_AGND
9		
8	Ch12_High	RTD2_Ch12
7	Ch12_Guard	RTD1_Ch12
6	Ch12_Low	Ch12_AGND
5		
4	Ch4_High	RTD2_Ch4
3	Ch4_Guard	RTD1_Ch4
2	Ch4_Low	Ch4_AGND
1	P2_CAL_High	P2_CAL_Return

Table 5.5-2. P4 Connector Assignments

Pin#	Row A	Row C
32	Ch11_High	RTD2_Ch11
31	Ch11_Guard	RTD1_Ch11
30	Ch11_Low	Ch11_AGND
29		
28	Ch3_High	RTD2_Ch3
27	Ch3_Guard	RTD1_Ch3
26	Ch3_Low	Ch3_AGND
25		
24	Ch10_ High	RTD2_Ch10
23	Ch10_Guard	RTD1_Ch10
22	Ch10_Low	Ch10_AGND
21		
20	Ch2_High	RTD2_Ch2
19	Ch2_Guard	RTD1_Ch2
18	Ch2_Low	Ch2_AGND
17		
16	Ch9_High	RTD2_Ch9
15	Ch9_Guard	RTD1_Ch9
14	Ch9_Low	Ch9_AGND
13		
12	Ch1_High	RTD2_Ch1
11	Ch1_Guard	RTD1_Ch1
10	Ch1_Low	Ch1_AGND
9		
8	Ch8_High	RTD2_Ch8
7	Ch8_Guard	RTD1_Ch8
6	Ch8_Low	Ch8_AGND
5		
4	Ch0_High	RTD2_Ch0
3	Ch0_Guard	RTD1_Ch0
2	Ch0_Low	Ch0_AGND
1	P2_CAL_High	P2_CAL_Return

5.6 CALIBRATION

Before delivery from the factory, the VMIVME-3126 board is fully calibrated for each range and conforms to all specifications. Please refer to Section 3.2.5 and Figure 3.2.5-1 on page 3-6 for steps in calibrating.

The calculated gain and offset coefficients are only as good as the source used for calibration. The calibration source should have very little noise. Although the calibration routine takes an average of the input samples, a low noise source is essential on the lower ranges to get maximum results. If the accuracy of the source is in question, a precision multimeter can be connected to the board's input to measure the exact input voltage. This reading would then be used in computing the value to enter into the TCVH and TCVL registers.

A recommended source is the Hewlett Packard HP3245A Universal Source. in addition to the accurate, low noise output, this source also has a General Purpose Instrumentation Bus (GPIB) interface. This enables calibration to be handled entirely by a PC, commanding the source which determines the voltage to output. A recommended multimeter is the Hewlett Packard HP34401A. This meter also has a GPIB interface to aid in automating the calibration process.

The voltages used for calibration do not need to be symmetrical around ground for bipolar or mid-scale for unipolar scales. Due to the presence of noise in any system, the voltages used should not be very close to positive or negative full-scale. If voltages near the extremes were used, noise could cause the value to clip to full-scale and degrade the accuracy. With this in mind, the following table shows a guideline to follow for the calibration voltages.

Table 5.6-1. Calibration Guidelines

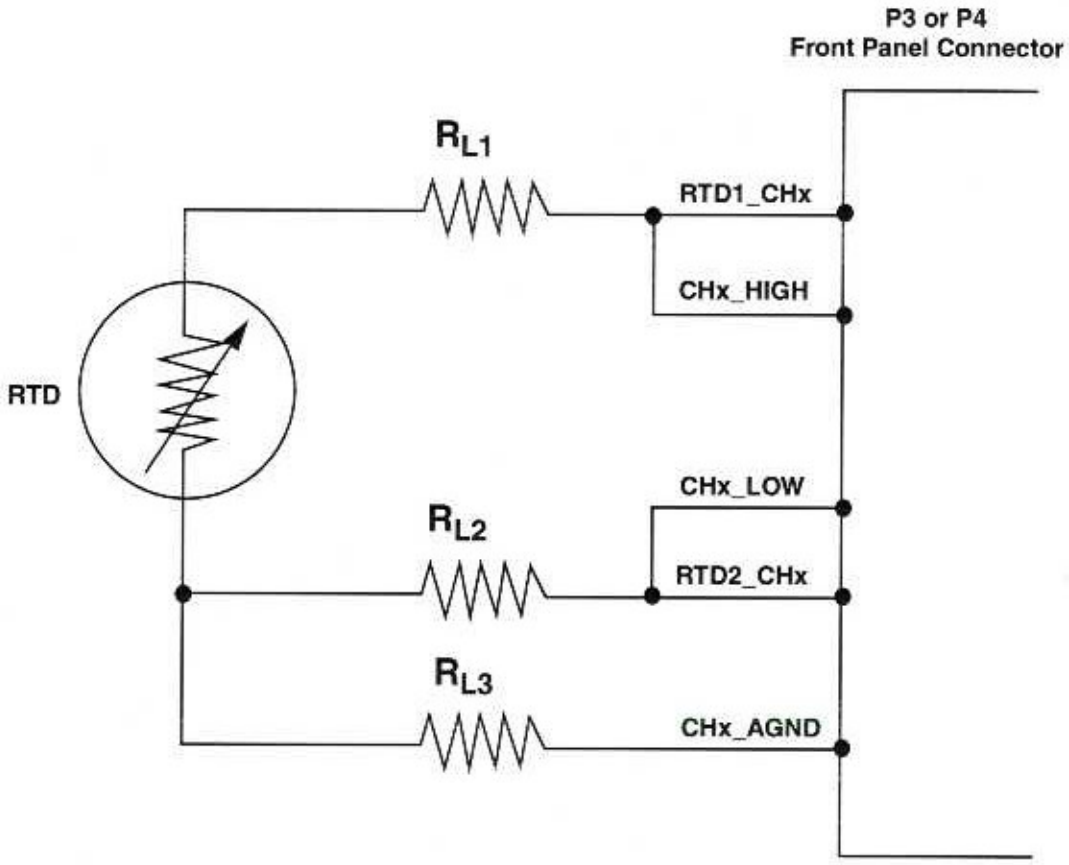
Input Scale	3-Point, %Full-Scale	5-Point, %Full-Scale	7-Point, %Full-Scale
Unipolar	75%, 50%, 25%	80%, 60%, 50%, 40%, 20%	80%, 70%, 60%, 50%, 40%, 20%, 10%
Bipolar	±75%, 0%	±75%, ±25%, 0%	±75%, ±50%, ±25%, 0%

5.7 RTD APPLICATIONS AND CONFIGURATIONS

The two main configurations for RTDs are the three-wire and four-wire interfaces. Each of these configurations will be described, along with figures showing the connections necessary.

5.7.1 Three-Wire RTD Configuration

In the three-wire configuration, shown in Figure 5.7.1-1, lead resistances will result in errors in the measurement if only one of the RTD excitation currents is used. This is because the current will flow through R_{L1} developing a voltage error between inputs CH_H and CH_L. The second RTD excitation current is used to compensate for this error by suppling the same current through R_{L2}. Assuming the lead resistances are equal, due to being the same material and same length, and the RTD sources match, the error voltages generated will match and no error voltage will be developed between the input pins. Twice the voltage is developed across R_{L3} as a common-mode voltage and will not introduce any errors.



5.7.1-1. Three-wire RTD Configuration

5.7.2 Four-Wire RTD Configuration

The RTD has to be connected to the board using wire. Almost certainly, there will be an impedance mismatch between the HIGH and LOW sides. This impedance mismatch can result in significant errors in the temperature measurement. The four-wire configuration, shown in Figure 5.7.2-1, eliminates any errors associated with lead resistances because no current flows in the measurement leads. The board measures only the voltage dropped across the RTD and is insensitive to the length of the lead wires.

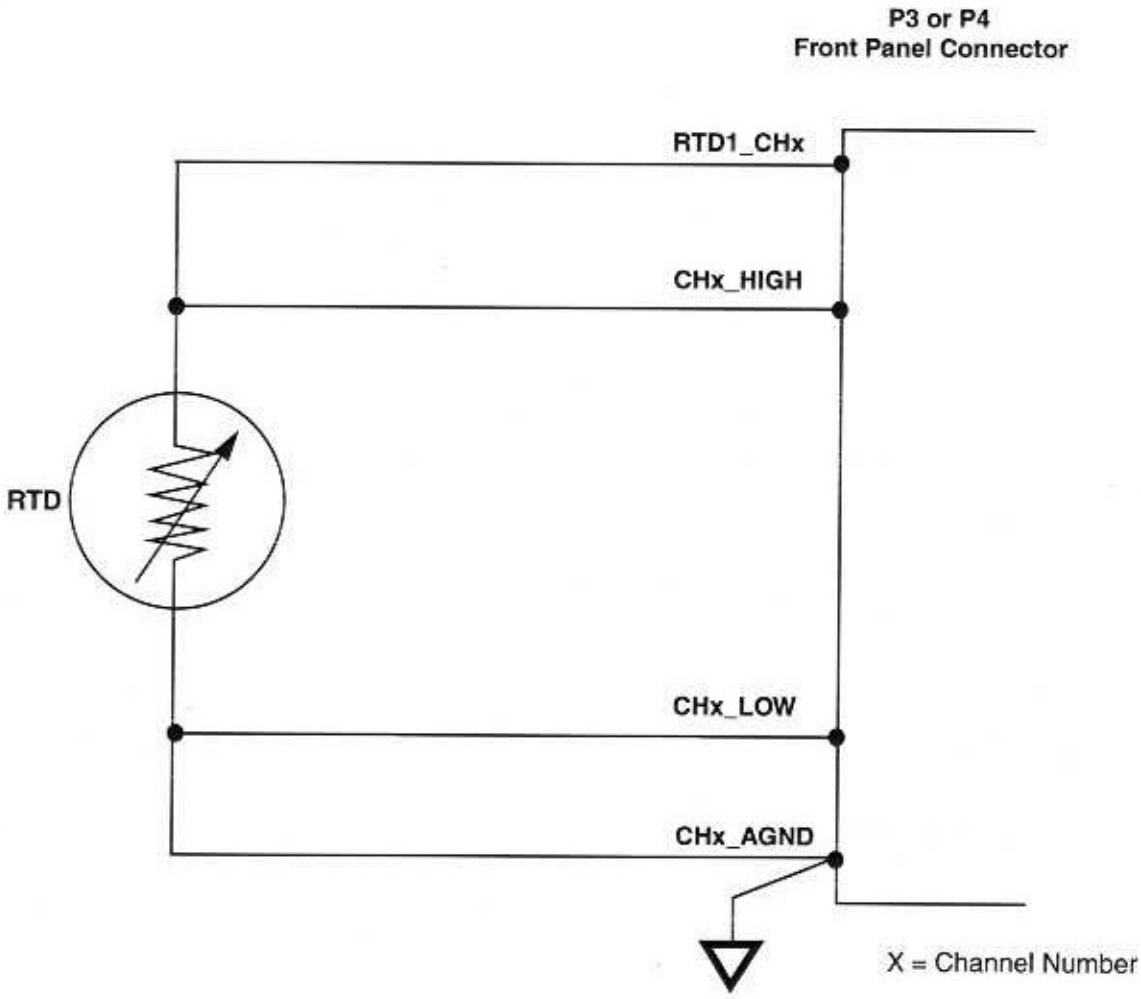


Figure 5.7.2-1. Four-Wire RTD Configuration

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software

b. System configuration

c. Electrical connections

d. Jumper or configuration options

e. Boards are fully inserted into their proper connector location

f. Connector pins are clean and free from contamination

g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis

h. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

ACKNOWLEDGEMENTS

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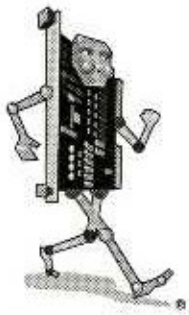

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APPENDIX A

ASSEMBLY DRAWINGS, PARTS LIST, AND SCHEMATIC