VMIVME-4122

8-channel 12-bit Analog Output Board

Product Manual

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Table of Contents

List of Figures

List of Tables

Overview

Introduction

The VMIVME-4122 is an Analog Output board providing 8-analog output channels, with 12-bit resolution. The VMIVME-4122 series are voltage output boards. The VMIVME-4122 is a 3U form factor board that fits in a VMEbus chassis. Each output has a dedicated Digital-to-Analog Converter (DAC) assigned to it (two quad DACs). After system resets, the DACs are driven to zero volts and, the field connect bit is cleared. The VMIVME-4122 output is disconnected from the field wiring. The analog voltage outputs can be disconnected from the field wiring for off-line testing. The output range is jumper selectable. The Built-In-Test (BIT) is used to verify correct operation of the unit. Each output can be read back, using an internal 12-bit Analog-to-Digital Converter to verify it's correct setting.

Features

Listed below are the primary features of the VMIVME-4122 board:

- 8-analog output channels
- One 12-bit D / A Converter (DAC) per output channel
- Built-In-Test (BIT) 12-bit ADC and 8-channel analog multiplexer
- Double buffered DAC input data latches
- Data read back capability from DAC output register
- Random update (Non-Scanning) and simultaneous update
- Discrete wire or mass terminated cables
- External Transistor Transistor Logic (TTL) level simultaneous update input
- External TTL output capable of triggering other VMIVME-4122 boards
- Software Trigger Update
- Front panel status LED
- Two's complement to offset binary data conversion
- Built-In ±15VDC power supply
- Unipolar (0 to +10V or 0 to +5V) or Bipolar (±2.5, ±5, ±10V)
- 10 mA maximum output current per channel
- Outputs can be disconnected from the field
- 0.8Ω output impedance
- 12-bit Built-In-Test (BIT) ADC range

VmeBus Products

The VMIVME-4122 is a single height 3U form factor board. This board complies with the VMEbus specification (ANSI / IEEE STD1014-1987 IEC 821 and 297) with the following mnemonics:

Addressing Mode A16	Responding Address Modifiers
	$29 (Short nonprivileged I / O access) or $2D (Short supervisory I / O access)
Data Accesses:	D16, D08(EO), D08(O)

NOTE: ADC and DAC access must be D16 (word) only.

The VMEbus physical base address for the board is selected address lines A15 through A07 and Address modifier bit AM2. These are jumper-selectable and decoded to support nonprivileged, supervisory or both address modifiers. Output data is written to a 16-bit register (12-bit right justified and sign extended) that corresponds to the output channel. This data is stored in on-board memory. The data is modified by the board and sent to the corresponding output DAC. Built-In-Test permits the user to select an output channel and determine if it is functioning properly. The voltage measured on the VMIVME-4122 board is the voltage fed to the buffer amp. After a system reset, the board will place all outputs to zero, clears all bits in the Control / Status Register (CSR), and turn on the panel LED. The LED must be extinguished under software control. This LED can be used to visually locate a faulty board in a system. Reset places the board in a known configuration. This is explained in detail in “Theory of Operation” on page 17 of this manual.

References

For a detailed description and specification of the VMEbus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook
VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

The following application and configuration guides are available from VMIC to assist the user in the selection, specification and implementation of systems based on VMIC's products.

Digital Input Board Application Guide (Document No. 825-000000-000)

Digital I/O (with Built-in-Test) Product Line Description (Document No. 825-000000-003)

Analog I/O Products (with Built-in-Test) Configuration Guide (Document No. 825-000000-005)

Connector and I/O Cable Application Guide (Document No. 825-000000-006)

Physical Description and Specification

Refer to VMIC's Specification No. 800-004122-000 for detailed specifications.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

CHAPTER

1

Theory of Operation

Introduction

The VMIVME-4122 Analog Output board provides 8-analog output channels with 12-bit resolution. The VMIVME-4122 can source or sink 10 mA at up to ±10V. Each output has a dedicated Digital-to-Analog Converter (DAC) assigned to it. After system resets the DACs are driven to zero. The analog outputs can be disconnected from the field wiring for off-line testing. The output voltage range is user selectable with jumpers. The base address and the access mode are jumper selectable.

Functional Organization

The VMIVME-4122 is divided into the following functional categories. Each category will be discussed in detail in this section of the manual.

- Bus interface
- Data manipulation
- Output DACs
- BIT multiplexer and ADC

VMEbus Interface

The VMIVME-4122 communications registers are memory mapped as 64 (decimal) 16-bit words (128-bytes) in memory. The registers are contiguous and may be user located on any 128-byte boundary within the short I/O space of the VMEbus. The board can be user configured to respond to short supervisory or short nonprivileged data accesses, or both.

During each read or write operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on board selection jumpers shown in Figure 2-1 on page 31 and the address and address modifier line from the back plane. The appropriate board response occurs if a valid match is detected, after which the open collector DTACK* interface signal is asserted (driven low). Subsequent completion of the bus master's read or write cycle causes the board-generated DTACK* signal to return to the OFF state.

After board-selection has occurred, three groups of VMEbus signals control communication with the board. They are as follows:

1. Data bus lines D00 to D15
2. Address lines A01, A02, A03, A04
3. Bus Control Signals:
    a. Write
    b. DS0*, DS1*

Data Bus lines are bi-directional and move data to and from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A07 map the 12 registers into the bottom of a 128-byte range within the VMEbus address space described in "Programming" on page 41. The control signals determine whether data is to be moved to the VMIVME-4122 (write) or from the VMIVME-4122 (read), provide the necessary Data Strobes (DS0*,DS1*). A SYSRESET* input resets all CSR bits.

Static controls are latched into the Control and Status Byte and are used to establish the operational mode of the board. Status flags, necessary for monitoring and controlling the external trigger logic and the ADC, are read through the Trigger Byte and ADC Status Byte respectively. The Control Registers and Status Registers are referred to collectively as the Control/Status Register (CSR), since they are at the same address. The WRITE signal determines which one is accessed.

Output DACs

The output DACs (two quad DACs) convert the manipulated data into a voltage based upon the reference voltage applied to the converters.

In the VMIVME-4122 this reference voltage is selected by jumpers. This determines the output voltage range of the DAC. See Table 2-2 on page 30 for jumper configuration.

VMIVME-4122 Buffers and Switches

The DAC's output is buffered, which provides the high current drive for the outputs. The output is routed through an electronic switch that is used to disconnect it from the cable for off-line operation.

Bit Multiplexer and Analog-to-Digital Converter

When the user *writes* data to the Board Data Access Pointer Registers, the Built-in-Test (BIT) Multiplexer (MUX) will decode the channel that is stored in three bits of the register. A write to the Board ADC Access Word Register will convert that channel's output voltage. The VMIVME-4122 BIT uses an internal 12-bit ADC. The *USER* may select the ADC input range to match the DAC's range or the user may leave the ADC in the ±10V range which has a reduced resolution with other DAC ranges.

Board ID Register

The first word location of the VMIVME-4122 family register set is a read / write register. It always reads 33XX HEX for the VMIVME-4122 (the last two digits are Trigger Byte bits). See “Programming” on page 41 for further definitions.

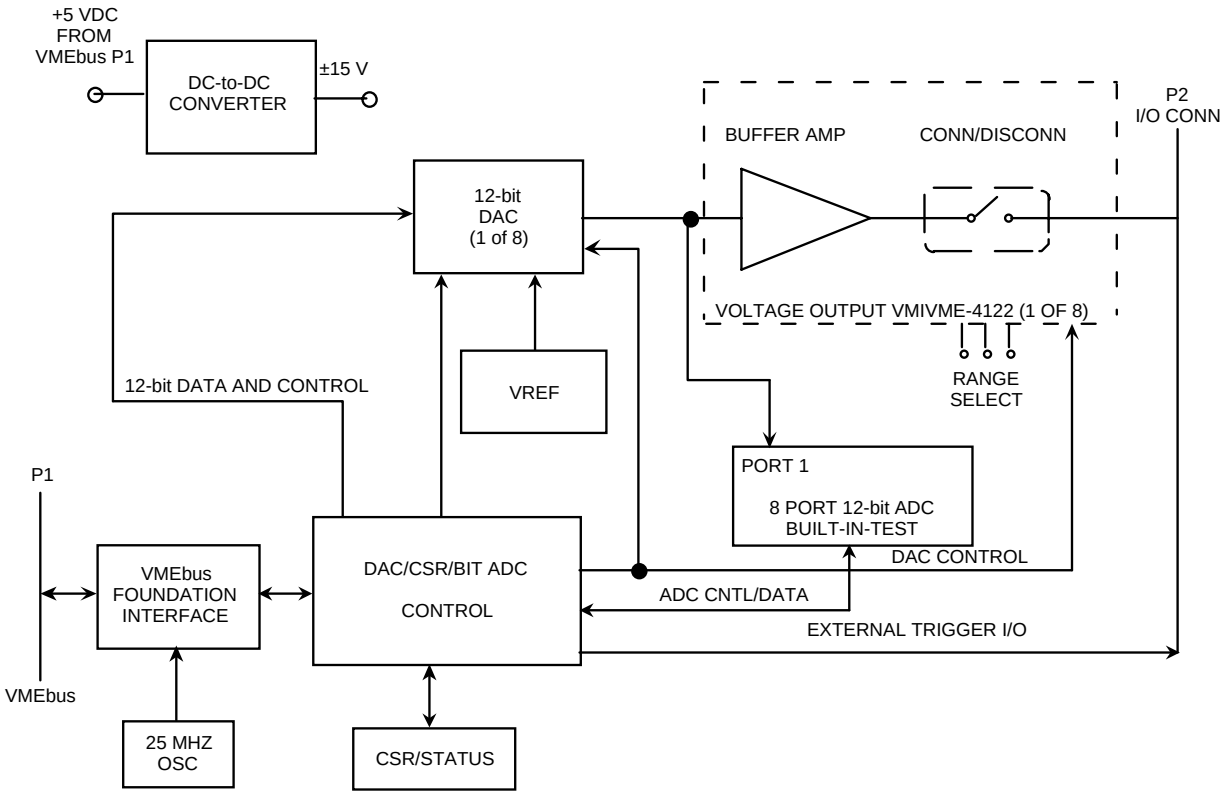
Built-in Power Converter and ADC Power Supply

Electrical power for the VMIVME-4122 analog circuitry is supplied by the on-board DC-to-DC converter as shown in Figure 1-1 on page 24. The DC-to-DC converter transforms +5VDC from the VMEbus P1 connector, into a regulated ±15VDC, with a load capacity of 170 mA on each 15V bus.

DAC Output Update Control

Bits in the CSR enable multiple ways to load the DAC's output register. After the input register is loaded, it takes a "load" signal to transfer the input register value to the output register. Once the load is generated, it takes typically 6 µsec for the DAC output to settle to 0.01%. There are four ways to cause the DAC to change outputs. The first is the automatic mode. In the automatic mode, once the input register is written, that channel is subsequently loaded. In the internal mode, a software-generated signal in the Board Trigger Byte Register is required to cause an 8-channel simultaneous update. In the last two modes, an external input signal is used to cause the load to occur. See "External Simultaneous Input / Output Update" on page 25.

Figure 1-1 VMIVME-4122 Functional Block Diagram



External Simultaneous Input/Output Update

An input is provided to allow an external signal to update simultaneously all eight DACs. The signal level should be TTL CMOS compatible. Either edge high to low or low to high may be used to trigger the event. The trigger edge is programmable in the CSR register. The external input can be enabled or disabled by the CSR register. Status bits in the Board Trigger register are provided so that the controlling software can detect when a load has occurred. Once detected, the controller must load the next new value to be output. A hardware register bit is routed to the external input trigger so that software may test this input. This signal may also be driven as an output. The customer may use it to generate an external update to other VMIVME-4122 boards in the system. Thus, one VMIVME-4122 acts as a master and the other boards are updated simultaneously as slaves.

CHAPTER
2

Configuration and Installation

Contents

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

NOTE: Do not install or remove board while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated. Review "Before Applying Power: Checklist" below and "Configuration" on page 29 before operating the board.

Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming of the board, "Theory of Operation" on page 17 and "Programming" on page 41, been read and applied to system requirements?
2. Review "Configuration" on page 29 to verify that all jumpers are configured correctly for the application.
3. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to "Analog Output Connector Description" on page 30 for connector descriptions.
4. Physical installation should have been completed as described in "Physical Installation" above.
5. Ensure that all system cable connections are correct.

Configuration

There are a number of jumpers used to configure this unit for a particular application. The test points are shown in Table 2-1 below and Table 2-2 on page 30 shows the analog output range settings. Table 2-3 on page 30 shows the factory installed jumpers while Figure 2-1 on page 31 is a diagram of the user configurable jumpers and test points.

Table 2-1 VMIVME-4122 Test Points

Test Point	Description
TP1	Voltage Reference Test Point
TP2	Analog Ground
TP3	Input to Built-In-Test ADC

Analog Output Connector Description

The 8-analog output connections to the VMIVME-4122 board are made using the front panel 37 pin D-Shell subminiature Connector labeled P2. See Table 2-4 on page 32 and Figure 2-2 on page 33 for connector pin and signal assignments.

Table 2-2 Analog Output Range Jumper Settings

		E1	E3	E4	E5	E6	E7	E8
UNIPOLAR	0 to 2.5	IN	1-2	OUT	IN	1-2	1-2	2-3
	0 to 5	OUT	1-2	IN	OUT	1-2	1-2	2-3
	0 to 10	OUT	1-2	OUT	OUT	1-2	1-2	2-3
BIPOLAR	-2.5 to +2.5	IN	2-3	OUT	IN	2-3	2-3	2-3
	-5.0 to +5.0	OUT	2-3	IN	OUT	2-3	2-3	2-3
	-10.0 to +10.0	OUT	2-3	OUT	OUT	2-3	2-3	1-2

Table 2-3 VMIVME-4122 Analog Factory-Installed Jumpers

VMIVME-4122 Jumper E No.	Description	Pins 1-2	Pins 2-3	Omitted
E1	Jumper pins 1-2 2.5VDC outputs, pins 2-3 all other ranges (VREF ADJ)		X	
E3	Ch 4: Pins 1-2 unipolar, pins 2-3 bipolar		X	
E4	Jumper for 5VDC outputs only			X
E5	Jumper for 2.5VDC outputs only			X
E6	Ch 0 to 3: Pins 1-2 unipolar, pins 2-3 bipolar		X	
E7	Jumper pins 1-2 unipolar ADC input, pins 2-3 bipolar ADC input (ADC offset ADJ)		X	
E8	Jumper pins 1-2 ±10.000VDC ADC input range, pins 2-3 all other ranges	X		
E9	(Factory only) ADC ground			X
E10	Access jumper, pins 1-2 user only, pins 2-3 supervisory only, no jumper both supervisory and user			X

Figure 2-1 VMIVME-4122 Configuration Jumpers

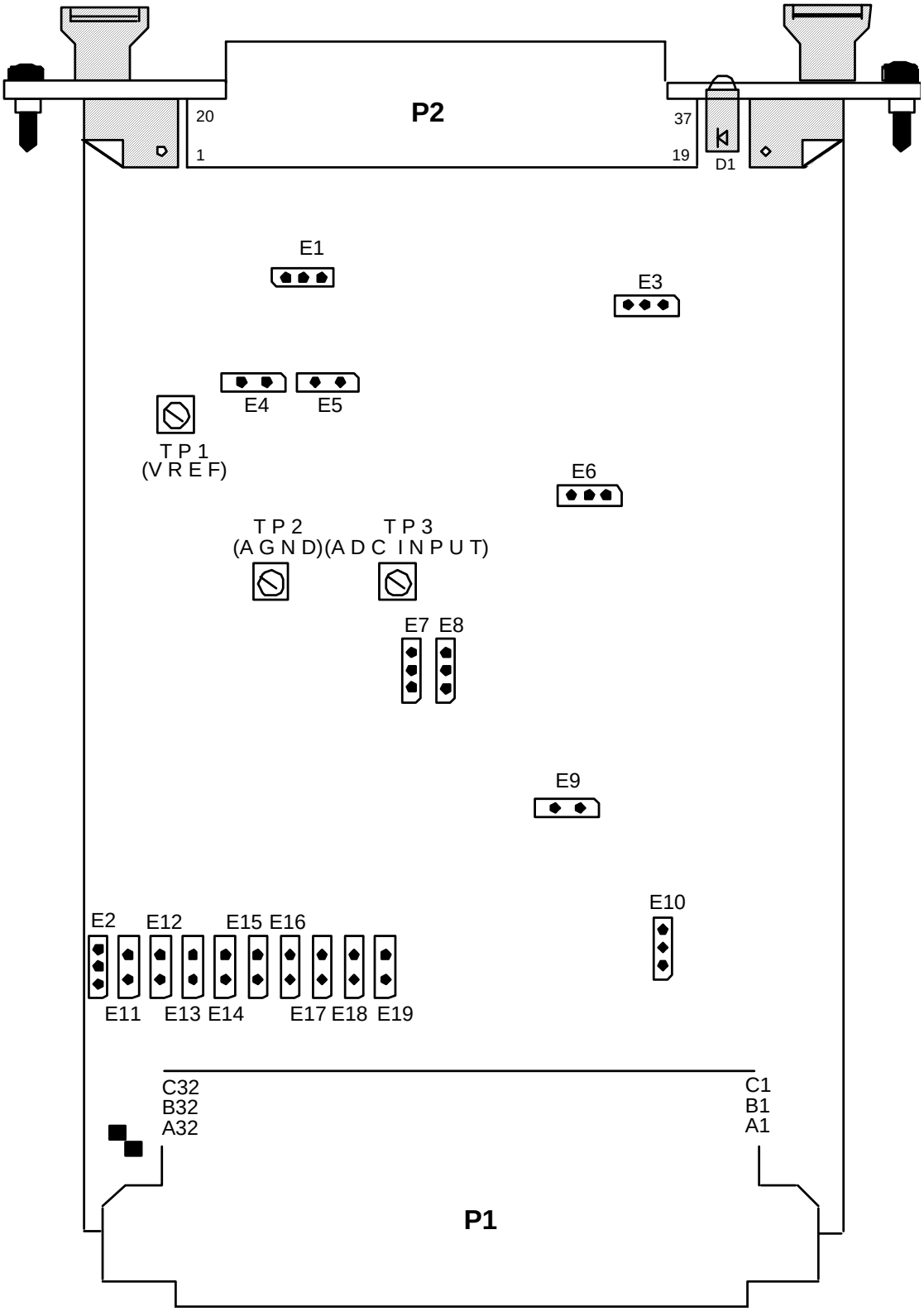
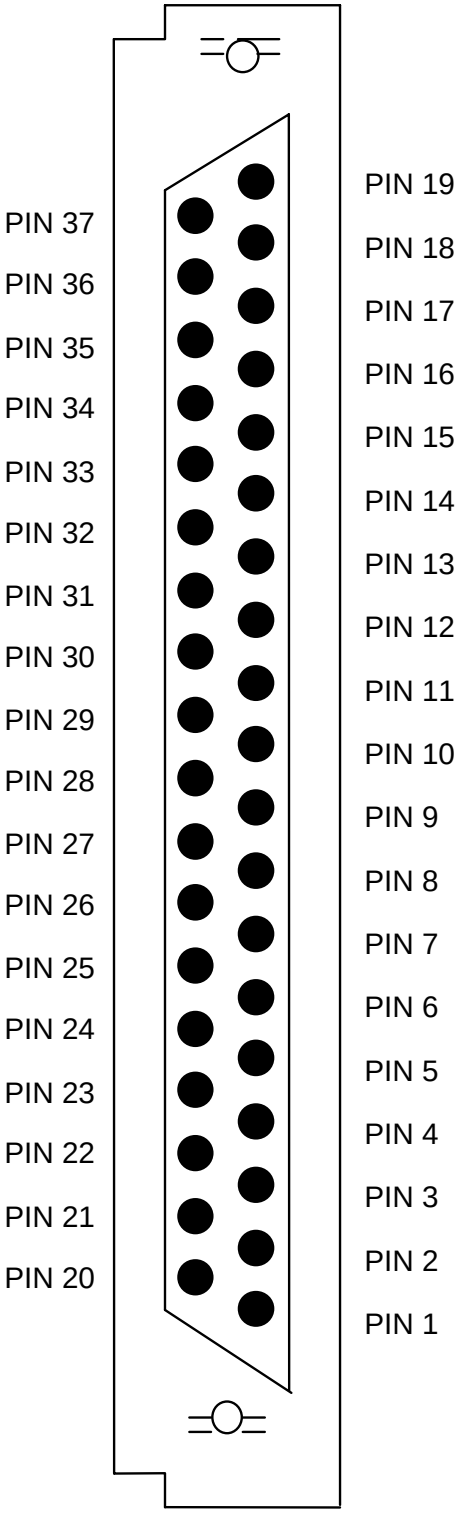


Table 2-4 VMIVME-4122 P2 Connector Pin-Out

Pin No.	Signal Description
1	Channel Zero Output
2	
3	Channel One Output
4	
5	Channel Two Output
6	
7	Channel Three Output
8	
9	Channel Four Output
10	
11	Channel Five Output
12	
13	Channel Six Output
14	
15	Channel Seven Output
16	
17	Voltage Reference Output Low
18	Voltage Reference Output High
19	External Trigger Input
20	Ground (Analog Ground)
21	
22	Ground (Analog Ground)
23	
24	Ground (Analog Ground)
25	
26	Ground (Analog Ground)
27	
28	Ground (Analog Ground)
29	
30	Ground (Analog Ground)
31	
32	Ground (Analog Ground)
33	
34	Ground (Analog Ground)
35	
36	
37	Digital Ground

Figure 2-2 VMIVME-4122 P2 Connector

FRONT VIEW (CABLE SIDE) OF "P2" CONNECTOR



VMIVME-4122 Analog Output Range

There are three output ranges which can be selected 10V, 5V, and 2.5V. Selection is made using on-board jumpers, see Table 2-2 on page 30.

VMIVME-4122 Analog Output: Bipolar, Unipolar

The output can be either unipolar 0 to 10V, 0 to 5V, 0 to 2.5V or bipolar ±10, ±5 and ±2.5V. Selection is made using on-board jumpers, see Table 2-2 on page 30.

Board Address Jumpers

An installed jumper indicates a logic “0” is selected for the match requirement.

Table 2-5 Board Address Jumpers

VMIVME-4122 E No.	Description	Jumper (Default)
11	Board Address A7	Installed
12	Board Address A8	Installed
13	Board Address A9	Installed
14	Board Address A10	Installed
15	Board Address A11	Installed
16	Board Address A12	Installed
17	Board Address A13	Installed
18	Board Address A14	Installed
19	Board Address A15	Installed
10	Supervisory 1-2, User 2-3	Omitted

Address Modifiers Jumpers

Jumper E10 selects the required address modifier; either nonprivileged, supervisory or both nonprivileged and supervisory.

Table 2-6 Address Modifier Selections

VMIVME-4121 E No.	Description	Pin Selection
E10	A16 Both Nonprivileged And Supervisory	No Jumper (Default)
E10	A16 Supervisory Access Only	PINS 1-2
E10	A16 Nonprivileged Access Only	PINS 2-3

Calibration

See Figure 2-3 on page 36 for the locations of user adjustable potentiometers and Figure 2-4 on page 39 for the calibration connector test fixture.

Equipment Required

- 4 1/2-digit DVM
- Load resistor(s) 1 kΩ watt 1 percent
- Standard 37-pin D-Shell subminiature Connector (male)

Analog Offset and Gain Calibrations

Calibrating the VMIVME-4122: Potentiometer Adjustments

This section assumes a unipolar 0 to 10VDC output.

1. R1 *Voltage Reference*. Adjust POT until test point TP1 = 10.240VDC.
2. Adjust *Output Voltage Span*. With selected channel at full-scale, adjust for maximum output, then *Adjust Output Voltage Offset*. With selected channel at $000, adjust for minimum output.

NOTE: Toggle between adjustments, these adjustments are interrelated.

Use a DVM to measure the output voltage across a 1 kΩ load resistor.

a. Channel 0 Span: R2

b. Write to all DACs (4095)

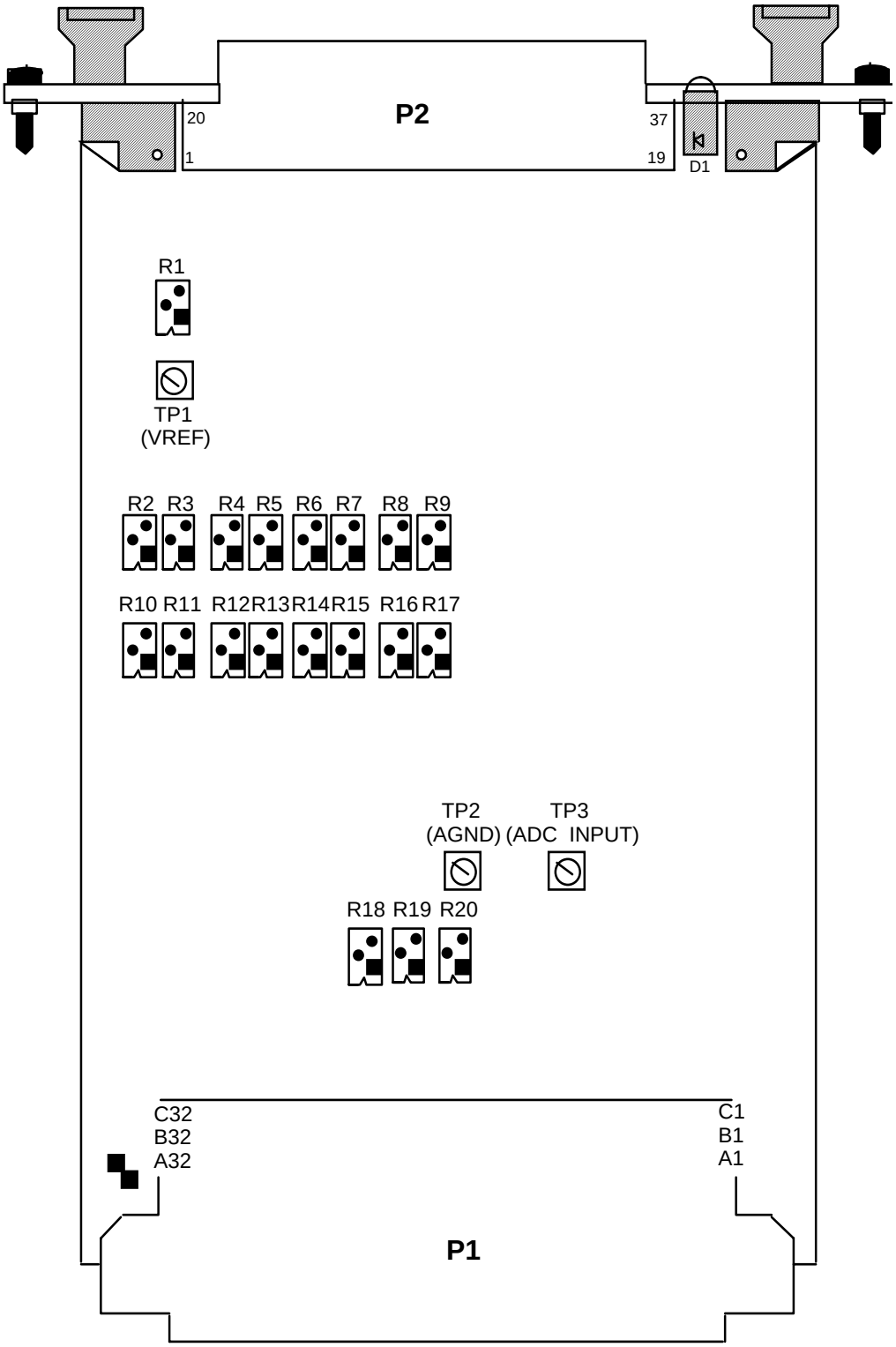
c. Read Output with A DVM, adjust POT to full-scale of the desired output range.

d. Channel 0 Offset: R3

e. Write to all DACs (0)

f. Read Output with A DVM, adjust POT for 0.00VDC.

Figure 2-3 VMIVME-4122 Potentiometer Locations



Repeat steps a through f above for the next 6 pairs of POTs for channelsone to seven:

Channel 1 Span: R4	Channel 5 Span: R12
Channel 1 Offset: R5	Channel 5 Offset: R13
Channel 2 Span: R6	Channel 6 Span: R14
Channel 2 Offset: R7	Channel 6 Offset: R15
Channel 3 Span: R8	Channel 7 Span: R16
Channel 3 Offset: R9	Channel 7 Offset: R17
Channel 4 Span: R10	
Channel 4 Offset: R11	

Calibrating The VMIVME-4122

This section assumes a unipolar 0 to 10VDC output

R18: *Unipolar ADC offset* or R20 *Bipolar offset*

Unipolar: With 0.0VDC at TP3 (ADC input) TP2 (ADC GND) (monitoring a zero volt DAC output channel) adjust offset POT for an output code of 000/001 toggle.

1. Configure unit for unipolar 0 to 10VDC output range (see Table 2-2 on page 30).
    a. Write to all DAC zero HEX
    b. Read DAC zero with BIT
    c. Confirm 0.0 at TP3
    d. Adjust POT R18 until reading toggles 000/001

Bipolar: With full-scale negative -10.000VDC at TP2 (ADC input) (monitoring a bipolar full-scale negative DAC output channel) adjust offset POT for an output code of 000/001 toggle.

1. Configure unit for bipolar output range (see Table 2-2 on page 30).
    a. Write to all DACs (zero, full-negative scale)
    b. Read DAC zero with BIT
    c. Confirm -10.000 at TP3
    d. Adjust POT R18 until reading toggles 000/001

2. R19: ADC GAIN

   With unit configured for unipolar or bipolar range: With full-scale output (+10.000) VDC at TP3 (ADC input) TP2 (ADC GND) (monitoring a full-scale DAC output channel) adjust R19 for an output code of FFF.

   a. Write to all DACs (4095)

   b. Read DAC zero with BIT

   c. Confirm +10.000VDC at TP3

   d. Adjust POT until reading is FFF HEX

Figure 2-4 VMIVME-4122 37-Pin D-Shell Calibration Connector

R = 1 kΩ 0.1% 1/4 watt or better resistors

CHAPTER
3

Programming

Contents

Introduction

The VMIVME-4122 Analog Output boards are controlled through 12 registers. The base VMEbus address is set by configuration of a jumper field. A jumper exists for each of the addresses A15 through A7; thus, the address space occupied by this board is 128 consecutive bytes. Address modifier bits are jumper-selected and decoded to support nonprivileged, supervisory, or both nonprivileged and supervisory board accesses.

Base Registers

The base registers are the Board ID registers (BID), the Control / Status Register (CSR) and the Board Data Access Pointer register. The base address of the board is set by user configurable jumpers. The address modifier for the board can be fixed at nonprivileged or supervisory accesses or it can be set to respond to either address modifier. The remaining jumpers fix the base address of the board.

Table 3-1 VMIVME-4122 Board Register Map

Register Address (Hex)	Register Designation	DESIG	Access
00	Board Identification Byte	BID	Read
01	Trigger Byte	TB	Read / Trigger
02	Control and Status Byte	CSR	Read / Write
03	ADC Status Byte	ADCS	Read
04	Reserved	...	...
05	Board Data Access Pointer	DAP	Read / Write
06	Board ADC Access Word	ADC	Read / Write
08	DAC Channel 0 Data Word	DAC 0	Read / Write
0A	DAC Channel 1 Data Word	DAC 1	Read / Write
0C	DAC Channel 2 Data Word	DAC 2	Read / Write
0E	DAC Channel 3 Data Word	DAC 3	Read / Write
10	DAC Channel 4 Data Word	DAC 4	Read / Write
12	DAC Channel 5 Data Word	DAC 5	Read / Write
14	DAC Channel 6 Data Word	DAC 6	Read / Write
16	DAC Channel 7 Data Word	DAC 7	Read / Write
18 - 7E	Reserved	—	—

Board ID Register

The first word location of the VMIVME-4122 register set is a read register. It will read 33XX Hex for the VMIVME-4122 (the last two digits are Board Trigger Byte bits). This allows general-purpose system software to automatically determine what boards have been installed (by reading from a predetermined list of addresses).

Byte zero contains the unique Board ID. Byte one (see Table 3-2 on page 43) is used as external trigger status information. When an external trigger is detected, the LSB is set to indicate an external trigger has occurred. This status flag may be reset by writing to the Board Trigger Byte.

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Table 3-2 Word 0: Board Identification Register Bit Map (Read)

Board ID (Byte 0) Read Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0		1		0		1	

Board Trigger Byte (Byte 1) Read/Trigger							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0						EXT TRIG Status	

Word 0 Board Identification Register Bit Definitions:

Bit 8 to Bit 15 These bits contains the Board ID (33XX)

Bit 2 to Bit 7 Reserved forced to zero's

Bit 1 to Bit 0 EXT TRIG Status — These bits contains the External Trigger Status (see Table 3-3)

Table 3-3 External Trigger Status Bit Map

Bit Position	Bit Name	Indication
0-1	External Trigger Status	00 = No external triggers seen 01 = 1 trigger has occurred 11 = 2 triggers have occurred, 'over run DAC' 10 = Undefined

External Trigger Status Bits

The Board ID Word 1 register bits D0 and D1 contain the external trigger status information bits. These bits are read to indicate activity on the external input trigger. Reading a 00 will indicate that the trigger has not occurred. Reading a 01 indicates that a trigger has occurred. If you write to this register, the status bits are cleared to a zero. The register is normally cleared by software after all 8-DAC input registers have been rewritten. If you do not reset the 01 status condition, it will sequence to 11 on the next trigger input. This indicates the DAC was 'over run' by the external signal. The software did not refresh the DACs before the next update request was received.

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Table 3-4 Word 2: Control and Status/ADC Status Register

Control and Status (Byte 2) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED Off	Field	SYNC Drive	Reserved		Two's Complement	Tmode 1	Tmode 0

ADC Status Byte (Byte 3) Read Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0							ADC Busy

Word 2: Control and Status/ADC Status Register Bit Definitions:

Bit 15 — LED Off — A logical 1 written to this bit location causes the front panel status LED to be turned off. A logical 0 written to this bit location causes the front panel status LED to be turned on. (Default is logic 0).

Bit 14 — Field Connect — A logic one enables the DAC outputs to the external field wiring. A logic zero disconnects field wiring.

Bit 13 — SYNC Drive — A one in this bit location will drive the external Trigger pin low to allow off-line testing.

Bit 11 to Bit 12 — Reserved — Not Used

Bit 10 — Two's Complement — Reset or power-up will disable 2's complement read / write data. (Default is logic 0)

Bit 9 to Bit 10 — Tmode [1:0]) — Trigger Mode control bits. This field is used to select the trigger event as shown in Table 4.2.3-2. (Default is logic 00). There are four trigger modes supported on the VMIVME-4122. Two of these are internal modes and two are external modes. The last mode is something of a hybrid between internal and external and is useful for self tests and for synchronizing the outputs of up to four VMIVME-4122 boards in a single VMEbus chassis. The term "trigger" as used here means to transfer data from all DAC input registers to their associated output registers. This transfer signal is simultaneous to the 8 DACs on a single board within a few nanoseconds and simultaneous to within a few tens of a nanosecond between multiple boards tied to a common trigger signal. Note that these numbers do not include the slewing time required by each DAC to reach its new output value.

Table 3-5 Trigger Mode Function

Mode 1	Mode 0	Function
0	0	Auto Trigger (Default)
0	1	External (+) Trigger
1	0	External (-) Trigger
1	1	Internal Only Trigger

Trigger Mode Function Definitions

The VMIVME-4122 has been designed to meet the systems requirements of a broad range of applications. It offers a very flexible set of triggering modes. Systems designers / integrators using a VMIVME-4122 will find their DAC output triggering requirements fall into one of the following classifications:

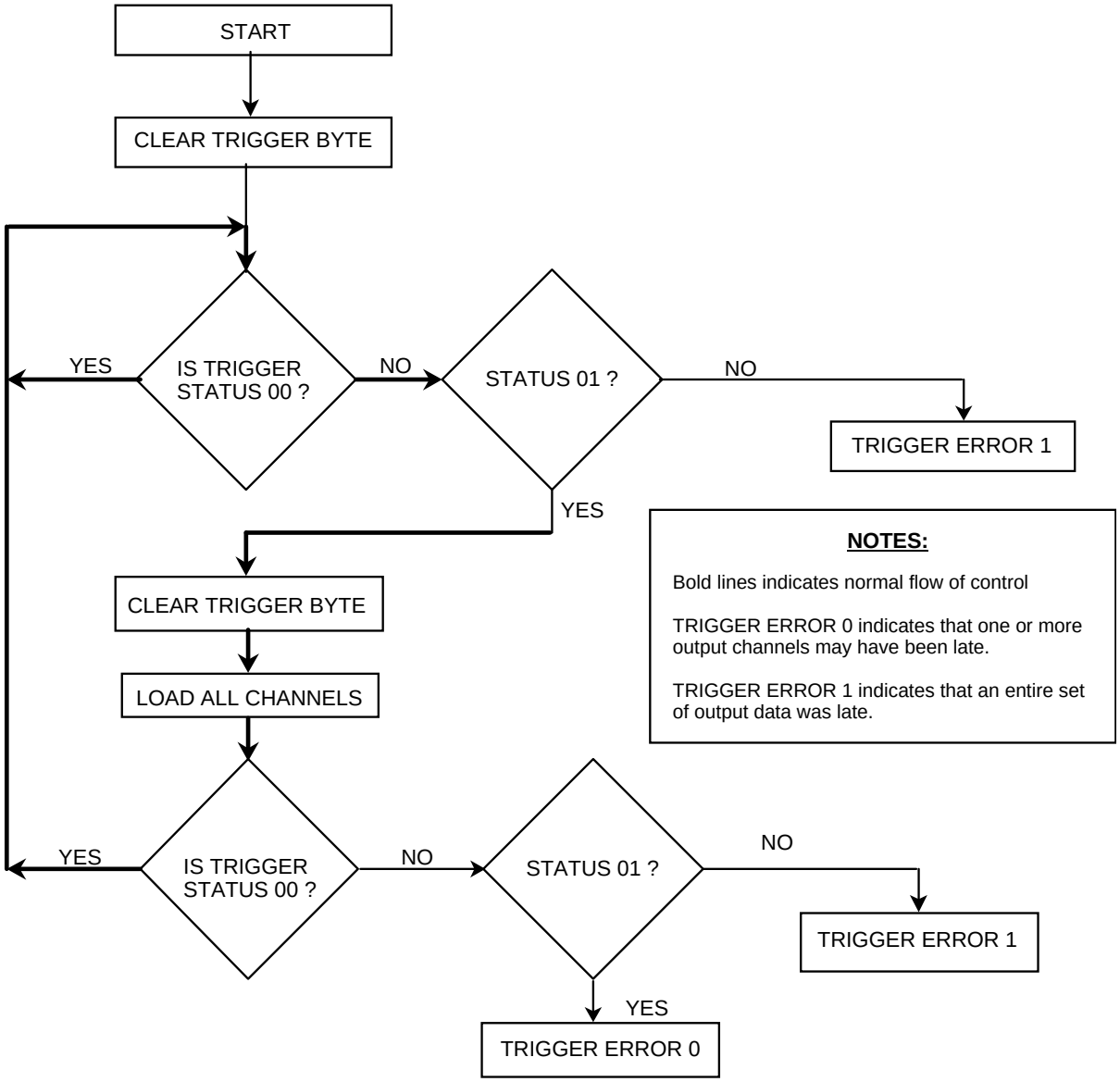
- **No Trigger required (Autoload outputs)** — Each VMIVME-4122 DAC output will change immediately in response to a new data value written into its input register. Any data loaded into the input register is immediately transferred to the output register (and will immediately change the VMIVME-4122 output voltage). This is the default trigger mode upon reception of a backplane reset signal. Many applications do not require tight time synchronization of the multiple output channels of an output card (or of outputs of multiple cards). For these applications this is the simplest mode of operation.
- **Trigger on software issued command (Internal mode)** — Each VMIVME-4122 DAC output will hold its previous output value even after a new and different value has been written to its input register. Any data written to an input register may be read back as desired but will not be transferred to its associated output register until the trigger command occurs. Use of this mode allows all eight DAC channels to be loaded with new data without any output changes. The simultaneous transfer of all data from the 8 input registers to the 8 output registers occurs when the trigger command is recognized. The trigger command is a byte or word write to the Trigger Byte. The data written is ignored. This mode is useful when the system software knows when to update all DAC outputs to the new state and there is desire to have all DAC outputs begin slewing to their new values simultaneously.
- **Trigger on externally supplied signal (External +, External -)** — The storage of data into each of the DAC input registers occurs under software control as above, but the trigger command that moves all data to the output registers now comes from an externally supplied TTL level logic signal. The detection of an edge on the External Trigger pin is the trigger event. Either a rising edge logic transition (in External + mode) or a falling edge logic transition (in External - mode) may be selected. In either case the non-selected transition is ignored. The External Trigger pin may be driven with almost any TTL, LS TTL, or CMOS logic gate source, either totem-pole, tri-state or open collector driver. [logic 0 level: 0.0 to 0.6V, logic 1 level: 2.4 to 5.5V].

The VMIVME-4122 External Trigger pin has an onboard 10kΩ pull-up resistor to 5V, to support use with open collector drivers. Note that the use of very high speed logic is not desirable, but the resulting line reflections will likely be ignored. Undershoot should be limited to less than -1.0V. Pulse widths (either high or low) should not be less than 300 nanoseconds wide for reliable edge detection, although substantially shorter pulses may result in a trigger event. Pulses less than 50 nanoseconds wide will be ignored.

In order to coordinate the activity of the software that loads new data into the DAC input registers with the occurrence of the trigger event a means of recording it is provided. The same Trigger Register that served as the means of initiating a trigger event in internal mode (see text above) is now used to monitor the status of an external trigger event. When either external + or external- trigger mode is selected, a write to the Trigger Register does not cause a trigger event. It does set its two bit status field to 00. A transition on the External Trigger pin such as a rising edge with external + or falling edge with the external - mode will cause a trigger event. This will also cause the status field to change to 01. Software may detect this via polling, and upon finding this value, may clear it back to 00 and begin loading new data into the DAC input registers (with confidence that the previous contents has now been transferred to the output registers).

After all new data has been written to the input registers another read of the Trigger Register is expected to return 00. If it does not, the software has missed its time constraint (it did not complete reloading of all DAC registers prior to arrival of the external trigger edge). If the VMIVME-4122 returns a value of 11 in the Trigger Register then more than one time constraint was missed. Note that this mode of trigger operation is useful for more than one VMIVME-4122 board in a backplane, as long as their External Trigger pins are tied together and driven from a common source, and set for the same external trigger edge. Any one Trigger Register will serve to allow control of all boards. See Figure 3-1 on page 47 for a simple flow chart of this method.

Figure 3-1 Flow Chart of the External Synchronization Control



- **SYNC Trigger Mode (External Mode with software controlled drive)** — The normal use of the External Trigger Pin is as an input, but the CSR SYNC bit (default 0 at board reset time) may be used to drive it as an output/input under software control. Setting the SYNC bit to a "1" turns on an open drain transistor to force the External Trigger pin to a logic low state. This is used in conjunction with one of the two external trigger modes for both self-test and synchronizing up to three VMIVME-4122 boards under software control. Note that any external driver must be set to Hi-Z state, must be of open collector type or must be disconnected to use this mode.

Bit 7 to Bit 1 Reserved — Not Used

Bit 0 ADC Busy — This bit determines the status of the ADC (see Figure 3-6 below).

Table 3-6 Board ADC Busy Bit Map

Bit Position	Bit Name	Indication
0	ADC Busy	1 = ADC Busy 0 = ADC conversion completed

Word 4: Data Access Pointer Register.

Table 3-7 Word 4: Data Access Pointer Register Bit Map

Data Access Pointer (Byte 4) Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Data Access Pointer (Byte 5) Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved					CH ADDR 2	CH ADDR 1	CH ADDR 0

Word 4: Data Access Pointer Bit Definitions

Bit 15 to Bit 8 Reserved — Not Used

Bit 7 to Bit 3 Reserved — Not Used

Bit 2 to Bit 0 Channel Address [2:0] — Bits 0 thru 2 will determine the ADC channel address (see Table 3-8 below).

Table 3-8 ADC Channel Address Bit map

Bit Position	Bit Name	Indication
2	CH ADDR 2	Channel Address Pointer bit 2
1	CH ADDR 1	Channel Address Pointer bit 1
0	CH ADDR 0	Channel Address Pointer bit 0

Word 6: ADC Access Word Register

ADC channels are read / convert (a write initiates conversion). This read / write register can only be accessed as a word (see Table 3-9 below for bit map). The procedure for using the ADC subsystem is as follows.

1. Write the desired channel number into the Data Access Pointer register. Channel numbers may range from 0 to 7.
2. Write any data value to the ADC Access Word. The data written will be ignored, but the analog to digital conversion process will begin. Access must be a WORD write only.
3. Test the ADC Busy Flag (bit 0) of the ADC Status register for a zero. Keep reading this register until it reads 0. A byte access is recommended.
4. Read the newly converted data from the ADC Access Word. (As a WORD ONLY)..

Table 3-9 Word 6: ADC Access Word Bit Map

ADC Access Word Read/Write, Word Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
MSD							

ADC Access Word Read/Write, Word Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
LSD							

DAC Registers

The 8-DAC registers are 16-bit registers that are accessed as a word. Each DAC register corresponds to a channel which is read / write. The Digital-To-Analog Converters used in the VMIVME-4122 contain two registers associated with each of the 8-analog channel outputs. They are the "input / output registers". These 12-bit wide registers are arranged such that all data read or write operations access the input register only. The input register's outputs drive the output register's inputs. This write only output register's outputs drive the DAC conversion circuits directly and its contents is translated immediately into the analog output signal. This double buffered arrangement supports simultaneous update of all DAC outputs by means of a signal that clocks data from all input registers to all output registers. See Figure 3-2 on page 50.

Figure 3-2 DAC Register for One Channel

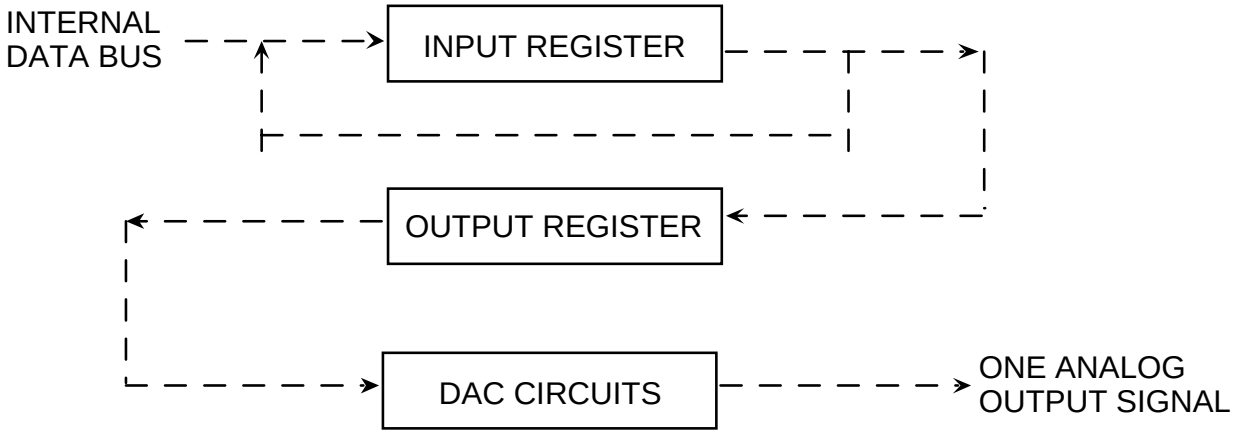


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Table 3-10 DAC Registers Bit Map

Bit Position	Bit Name	Access	Indication
0-15	Word 8	Read / Write	DAC CH 0 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word A	Read / Write	DAC CH 1 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word C	Read / Write	DAC CH 2 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word E	Read / Write	DAC CH 3 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word 10	Read / Write	DAC CH 4 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word 12	Read / Write	DAC CH 5 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word 14	Read / Write	DAC CH 6 Data Word

Bit Position	Bit Name	Access	Indication
0-15	Word 16	Read / Write	DAC CH 7 Data Word

NOTE: The DAC Registers are word access *only.*

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.