VMIVME-4512
16-Channels 12-Bit Analog I/O Board

Product Manual

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500-004512-000 Rev. U

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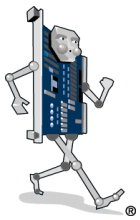

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Overview

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Introduction

The VMIVME-4512 16-Channel 12-Bit Analog Input / Output (AIO) Board provides both the stimulus and the response functions encountered in VME closed-loop analog systems. Self contained, with a resident 12-bit Analog-to-Digital Converter (ADC) and a Digital-to-Analog Converter (DAC), the VMIVME-4512 represents a single board solution to the analog input / output requirements of such VME applications as process control, simulators, trainers and supervisory control.

Analog inputs can be configured either as 16 differential channels or as 16 single-ended channels, and are available with low pass filters for noise elimination and anti-aliasing. A resident smart controller permits “pipelined” ADC operation, and automatically inserts all necessary settling delays. This feature reduces program control of the ADC to a simple handshake sequence.

The 16 analog outputs can supply 10 milliampere of drive current over the full output range of ±10 V, and can be operated off-line for self-test. Built-in-Test (BIT) features permit off-line verification of all active components by routing the analog outputs through the analog input multiplexers.

Features

The VMIVME-4512 does not rely upon additional supporting analog boards for Analog-to-Digital (AD) or Digital-to-Analog (DA) conversion, which simplifies the task of designing a VME system which requires both analog inputs and outputs. A brief overview of principal features illustrates the flexibility and the performance that is available with the VMIVME-4512 board:

- 16 differential or single-ended analog input channels
- 16 analog output channels with 10-milliamperes drive capability
- Resident 12-bit ADCs and DACs
- Input and output ranges are jumper-selectable as 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, ±10 V
- Optional low pass filters available for analog input noise elimination and anti-aliasing
- Program-controlled off-line operation of analog outputs
- AD data coding program-selectable as either binary, offset binary or two's complement format
- Total acquisition and conversion time is 25 µs resulting in 40 kHz maximum throughput in non-pipelined mode
- On-board smart controller permits interleaved (pipelined) operation for maximum AD conversion throughput
- All inputs and outputs protected against line transients and short circuits
- Front-panel Fail LED indicator
- Double Eurocard form factor
- Individually coded / keyed VME connectors

Functional Description

The VMIVME-4512 (Figure 1 on page 16) is a self-contained, 16-channel, 12-bit VME AIO Board. Analog inputs are user-selectable either as single-ended pseudo-differential channels, or as differential-pair channels. Each of the 16 analog outputs will supply up to 10 milliamperes of drive current, and can be operated off-line for both loopback self-testing and for single-point analog input/output applications. Built-in-test of all active components is provided by loopback testing of the analog input multiplexers with either on-line or off-line analog outputs.

Interleaved (pipelined) AD conversion capability is provided as a standard feature, and in high throughput applications, permits the acquisition settling time of each channel to begin while the conversion (digitizing) of the preceding channel is still in progress. This analog “pipelining” provides the highest possible throughput, or sample rate, without degrading accuracy.

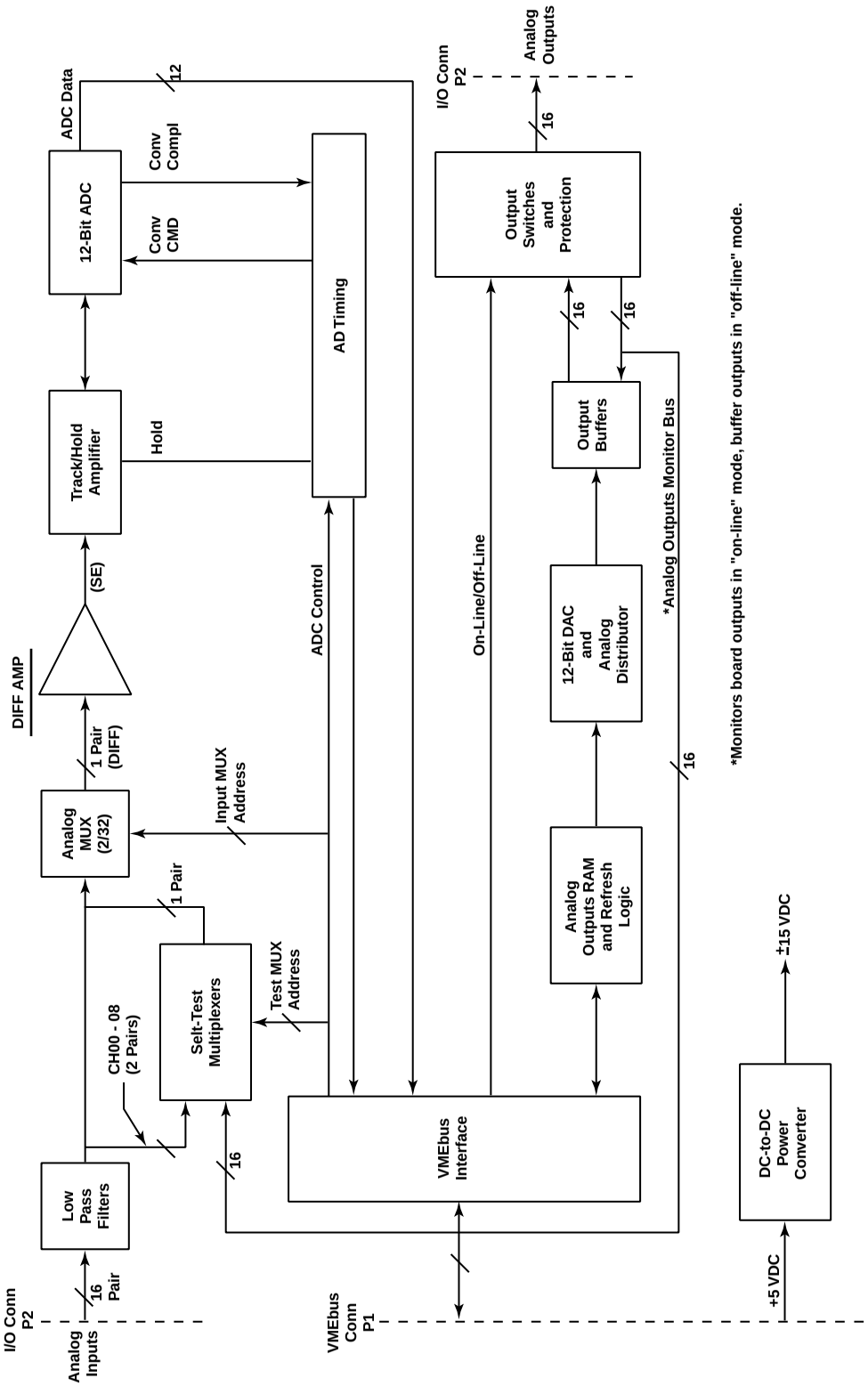

Figure 1 VMIVME-4512 Functional Block Diagram

Reference Material List

For a detailed explanation of the VMEbus and its characteristics, refer to “The VMEbus Specification” available from:

VMEbus Specification Rev. C1
and *The VMEbus Handbook*
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Refer to VMIC Specification No. ***800-004512-000*** for a detailed explanation of the physical description and specifications of the 16-Channel 12-Bit Analog I/O Board.

The following application and configuration guides are available from VMIC to assist in the selection, specification and implementation of systems based upon VMIC's products:

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem	825-000000-004
Analog I/O product (with Built-in-Test)	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

CHAPTER
1

Theory of Operation

Contents

Introduction

The VMIVME-4512 is a 16-channel, 12-bit Analog Input/Output (AIO) Board designed to operate on the standard VMEbus. The board is self-contained with a resident 12-bit Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) with loopback self-test features. The VMIVME-4512 does not require additional boards to provide high quality analog input and output functions. The VMIVME-4512 is a flexible system I/O element which offers Built-In-Test and off-line operational features not found in many other products.

Internal Functional Organization

The board is divided into the following functional categories, as illustrated in Figure 1 on page 16. All VMIVME-4512 functions are discussed in detail in this section. Below is a diagram of the VMEbus control signals and interface logic (Figure 1-1).

- VMEbus Interface
- Analog-to-Digital Converter (ADC)
- Analog Input Filters and Multiplexer
- DAC and Analog Distributor
- Analog Output Buffers and Switches
- Analog Outputs Refresh Logic
- Self-Test Multiplexers
- Power Converter

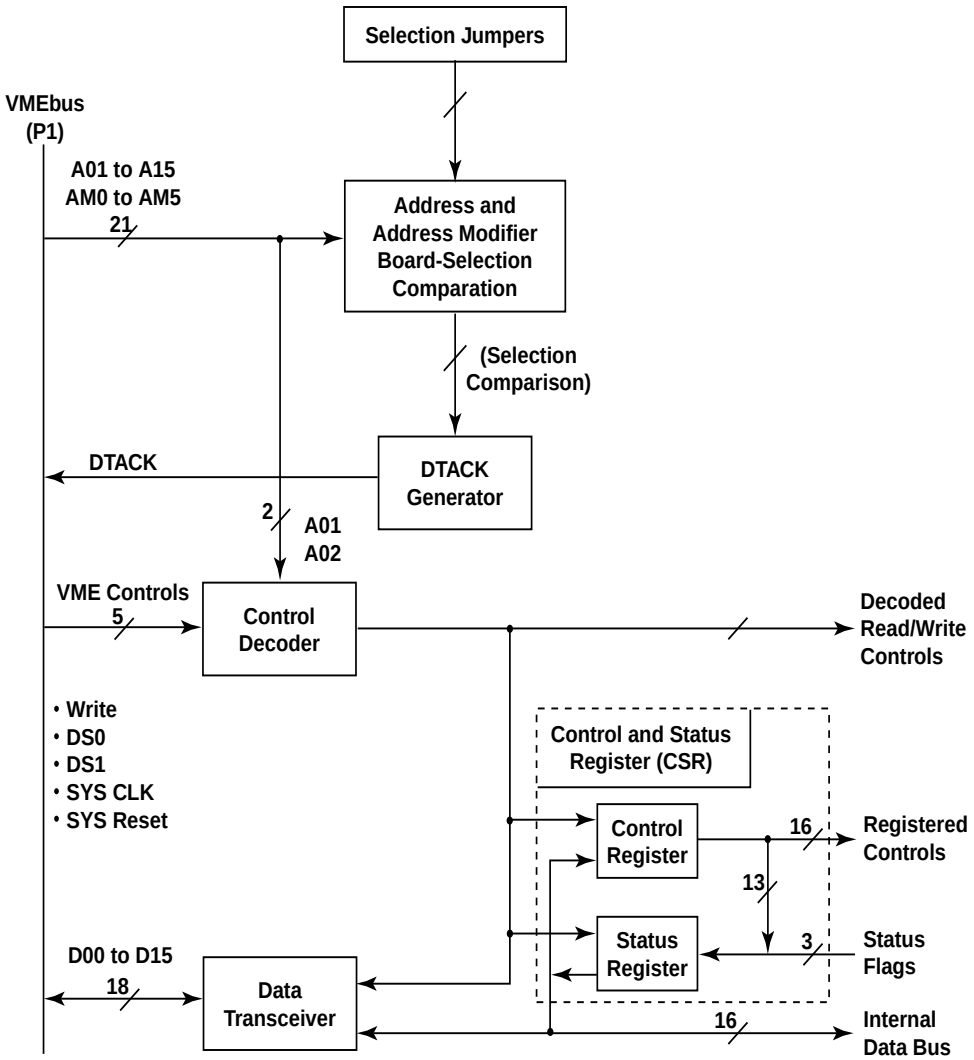


Figure 1-1 VMEbus Control Signals and Interface Logic

VMEbus Control Interface

The VMIVME-4512 communications registers are memory mapped as 32 (decimal) 16-bit words. The registers are contiguous, and may be user-located on any 64-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or non-privileged bus communications.

During each *read* or *write* operation, all VMEbus control signals are ignored unless the board-selection comparator detects a match between the on-board selection jumpers shown in Figure 1-1 on page 20 and the address and address-modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted (driven LOW). Subsequent removal of the Central Processing Unit (CPU) *read* or *write* command causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, the following three groups of VMEbus signals control communications with the board:

- Data Bus lines D00 to D15
- Address lines A01, A02, A03, A04, A05
- Bus Control Signals:
    1. WRITE
    2. DS0,* DS1*
    3. SYS CLK
    4. SYS RESET*

Data Bus lines are bidirectional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A05 map the 32 communication registers onto a 64-byte range within the VMEbus address space (see Chapter 3 "Programming" on page 45). The control signals determine whether data is to be moved to the board (*write*) or from the board (*read*), provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET* input resets all timers and flags.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board. Status flags, necessary for monitoring and controlling the analog input multiplexer and the ADC, are read through the Status Register. The Control and Status Registers are referred to collectively as the Control and Status Register (CSR), since they are at the same address. The *WRITE* signal determines which one is accessed. Most of the control register outputs can be monitored directly through the status register.

Each of the 16 analog output channels is controlled by writing 12-bit right-justified data into a dedicated 16-bit *read/write* register. The 16 analog output control registers constitute the VMEbus port of a 16-word dual port memory. The other memory port is controlled by the analog output refresh logic.

ADC Control and Timing

Control commands and status flags associated with controlling the ADC are illustrated in Figure 1-2 below, and described in the following paragraphs and Chapter 3 *"Programming"*.

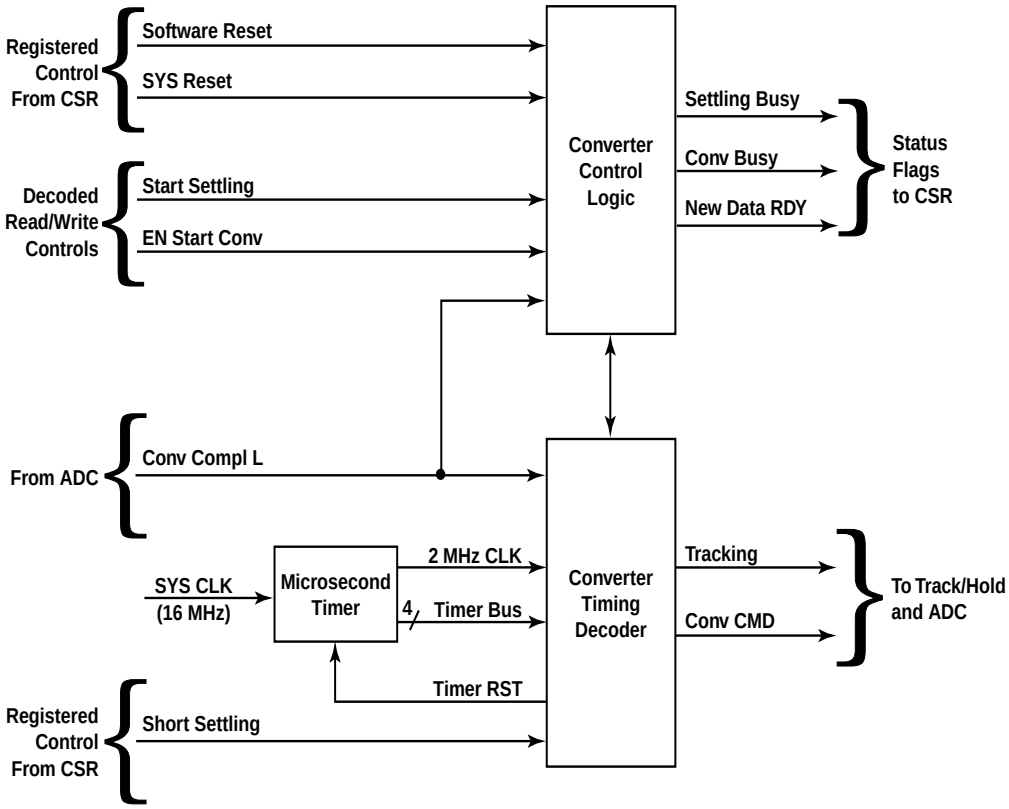


Figure 1-2 ADC Timing Logic and Control Signals

Converter Controls and Status Flags

A conversion sequence is initiated by writing a one (1) to the START SETTLING and EN START CONV controls bits, and is composed of the following consecutive time intervals:

- Settling Delay
- Tracking Interval
- Analog-to-Digital (AD) Conversion

All ADC timing intervals discussed in this section are performed automatically by the on-board smart controller. Program control of the converter consists of basic handshake sequences.

The settling delay occurs directly after a state change has occurred in the analog networks (such as selecting a new input channel), and represents the settling time of the networks. After the settling delay has been completed, the Track-and-Hold (T&H) amplifier (Figure 1 on page 16) enters the tracking mode, and the tracking interval begins.

During the tracking interval, the output of the T&H amplifier settles to a value which is equal to its input voltage. The SETTLING BUSY flag is set HIGH at the beginning of the settling delay, and is cleared LOW at the end of the tracking interval. The CONV BUSY flag is set HIGH by the EN START CONV control bit, and remains HIGH until the conversion sequence has been completed.

At the end of the tracking interval, the T&H amplifier enters the HOLD MODE, in which the output of the amplifier is held at a constant level, and a CONV CMD from the timing decoder causes the AD conversion to begin. The AD conversion digitizes the output of the T&H amplifier into a 12-bit data word, and then terminates the conversion sequence. The CONV COMPL L flag from the ADC is HIGH during the conversion, and is LOW otherwise.

Completion of the AD conversion causes the NEW DATA RDY flag to be set HIGH, indicating that valid data is present in the Converter Data Register (CDR). The action of reading the CDR resets the NEW DATA RDY and CONV BUSY flags to the LOW state a zero (0). ADC output coding can be program-selected as either binary or two's complement. A read of the CDR is non-destructive.

The microsecond timer uses the 16 MHz system clock to generate the TRACKING and CONV CMD control signals for the converter, and also provides the settling delay. Setting the SHORT SETTLING control bit HIGH provides increased throughput by reducing both the settling delay and the tracking interval.

Throughput (Sample Rate) Factors

Total system throughput (sample rate) F_T can be expressed generally as: $F_T = 1/[N \times (+1 +T2 +T3 +T4)]$, where:

F_T = Throughput (samples per second, per channel)

N = Number of channels

T1 = 4512 settling delay

T2 = 4512 tracking interval

T3 = 4512 A / D conversion time

T4 = CPU (controlling processor) time invested per channel

In a typical situation, for example, in which the CPU overhead (T4) is 2 microseconds, the expression for maximum throughput (N = 1) is:

T1 = 8 µs (default), 6 µs (SHORT SETTLING)

T2 = 2 µs (default), 1.5 µs (SHORT SETTLING)

T3 = 15 µs

T4 = 2 µs

$$F_T(\text{max}) = \frac{1}{27\ \mu s} = 37\ \text{kHz}$$

Maximum throughput then, is 37 kHz (37,000 samples per second) for a single input channel. Setting the SHORT SETTLING control bit HIGH increases the throughput to 41 kHz.

Interleaved (Pipelined) Operation

By allowing a new channel to settle before conversion of the previously selected channel has been completed, T1 will be eliminated for F_T (maximum). The VMIVME-4512 control logic permits this to take place if the board is operated in the interleaved (pipelined) mode. Operating requirements for the interleaved mode are discussed in Chapter 3 *"Programming"*. By eliminating T1 and ignoring CPU overhead, maximum throughput in this mode is:

F_T (maximum) = 58 kHz (default), 60 kHz (SHORT SETTLING)

Analog Inputs

Sixteen differential or single-ended analog input channels are available at the rear panel through the P2 connector. By connecting the analog return in the remote device to the INPUT GROUND SENSE input on the P2 connector as shown in Figure 1-3 below, the single-ended lines can be operated as pseudo-differential inputs. It is recommended that the differential mode be used for increased noise and common mode rejection.

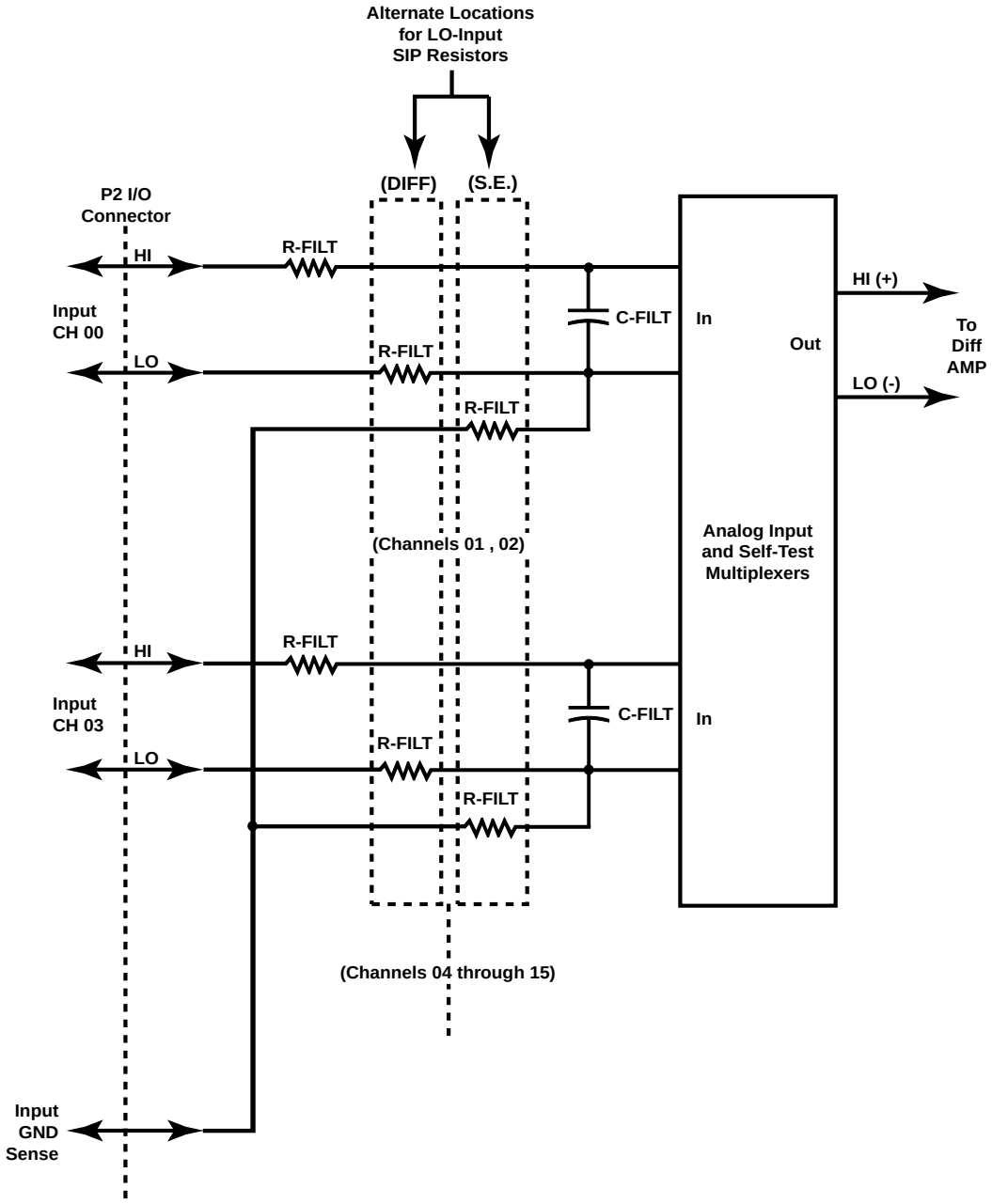


Figure 1-3 Single-Ended and Differential Input Configurations

Low Pass Filters and Input Multiplexer

The 16 analog input channels can be provided with individual, single-pole, low pass filters as shown in Figure 1-4 below. Input channels can be user-configured to operate either single-ended or differentially. See document number 800-004512-000 for input filter specifications.

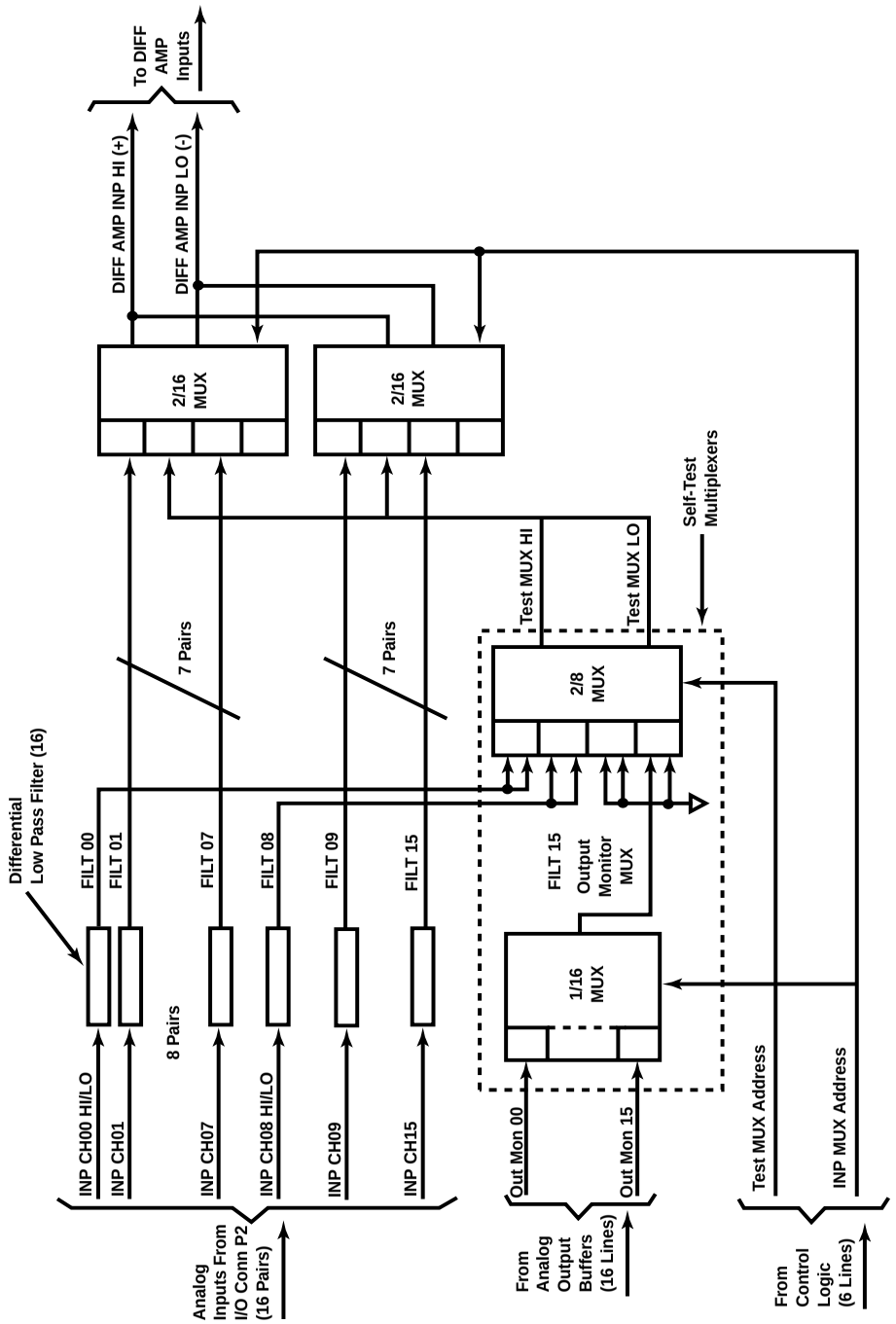


Figure 1-4 Analog Inputs and Signal Routing

To achieve maximum system accuracy with filtered analog inputs, the sample rate should be limited to 1,000 Hz or less per channel (16 kHz for 16 channels). Higher sample rates will produce reflected “pumpback” currents at the inputs which can induce error voltages across the filter input resistors.

Each of the 16 analog inputs is selectable through one of two multiplexer sections. Each multiplexer accepts eight differential input pairs, one of which is first routed through a self-test multiplexer.

Both multiplexer sections are controlled by the same set of four address lines (INP MUX ADDRESS), which are derived from control bits “MUX A00” through “MUX A03” from the Control Register. The INP MUX ADDRESS A03 is inverted for the CH00 to CH07 multiplexer to permit both multiplexers to operate on a common differential node.

Single-Ended Operation

Differential or single-ended operation of the analog inputs is selected by the location of Single-In-Line-Package (SIP) resistors, as illustrated in Figure 1-3 on page 25. The input multiplexers are ***always*** operated in the differential mode; single-ended (pseudo-differential) operation is obtained by connecting the LOW input resistor to the common INPUT GROUND SENSE input instead of to the individual LOW signal inputs.

All VMIVME-4512 input channels are over voltage protected by current-limiting input resistors. See document number 800-004512-000 for input over voltage specifications.

Analog Outputs

In addition to the analog inputs, 16 analog outputs are available at the P2 connector. The analog outputs are updated (refreshed) periodically from dual port memory by the REFRESH control logic, as illustrated in Figure 1-5 below. Each output receives an update once every 1.7 milliseconds in the default refresh mode. A program-controlled FAST REFRESH control bit can be used to reduce the refresh cycle time to approximately 0.4 milliseconds, thereby raising the maximum output sampling rate from 588 Hz to 2.5 kHz.

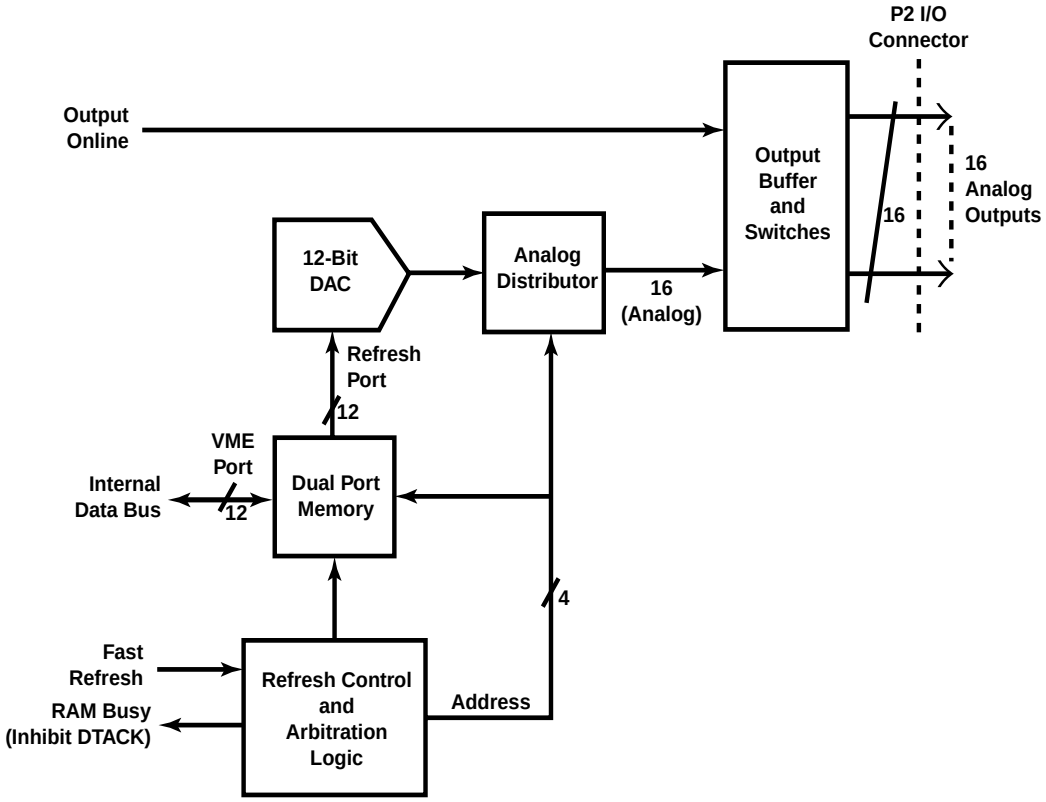


Figure 1-5 Analog Output Channels

Digital-to-Analog Converter (DAC)

All 16 analog outputs are serviced by a single 12-bit DAC. The DAC is controlled by the REFRESH control logic, which periodically transfers data from the dual-port memory's REFRESH port to the DAC, and simultaneously connects the DAC to the appropriate section of the analog distributor. Analog output data in the dual port memory is placed there through the VME port by the controlling processor.

Analog Distributor

The analog distributor consists of the following elements:

- One of 16 decoder
- Low charge injection analog de-multiplexer
- Sixteen capacitive storage elements

As the DAC is updated with data for each channel in the output REFRESH sequence, the one of 16 decoder receives the same four address lines that are used to select the dual port memory data location. In this manner, the converted analog level is always routed to the distributor section which corresponds to the dual port memory location for the same channel. After allowing the DAC to settle, the REFRESH logic enables (turns on) the demultiplexer, and the converted voltage level is transferred to the corresponding storage capacitor. A settling interval of approximately 100 µs is provided by the REFRESH logic, after which the demultiplexer is disabled and the next channel in the REFRESH sequence is accessed.

Output Buffers and Switches

Voltage levels stored by the analog distributor are buffered and then switched to the P2 connector for routing through system I/O cables. The output buffers are low leakage, precision operational amplifiers which can supply 10 milliamperes of drive current over the full available output voltage range of ±10 V, and which can withstand sustained short circuits to ground without damage.

Output switches permit the analog outputs to be disconnected from P2 for “off-line” self-testing and for low impedance, single-point analog input/output system applications. To eliminate the effect of switch resistance on output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operations. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ±15 V supply rails. All outputs are monitored through a self-test multiplexer. By deriving the output monitor multiplexer inputs from the sense inputs of the output buffers, the measured output signals are correct in both the on-line and off-line operational modes.

Data RAM and Refresh Control

The dual port memory which services the analog outputs is organized as a 16-bit wide, 16-location array, in which each location can be accessed from either of two ports. The random access VME port is used by the VME host to load the analog output digital codes into memory. The digital codes are then transferred sequentially through the DAC port to the DAC, where they are converted into voltage levels and subsequently distributed to the appropriate analog output channels. The REFRESH logic control sequence is shown in flow diagram form in Figure 1-6 on page 30.

Operation of the dual port memory is controlled by the REFRESH control logic which derives its timing from the 16 MHz system clock. The REFRESH control logic supervises all data transfers between the memory and the DAC, and controls the distribution of analog voltage levels to the analog outputs. Because the dual port memory must be accessed through both the VME and DAC ports, arbitration logic is employed during the transfer of data to the DAC to ensure that only one port is active at any time.

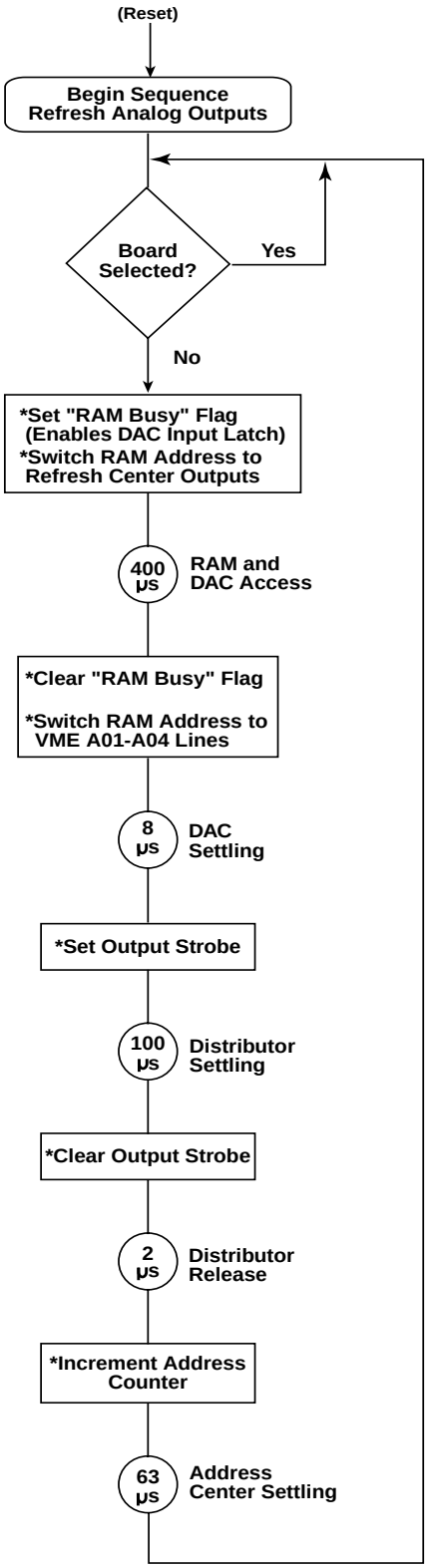


Figure 1-6 Analog Outputs Refresh Logic; Flow Diagram

Built-In-Test (BIT)

Self-test provisions in the VMIVME-4512 design permit program-controlled verification of all active components on the board.

Self-Test Multiplexers

The signal routing paths and multiplexers involved in board level self-test are shown in Figure 1-4 on page 26. The 16 analog outputs are switched by the output monitor multiplexer onto a single line which is, in turn, connected by the self-test multiplexer to the low channel input of either analog input multiplexer. This arrangement permits any one of the analog outputs to be sampled by the ADC. It also verifies the operation of the analog input multiplexers by exercising them with known signal levels.

In addition to accepting the selected analog output signal, the self-test multiplexer permits the HIGH and LOW inputs of the differential amplifier to be switched simultaneously to signal return. This feature provides a precision “zero” signal for software-correcting common “zero” offsets in the analog input channels.

Because the low channel inputs of the two input multiplexers are shared by both the analog inputs and the output-monitor signal, the analog inputs corresponding to input channels 00 and 08 are routed through the self-test multiplexer.

Loopback Testing of Inputs and Outputs

By routing the analog outputs through the analog input multiplexers (see previous section), all active components are exercised in a “loopback” arrangement. The controlling processor can perform a loopback test in either the on-line or off-line mode by sending a voltage-level code to a specific output channel and then verifying that the ADC produces the same code after sampling the signal. This technique is described in detail in Chapter 3 “*Programming*”.

Built-In Power Converter

Electrical power for the VMIVME-4512 analog network is supplied by the DC-to-DC converter shown in Figure 1-7 below. The converter transforms 5 V logic power into regulated and isolated ±15 VDC power, with a load capacity of approximately 300 milliamperes on each 15 V bus.

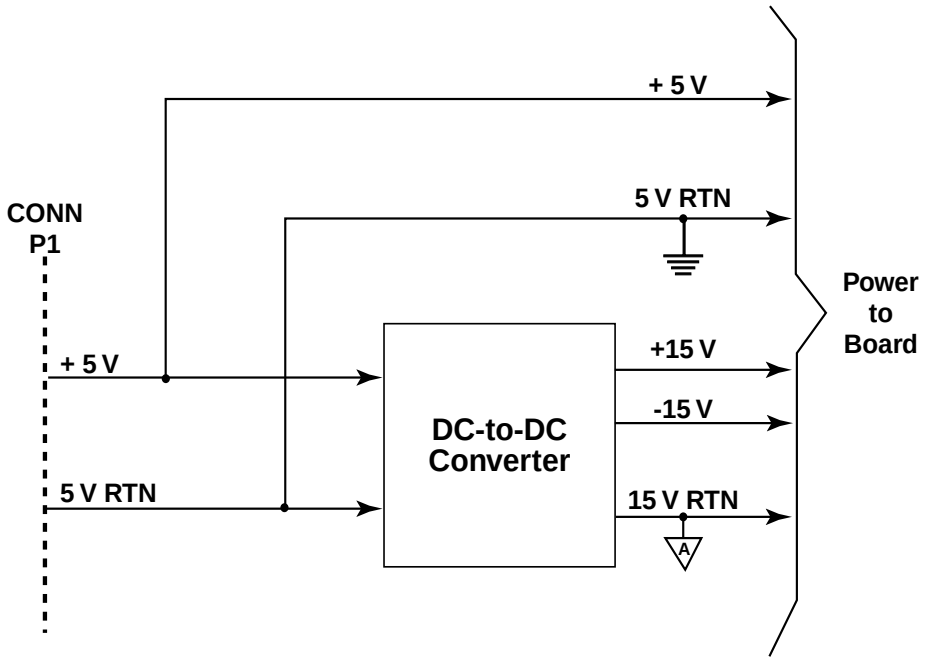


Figure 1-7 Power Converter

CHAPTER
2

Configuration and Installation

Contents

Introduction

This chapter leads you through the configuration and installation of the VMIVME-4512 16-Channel 12-Bit Analog I/O Board.

Unpacking Procedures

CAUTION: Some of the components assembled on VMIC products can be sensitive to electrostatic discharge and damage can occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that may have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Disconnect power from the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. The VMIVME-4512 can be installed in any slot position, with the exception of slot one which is reserved for the system controller.

WARNING: Do not install or remove the board while power is applied.

Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Have the sections pertaining to theory and programming, Sections 1 and 3, been reviewed and applied to system requirements?
2. Review "Factory-Installed Jumpers" on page 36 and Table 2-1 on page 36 to verify that all factory-installed jumpers are in place. To change the board address or address modifier response, refer to "Board Address and Address Modifier Selection" on page 38.
3. Have the I/O cables, with the proper mating connectors, been connected to the input/output connector P2? Refer to "Connector Descriptions" on page 43 for a description of the P2 connector.
4. Calibration has been performed at the factory. If re-calibration should be required, refer to "Calibration" on page 40.

WARNING: Do not install or remove this board with power applied to the system, unless the board is equipped with the power-on option (Extended Ground Pins).

Operational Configuration

Control of the VMIVME-4512 Board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all VMIVME-4512 jumpers are shown in Figure 2-1 on page 37 and Table 2-1 below.

Factory-Installed Jumpers

Each VMIVME-4512 Board is configured at the factory with the specific jumper arrangement shown in Table 2-1 below. The factory configuration establishes the following functional baseline for the VMIVME-4512 Board, and ensures that all essential jumpers are installed.

- Board short address is set at 0000 HEX
- I/O access mode is short non-privileged
- Analog input and output ranges are set to ±10 V full scale range

Table 2-1 Programmable Jumpers Configuration

Jumper ID	Function (Installed)	Factory Conf
JK	Board Address Bit A06 = 0	Installed
JI	Board Address Bit A07 = 0	Installed
JG - 0	Board Address Bit A08 = 0	Installed
JG - 1	Board Address Bit A09 = 0	Installed
JG - 2	Board Address Bit A10 = 0	Installed
JG - 3	Board Address Bit A11 = 0	Installed
JG - 4	Board Address Bit A12 = 0	Installed
JG - 5	Board Address Bit A13 = 0	Installed
JG - 6	Board Address Bit A14 = 0	Installed
JG - 7	Board Address Bit A15 = 0	Installed
JH	Short Supervisory Access	Omitted
JA, B	Inputs, 5 V Full Scale Range	Omitted**
JC - 1, 2	Inputs, 20 V Full Scale Range	Installed**
JC - 2, 3	Inputs, 10 V or 5 V Full Scale Range	Omitted**
JM - 1, 2	Inputs, Bipolar Operation	Installed**
JM - 2, 3	Inputs, Unipolar Operation	Omitted**
JD - 1, 2	Outputs, Unipolar Operation	Omitted**
JD - 2, 3	Outputs, Bipolar Operation	Installed**
JE - 1, 2*	Outputs, 10 V Full Scale Range	Omitted**
JE - 2, 3*	Outputs, 5 V Full Scale Range	Omitted**
JL - 1, 2	Outputs Ground to P2 Connector Pin C16	Installed
JL - 2, 3	Single-Ended Input Ground Sense to P2 Connector Pin C16	Omitted

NOTES: * The JE jumper is omitted for the 20 V FSR.
** Factory configuration of these jumpers is for ±10 V FSR.

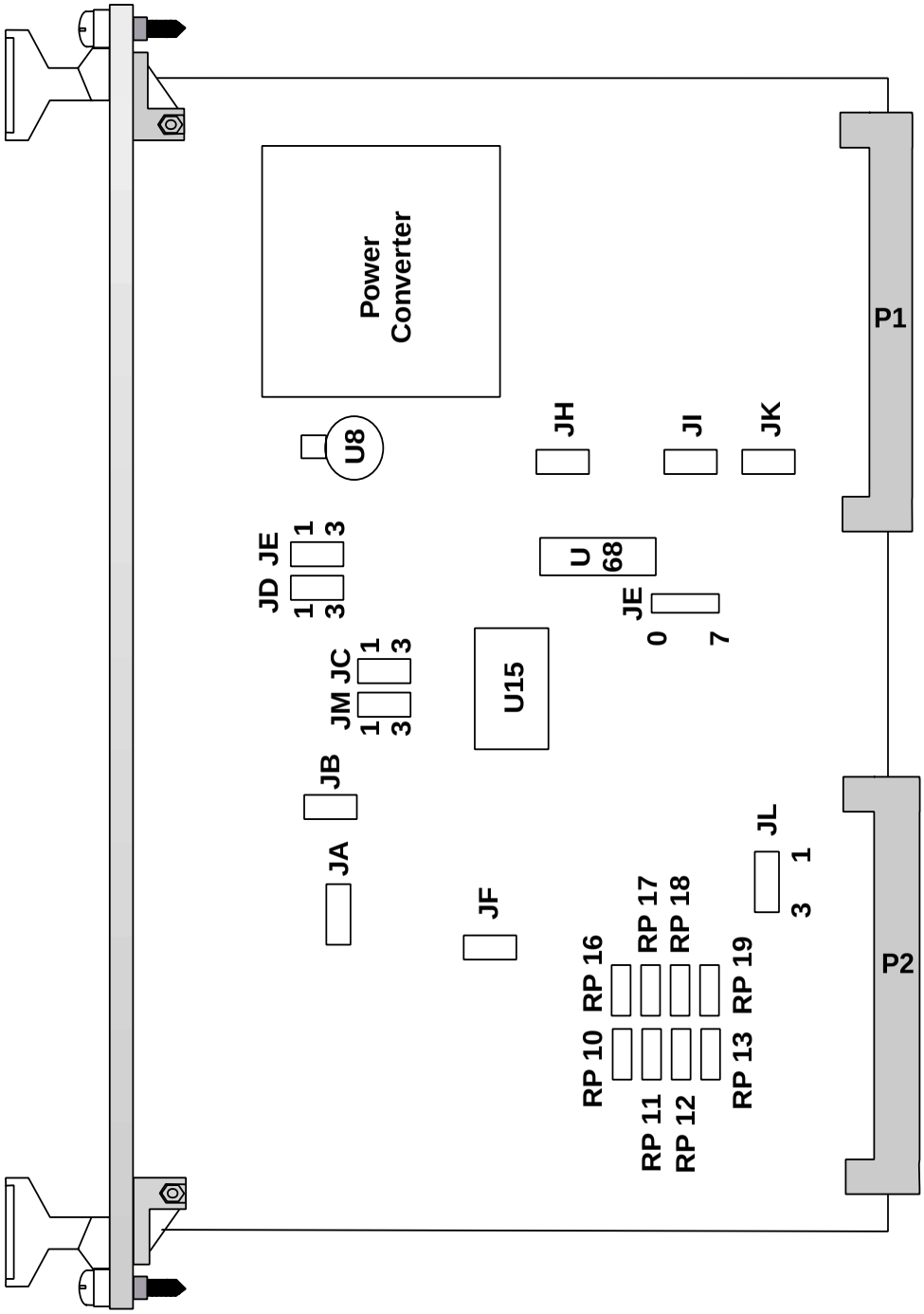


Figure 2-1 Programmable Jumper and Resistor Network Locations

Board Address and Address Modifier Selection

Jumper header JG, and jumpers JI and JK permit the VMIVME-4512 Board to be located on any 64-byte boundary within the short I/O address space. The short I/O address space consists of all addresses between NNNN0000 HEX* and NNNNFFFF HEX, and requires that 15 (word) address lines be decoded in order to account for all locations. Since five lines are used for decoding on-board functions, the VMIVME-4512 Board address is defined by ten lines; address bits A06 through A15.

NOTE: *The value NNNN depends on the make and model of CPU board used.

The board address is programmed by installing shorting plugs at all zero (0) or LOW address bit jumper positions, and by omitting the shorting plugs at the one (1) or HIGH positions. Address bit A06 has a weight of 64 byte-locations. As an example, the typical jumper arrangement shown in Table 2-2 below would produce a board address of NNNN8840 HEX.

I/O access mode is programmed by selecting address modifier AM2 using jumper JH. Short supervisory access is selected by omitting the jumper. Short nonprivileged access is selected by installing the jumper.

Table 2-2 Typical Board Address (NNNN8840 Hex) Selection

Jumper	Address Bit	State*
JK	A06	Open
JI	A07	Shorted
JG - 0	A08	Shorted
JG - 1	A09	Shorted
JG - 2	A10	Shorted
JG - 3	A11	Open
JG - 4	A12	Shorted
JG - 5	A13	Shorted
JG - 6	A14	Shorted
JG - 7	A15	Open

NOTE: *Shorted = zero (jumper installed).
Open = one (jumper omitted).

Analog Input Modes

Differential or Single-Ended Operation

The VMIVME-4512 Board is shipped with the analog inputs configured for differential operation. To select single-ended operation, move the resistor networks located at RP13, 11, 17 and 19 to locations RP10, 12, 16 and 18.

In the single-ended mode, the external ground sense input can be used to compensate for the potential differences between equipment signal returns. If jumper JL is in the 1, 2 position, the ground sense pin C16 of the input/output connector P2 is grounded on the VMIVME-4512 Board. If jumper JL is in the 2, 3 position, P2-C16 becomes the external ground sense input.

Input Voltage Range

Input voltage range is controlled by jumpers JA, JB and JC. The maximum full scale range is 20 V. To modify the full scale range to the 10 or 5 V range, configure the jumpers as indicated in Table 2-1 on page 36.

Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog inputs is selected with jumper JM, as indicated in Table 2-1 on page 36.

NOTE: The value NNNN depends on the make and model of CPU board used.

Analog Output Mode

Output Voltage Range

Output voltage range is controlled by jumper block JE. The maximum full scale range is 20 V. To modify the full scale range to 10 V or 5 V, configure jumper block JE as indicated in Table 2-1 on page 36. The 20 V full scale range is selected by omitting the JE jumper entirely.

Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog outputs is selected with jumper block JD, as indicated in Table 2-1 on page 36.

Calibration

Before delivery from the factory, the VMIVME-4512 Board is fully calibrated and conforms to all specifications listed (See “Reference Material List” on page 17). Should re-calibration be required, perform the “"Analog Inputs Calibration Procedure"” below or the “Analog Outputs Calibration Procedure” on page 41 with the equipment listed in "Equipment Required" below. The locations of all adjustments and test points are shown in Figure 2-2 on page 42.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for re-calibration, however. All adjustments should be re-sealed with a suitable fast-cure sealing compound after re-calibration has been completed.

CAUTION: Do not install or remove this board with power applied to the system unless the board is equipped with the extended ground pins option.

Equipment Required

- **Digital Voltmeter (DVM)**: ±1.0000 VDC and ±10.000 VDC ranges; 5 or more digits; ±0.005 percent of reading voltage measurement accuracy; 10 MΩ minimum input impedance.
- **Digital Voltage Source:** ±10.000 VDC Range; resolution 0.0005 VDC; Accuracy, ±0.005 percent of expected value; 0.10 Ω maximum output impedance.
- **Cardcage:** VMEbus backplane or equivalent, J1 and J2 connectors, VMEbus master controller, +5 V, ±0.1 VDC, power supply. One slot allocated for testing the VMIVME-4512 Board.
- **Extender card:** VMEbus extender card.
- **Test cables:** Test cables for the equipment listed above.

Analog Inputs Calibration Procedure

1. Install the VMIVME-4512 Board on an extender board in a VMEbus backplane.
2. Configure the analog inputs and outputs for 20 Volts full scale range and bipolar operation.
3. Apply power to the backplane. Allow a minimum warm-up interval of ten minutes after power has been applied before proceeding.
4. Connect the digital voltage source between connector pins P2-A17 (+) and P2-C17 (-).
5. Write the 16-bit value 7840 (HEX) to the Control Status Register (CSR) at board relative address 0002.
6. Adjust the digital voltage source for an output of 0.0000 VDC.
7. While reading the ADC (16-bit word at board relative address 0004), adjust R27 (BIPOLAR OFFSET) for an ADC indication of 0800 (HEX).
8. Adjust the digital voltage source for an output of +9.9975 VDC.

9. While reading the ADC, adjust R26 (GAIN ADJ) for an ADC indication that alternates between 0FFE and 0FFF (HEX).
10. Repeat steps 6, 7, 8 and 9, until no further adjustments are required.
11. Move the JC-A, B, C jumper to the JC-B, C position.
12. Adjust the digital voltage source for an output of +5.0000 VDC.
13. While reading the ADC, adjust R25 (UNIPOLAR ZERO ADJUST) for an ADC indication of 0800 (HEX).
14. Calibration of the analog inputs is completed. Remove all test connections, and restore the board to its original configuration.

Analog Outputs Calibration Procedure

1. Perform steps 1, 2 and 3 of the analog Inputs Calibration Procedure. (It is not necessary to perform this step if the Analog Inputs Calibration Procedure was performed within one hour of beginning this procedure).
2. Connect the digital voltmeter to connector pins P2-A1 (+) and P2-C1 (-).
3. Move the JD jumper to the JD-1, 2 position. Remove the JE jumper.
4. Write the 16-bit value 7840 (HEX) to the CSR at board relative address 0002.
5. Write the 16-bit value 0000 (HEX) to the analog output channel 00 register at board relative address 0020 (HEX).
6. Adjust R15 for a digital voltmeter indication of 0.0000 ±0.0010 VDC.
7. Move the JD jumper to the JD-2 or 3 position.
8. Write the 16-bit value 0800 (HEX) to the analog output channel 00 register at board relative address 0020 (HEX).
9. Adjust R9 for a digital voltmeter indication of 0.0000 ±0.0010 VDC.
10. Write the 16-bit value 0FFF (HEX) to the analog output channel 00 register at board relative address 0020 (HEX).
11. Adjust R2 for a digital voltmeter indication of +9.9951 ±0.0010 VDC.
12. Calibration of the analog outputs is completed. Remove power and all test connections. Restore the board to its original configuration.

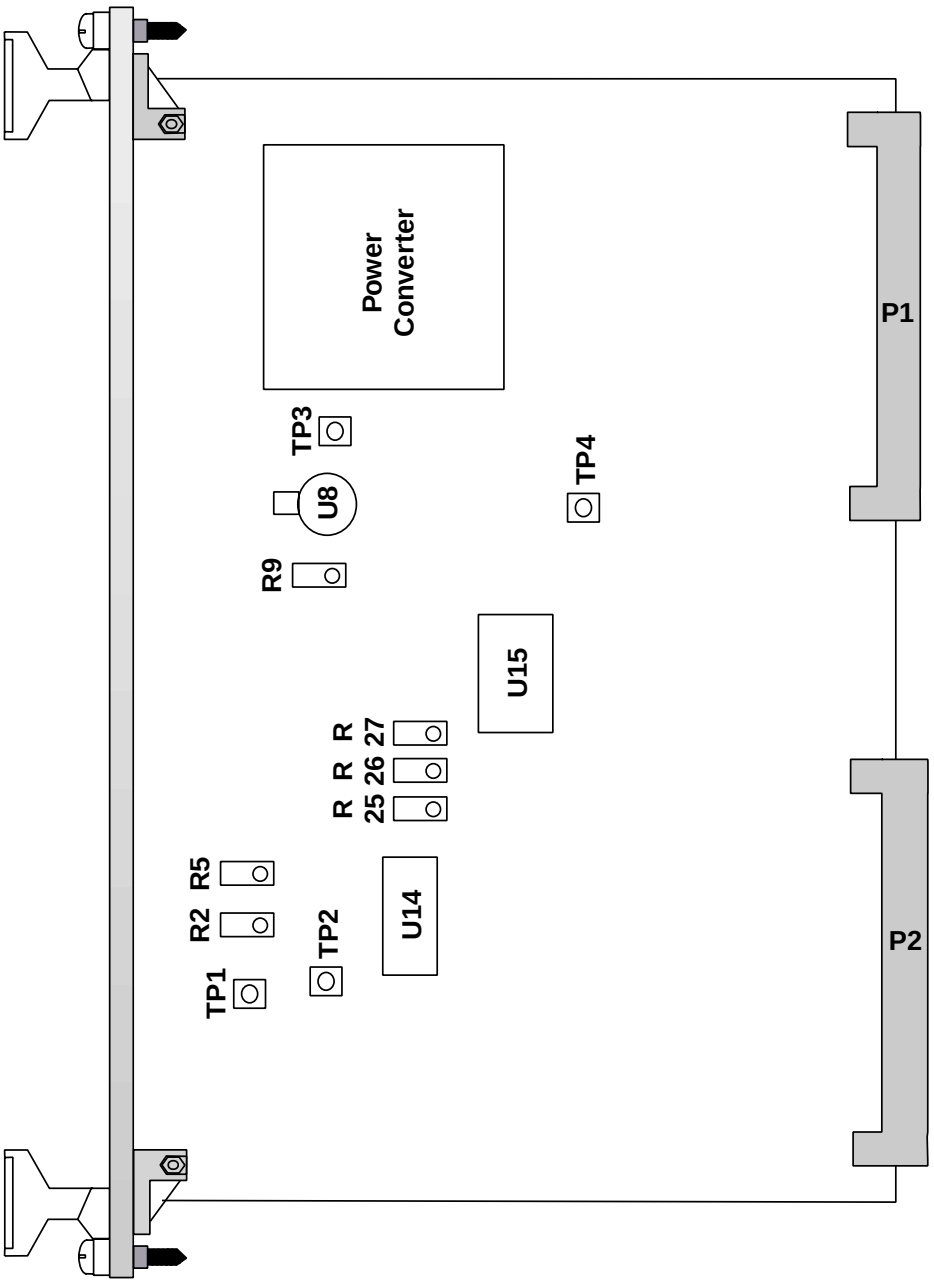


Figure 2-2 VMIVME-4512 Calibration Adjustments and Test Points

Connector Descriptions

Two 96-pin DIN connectors, P1 and P2, provide all connections to the VMIVME-4512 board. P1 contains the address, data and control lines, and all additional signals necessary to control VMEbus functions related to the board. P2 provides the connections for the 16 analog input channels and the 16 analog output channels.

Orientation of the P1 / P2 connector is shown in Figure 2-3 below, and the P2 signal assignments are listed in Table 2-3 on page 44. The mating connector for P2 (Panduit Model 120-964-455E or equivalent) is designed to be used with a standard 64-wire ribbon cable with a conductor spacing of 0.050 inches.

A twisted-pair ribbon cable with an overall shield is recommended for applications involving low level signals in high electrical noise environments.

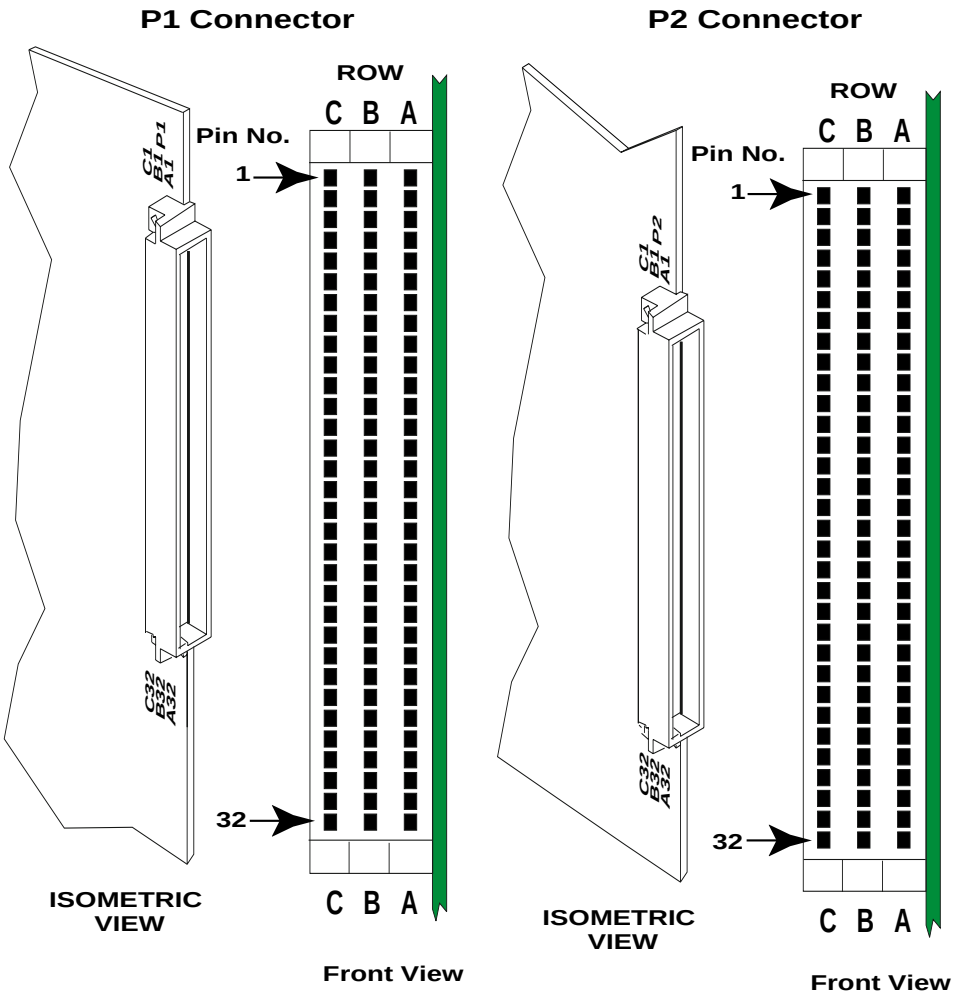


Figure 2-3 P1/P2 Connector - Pin Assignments

Table 2-3 P2 Connector Signal Assignments

P2 Output Signals			P2 Input Signals		
Analog Output CH#	**Signal**	**Return**	**Analog Input CH#**	**Signal**	**Return**
00	A1	C1	00	A17	C17
01	A2	C2	01	A18	C18
02	A3	C3	02	A19	C19
03	A4	C4	03	A20	C20
04	A5	C5	04	A21	C21
05	A6	C6	05	A22	C22
06	A7	C7	06	A23	C23
07	A8	C8	07	A24	C24
08	A9	C9	08	A25	C25
09	A10	C10	09	A26	C26
10	A11	C11	10	A27	C27
11	A12	C12	11	A28	C28
12	A13	C13	12	A29	C29
13	A14	C14	13	A30	C30
14	A15	C15	14	A31	C31
15	A16	C16	15	A32	C32
			GND Sense	------	C16

CHAPTER 3

Programming

Contents

Introduction

Communication with the VMIVME-4512 Analog I/O (AIO) Board takes place through 32 contiguous 16-bit register locations which are mapped into the VME short I/O address space. The short I/O address space consists of all locations within the address range from NNNN0000 HEX to NNNNFFFF HEX*. Functions of the communication registers, which are discussed in detail within this section, are summarized in Table 3-1 on page 47.

NOTE: *The value NNNN depends on the make and model of CPU board used.

Control and Status Register Descriptions

The communication register located at relative address 02 HEX is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

- Analog input channel selection
- Analog-to-Digital (AD) conversion
- Built-in-Test (BIT)
- Analog outputs on-line / off-line
- Analog outputs refresh rate
- Front panel Fail indicator
- Board RESET

The CSR is 16 bits in length, and is detailed in Table 3-2 on page 48 and Table 3-3 on page 50. The function of each control bit and status flag is described in detail subsequently in the associated programming discussions.

Table 3-1 Communication Register Map

Relative Address			
HEX	**DEC**	**Register Name**	**Access Mode**
00	00	Board Identification	Read (03XX Hex)
02	02	Control and Status Register (CSR)	Read / Write
04	04	Converter Data Register	Read
06 to 1E	06 to 30	Reserved	----
20	32	Analog Output Channel 00	Read / Write
22	34	Analog Output Channel 01	Read / Write
24	36	Analog Output Channel 02	Read / Write
26	38	Analog Output Channel 03	Read / Write
28	40	Analog Output Channel 04	Read / Write
2A	42	Analog Output Channel 05	Read / Write
2C	44	Analog Output Channel 06	Read / Write
2E	46	Analog Output Channel 07	Read / Write
30	48	Analog Output Channel 08	Read / Write
32	50	Analog Output Channel 09	Read / Write
34	52	Analog Output Channel 10	Read / Write
36	54	Analog Output Channel 11	Read / Write
38	56	Analog Output Channel 12	Read / Write
3A	58	Analog Output Channel 13	Read / Write
3C	60	Analog Output Channel 14	Read / Write
3E	62	Analog Output Channel 15	Read / Write

*Register address is the sum of the relative address and the board address.

Control Register Data Format

Table 3-2 Control Register Bit Map

Control Register: Offset 02 (Hex), 02 (Dec), Read/Write							
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Short Settling H (MSB)	Fail LED L	EN Start Conv H	Two's Compl L	Output On-line H	Test Mode 1 H	Test Mode 0 H	Fast Refresh H

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	Start Settling H	Software Reset H	Reserved	MUX A3 H	MUX A2 H	MUX A1 H	MUX A0 H (LSB)

Control Register Bit Definitions

D15*: **Short Settling H** - D15 controls the selection of two distinct input settling (acquisition) times. The zero (0) state selects the default settling time that ensures that the full accuracy of the converter is utilized. Settling D15 to one (1) reduces the settling time to accommodate situations in which a small degradation in accuracy is acceptable in order to increase overall throughput.

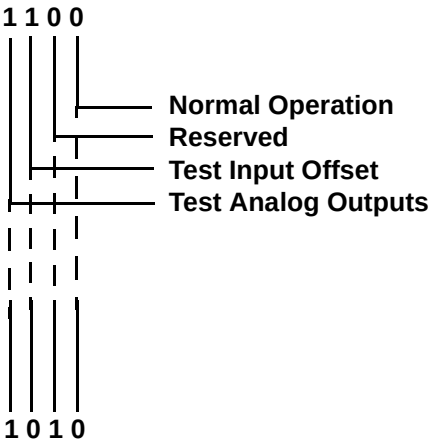
D14: **Fail LED L** - The Fail LED is OFF if this bit is set to one (1), and ON if set to zero (0).

D13*: **EN Start Conv H** - A single AD conversion is enabled each time a one (1) is written to this control bit. D13 will be ignored if the Converter Data Register (CDR) contains unread data from a previous conversion. The current settling sequence will be sustained until the READ DTA command occurs.

D12: **Two's Compl L** - ADC coding format is offset binary if D12 is high when set to one (1), and two's complement if D12 is low when set to zero (0).

D11: **Output On-Line H** - If D11 is set to a one (1) high, the analog outputs are connected to the P2 I/O connector. The analog outputs are disabled disconnected from P2 if D11 is set to zero (0) low.

D10: **Test Mode 1 H -**



D9: **Test Mode 0 H -**

Control Register Bit Definitions (Continued)

D8: **Fast Refresh H** - The analog output refresh nominal interval is 1.7 milliseconds if D8 is set to zero (0) low, 0.4 milliseconds if D8 is set to one (1) high.

D7: **Reserved**

D6*: **Start Settling H** - When D6 is set to a one (1), the analog input settling (acquisition) interval is initiated.

D5: **Software Reset H** - When D5 is set to a one (1) high all on-board A / D timing networks are cleared.

D4: **Reserved**

D3 through D0: **MUX A3 through A0 H** - D0 through D3 select the analog input channels.

NOTE: *Each control bit is mapped directly into the corresponding bit in the Status register unless it is indicated with (*).

Status Register Flags

Table 3-3 Status Register Bit Map

Status Register: Offset 02 (Hex), 02 (Dec), Read/Write							
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
New Data RDY (MSB)	Fail LED L	Conv Busy H	Two's Compl L	Output On-line H	Test Mode 1 H	Test Mode 0 H	Fast Refresh H

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Reserved	Settling Busy H	Software Reset H	Reserved	Input Channel Select 3	Input Channel Select 2	Input Channel Select 1	Input Channel Select 0 (LSB)

Status Register Bit Definitions

D15: **New Data RDY** - When set to a one (1) this flag indicates that a conversion has been completed and that data is available in the CDR. Reading the CDR clears this flag.

D14*: **Fail LED L**

D13: **Conv Busy H** - Writing a one (1) to the EN Start CMD control bit causes the D13 flag to be set to a one (1). The flag will remain set until the next conversion has been completed and new data is available in the CDR. The settling sequence will not run to completion if this flag is not set.

D12*: **Two's Compl L**

D11*: **Output On-Line H**

D10*: **Test Mode 1 H**

D9*: **Test Mode 0 H**

D8*: **Fast Refresh H**

D7*: **Reserved**

D6: **Settling Busy H -** When set to a one (1) this flag indicates that the input settling sequence is in progress, and that the Start Settling command will be ignored. The Start Settling command will be recognized if this flag is set to a zero (0) low.

D5*: **Software Reset H**

D4*: **Reserved**

D3*: **Input Channel Select 3**

D2*: **Input Channel Select 2**

D1*: **Input Channel Select 1**

D0*: **Input Channel Select 0**

NOTE: *The corresponding control register bit is mapped directly to this flag.

Controlling and Reading the Analog-to-Digital Converter (ADC)

Two principal methods are available for controlling the ADC on the VMIVME-4512 Board. For applications in which conversion speed is not a critical factor, the basic method usually will provide suitable performance. This is the simpler of the two methods to implement, and will produce a maximum throughput of approximately 40 kHz (40,000 samples per second).

If higher throughput is essential, the interleaved (pipelined) method can be used. The interleaved control approach permits the settling interval of a new channel to begin while a conversion is in progress. This technique eliminates the settling interval from the throughput equation, and raises the throughput to approximately 58 kHz.

Short-settling conversions may be used in those situations in which a small degradation in accuracy may be tolerated in order to obtain a higher throughput. Setting the SHORT SETTLING control bit to one (1) decreases all major contributors to settling time, and increases the maximum throughput to 44 kHz (60 kHz pipelined).

ADC Timing

All timing operations for the ADC are performed by the on-board controller. Control of the converter consists of the “handshake” programming sequences described in the following paragraphs.

ADC Controls and Flags

The following controls, flags and registers are available for use in controlling the ADC (controls and flags are summarized in Table 3-2 on page 48 and Table 3-3 on page 50):

Controls (Control Register)

- START SETTLING H... D06*
- TWO's COMPL L..... D12
- EN START CONV H....D13 *
- SHORT SETTLING H...D15

NOTE: *Effective only upon writing. (“strobed”).

Flags (Status Register)

- SETTLING BUSY H....D06
- CONV BUSY H.....D13
- NEW DATA RDY H.....D15

NOTE: Set when data is available in the ADC data register.

Converter Data Register (CDR)

The Converter Data Register is a 16-bit *read only* register at relative address 04 (HEX). Data in this register is 12 bits, right-justified. D12 through D15 are always zero (0) in the binary data mode, and are sign extensions in the two's complement data mode (Table 3-5 on page 57).

The START SETTLING and EN START CONV controls are essentially strobes, and are effective only at the moment of writing to the Control Register. Although supplied as two separate control bits for flexibility, these controls usually are written to the register simultaneously along with the operational mode and channel selections.

A measurement sequence which uses the basic conversion control method is illustrated in Figure 3-1 on page 53 and Figure 3-2 on page 54. The sequence is simple because only the NEW DATA RDY flag must be monitored to determine when each conversion has been completed. The interleaved (pipelined) control method is presented in Figure 3-4 on page 56 and Figure 3-6 on page 63. A higher throughput is achieved by using a somewhat more complex control sequence. With this method, both the SETTLING BUSY and NEW DATA RDY flags must be monitored.

Reading ADC Codes

The data format which applies when reading the CDR is shown in Table 3-4 on page 57. Coding can be straight binary, offset binary or two's complement, depending upon the configuration of the ADC input range selection jumpers and the state of the TWO's COMPL control bit. Converter output codes that are produced at major points within the full scale ranges shown are summarized in Table 3-5 on page 57.
For any offset binary converter output code (BIPOLAR RANGE), the associated input voltage is obtained with the expressions:

INPUT (Volts) = $E_{FSR}/2 + E_{FSR}$ X [Decimal Output Code] / 4096,

where E_{FSR} is the full scale range voltage. (EG: E_{FSR} = 10 Volts for the ±5 V range.)

The input voltage for a straight binary code (Unipolar Range) is:

INPUT (Volts) = $+E_{FSR}$ X [Decimal Output Code] / 4096.

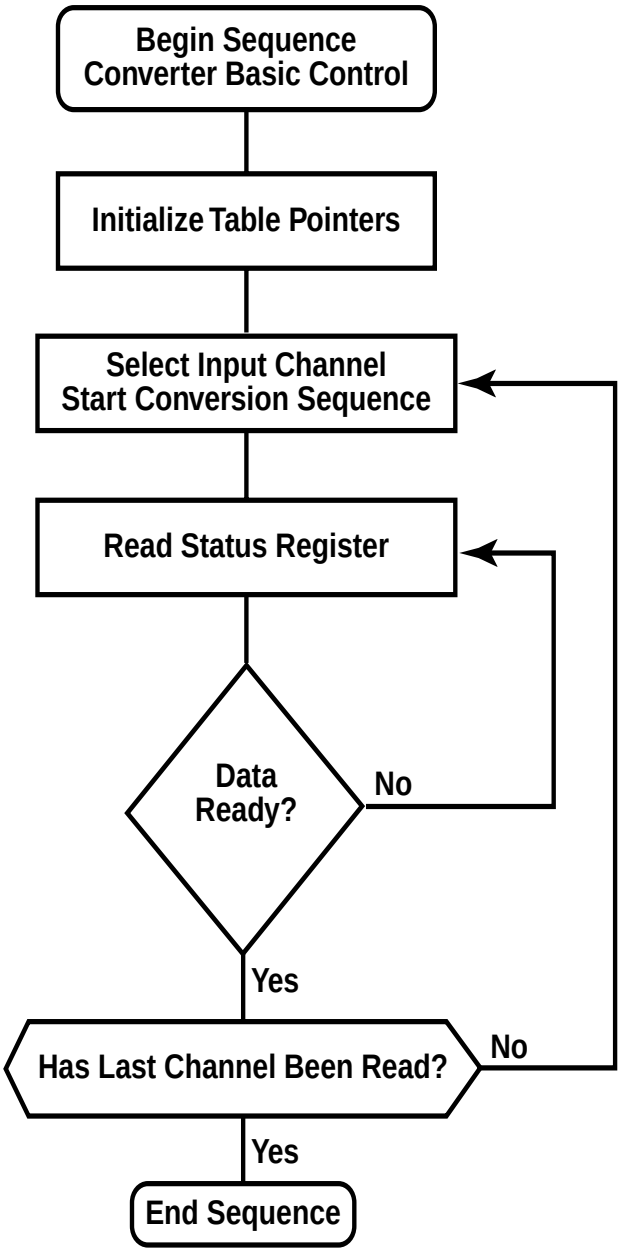


Figure 3-1 Program Flowchart - Basic ADC Control Sequence

```
            opt         P = 68020
*this program was written for a 68020 or later processor
            org         $1000
*this first line is for a FORCE CPU 21
            lea.l       $FBFF0000, A0       load DUT address (CPU board specific)
            bsr.s       setup               preparation for the example
            bsr.s       example             example written as a subroutine
            dc.w        $A002               end (depends on debug software)

setup       move.w      #$20, (2, A0)       reset 4512 (optional)
            move.w      #$5000, (2, A0)     un-reset 4512
            cmp.w       (4, A0), D0         dummy read of A/D register (must after reset)
            lea.l       $2000, A1           pointer to beginning of data buffer
*the following example uses normal (non-pipelined) mode to read all 16 analog
*input channels, and it stores them in a buffer in RAM.
example     moveq.l     #15, D3             for 16 loop cycles, init counter to 15
            move.w      #$7040, D0          init settle, convert control word

loop        move.w      D0, (2, A0)         select input and start settling and convert
convwait    btst.b      #7, (2, A0)         check for conversion complete
            beq.s       convwait            loop until conversion complete
            move.w      (4, A0), (A1) +     read conversion into data buffer
            addq.l      #1, D0              set command word to next channel
            dbf         D3, loop            take next of 16 readings
            rts
            END
```

Figure 3-2 Program Example - A/D Conversion

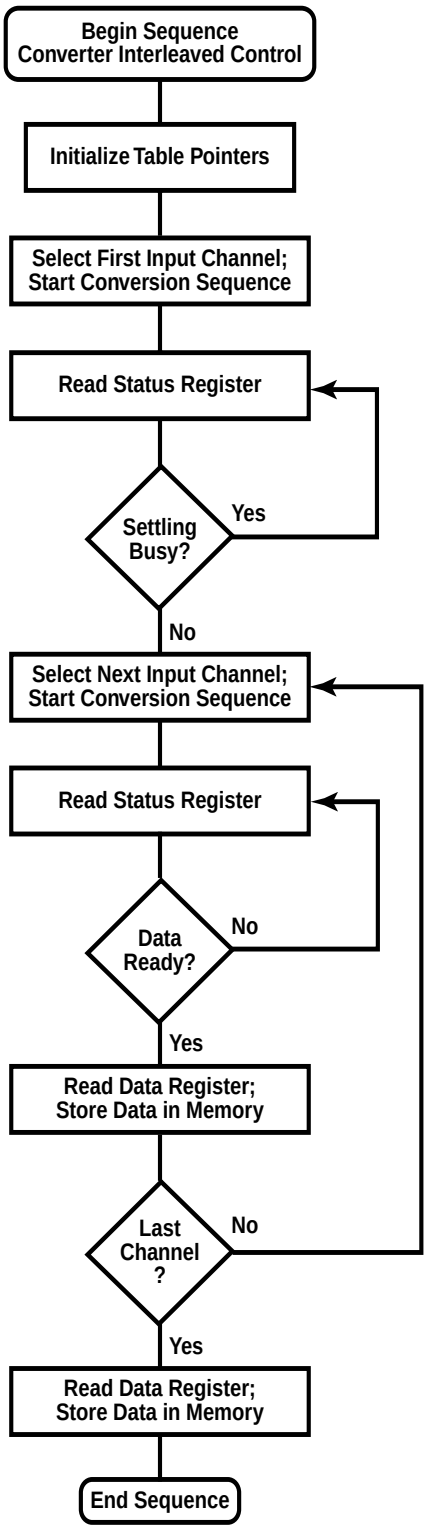


Figure 3-3 Program Flowchart - Pipelined A/D Control Sequence

```
            opt         P = 68020
*this program was written for a 68020 or later processor
            org         $1000
*these first four lines are for a FORCE CPU 21 with FORCEBUG:
            lea.l       $FBFF0000, A0       load DUT address (CPU board specific)
            bsr.s       setup               preparation for the example
            bsr.s       example             example written as a subroutine
            dc.w        $A002               end (depends on debug software)

setup       move.w      #$20, (2, A0)       reset 4512 (optional)
            move.w      #$5800, (2, A0)     un-reset 4512
            move.w      #$FFFF, D0
            cmp.w       (4, A0), D0         dummy read of A/D reg (must after reset)
            lea.l       $2000, A1           pointer to beginning of data buffer

            move.l      #$F08, D0           set first DAC fill value
            moveq.l     #15, D1             set count of fills to do
filloop     move.w      D0, ($20,A0,D1.W*2) fill a DAC RAM location
            move.l      #0, (A1)+           clear reading array
            sub.w       #$100,D0            change fill value
            dbf         D1, filloop
            lea.l       $2000,A1            fix pointer to beginning of data buffer
            rts

*the following example uses pipelined mode to read all 16 analog input
*channels, and it stores them in a buffer in RAM.
example     move.w      #$7640, D0          init command word (output on; read input)
            moveq.l     #14, D3             for 15 loop cycles, init counter to 14

            move.w      #$7640, (2, A0)     command: settle, convert (nonpipeline)
*           move.w      D0, (2, A0)         command: settle, convert (nonpipeline)
setlwait    btst.b      #6, (3, A0)         check for settling complete
            bne.s       setlwait            loop until settling complete
loop        addq.l      #1, D0              set settling command word to next chan.
            move.w      D0, (2, A0)         select next input & start settling
convwait    btst.b      #7, (2, A0)         check for conversion complete
            beq.s       convwait            loop until conversion complete
            move.w      (4, A0), (A1)+      read conversion into data buffer
            dbf         D3, loop            take next of 15 pipelined readings
            move.w      (4, A0), (A1)+      make 16th reading to data buffer
            rts
            END
```

Figure 3-4 Program Example - Pipelined A/D Control Sequence

ADC Data Format and Coding

Table 3-4 ADC Data Format/Coding Bit Map

ADC Data Format/Coding (Converter Data Register): Offset 04 (Hex), 04 (Dec), Read-Only							
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
* (MSB)	*	*	*	D	D	D	D

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	D	D	D	D	D	D	D (LSB)

NOTE: (*) = zero (offset binary, straight binary) or extended sign (two's complement).

Table 3-5 ADC Coding

Unipolar Ranges			**Straight Binary**			
Input	**0 to +10 V**	**0 to +5 V**	**D15**			**D0**
+FS-1 LSB	+9.9975 V	+4.9988 V	0000	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	0000	0000	0000	0001
Bipolar Ranges			**Offset Binary**			
Input	**±10 V**	**±5 V**	**D15**			**D0**
+FS-1 LSB	+9.9951 V	+4.9976 V	0000	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	0000	1000	0000	0001
Zero	0.0000 V	0.0000 V	0000	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	0000	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	0000	0000	0000	0000
Bipolar Ranges			**Two's Complement**			
Input	**±10 V**	**±5 V**	**D15**			**D0**
+FS-1 LSB	+9.9951 V	+4.9976 V	0000	0111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	0000	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	0000	0000	0000	0001
Zero	0.0000 V	0.0000 V	0000	0000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	1111	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	1111	1000	0000	0000

Accessing the Analog Input Channels

Selection of the analog input channels at the P2 I/O connector is controlled by the four least significant control bits (D00 through D03) in the Control Register. The control code for each input channel is listed in Table 3-6 below.

Table 3-6 Analog Input Channel Selection

Control Register					
Hex	**D03**	**D02**	**D01**	**D00**	**Selected Input Channel No.**
0	0	0	0	0	00
1	0	0	0	1	01
2	0	0	1	0	02
3	0	0	1	1	03
4	0	1	0	0	04
5	0	1	0	1	05
6	0	1	1	0	06
7	0	1	1	1	07
8	1	0	0	0	08
9	1	0	0	1	09
A	1	0	1	0	10
B	1	0	1	1	11
C	1	1	0	0	12
D	1	1	0	1	13
E	1	1	1	0	14
F	1	1	1	1	15

Controlling the Analog Outputs

The 16 analog output channels appear to the controlling processor as 16 consecutive 16-bit words in the address space assigned to the VMIVME-4512 board. The communication register map shown in Table 3-1 on page 47 lists the board-relative address of each output channel. Each analog output register supports both *read* and *write* operations, eliminating the need for corresponding "shadow" latches in the processor Random Access Memory (RAM) space.

Writing to Outputs

Digital codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four Most Significant Bits (MSBs) (D12 to D15) will be ignored, and will not be retained for read back. The Digital-to-Analog coding conventions used by the Digital-to-Analog Converter (DAC) are shown in Table 3-8 on page 60. Each output will respond to a new code within 1.7 milliseconds after the code is written to the output register (0.4 milliseconds in FAST REFRESH MODE).

DAC Data Format and Coding

Table 3-7 DAC Data Format and Coding Bit Map

DAC Data Register (Converter Data Register): Offset 04 (Hex), 04 (Dec), Read-Only							
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
X (MSB)	X	X	X	D	D	D	D

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	D	D	D	D	D	D	D (LSB)

.

Table 3-8 DAC Coding

Unipolar Ranges			Straight Binary			
Output	**0 to +10 V**	**0 to +5 V**	**D15**			**D0**
+FS-1 LSB	+9.9975 V	+4.9988 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	XXXX	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001
Bipolar Ranges			**Offset Binary**			
Output	**±10 V**	**±5 V**	**D15**			**D0**
+FS-1 LSB	+9.9951 V	+4.9976 V	XXXX	1111	1111	1111
+1 / 2 FS	+5.0000 V	+2.5000 V	XXXX	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	XXXX	0000	0000	0001
Zero	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	XXXX	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	XXXX	0000	0000	0000

NOTE: X = don't care.

"FAST REFRESH"

Settling the FAST REFRESH control bit (Table 3-2 on page 48) HIGH will reduce the analog output REFRESH time from the default value of 1.7 milliseconds to 0.4 milliseconds. The FAST REFRESH MODE raises the output Nyquist frequency (maximum output signal frequency) from approximately 300 Hz to 1.2 kHz.

Off-line Operation

Settling the OUTPUT ON-LINE control bit HIGH (Table 3-2 on page 48) connects the analog outputs to the P2 I/O connector for normal system operation. Clearing the bit LOW disconnects the analog outputs from P2. However, the output buffers can still be monitored through the self-test multiplexers. This operating mode is normally used for loopback testing.

Self-Testing the VMIVME-4512 Board

Built-in-Test (BIT) provisions include loopback testing and the measurement of analog input offset voltages. These capabilities permit self-contained, board level verification of performance. The control of VMIVME-4512 self-test modes is summarized in Table 3-9 below.

Table 3-9 Self-Test Control Modes

CSR Control Bits						
Self-Test Mode	**D10**	**D9**	**D3**	**D2**	**D1**	**D0**
Normal Operation	0	0	Selected Analog Input Channel			
Reserved	0	1	X	X	X	X
Test Input Offset	1	0	*	X	X	X
Test Analog Outputs	1	1	Selected Analog Output Channel			

NOTE: * is zero (0) to test the input Channels 00 to 07 multiplexer, one (1) to test the Channels 08 to 15 multiplexer.

Loopback Testing of Inputs and Outputs

By routing the analog outputs through the input multiplexers, the operation of all active components on the VMIVME-4512 Board can be verified. This loopback test is performed by selecting one of the 16 analog output channels. The selected output channel can then be exercised by the controlling processor, and monitored by the ADC to verify that all components in the loopback signal path are operating correctly. This technique is illustrated in Figure 3-5 on page 62 and Figure 3-6 on page 63.

Output Channels 00 to 07 are routed through the input multiplexer for input Channels 00 through 07. Outputs 08 through 15 are routed through the multiplexer for inputs 08 through 15.

Testing and Correcting Analog Input Zero Offsets

Zero offset errors which can be present in the analog input signal path can be corrected by first performing the input offset self-test procedure shown in Figure 3-7 on page 64 and Figure 3-8 on page 65, and by applying the results of the test in the input multiplexer zero correction procedure illustrated in Figure 3-9 on page 66 and Figure 3-10 on page 67. This offset is normally small and in most cases does not affect accuracy.

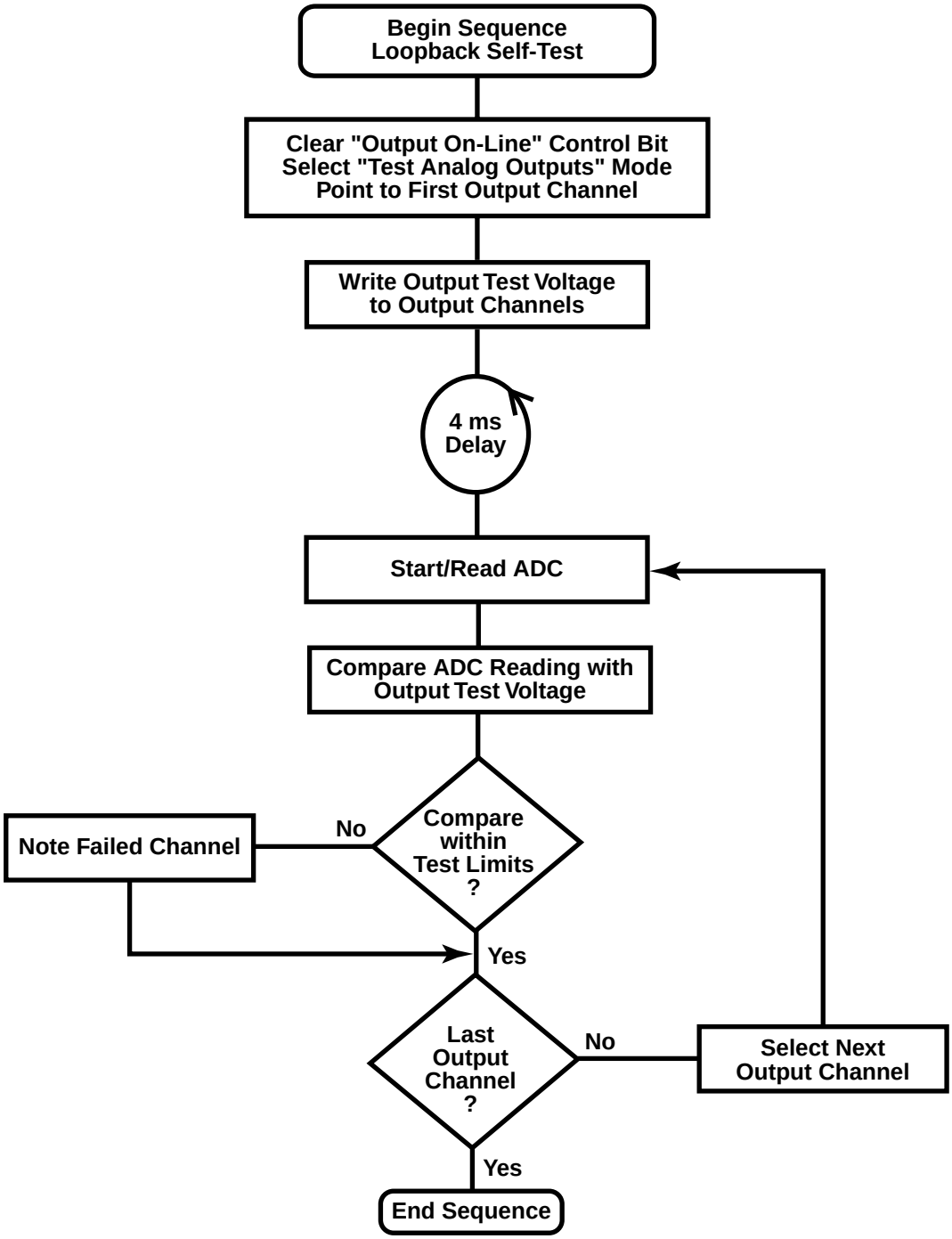


Figure 3-5 Program Flowchart - Loopback Self-Test

```
                opt         P = 68020
*this program was written for a 68020 or later processor
                org         $1000

*these first four lines are for a FORCE CPU 21 with FORCEBUG:
                lea.l       $FBFF0000, A0       load 4512 address (CPU board specific)
                bsr.s       setup               use 4512 some prior to self-test
                bsr.s       example             self-test example written as a subroutine
                dc.w        $A002               end (depends on debug software)

*"setup" loads the analog outputs with typical values for the self-test example
setup           move.w      #$20, (2, A0)       reset 4512
                move.w      #$5600, (2, A0)     un-reset 4512
                cmp.w       (4, A0), D0         dummy read of ADC output
                moveq.l     #15, D0             fill the 16 different...
                moveq.l     #0, D7              ... analog output registers...
load            move.w      D7,($20,A0,D0.W*2)  ... with 16 different values
                add.w       #$111, D7           compute next fill value
                dbf         D0, load
                move.w      #$F000, D0          load delay constant (varies with system)
delay           dbf         D0, delay           delay for at least 4 milliseconds.
                rts

*this subroutine uses the 4512 self-test ability to read the analog outputs and
*compare them to the expected outputs. It counts the channels which deviate too
*much from the expected value (in D2). On entry, it is assumed that the outputs
*have had time to stabilize, and the ADC is ready.
**The 4512 inputs and outputs must be on the same voltage range (e.g., ±10 V).

example         moveq.l     #15, D1             initialize counter for 16 channels
                moveq.l     #0, D2              clear out-of-tolerance channel counter
                moveq.w     #$764F, D3          load control word ($7E4F for outputs on)

loop            move.w      D3, (2, A0)         command analog-to-digital conversion
wait            btst.b      #7, (2, A0)         check for conversion complete
                beq.s       wait                branch if conversion not finished
                move.w      (4, A0), D4         read conversion value

                move.w      ($20,A0,D1.W*2),D5  read expected value from DAC RAM
*the above addressing mode translates as "word at A0 + $20 + 2 * (word in D1)"
                andi.w      #$FFF, D5           set bits 12-15 (unused) to zero
                sub.w       D4, D5              find difference
                bpl.s       posdiff             take absolute value of difference
                neg.w       D5                  (negate negative difference)
posdiff         cmpi.w      #5, D5              is difference within tolerance?
                bmi.s       nocount             branch if difference < tolerance
                addq.I      #1, D2              count one possibly bad channel
nocount         subq.I      #1, D3              make control word to read next channel
                dbf         D1, loop            on to the next channel
                rts
                END
```

Figure 3-6 Program Example - Self-Test Program Example

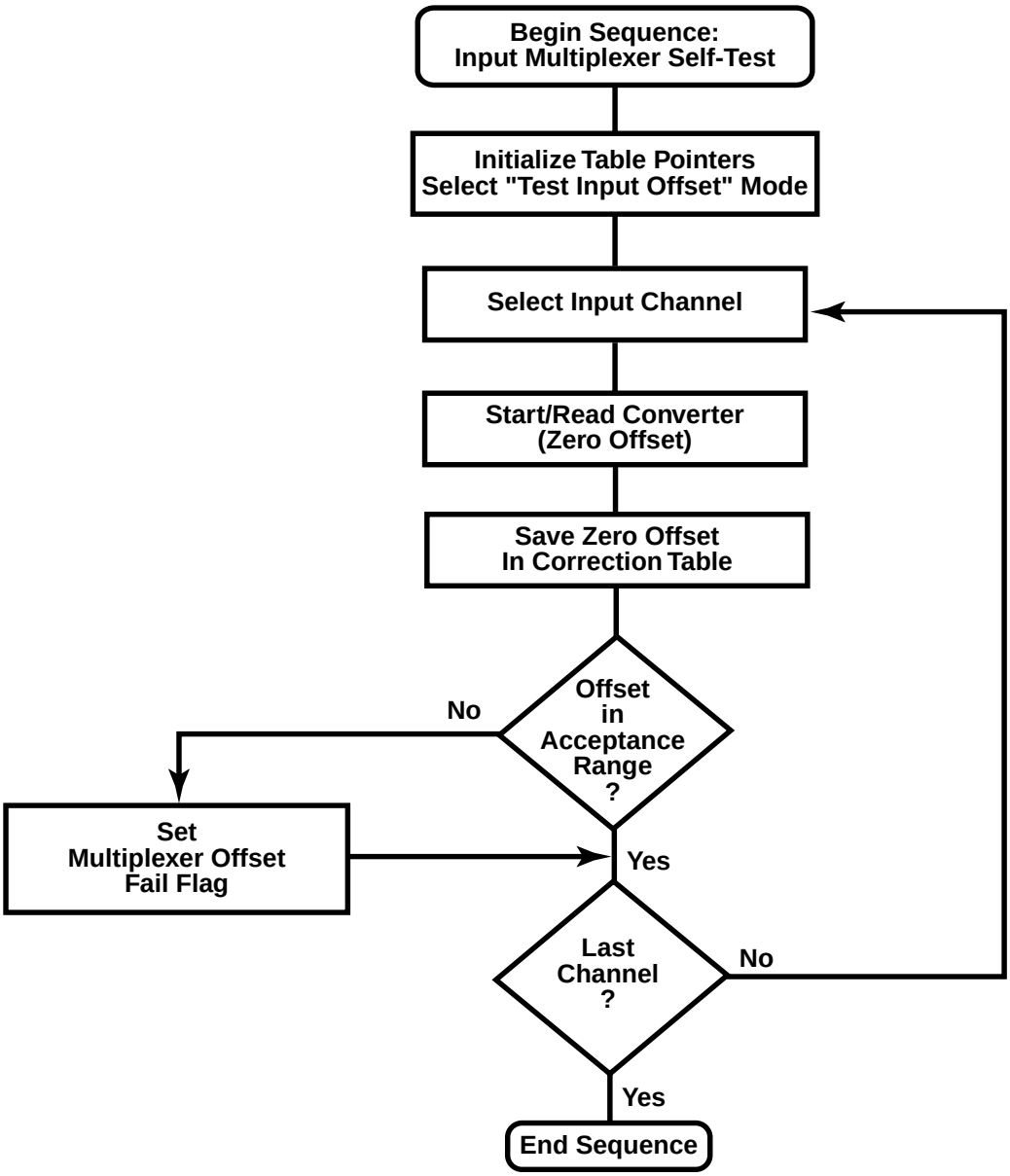


Figure 3-7 Program Flowchart - Self-Testing the Input Multiplexer

```
            opt         P = 68020
*this program was written for a 68020 or later processor
            org         $1000
*these first four lines are for a FORCE CPU 21 with FORCEBUG:
            lea.l       $FBFF0000, A0       load DUT address (CPU board specific)
            bsr.s       setup               preparation for the example
            bsr.s       example             example written as a subroutine
            dc.w        $A002               end (depends on debug software)
setup       move.w      #$20, (2, A0)       reset 4512 (optional)
            move.w      #$5000, (2, A0)     un-reset 4512
            cmp.w       (4, A0), D0         dummy read of AD register (must after reset)
            lea.l       $2000, A1           pointer to beginning of offset data
            clr.b       D4                  clear "mux offset fail" flag
            rts
*the following example uses normal (non-pipelined) mode to read all 16 analog
*input channels, and it stores them in a buffer in RAM.
example     moveq.l     #15, D3             for 16 loop cycles, init counter to 15
            move.w      #$7440, D0          init settle, convert control word
loop        move.w      D0, (2, A0)         select input and start settling and convert
convwait    btst.b      #7, (2, A0)         check for conversion complete
            beq.s       convwait            loop until conversion complete
            move.w      (4, A0), D1         read conversion into register
            cmp2.w      ofsrange, D1        set Carry if offset too big
            bcc.s       ofsok               branch if offset is acceptable
            moveq.l     #1, D4              set "mux offsets fail" flag
ofsok       sub.w       #$800, D1           convert offset to two's complement
            move.w      D1, (A1) +          store conversion in data buffer
            addq.l      #1, D0              set command word to next channel
            dbf         D3, loop            take next of 16 readings
            rts
ofsrange    dc.w        $7F8, $808          acceptable input mux offset limits
            END
```

Figure 3-8 Self-Test the Input Multiplexer Example

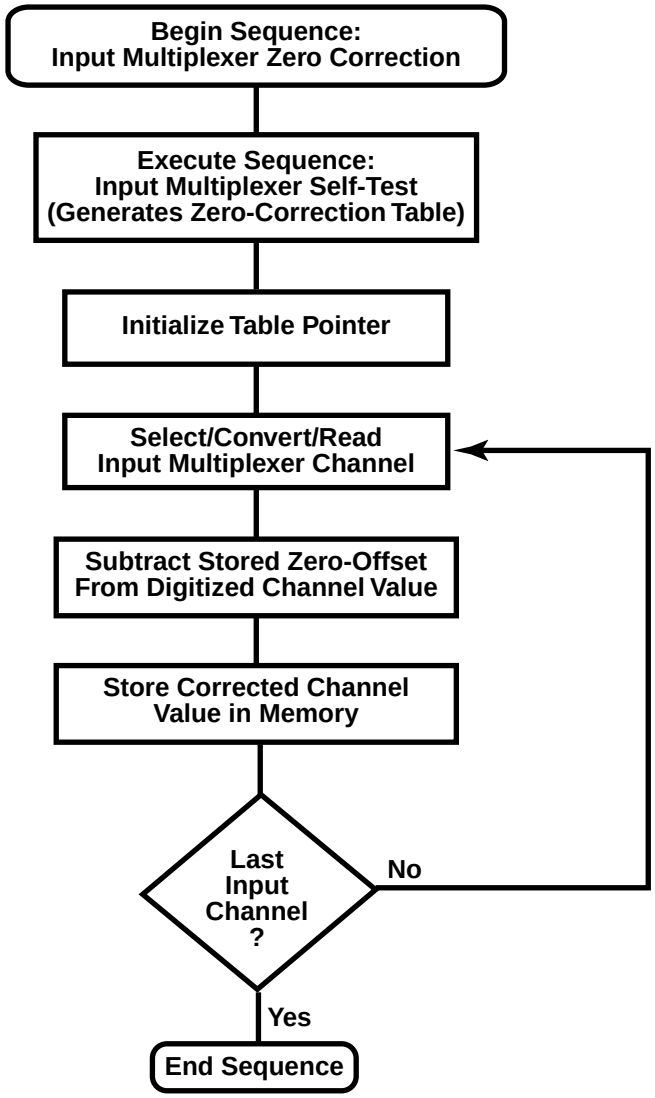


Figure 3-9 Program Flowchart - Input Multiplexer Zero Correction

```
                opt         P = 68020
*this program was written for a 68020 or later processor
                org         $1200

*these first four lines are for a FORCE CPU 21 with FORCEBUG:
                lea.l       $FBFF0000, A0       load DUT address (CPU board specific)
                bsr.s       setup               preparation for the example
                bsr.s       example             example written as a subroutine
                dc.w        $A002               end (depends on debug software)

setup           move.w      #$20, (2, A0)       reset 4512 (optional)
                move.w      #$5000, (2, A0)     un-reset 4512
                cmp.w       (4, A0), D0         dummy read of AD register (must after reset)
                lea.l       $2000, A1           pointer to beginning of offset data
                lea.l       $2020, A2           pointer to beginning of corrected readings
                rts

*the following example uses normal (non-pipelined) mode to read all 16 analog
*inputs; then it corrects for input offset and stores the result in RAM.

example         moveq.l     #15, D3             for 16 loop cycles, init counter to 15 init
                move.w      #$7040, D0          init settle, convert control word

loop            move.w      D0, (2, A0)         select input and start settling and convert
convwait        btst.b      #7, (2, A0)         check for conversion complete
                beq.s       convwait            loop until conversion complete
                move.w      (4, A0), D1         read conversion into register
                sub.w       (A1) +, D1          subtract offset
                move.w      D1, (A1) +          store conversion in data buffer
                addq.l      #1, D0              set command word to next channel
                dbf         D3, loop            take next of 16 readings
                rts

                END
```

Figure 3-10 Example A/D Conversion with Input Multiplexer Zero Correction

Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- System power
- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC Customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.